National Semiconductor

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T-67-21-55

54VHC/74VHC139
Dual 2-to-4 Decoder/Demultiplexer

General Description

The VHC139 is an advanced high speed CMOS 2 to 4 line decoder/demultiplexer fabricated with silicon gate CMOS technology.

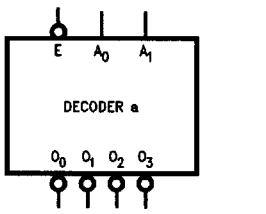
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications. When the enable input is held High, all four outputs are fixed at a high logic level independent of the other inputs. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: t_{PD} = 5.0 ns (Typ.) at V_{CC} = 5V
- Low power dissipation: I_{CC} = 4 μA (Max.) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2V ~ 5.5V
- Pin and function compatible with 74HC139

Logic Symbols



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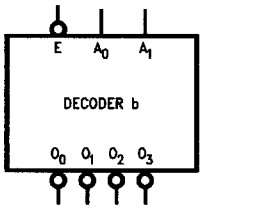

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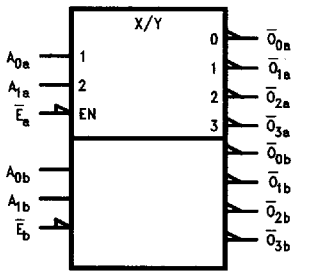
IEEE/IEC



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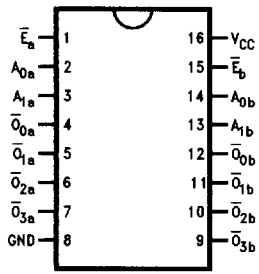
Connection Diagram

Pin Assignment



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Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs
$\overline{O}_0$–$\overline{O}_3$	Outputs

Functional Description

The 'VHC139 is a high-speed dual 2-to-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0–A_1) and provides four mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_3$). Each decoder has an active-LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'VHC139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure 1*, and thereby reducing the number of packages required in a logic network.

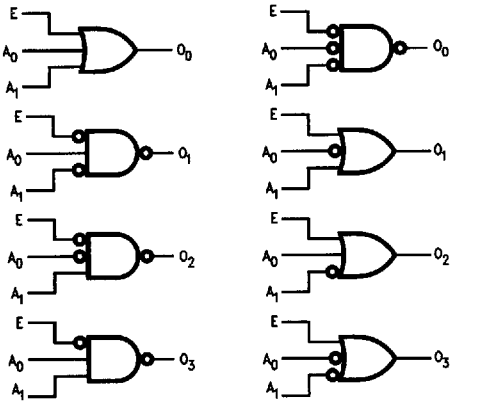

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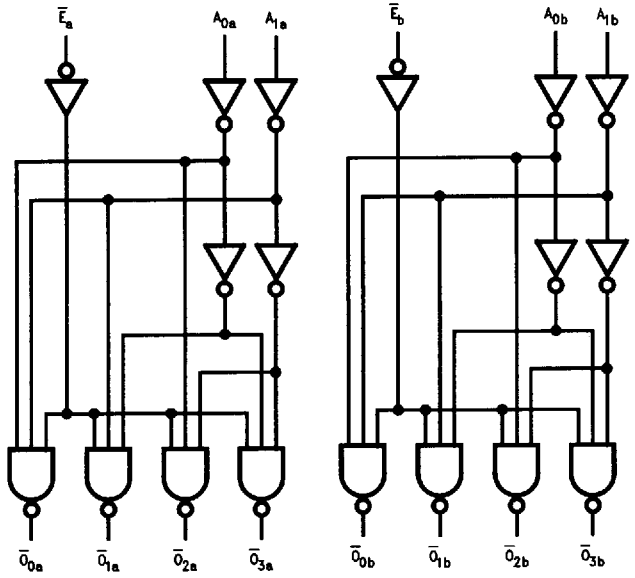
FIGURE 1. Gate Functions (Each Half)

Truth Table

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 sec.)	300°C

Note: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
54VHC	−55°C to +125°C
74VHC	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C Min	Typ	Max	54VHC T_A = −55°C to +125°C Min	Max	74VHC T_A = −40°C to +85°C Min	Max	Units	Conditions	
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}		0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9		2.9				
		4.5	4.4	4.5		4.4		4.4				
		3.0	2.58			2.40		2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.70		3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1		0.1			
		4.5		0.0	0.1		0.1		0.1			
		3.0			0.36		0.50		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.50		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		80.0		40.0	μA	V_{IN} = V_{CC} or GND	

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			54VHC $T_A = -55°C$ to $+125°C$		74VHC $T_A = -40°C$ to $+85°C$	
			Min	Typ	Max	Min	Max	Min	Max
t_{PLH}, t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3 ±0.3		7.2	11.0			1.0	13.0
				9.7	14.5			1.0	16.5
		5.0 ± 0.5		5.0	7.2			1.0	8.5
				6.5	9.2			1.0	10.5
t_{PLH}, t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3 ±0.3		6.4	9.2			1.0	11.0
				8.9	12.7			1.0	14.5
		5.0 ± 0.5		4.4	6.3			1.0	7.5
				5.9	8.3			1.0	9.5
C_{IN}	Input Capacitance			4	10				10
C_{PD}	Power Dissipation Capacitance			26					

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/2 (per decoder).

Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:

74VHC 139 M X

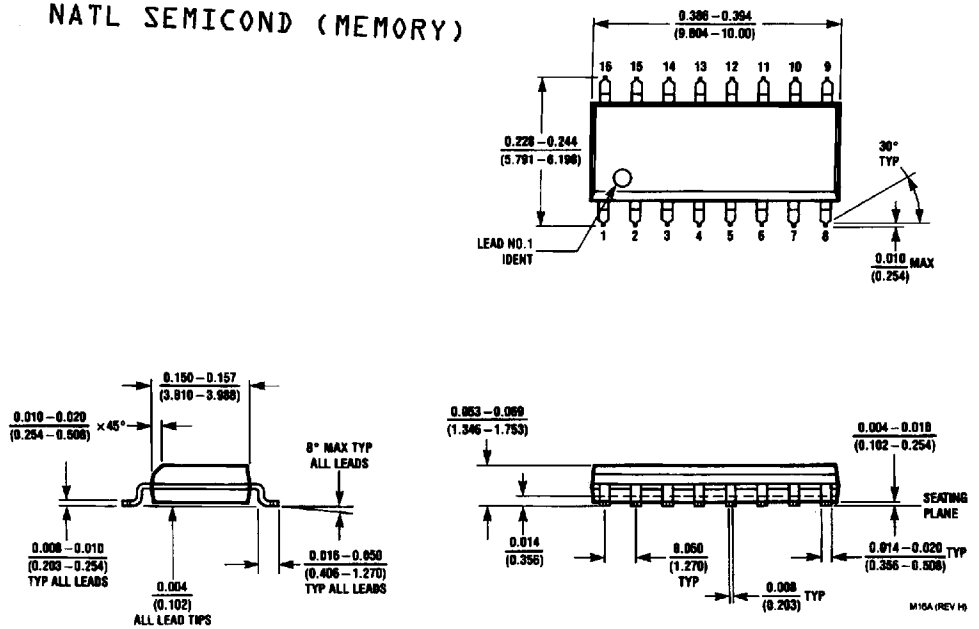
Temperature Range Family
- 74VHC = Commercial
- 54VHC = Military

Device Type

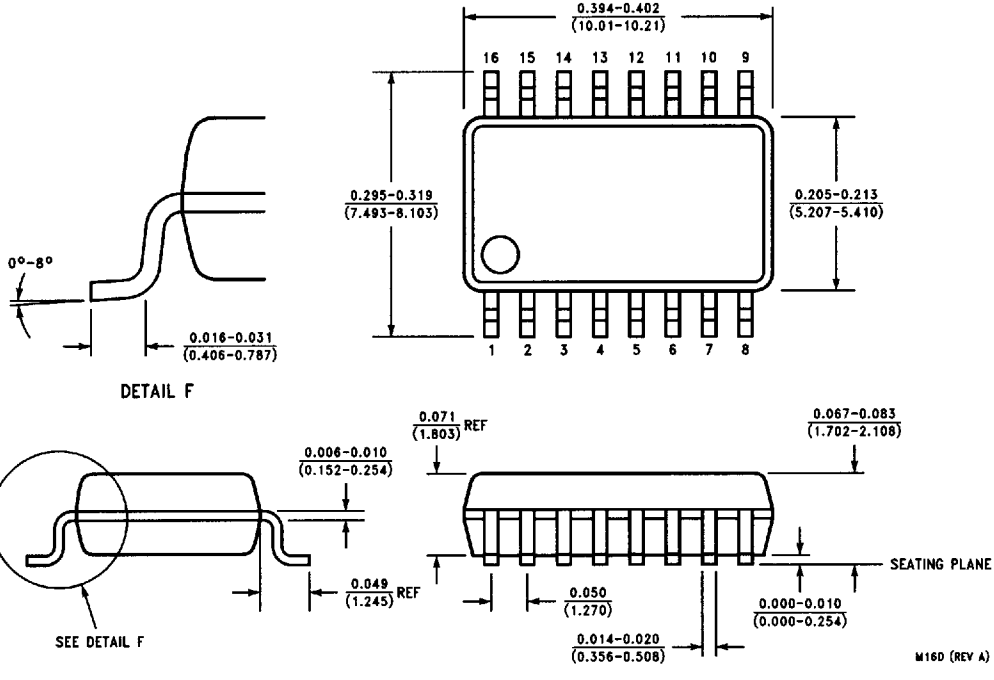
Package Code
- M = Small Outline JEDEC SOIC
- SJ = Small Outline EIAJ SOIC
- MSC = Shrink Small Outline EIAJ SSOP Type 1
- J/883 = Ceramic DIP
- W/883 = Ceramic Flatpak
- E/883 = Leadless Ceramic Chip Carrier

Special Variations
- "X" = Tape and Reel
- " " = Rail/Tube

Physical Dimensions inches (millimeters)

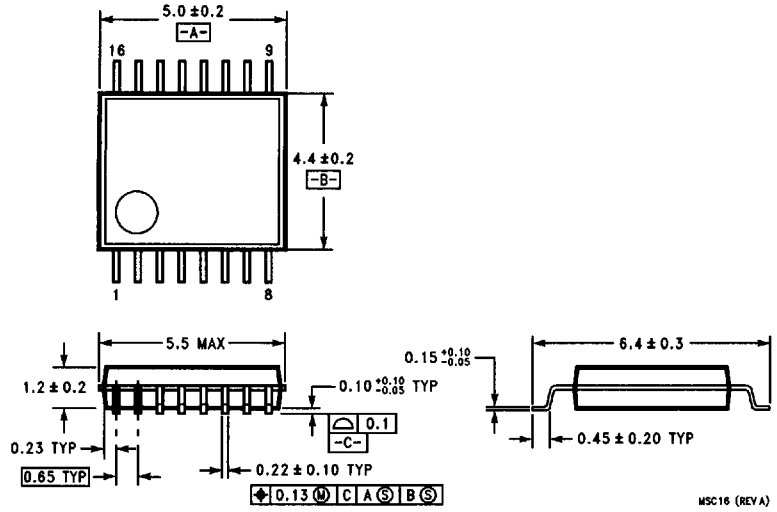


16-Lead Small Outline Integrated Circuit JEDEC SOIC (M)
NS Package Number M16A



16-Lead Plastic—EIAJ SOIC (SJ)
NS Package Number M16D

Physical Dimensions inches (millimeters) (Continued)



16-Lead Plastic EIAJ SSOP Type I (MSC)
NS Package Number MSC16

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Fürstenfeldbruck
Germany
Tel: (0-81-41) 103-0
Telex: 527649
Fax: (0-81-41) 10-35-06

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15-3 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-3299-7001
FAX: 3-3299-7000

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 737-1600
Telex: 51292 NSHKL
Fax: (852) 736-9960

National Semiconductores Do Brazil Ltda.
Av. Brig. Faria Lima, 1409
6 Andar
Cep-01451, Paulistano,
Sao Paulo, SP, Brazil
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
16 Business Park Dr.
Notting Hill, VIC 3168
Australia
Tel: (3) 558-9999
Fax: (3) 558-9998