

Silicon NPN Power Transistors

2SD536

DESCRIPTION

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- With TO-3 package
- High voltage,high speed
- Low collector saturation voltage

APPLICATIONS

- Switching regulators
- DC-DC converters
- General purpose power amplifiers

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

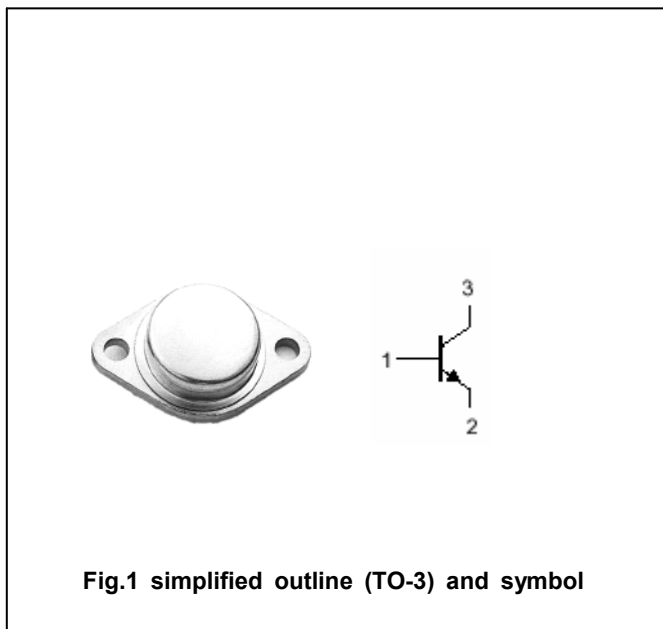


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	200	V
V _{CEO}	Collector-emitter voltage	Open base	200	V
V _{EBO}	Emitter-base voltage	Open collector	5	V
I _C	Collector current		10	A
I _B	Base current		5	A
P _C	Collector power dissipation	T _C =25□	100	W
T _j	Junction temperature		150	□
T _{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

T_j=25°C unless otherwise specified

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CE0(SUS)}	Collector-emitter sustaining voltage	I _C =100mA ; I _B =0	200			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =0.1mA ; I _E =0	200			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =0.1mA ; I _C =0	5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =5A ; I _B =1A			1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =5A ; I _B =1A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =200V ; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =5V ; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =5A ; V _{CE} =5V	50			

PACKAGE OUTLINE

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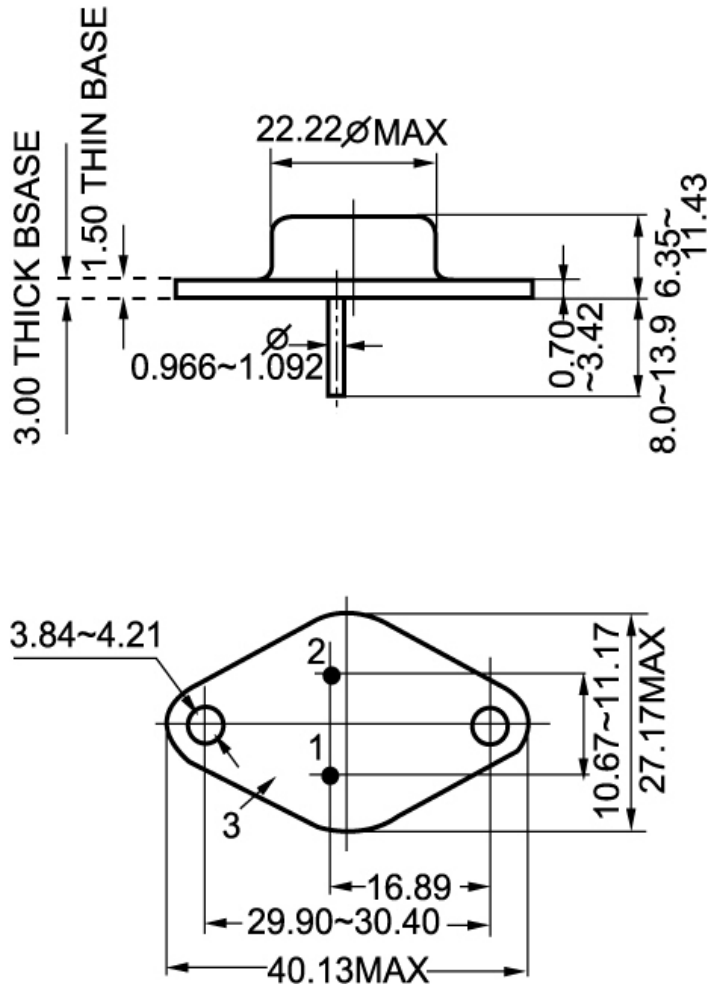


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)