

TENTATIVE TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

# TA1303AFN

## MIXER / OSCILLATOR BUILT-IN FREQUENCY SYNTHESIZER FOR VHF, CATV AND UHF BAND.

The TA1303AFN is a single chip which integrates a PLL and a MIX-OSC for VHF, CATV and UHF band.

The control data conforms to 3-wire bus and I<sup>2</sup>C bus formats. Bus-SW can be used to easily switch for easy tuner system set-up.

Flat, compact package : SSOP30 (0.65 mm pitch)

### FEATURES

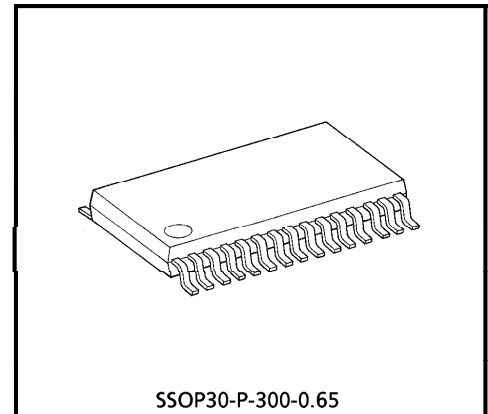
#### MIX-OSC block

- VHF·CATV bands : Mixer and Oscillator
- UHF bands : Mixer and Oscillator
- Built-in IF amplifier
- Single IF output terminal

#### PLL block

- Standard bi-directional I<sup>2</sup>C bus format control
- 3-wire bus format control
- 18-bit and 19-bit automatical discrimination circuit (when 3-wire bus selected)
- Tuning amplifier
- 4-bit bandswitch drive transistor
- 5-levels A/D convertor (when I<sup>2</sup>C bus selected)
- Frequency step : 31.25 kHz, 50 kHz and 62.5 kHz (at 4 MHz X'tal used)
- 4 programmable chip addresses (when I<sup>2</sup>C bus selected)
- Power on reset circuit
- 1/4 prescaler

(Note) These devices are easy to be damaged by high static voltage or electric fields.  
In regard to this, please handle with care.

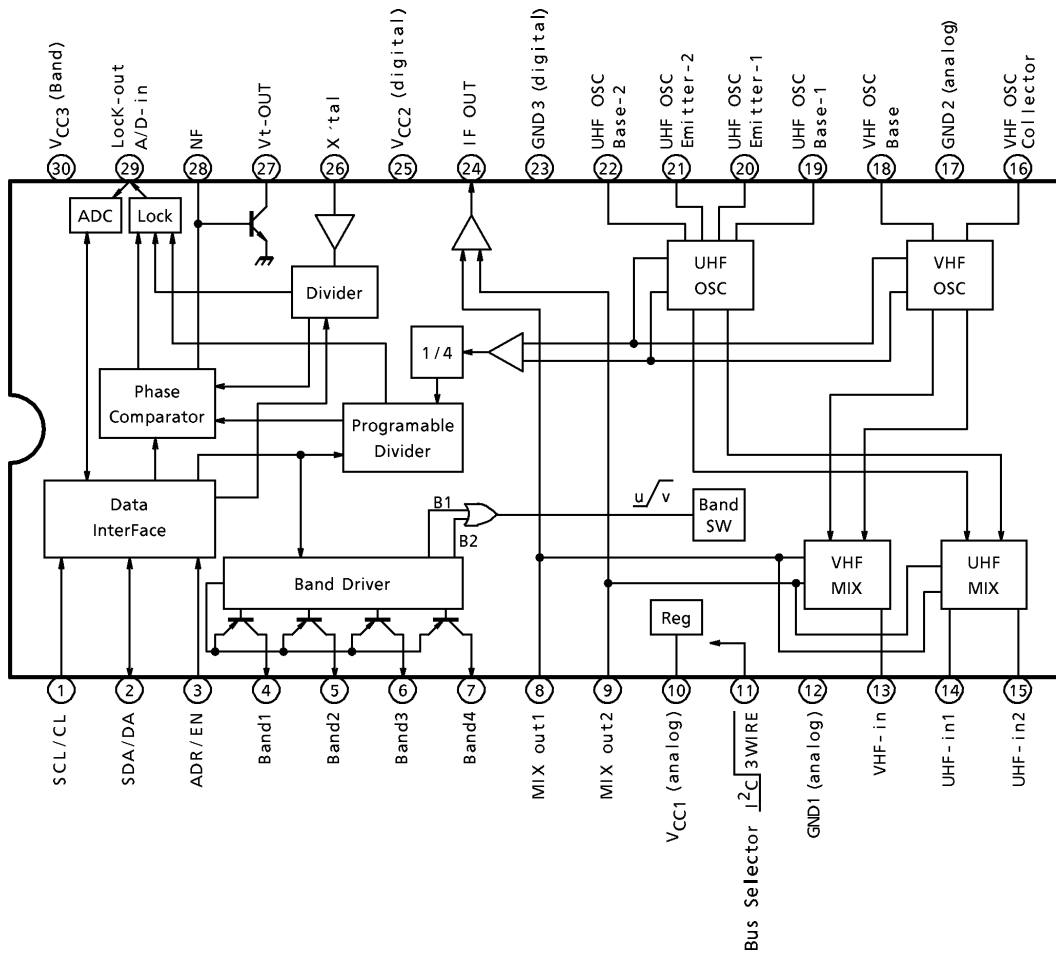


Weight : 0.17 g (Typ.)

980910EBA1

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**BLOCK DIAGRAM**



TERMINAL FUNCTION

| PIN No.          | PIN NAME    | FUNCTION  | INTERFACE |
|------------------|-------------|---|-----------|
| 1                | CL/SCL      | 3-wire bus : clock data input<br>I <sup>2</sup> C bus : serial clock data input<br>Please refer the description (Table. 1) on page 13.  |           |
| 2                | DA/SDA      | 3-wire bus : data input<br>I <sup>2</sup> C bus : serial data input/output<br>Please refer the description (Table. 1) on page 13.   |           |
| 3                | EN/ADR      | 3-wire bus : enable data input<br>I <sup>2</sup> C : address select input<br>Please refer the description (Table. 1) on page 13.  |           |
| 30               | VCC3        | This is power supply pin for Band circuits.<br>This can use, from 5 V to 9 V.   |           |
| 4<br>5<br>6<br>7 | Band1~Band4 | Output can be controlled by setting the band switch data.<br>U/V band can be switched by setting the band switch data.<br>Please refer the description (Table. 5) on page 21. |           |

| PIN No.  | PIN NAME       | FUNCTION   | INTERFACE |
|----------|----------------|--|-----------|
| 8<br>9   | MIX Output     | The output terminal of MIXER. For tuning, connect a tank circuit between pins 8 and 9.   |           |
| 10       | VCC1           | This is power supply pin for analog circuit  | —         |
| 11       | BUS-SW         | A changeover switch of control data. 3-wire bus and standard I <sup>2</sup> C bus are switches by the voltage applied on this pin. Please refer the description (Table. 1, 2) on page 13 and 14. |           |
| 12       | GND1           | This is the ground pin for analog circuit.   | —         |
| 13       | VHF Input      | VHF-RF input.  |           |
| 14<br>15 | UHF Input      | UHF-RF input. It is possible to input either balanced or unbalanced circuit.   |           |
| 16<br>18 | VHF Oscillator | VHF oscillator pins. In case of production abnormal oscillation, connect a resistor between pin 1 and the external capacitor.  |           |
| 17       | GND2           | This is the ground pin for analog circuit.   | —         |

| PIN No.              | PIN NAME           | FUNCTION   | INTERFACE |
|----------------------|--------------------|--|-----------|
| 19<br>20<br>21<br>22 | UHF Oscillator     | UHF oscillator pins.<br>They are colpitts oscillator.                          |           |
| 23                   | GND2               | This is the ground pin for digital circuit.                                    | —         |
| 24                   | IF Output          | Output terminal of IF signal which output impedance, 75 Ω.                     |           |
| 25                   | VCC2               | This is power supply pin for digital circuit.                                  | —         |
| 26                   | X'tal              | Crystal oscillator input.<br>At this block, the reference signal is generated. |           |
| 27                   | Charge Pump Output | Tuning voltage output terminal.<br>This LSI has a built-in tuning amplifier.   |           |
| 28                   | NF                 |  |           |

| PIN No. | PIN NAME                      | FUNCTION   | INTERFACE |
|---------|-------------------------------|--|-----------|
| 29      | ADC/ $\overline{\text{LOCK}}$ | <p>At 3 wire bus mode :<br/>this functions as lock detector.<br/>If the PLL has locked, the output becomes low.</p> <p>At I<sup>2</sup>C bus mode :<br/>this functions as terminal of AD convertor.<br/>This converts the input voltages into proper digital data.<br/>Please refer the description (Table. 6) on page 21.</p> |           |

**MAXIMUM RATINGS (Ta = 25°C)**

| CHARACTERISTIC        | SYMBOL           | RATING                    | UNIT       |
|-----------------------|------------------|---------------------------|------------|
| MIX-OSC Block         | V <sub>CC1</sub> | 6                         | V          |
|                       | f <sub>IN</sub>  | 120                       | dB $\mu$ V |
| PLL Block             | V <sub>CC2</sub> | 6                         | V          |
|                       | V <sub>CC3</sub> | 12                        | V          |
|                       | V <sub>BT</sub>  | 38                        | V          |
| Power Dissipation     | PD               | 780 [ IC only ]<br>(Note) | mW         |
| Operating Temperature | T <sub>opr</sub> | - 20~85                   | °C         |
| Storage Temperature   | T <sub>stg</sub> | - 55~150                  | °C         |

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 6.3 mW for each increase of 1°C.

**RECOMMENDED OPERATING CONDITION**

| PIN No. | SYMBOL        | MIN.             | TYP.             | MAX. | UNIT |   |
|---------|---------------|------------------|------------------|------|------|---|
| 10      | MIX-OSC block | V <sub>CC1</sub> | 4.5              | 5    | 5.5  | V |
| 25      | PLL block     | V <sub>CC2</sub> | 4.5              | 5    | 5.5  | V |
| 30      |               | V <sub>CC3</sub> | V <sub>CC2</sub> | —    | 9.9  | V |

**ELECTRICAL CHARACTERISTICS**

PC CHARACTERISTICS (Unless otherwise specified,  $V_{CC1} = 5V$ ,  $V_{CC2} = 5V$ ,  $V_{CC3} = 9V$ ,  $T_a = 25C^\circ$ )

| CHARACTERISTIC             |        | SYMBOL             | TEST CIRCUIT | BAND  | TEST CONDITION                                | MIN. | TYP. | MAX. | UNIT |
|----------------------------|--------|--------------------|--------------|---|---|------|------|------|------|
|                            |        |                    |              |   |   |      |      |      |      |
| Power Supply and Current 1 |        | I <sub>CC1-1</sub> | 1            | VHF   | —   | 24   | 32   | 40   | mA   |
|                            |        | I <sub>CC1-2</sub> |              | UHF   | —   | 26   | 34   | 43   |      |
| Power Supply and Current 2 |        | I <sub>CC2</sub>   |              | —   | —   | 12   | 16   | 21   |      |
| Power Supply and Current 3 |        | I <sub>CC3-1</sub> |              | —   | Band switch : 1 Band ON<br>IBD = 30 mA (LOAD) | —    | 34   | 36   |      |
|                            |        | I <sub>CC3-2</sub> | —            | Band switch : 2 Band ON<br>IBD = 40 mA (TOTAL LOAD) | —   | 48   | 52   |      |      |
| Terminal Voltage           | PIN 8  | V8-V               | 1            | VHF   | —   | 3.6  | 4.1  | 4.6  | V    |
|                            |        | V8-U               |              | UHF   | —   | 3.4  | 3.9  | 4.4  |      |
|                            | PIN 9  | V9-V               |              | VHF   | —   | 3.6  | 4.1  | 4.6  |      |
|                            |        | V9-U               |              | UHF   | —   | 3.4  | 3.9  | 4.4  |      |
|                            | PIN 13 | V13-V              |              | VHF   | —   | 1.8  | 2.1  | 2.4  |      |
|                            |        | V13-U              |              | UHF   | —   | 2.0  | 2.2  | 2.5  |      |
|                            | PIN 14 | V14-V              |              | VHF   | —   | 2.0  | 2.2  | 2.5  |      |
|                            |        | V14-U              |              | UHF   | —   | 1.7  | 2.0  | 2.4  |      |
|                            | PIN 15 | V15-V              |              | VHF   | —   | 2.0  | 2.2  | 2.5  |      |
|                            |        | V15-U              |              | UHF   | —   | 1.7  | 2.0  | 2.4  |      |
|                            | PIN 16 | V16-V              |              | VHF   | —   | 2.3  | 2.7  | 3.0  |      |
|                            |        | V16-U              |              | UHF   | —   | 3.8  | 4.1  | 4.4  |      |
|                            | PIN 18 | V18-V              |              | VHF   | —   | 1.7  | 2.2  | 2.7  |      |
|                            |        | V18-U              |              | UHF   | —   | 2.6  | 2.9  | 3.1  |      |
|                            | PIN 19 | V19-V              |              | VHF   | —   | 2.5  | 2.7  | 2.9  |      |
|                            |        | V19-U              |              | UHF   | —   | 2.1  | 2.4  | 2.7  |      |
|                            | PIN 20 | V20-V              |              | VHF   | —   | 1.9  | 2.2  | 2.5  |      |
|                            |        | V20-U              |              | UHF   | —   | 1.4  | 1.7  | 2.0  |      |
|                            | PIN 21 | V21-V              |              | VHF   | —   | 1.9  | 2.2  | 2.5  |      |
|                            |        | V21-U              |              | UHF   | —   | 1.4  | 1.7  | 2.0  |      |
| PIN 22                     | V22-V  | VHF                | —            | 2.5   | 2.7   | 2.9  |      |      |      |
|                            | V22-U  | UHF                | —            | 2.1   | 2.4   | 2.7  |      |      |      |
| PIN 24                     | V24    | —                  | —            | 1.9   | 2.3   | 2.6  |      |      |      |

**ELECTRICAL CHARACTERISTICS**

MIX-OSC block (Unless otherwise specified,  $V_{CC1} = 5V$ ,  $V_{CC2} = 5V$ ,  $V_{CC3} = 9V$ ,  $T_a = 25^\circ C$ )

| CHARACTERISTIC   | SYMBOL       | TEST CIR-CUIT | BAND | TEST CONDITION (*)  | MIN. | TYP. | MAX.      | UNIT       |
|--|--------------|---------------|------|---|------|------|-----------|------------|
|  |              |               |      |   |      |      |           |            |
| Conversion Gain<br>(Note 1)                                  | CG           | 3             | VHF  | $f_{RF} = 55.25 \text{ MHz}$  | 21   | 24   | 27        | dB         |
|  |              |               | VHF  | $f_{RF} = 367.25 \text{ MHz}$   | 21   | 24   | 27        |            |
|  |              |               | UHF  | $f_{RF} = 373.25 \text{ MHz}$   | 25   | 28   | 31        |            |
|  |              |               | UHF  | $f_{RF} = 801.25 \text{ MHz}$   | 25   | 28   | 31        |            |
| Noise Figure<br>(Note 2)                                     | NF           | 3             | VHF  | $f_{RF} = 55.25 \text{ MHz}$  | —    | 11   | 13        | dB         |
|  |              |               | VHF  | $f_{RF} = 367.25 \text{ MHz}$   | —    | 11   | 13        |            |
|  |              |               | UHF  | $f_{RF} = 373.25 \text{ MHz}$   | —    | 8.5  | 11        |            |
|  |              |               | UHF  | $f_{RF} = 801.25 \text{ MHz}$   | —    | 9.5  | 12        |            |
| IF Out Power Level<br>(Note 3)                               | IFp          | 3             | VHF  | $f_{RF} = 55.25 \text{ MHz}$  | 6    | 8.5  | —         | dBmW       |
|  |              |               | VHF  | $f_{RF} = 367.25 \text{ MHz}$   | 6    | 8.5  | —         |            |
|  |              |               | UHF  | $f_{RF} = 373.25 \text{ MHz}$   | 6    | 8.5  | —         |            |
|  |              |               | UHF  | $f_{RF} = 801.25 \text{ MHz}$   | 6    | 8.5  | —         |            |
| Conversion Gain Shift<br>(Note 4)                            | CGs          | 3             | VHF  | $f_{RF} = 55.25 \text{ MHz}$  | —    | —    | $\pm 0.5$ | dB         |
|  |              |               | VHF  | $f_{RF} = 367.25 \text{ MHz}$   | —    | —    | $\pm 0.5$ |            |
|  |              |               | UHF  | $f_{RF} = 373.25 \text{ MHz}$   | —    | —    | $\pm 0.5$ |            |
|  |              |               | UHF  | $f_{RF} = 801.25 \text{ MHz}$   | —    | —    | $\pm 0.5$ |            |
| Frequency Shift (The PLL<br>is not operating)<br>(Note 5)    | $\Delta f_B$ | 3             | VHF  | $f_{osc} = 101 \text{ MHz}$   | —    | —    | $\pm 100$ | kHz        |
|  |              |               | VHF  | $f_{osc} = 413 \text{ MHz}$   | —    | —    | $\pm 150$ |            |
|  |              |               | UHF  | $f_{osc} = 419 \text{ MHz}$   | —    | —    | $\pm 150$ |            |
|  |              |               | UHF  | $f_{osc} = 847 \text{ MHz}$   | —    | —    | $\pm 150$ |            |
| Switching On Drift (The<br>PLL is not operating)<br>(Note 6) | $\Delta f_s$ | 3             | VHF  | $f_{osc} = 101 \text{ MHz}$   | —    | —    | $\pm 100$ | kHz        |
|  |              |               | VHF  | $f_{osc} = 413 \text{ MHz}$   | —    | —    | $\pm 200$ |            |
|  |              |               | UHF  | $f_{osc} = 419 \text{ MHz}$   | —    | —    | $\pm 150$ |            |
|  |              |               | UHF  | $f_{osc} = 847 \text{ MHz}$   | —    | —    | $\pm 200$ |            |
| 1% Cross Modulation<br>(Note 7)                              | CM           | 3             | VHF  | $f_D = 55.25 \text{ MHz}$   | 81   | 85   | —         | dB $\mu$ V |
|  |              |               | VHF  | $f_D = 367.25 \text{ MHz}$  | 80   | 84   | —         |            |
|  |              |               | UHF  | $f_D = 373.25 \text{ MHz}$  | 76   | 80   | —         |            |
|  |              |               | UHF  | $f_D = 801.25 \text{ MHz}$  | 76   | 80   | —         |            |
| 3rd Inter Modulation<br>(Note 8)                             | IM3          | 3             | VHF  | $f_D = 55.25 \text{ MHz}$   | 49   | 54   | —         | dB         |
|  |              |               | VHF  | $f_D = 367.25 \text{ MHz}$  | 50   | 55   | —         |            |
|  |              |               | UHF  | $f_D = 373.25 \text{ MHz}$  | 38   | 45   | —         |            |
|  |              |               | UHF  | $f_D = 801.25 \text{ MHz}$  | 38   | 45   | —         |            |
| 6-ch Beat<br>(Note 9)  | B6           | 3             | VHF  | $f_p = 83.25 \text{ MHz}$<br>$f_s = 87.75 \text{ MHz}$  | 49   | 50   | —         | dB         |
| Prescaler Beat<br>(Note 10)                                  | Bpre         | 3             | VHF  | $f_{osc} = 167 \text{ MHz (A-ch),}$<br>$173 \text{ MHz (B-ch),}$<br>$179 \text{ MHz (C-ch),}$<br>$185 \text{ MHz (D-ch)}$ | —    | 13   | 18        | dB $\mu$ V |

(\*) IF : 45.75 MHz



PLL block (Unless otherwise specified,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $V_{CC3} = 9\text{ V}$ ,  $T_a = 25\text{ C}^\circ$ )

| CHARACTERISTIC                               | SYMBOL             | TEST CIR-CUIT | TEST CONDITION  | MIN.                  | TYP.                  | MAX.                  | UNIT              |
|--|--------------------|---------------|---|-----------------------|-----------------------|-----------------------|-------------------|
| Bandswitch Drive Current                     | IBD                | 1             | Maximum drive current / 1 port                              | —                     | —                     | 30                    | mA                |
| Bandswitch Drive Maximum LOAD                | IBD <sub>MAX</sub> | 1             | Maximum total drive current                                 | —                     | —                     | 50                    | mA                |
| Bandswitch Drive Voltage Drop                | VBD Sat            | 1             | IBD = 30 mA   | —                     | 0.15                  | 0.2                   | V                 |
| Tuning Amplifier Output Voltage (Close Loop) | Vt Out             | —             | $V_{BT} = 33\text{ V}$ , $R_L = 33\text{ [k}\Omega\text{]}$ | 0.3                   | —                     | 33                    | V                 |
| Tuning Amplifier Maximum Current             | IVt                | —             | $V_{BT} = 33\text{ V}$                                      | —                     | —                     | 3                     | mA                |
| X'tal Negative Resistance                    | XtR                | 1             |   | 1                     | 2.5                   | —                     | k $\Omega$        |
| X'tal Operating Range                        | OSC $f_{in}$       | 1             | —   | 3.2                   | —                     | 4.5                   | MHz               |
| X'tal External Input Level                   | OSC <sub>in</sub>  | 2             | —   | 100                   | —                     | 1000                  | mV <sub>p-p</sub> |
| Lock Output Low Voltage                      | VLKL               | 1             | (Lock mode, 3-wire bus mode)                                | —                     | —                     | 0.4                   | V                 |
| Lock Output High Voltage                     | VLKH               | 1             | (Unlock mode, 3-wire bus mode)                              | 4.6                   | —                     | —                     | V                 |
| Logic Input Low Voltage                      | VBsL               | 1             | Pins 1 to 3   | -0.3                  | —                     | 1.5                   | V                 |
| Logic Input High Voltage                     | VBsH               | 1             | Pins 1 to 3   | 3                     | —                     | $V_{CC2} + 0.3$       | V                 |
| Logic Input Current (Low)                    | IBsL               | 1             | Pin 1<br>Pin 3  | -20<br>-55            | —                     | 10<br>-20             | $\mu\text{A}$     |
| Logic Input Current (High)                   | IBsH               | 1             | Pin 1, Pin 2<br>Pin 3                                       | -10<br>75             | —                     | 20<br>150             |                   |
| Bus-SW Low Input Voltage                     | VBIL               | 1             | —   | 0                     | —                     | 0.8                   | V                 |
| Bus-SW High Input Voltage                    | VBIH               | 1             | —   | 4.2                   | —                     | $V_{CC2}$             |                   |
| Bus-SW Low Current (Low)                     | IBIL               | 1             | —   | -200                  | —                     | —                     | $\mu\text{A}$     |
| Bus-SW Low Current (High)                    | IBIH               | 1             | —   | —                     | —                     | 200                   | $\mu\text{A}$     |
| Charge Pump Output Current                   | Ichg               | 1             | CP = 『 0 』<br>CP = 『 1 』                                    | $\pm 30$<br>$\pm 140$ | $\pm 60$<br>$\pm 280$ | $\pm 90$<br>$\pm 420$ | $\mu\text{A}$     |
| ACK Output Voltage                           | V <sub>ACK</sub>   | 1             | I <sub>SINK</sub> = 3 mA (I <sup>2</sup> C-bus mode)        | —                     | —                     | 0.4                   | V                 |

| CHARACTERISTIC                                   | SYMBOL       | TEST CIR-CUIT | TEST CONDITION  | MIN. | TYP. | MAX.    | UNIT    |    |
|--|--------------|---------------|---|------|------|---------|---------|----|
| Set-up Time                                      | $T_S$        | —             | (3-wire bus mode)<br>Refer to data timing chart           | 2    | —    | —       | $\mu$ S |    |
| Enable Hold Time                                 | $T_{SL}$     |               |   | 2    | —    | —       |         |    |
| Next Enable Stop Time                            | $T_{NE}$     |               |   | 6    | —    | —       |         |    |
| Next Clock Stop Time                             | $T_{NC}$     |               |   | 6    | —    | —       |         |    |
| Clock Width                                      | $T_C$        |               |   | 2    | —    | —       |         |    |
| Enable Set-up Time                               | $T_L$        |               |   | 10   | —    | —       |         |    |
| Data Hold Time                                   | $T_H$        |               |   | 2    | —    | —       |         |    |
| SCL Clock Frequency                              | $f_{SCL}$    |               | 0   | —    | 100  | kHz     |         |    |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$    |               | (I <sup>2</sup> C bus mode)<br>Refer to data timing chart | 4.7  | —    | —       | $\mu$ S |    |
| Hold Time (Repeated) START Condition             | $t_{HD;STA}$ |               |   | 4.0  | —    | —       |         |    |
| Low Period of the SCL Clock                      | $t_{LOW}$    |               |   | 4.7  | —    | —       |         |    |
| High Period of the SCL Clock                     | $t_{HIGH}$   |               |   | 4.0  | —    | —       |         |    |
| Set-up Time for a Repeated START Condition       | $t_{SU;STA}$ |               |   | 4.7  | —    | —       |         |    |
| Data Hold Time                                   | $t_{HD;DAT}$ |               |   | 0    | —    | —       |         |    |
| Data Set-up Time                                 | $t_{SU;DAT}$ |               |   | 250  | —    | —       |         |    |
| Rise Time of both SDA and SCL Signals            | $t_R$        |               |   | —    | —    | 1000    |         | ns |
| Fall Time of both SDA and SCL Signals            | $t_F$        |               |   | —    | —    | 300     |         |    |
| Set-up Time for STOP Condition                   | $t_{SU;STO}$ | 4.0           |   | —    | —    | $\mu$ S |         |    |

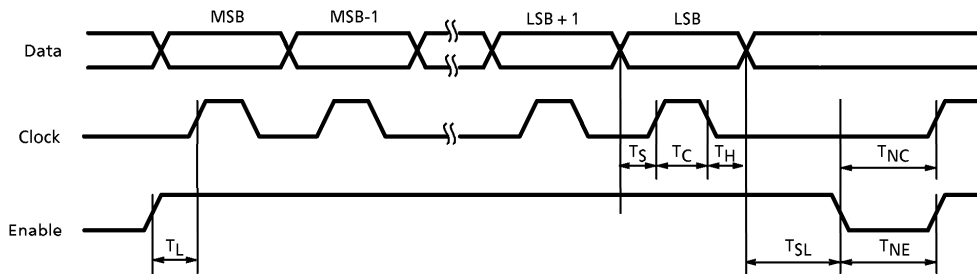


Fig.1 3-wire bus data timing chart (Falling edge timing)

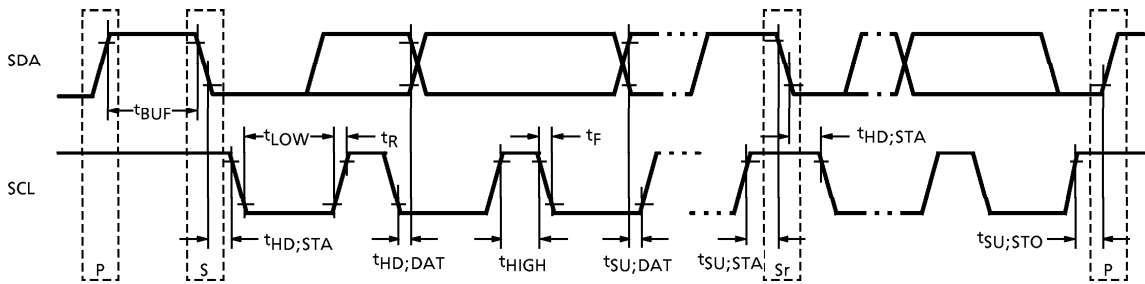


Fig.2 I<sup>2</sup>C bus data timing chart (Rising edge timing)

REFERENCE DATA ( $V_{CC1} = 5V, V_{CC2} = 5V, V_{CC3} = 9V, T_a = 25C^\circ$ )

| CHARACTERISTIC   | SYMBOL   | TEST CIR-CUIT | BAND | TEST CONDITION  | MIN. | TYP. | MAX. | UNIT |
|--|----------|---------------|------|---|------|------|------|------|
|  |          |               |      |   |      |      |      |      |
| Lock Up Time   | Lupt     | 3             | VHF  | $f_{osc} = 101\text{ MHz} \rightarrow f_{osc} = 173\text{ MHz}$           | —    | 40   | —    | ms   |
|  |          |               | VHF  | $f_{osc} = 179\text{ MHz} \rightarrow f_{osc} = 413\text{ MHz}$           | —    | 60   | —    |      |
|  |          |               | UHF  | $f_{osc} = 419\text{ MHz} \rightarrow f_{osc} = 847\text{ MHz}$           | —    | 30   | —    |      |
| Reference Leak Suppression Level                           | fref S/I | 3             | VHF  | $f_{RF} = 55.25\text{ MHz}$ (-30 dBmW入力)<br>(CP = 「1」、fref = 15.625 kHz)  | —    | 65   | —    | dB   |
|  |          |               | VHF  | $f_{RF} = 367.25\text{ MHz}$ (-30 dBmW入力)<br>(CP = 「1」、fref = 15.625 kHz) | —    | 60   | —    |      |
|  |          |               | UHF  | $f_{RF} = 373.25\text{ MHz}$ (-30 dBmW入力)<br>(CP = 「1」、fref = 15.625 kHz) | —    | 48   | —    |      |
|  |          |               | UHF  | $f_{RF} = 801.25\text{ MHz}$ (-30 dBmW入力)<br>(CP = 「1」、fref = 15.625 kHz) | —    | 53   | —    |      |
| Local Oscillator Leak Level (To IF Output)<br>[Worst Case] | LOIF     | 3             | VHF  | $f_{osc} = 101\text{ MHz} \sim f_{osc} = 173\text{ MHz}$                  | —    | -36  | —    | dBmW |
|  |          |               | VHF  | $f_{osc} = 179\text{ MHz} \sim f_{osc} = 413\text{ MHz}$                  | —    | -36  | —    |      |
|  |          |               | UHF  | $f_{osc} = 419\text{ MHz} \sim f_{osc} = 847\text{ MHz}$                  | —    | -28  | —    |      |

## TEST CONDITIONS

(Note 1) Conversion Gain

$f_{RF}$  input level = -30 dBmW

(Note 2) Noise Figure

Noise Figure meter used.

(Note 3) IF Out Power Level

Measure IF output level when it is maximum level.

(Note 4) Conversion Gain Shift

The Conversion gain shift is defined as a change in conversion gain when supply voltage varies from  $V_{CC} = 5$  to 4.5 V or from  $V_{CC} = 5$  to 5.5 V.

(Note 5) Frequency Shift (The PLL is not operating)

The frequency shift is defined as a change in oscillator frequency when supply voltage varies from  $V_{CC} = 5$  to 4.5 V or from  $V_{CC} = 5$  to 5.5 V.

(Note 6) Switching On Drift (The PLL is not operating)

Measure frequency change from 2 seconds after switching on to 3 minutes.

(Note 7) 1% Cross Modulation

- $f_d = f_p$  ( $f_{dRF}$  input level = -30 dBmW)

- $f_{ud} = f_p + 12 \text{ MHz}$  100 kHz, 30%AM

Input two signals, and increase the  $f_{udRF}$  input level.

Measure the  $f_{udRF}$  input level when the suppression level reaches 56.5 dB.

(Note 8) 3rd Inter Modulation

- $f_d = f_p$  ( $f_{dRF}$  input level = -30 dBmW)

- $f_{ud} = f_p + 1 \text{ MHz}$  ( $f_{udRF}$  input level = -30 dBmW)

Input two signals, measure the suppression level.

(Note 9) 6-ch Beat

- $f_p = 83.25 \text{ MHz}$  ( $f_{pRF}$  input level = -30 dBmW)

- $f_s = 87.75 \text{ MHz}$  ( $f_{sRF}$  input level = -30 dBmW)

Input two signals, measure the suppression level IF output signal between below signals.

$$f_{udif1} = (f_p + f_s) - f_{osc} = (83.25 + 87.75) - 129 = 42 \text{ MHz}$$

$$f_{udif2} = (2 \times f_s) - f_{osc} = (2 \times 87.75) - 129 = 46.5 \text{ MHz}$$

(Note 10) Prescaler Beat

- $1/4 f_{osc} \text{ (A-ch)} = 1/4 \times 167 = 41.75 \text{ MHz}$

- $1/4 f_{osc} \text{ (B-ch)} = 1/4 \times 173 = 43.25 \text{ MHz}$

- $1/4 f_{osc} \text{ (C-ch)} = 1/4 \times 179 = 44.75 \text{ MHz}$

- $1/4 f_{osc} \text{ (D-ch)} = 1/4 \times 185 = 46.25 \text{ MHz}$

As for each channel, measure the level to IF output.

## PLL BLOCK

### Operation description

TA1303AFN can be controlled with either by 3-wire bus or standard I<sup>2</sup>C bus.

The 3-wire bus mode is equipped with an 18-bit / 19-bit automatic selection circuit.

Frequency steps can be switched, depending on the voltage applied to the BUS-SW pin.

The I<sup>2</sup>C bus conforms to the standard I<sup>2</sup>C bus format. The bus supports two-way bus communications control, consisting of WRITE mode where data are received and READ mode where data are transmitted. In READ mode, the voltage applied on the A/D converter input pin can be transmitted and output with 5-level resolution. (This function is only valid when the I<sup>2</sup>C bus is selected. When the 3-wire bus is selected, the A/D converter input pin functions as the  $\overline{\text{Lock}}$  output pin.)

Addresses can be set using the hardware bits. 4 programmable addresses are supported. 3-wire bus and standard I<sup>2</sup>C bus are switched by the voltage applied on the BUS-SW pin.

When the supply voltage ( $V_{CC2}$ ) is applied, the power-on reset circuit operates. Before data are input, counter data are all initialized to 『 0 』 ; band switches are all initialized to off.

### Function chart

Table. 1

| PIN NAME                       | 3-WIRE BUS                      | I <sup>2</sup> C BUS |
|--------------------------------|---------------------------------|----------------------|
| BUS-SW                         | 『 OPEN 』 or 『 V <sub>CC</sub> 』 | 『 GND 』              |
| CL / SCL                       | CLOCK INPUT                     | SCL INPUT            |
| DA / SDA                       | DATA INPUT                      | SDA IN / OUTPUT      |
| EN / ADR                       | ENABLE INPUT                    | ADDRESS              |
| $\overline{\text{Lock}}$ / ADC | $\overline{\text{Lock}}$        | ADC                  |

- 3-Wire bus communications control

The 3-wire bus uses normal 18-bit and 19-bit data (band switch information and programmable divider information) and 27-bit test data (charge-pump current setting, tuning amplifier on / off, reference frequency divider ratio setting, and testing item functions) are available.

The program frequency is sequentially calculated together with normal data and test data.

$$f_{osc} = f_r \times 4 \times N$$

$f_{osc}$  : Program frequency

$f_r$  : Phase comparator reference frequency

$N$  : Divider ratio

(1) Normal data

Depending on the voltage (OPEN, V<sub>CC</sub>) applied on the BUS-SW pin and the transfer DATA bit length, the X'tal divider ratio setting, phase comparator reference frequency, and step frequency of the normal data are as shown in the table below.

Normal data function table

Table. 2

| BUS-SW INPUT        | TRANSFER DATA | X'TAL RATIO   | REFERENCE FREQUENCY | STEP FREQUENCY |
|---------------------|---------------|---------------|---------------------|----------------|
| [ V <sub>CC</sub> ] | 18-bit        | Cannot be set | —                   | —              |
| [ V <sub>CC</sub> ] | 19-bit        | 1 / 320       | 12.5 kHz            | 50 kHz         |
| [ OPEN ]            | 18-bit        | 1 / 256       | 15.625 kHz          | 62.5 kHz       |
| [ OPEN ]            | 19-bit        | 1 / 512       | 7.8125 kHz          | 31.25 kHz      |

(Note 1) The step frequency at 4 MHz (X'tal used)

(Note 2) During OPEN, automatically set with transmitted bit length (18↔19 possible)

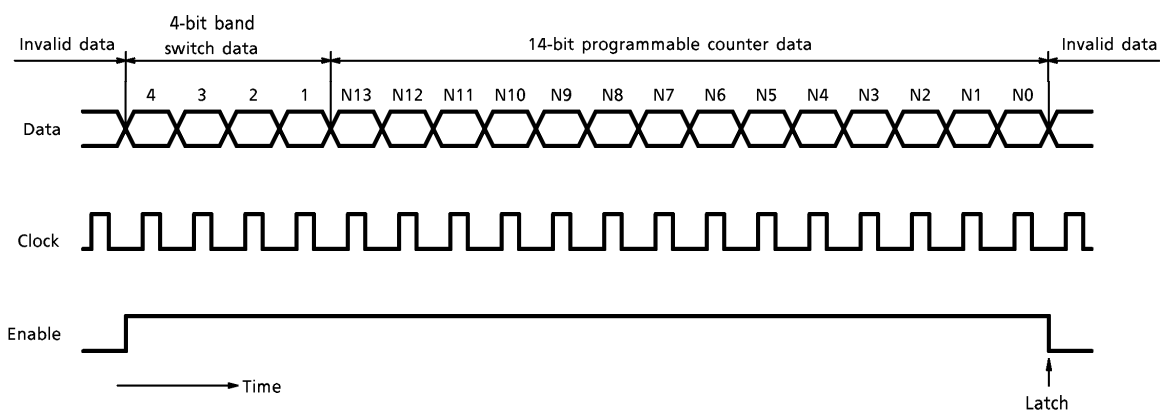


Fig.3 Normal data format (18-bit transmission)

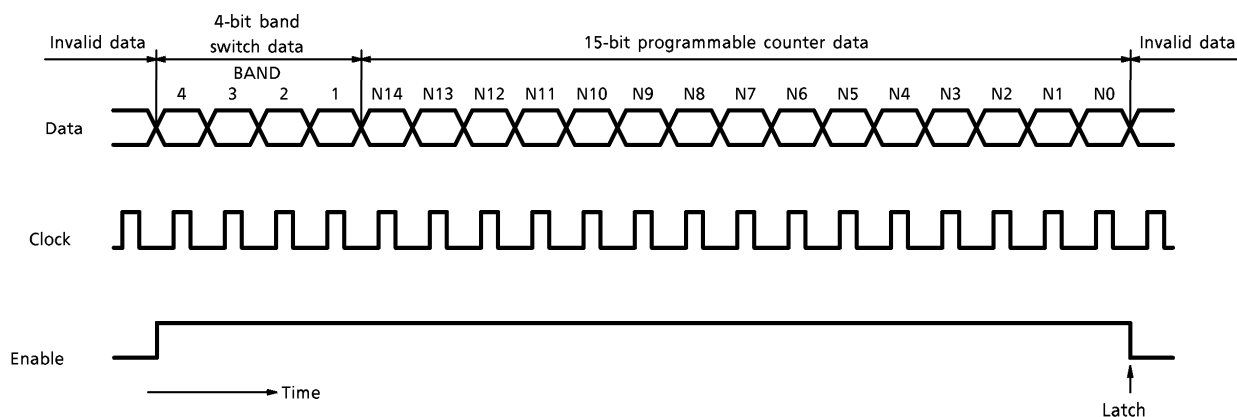


Fig.4 Normal data format (19-bit transmission)

a) 18-bit DATA TRANSMISSION :

During a high level of the enable signal, the data is clocked into the register on the falling edge of the clock.

Data are latched under the condition that the number of clocks while the enable signal is high is 18bits (the number of clock rising edges is 18).

Data are latched on the falling edge of the enable signal.

At 18-bit data transfer, N14 of the program divider is always automatically set to 『 0 』 ; the phase comparator reference frequency divider ratio is set to 1/256.

Please refer the description (Fig1. 3-wire bus data timing chart) on page 11.

b) 19-bit DATA TRANSMISSION :

During a high level of the enable signal, the data is clocked into register on the falling edge on the clock.

Data are latched under the condition that the number of clocks while the enable signal is high is 19bits (the number of clock rising edges is 19).

Data are latched on the falling edge of the enable signal.

At 19-bit data transfer, depending on the BUS-SW, the phase comparator reference frequency divider ratio is set to either 1/320 or 1/512.

Please refer the description (Fig1. 3-wire bus data timing chart) on page 11.

(2) TEST MODE

In the test mode, the settings can be changed and the function can be checked.

Change from the normal mode to the test mode with a 27-bit or more of clocks and data transmission during a high level of the enable signal.

The data are latched at the 27th falling edge of the clock signal, validating the previous 27-bit data. The latch timing is the same as normal data.

The 4-bit bandswitch data and the programmable divider data are latched at the 20th bit rising edge of the clock signal, and the data is updated.

The test data are latched at the 27th bit falling edge of the clock signal, and the data is updated.

When the mode is changed from test to normal, RSa changes depending on the data bit length (18 or 19 bits, automatic discrimination). The data set in RSb in test mode are retained (see the table below).

| REFERENCE FREQUENCY DIVIDER RATIO SETTING TEST MODE | DATA TRANSMISSION LENGTH | SET REFERENCE FREQUENCY DIVIDER RATIO |
|---|--------------------------|---------------------------------------|
| 1 / 256   | 18-bit                   | 1 / 256                               |
|   | 19-bit                   | 1 / 512                               |
| 1 / 320   | 18-bit                   | 1 / 320                               |
|   | 19-bit                   | 1 / 320                               |
| 1 / 512   | 18-bit                   | 1 / 256                               |
|   | 19-bit                   | 1 / 512                               |

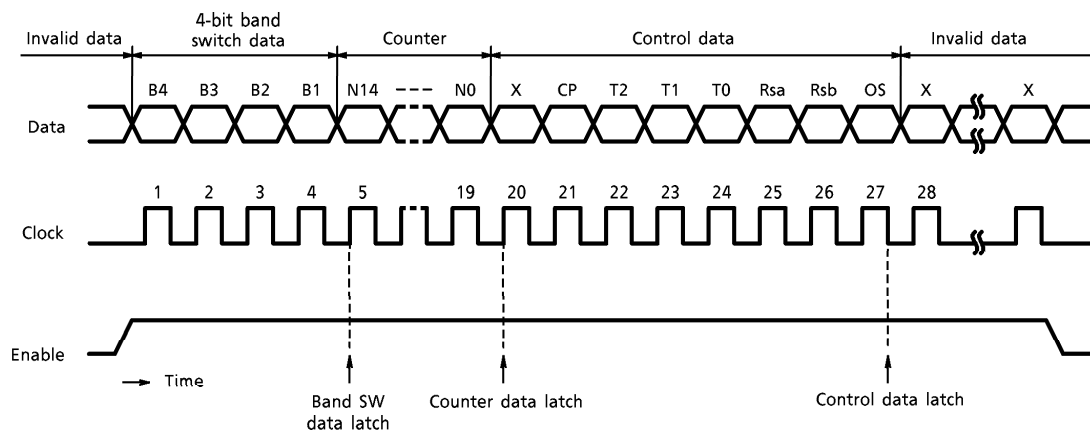


Fig.5 Test data format

(\*) The data timing is the same as normal data.



**TEST DATA SPECIFICATIONS**

- B4~1 : Band drive data  
     『 0 』 : OFF  
     『 1 』 : ON  
     When band drive data is 『 1 』 either Band 1 or Band 2, VHF mode.  
     When band drive data is 『 0 』 both Band 1 and Band 2, UHF mode.
- N14~N0 : Programmable counter data
- CP : Charge-pump output current  
     『 0 』 : ± 60 μA (Typ.)  
     『 1 』 : ± 280 μA (Typ.)
- T<sub>2</sub>, T<sub>1</sub>, T<sub>0</sub> : Test bits
- T<sub>2</sub>, T<sub>1</sub>, T<sub>0</sub> : Test mode setting

| CHARACTERISTIC             | T <sub>2</sub> | T <sub>1</sub> | T <sub>0</sub> | REMARKS  |   |
|----------------------------|----------------|----------------|----------------|--|---|
| Normal Operation           | 0              | 0              | 1              | —  |   |
| Charge-Pump                | OFF            | 0              | 1              | x  | Charge pump is "OFF" (Check output : NF)                    |
|                            | Sink           | 1              | 1              | 0  | Only charge pump Sink current is "ON" (Check output : NF)   |
|                            | Source         | 1              | 1              | 1  | Only charge pump Source current is "ON" (Check output : NF) |
| Reference Signal Output    | 1              | 0              | 0              | Reference signal output : $\overline{\text{Lock}}$                               |   |
| 1/2 Counter Divider Output | 1              | 0              | 1              | 1/2 counter output : $\overline{\text{Lock}}$                                    |   |
| Phase Comparator Test      | 0              | 0              | 0              | Comparative signal input : DA<br>Reference signal input : CL (Check output : NF) |   |

x : Don't Care

(Note) When testing the counter divider output, programmable counter data input is necessary.

- R<sub>sa</sub>, R<sub>sb</sub> : Reference frequency divider ratio select bit.
- R<sub>Sa</sub>, R<sub>Sb</sub> : X'tal reference frequency divider ratio select bits.

| DIVIDER RATIO | R <sub>Sa</sub> | R <sub>Sb</sub> |
|---------------|-----------------|-----------------|
| 1/256         | 1               | 1               |
| 1/512         | 0               | 1               |
| 1/320         | x               | 0               |

x : Don't Care

(Note) When the mode is changed from test to normal, R<sub>Sa</sub> changes depending on the data bit length (18 or 19 bits, automatic discrimination). The data set in R<sub>Sb</sub> in test mode are retained.

- OS : Tuning amplifier control bit  
     『 0 』 : Tuning amp ON (Normal operation)  
     『 1 』 : Tuning amp OFF (High impedance)
- x : Don't Care

- I<sup>2</sup>C Bus communications control

The TA1303AFN conforms to standard I<sup>2</sup>C bus format.

The I<sup>2</sup>C bus mode enables two-way bus communications with the WRITE mode, which receives data, and READ mode, which status data.

WRITE and READ modes are set using the last bit (R/W bit) of the address byte.

If the last address bit is set to [ 0 ], WRITE mode is set ; if set to [ 1 ], READ mode is set.

Addresses can be set using the hardware bits. 4 programmable addresses can be programmed.

With this setting, multiple frequency synthesizers can be used in the same I<sup>2</sup>C bus line.

The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR : Pin 3).

An address is selected according to the set bits.

When the correct address byte is received, during acknowledgment, serial data (SDA) line is "Low".

If WRITE mode is set at this time, when the data byte is programmed, the serial data (SDA) line is "Low" during the next acknowledgment. Please refer the description (Fig2. I<sup>2</sup>C bus data timing chart) on page 11.

(1) WRITE mode (setting command)

When WRITE mode is segment, byte 1 segment the address data ; bytes 2 and 3 segment the frequency data ; byte 4 segment the divider ratio setting and function setting data ; and byte 5 segment the output port data.

Data are latched and transferred at the end of, byte 3, byte 4, and byte 5.

Bytes 2 and 3 are latched and transferred is done with a two byte set (byte 2 + byte 3).

Once a correct address is received and acknowledged, the data type is determined according to [ 0 ] or [ 1 ] set in the first bit of the next byte. That is, if the first bit is [ 0 ], the data are frequency data ; if [ 1 ], function setting or output port data.

Until the I<sup>2</sup>C bus STOP CONDITION is detected, the additional data can be input without transmitting the address again. (EX : Frequency sweep is possible with additional frequency data.)

If data transmission is aborted, data programmed before the abort are valid.

Byte 1 can set the hardware bit with address data.

The hardware bit is set with voltage applied to the address setting pin (ADR : Pin 3).

Bytes 2 and 3 are stored in the 15-bit shift register with counter data for the frequency setting, and control the 15-bit programmable counter ratio.

The Lock frequency can be calculated in the following formula :

$$f_{osc} = f_r \times 4 \times N$$

$f_{osc}$  : Program frequency

$f_r$  : Phase comparator reference frequency (Step frequency)

$N$  : Counter total ratio

$f_r$  is calculated using the crystal oscillator frequency and the reference frequency divider ratio set in byte 4 (control byte). ( $f_r = X'tal \text{ oscillator frequency} / \text{reference frequency divider ratio}$ )

The reference frequency divider ratio can be set to, 1/256, 1/512, and 1/320. When using a 4MHz crystal oscillator,  $f_r = 15.625 \text{ kHz}$ ,  $7.8125 \text{ kHz}$ , and  $12.5 \text{ kHz}$ . The step frequency are  $62.5 \text{ kHz}$ ,  $31.25 \text{ kHz}$ , and  $50 \text{ kHz}$ .

Byte 4 is a control byte used to set functions. Bit 2 (CP) controls the output current of the charge-pump circuit. When bit 2 is set to  $\lceil 0 \rceil$ , the output current is set to  $\pm 60 \mu\text{A}$ ; when set to  $\lceil 1 \rceil$ ,  $\pm 280 \mu\text{A}$ .

Bit 3 ( $T_2$ ), bit 4 ( $T_1$ ) and bit 5 ( $T_0$ ) are used to set the test mode. They are used to set the charge-pump test, phase comparator reference signal output, and counter divider 1/2 output.

Please refer the description (Table. 3) on page 21.

Bit 6 (Rsa) and bit 7 (Rsb) are used to set the X'tal reference frequency divider ratios.

Please refer the description (Table. 4) on page 21.

Bit 8 (OS) is used to set the charge-pump drive amplifier output setting. When bit 8 is set to  $\lceil 0 \rceil$ , the output is ON (Normal use); when set to  $\lceil 1 \rceil$  the output is OFF (High impedance).

Byte 5 is used to set and control the output port (Bands 1~4). Select  $\lceil 0 \rceil$  for OFF, and  $\lceil 1 \rceil$  for ON. Please refer the description (Table. 5) on page 21.

When band switch data is  $\lceil 1 \rceil$  either Band 1 or Band 2, VHF mode.

When band switch data is  $\lceil 0 \rceil$  both Band 1 and Band 2, UHF mode.

Two output ports can be operation turned on, but be sure to keep the total output current under 50 mA.

## (2) READ mode (status request)

When READ mode is set, power-on reset operation status, phase comparator lock detector output status, and 5-level A/D converter pin input voltage status are output to the master device.

Bit 1 (POR) indicates the power-on reset operation status. When the power supply of  $V_{CC2}$  stops, bit 1 is set to  $\lceil 1 \rceil$ . The conditions for reset to  $\lceil 0 \rceil$  voltage supplied to  $V_{CC2}$  is 3V or higher, transmission is requested in READ mode, and the status is output. (When  $V_{CC2}$  is turned on, bit 1 is also set to  $\lceil 1 \rceil$ )

Bit 2 (FL) indicates the phase comparator lock status. When locked,  $\lceil 1 \rceil$  is output; when unlocked,  $\lceil 0 \rceil$  is output.

Bits 6, 7, and 8 ( $A_2$ ,  $A_1$ ,  $A_0$ ) indicate the 5-level A/D converter status. The voltage applied to the A/D converter input pin (pin 29) is output through a 5-level resolution.

Please refer the description (Table. 6) on page 21.

(EX : The AFT output voltage data can be given to the master device.)

**DATA FORMAT**

a) WRITE MODE

| BYTE |               | MSB |     |     |     |     |     |     | LSB     |      |
|------|---------------|-----|-----|-----|-----|-----|-----|-----|---------|------|
| 1    | Address Byte  | 1   | 1   | 0   | 0   | 0   | MA1 | MA0 | R/W = 0 | ACK  |
| 2    | Divider Byte① | 0   | N14 | N13 | N12 | N11 | N10 | N9  | N8      | ACK  |
| 3    | Divider Byte② | N7  | N6  | N5  | N4  | N3  | N2  | N1  | N0      | ACKⓁ |
| 4    | Control Byte  | 1   | CP  | T2  | T1  | T0  | RSa | RSb | OS      | ACKⓁ |
| 5    | Band SW Byte  | x   | x   | x   | x   | B4  | B3  | B2  | B1      | ACKⓁ |

x : DON'T Care  
 ACK : Acknowledged  
 Ⓛ : Latch and transfer timing

b) READ MODE

| BYTE |              | MSB |    |   |   |   |     |     | LSB     |     |
|------|--------------|-----|----|---|---|---|-----|-----|---------|-----|
| 1    | Address Byte | 1   | 1  | 0 | 0 | 0 | MA1 | MA0 | R/W = 1 | ACK |
| 2    | Status Byte  | POR | FL | 1 | 1 | 1 | A2  | A1  | A0      | —   |

x : DON'T Care  
 ACK : Acknowledged

**DATE SPECIFICATIONS**

- MA1, MA0 : Programmable hardware address bits

| ADDRESS PIN APPLIED VOLTAGE                            | MA1 | MA0 |
|--|-----|-----|
| 0~0.1 × V <sub>CC2</sub>                               | 0   | 0   |
| OPEN or 0.2 × V <sub>CC2</sub> ~0.3 × V <sub>CC2</sub> | 0   | 1   |
| 0.4 × V <sub>CC2</sub> ~0.6 × V <sub>CC2</sub>         | 1   | 0   |
| 0.9 × V <sub>CC2</sub> ~V <sub>CC2</sub>               | 1   | 1   |

- N14~N0 : Programmable counter data
- CP : Charge-pump output current setting  
 [ 0 ] : ± 60 μA (Typ.)  
 [ 1 ] : ± 280 μA (Typ.)

**Table. 3**

● T<sub>2</sub>, T<sub>1</sub>, T<sub>0</sub> : Test mode setting

| CHARACTERISTIC             | T <sub>2</sub> | T <sub>1</sub> | T <sub>0</sub> | REMARKS  |
|----------------------------|----------------|----------------|----------------|--|
| Normal Operation           | 0              | 0              | 1              | —  |
| Charge-Pump                | OFF            | 0              | 1              | × Charge-pump is "OFF" (Check output : NF)   |
|                            | Sink           | 1              | 1              | 0 Only charge-pump Sink current is "ON" (Check output : NF)                        |
|                            | Source         | 1              | 1              | 1 Only charge-pump Source current is "ON" (Check output : NF)                      |
| Reference Signal Output    | 1              | 0              | 0              | Reference signal output : ADC  |
| 1/2 Counter Divider Output | 1              | 0              | 1              | 1/2 counter divider output : ADC   |
| Phase Comparator Test      | 0              | 0              | 0              | Comparative signal input : SDA (Check output : NF)<br>Reference signal input : SCL |

× : DON'T Care

(Note) When testing the counter divider output, programmable counter data input is necessary.

**Table. 4**

● RSa, RSb : X'tal reference frequency divider ratio select bits.

| RSa | RSb | DIVIDER RATIO |
|-----|-----|---------------|
| 1   | 1   | 1/256         |
| 0   | 1   | 1/512         |
| ×   | 0   | 1/320         |

× : DON'T Care

- OS : Tuning amplifier control setting.  
     [ 0 ] : Tuning amplifier ON (Normal operation)  
     [ 1 ] : Tuning amplifier OFF (High impedance)

**Table. 5**

- B4~B1 : BAND switch data  
     [ 0 ] : OFF When band drive data is [ 1 ] either Band1 or Band2, VHF mode.  
     [ 1 ] : ON When band drive data is [ 0 ] both Band1 and Band2, UHF mode.
- POR : Power-on reset flag  
     [ 0 ] : Normal operation  
     [ 1 ] : Reset operation
- FL : Lock detect flag  
     [ 0 ] : Unlocked  
     [ 1 ] : Locked
- A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub> : 5-level A/D converter status.

**Table. 6**

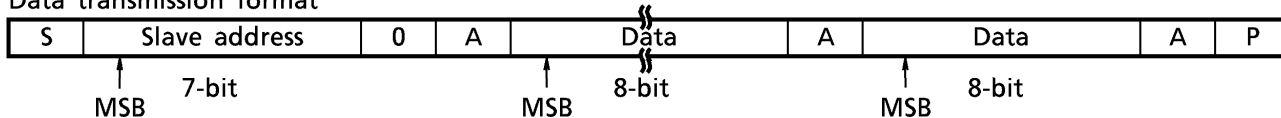
| ADC PIN APPLIED VOLTAGE                          | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |
|--|----------------|----------------|----------------|
| 0.60 × V <sub>CC2</sub> ~V <sub>CC2</sub>        | 1              | 0              | 0              |
| 0.45 × V <sub>CC2</sub> ~0.60 × V <sub>CC2</sub> | 0              | 1              | 1              |
| 0.30 × V <sub>CC2</sub> ~0.45 × V <sub>CC2</sub> | 0              | 1              | 0              |
| 0.15 × V <sub>CC2</sub> ~0.30 × V <sub>CC2</sub> | 0              | 0              | 1              |
| 0~0.15 × V <sub>CC2</sub>                        | 0              | 0              | 0              |

(\*) Accuracy is ± 0.03 × V<sub>CC2</sub>

**I<sup>2</sup>C BUS CONTROL SUMMARY**

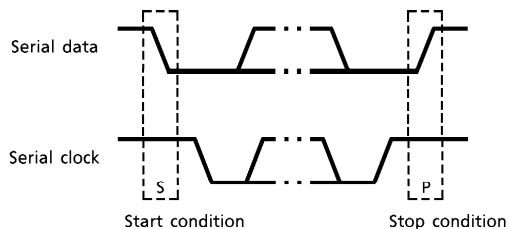
The bus control format for TA1303AFN conforms to the Philips I<sup>2</sup>C bus control format.

**Data transmission format**

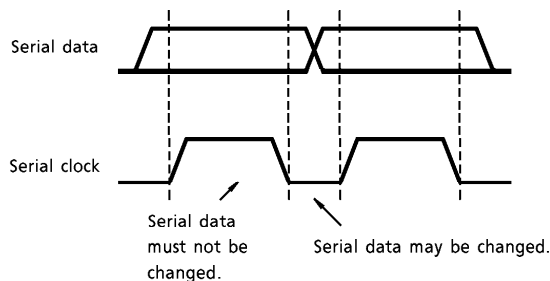


S : Start condition  
 P : Stop condition  
 A : Acknowledge

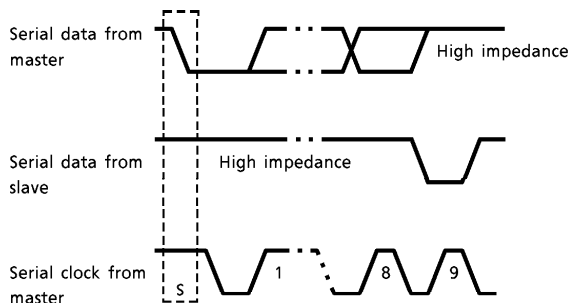
**(1) Start/stop conditions**



**(2) Bit transfer**



**(3) Acknowledge**

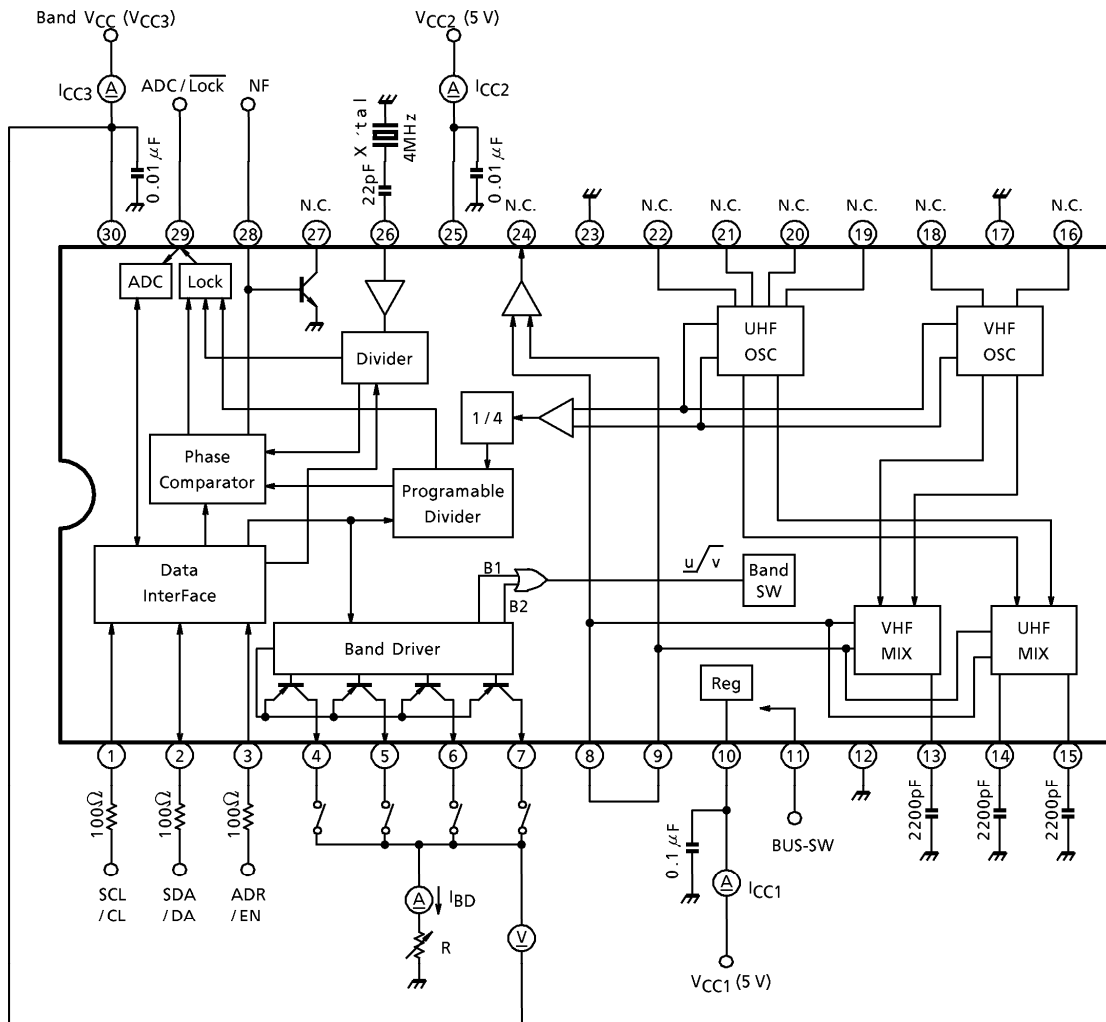


**(4) Slave addresses**

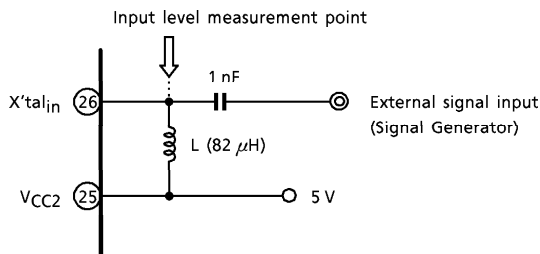
| A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | R/ $\bar{W}$ |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------|
| 1              | 1              | 0              | 0              | 0              | *              | *              | 0            |

Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Tights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

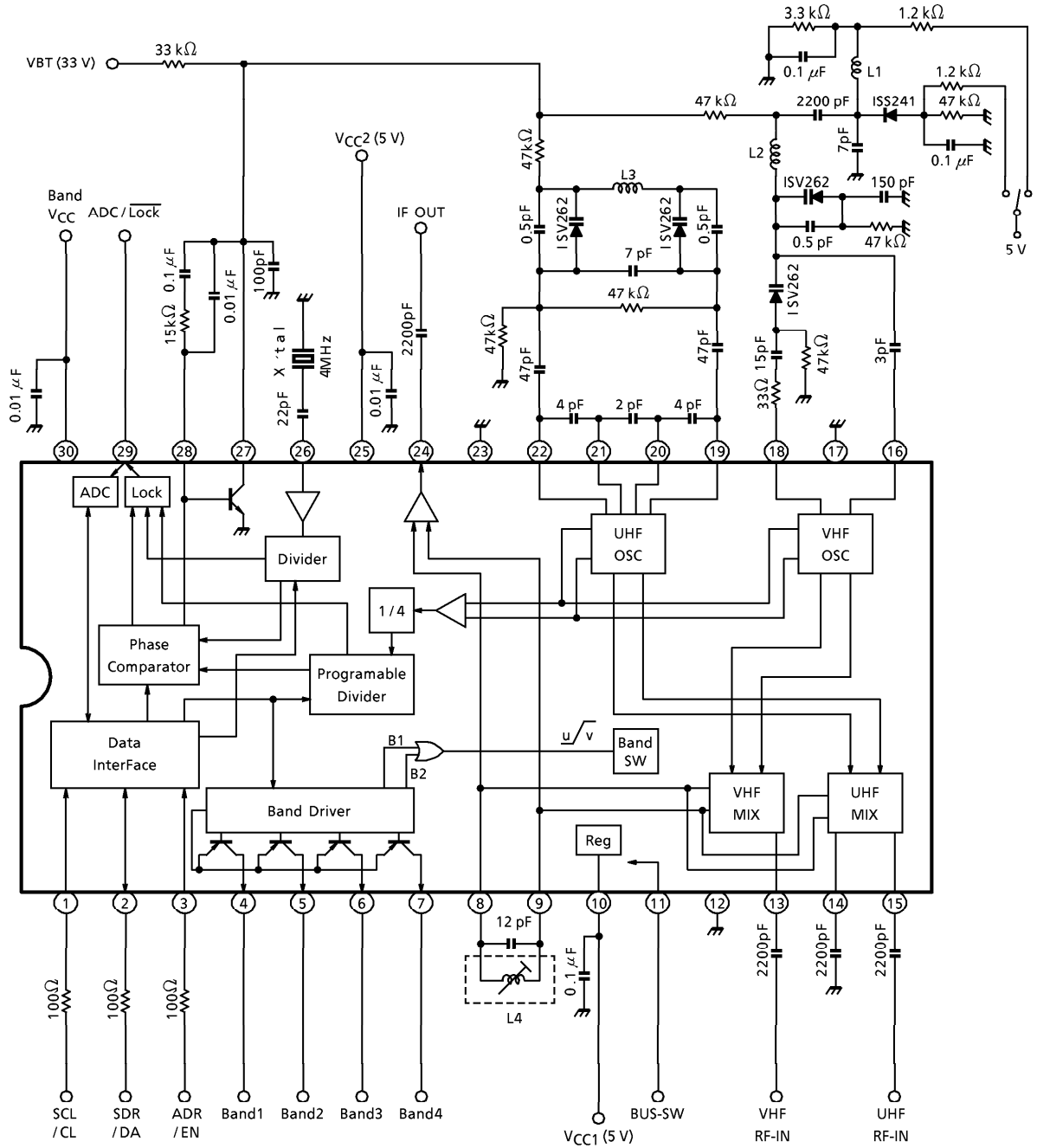
**TEST CIRCUIT 1**  
DC characteristics



**TEST CIRCUIT 2**  
X'tal external input measurement



**TEST CIRCUIT 3**  
AC characteristics



|    | LINE DIAMETER | TURN DIAMETER | NUMBER OF TURNS |
|----|---------------|---------------|-----------------|
| L1 | 0.3 mm        | 2.0 mm        | 7.5 T           |
| L2 | 0.3 mm        | 2.0 mm        | 2.5 T           |
| L3 | 0.3 mm        | 2.5 mm        | 2.5 T           |

L4 : 0.9 μH ± 5%

Band1 / Band2 = VHF-L or VHF-H  
Band3 / Band4 = UHF or FMIT



[REFERENCE DATA]

X'tal External Input Level

If it uses not only "TEST CIRCUIT 2" but "Fig.6", please refers to "Graph 1".

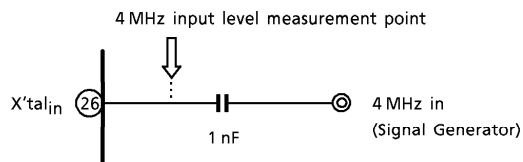
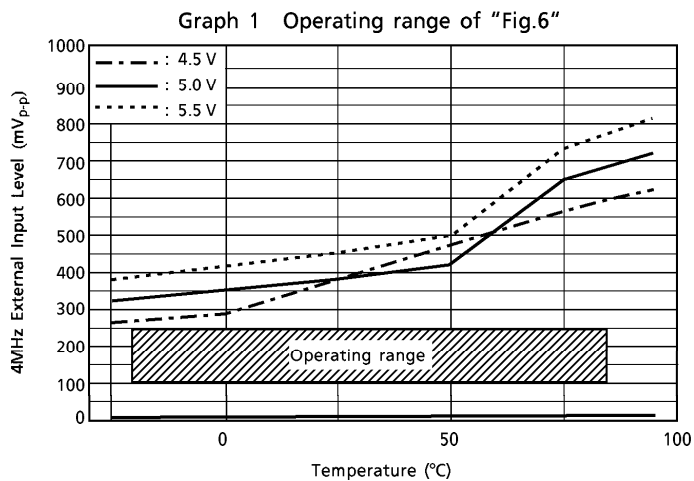
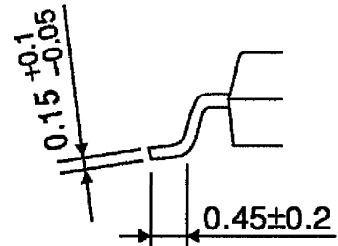
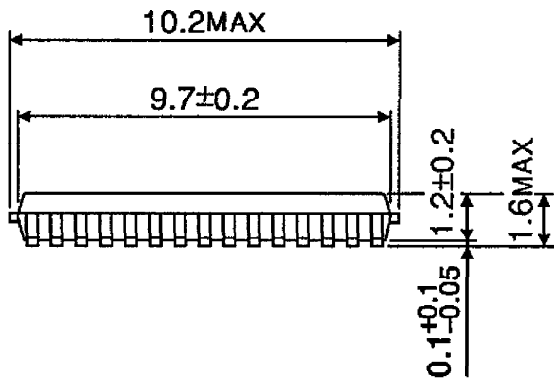
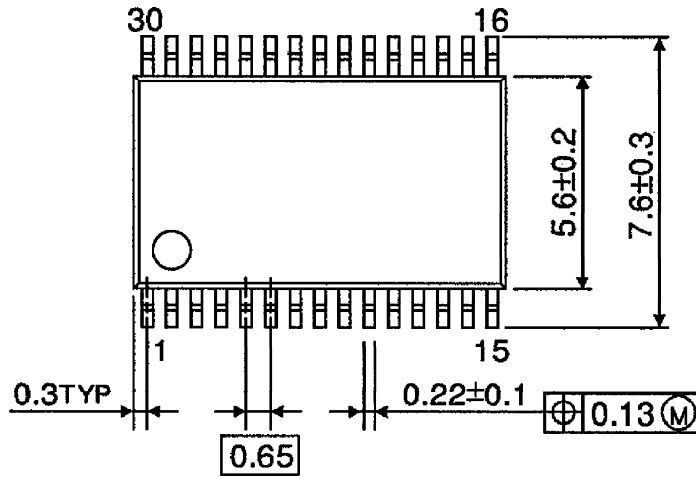


Fig.6 X'tal External Input Reference Application



OUTLINE DRAWING  
SSOP30-P-300-0.65

Unit : mm



Weight : 0.17 g (Typ.)