iT4031F
100-ps Wideband Phase Delay

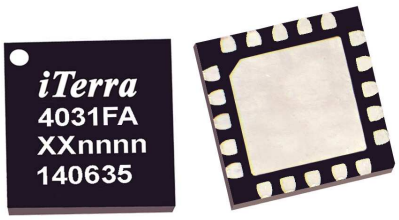
Description

The iT4031F is a RoHS-6-compliant, ultra-wideband phase delay fabricated using 1-um HBT GaAs technology and is based on ECL topology to guarantee high-speed operation. The high output voltage, excellent rise and fall time, and the high eye diagram quality at data rates to 12.5 Gb/s makes the iT4031F is suitable for timing adjustment in data and clock distribution at very high speed. Complex digital applications benefit from the iT4031F, including clock data recovery, edge detectors, NRZ-to-RZ converters, MUX/DEMUX, and data restoration.

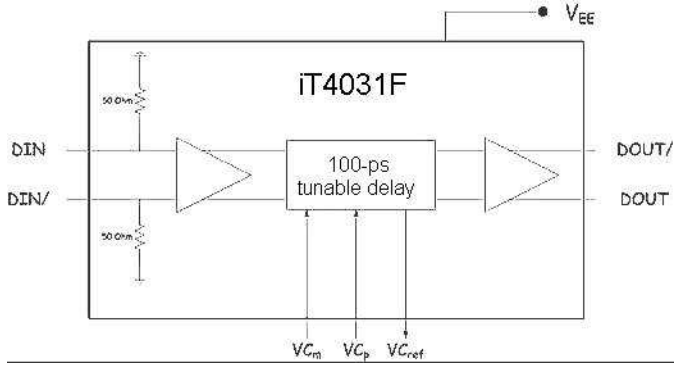
The device features a single delay element that provides up to 100-ps delay. Delay control can be either differential (using both VCp and VCm) or single-ended (VCm is the active control pad while VCp is shorted to VCref). The control voltage range for the delay input is from -2.2 V to -3.0 V whether the control is single-ended or differential. The device can delay NRZ streams with data rates to 12.5 Gb/s or a clock signal up to 10.7 GHz. Both inputs and outputs are DC-coupled. The iT4031F uses SCFL I/O levels and is designed so to allow for either single ended or differential data input.

Features

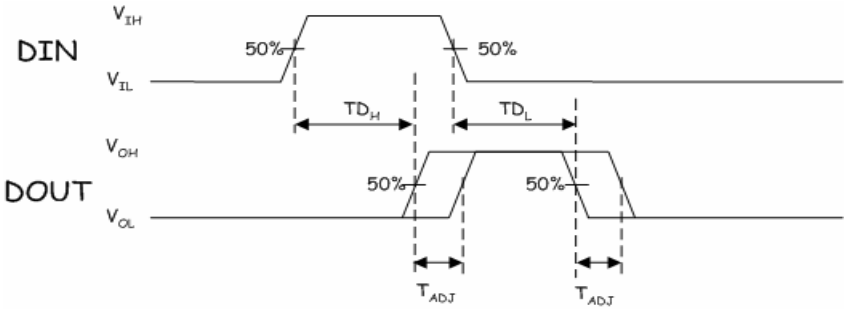
- Ultra wideband: Up to 12.5 Gb/s NRZ
- Delay adjustment to 100 ps
- 900 mVpp single-ended output
- Jitter degradation RMS: <1.5 ps
- Output rise time (20% – 80 %):25 ps typical
- Output fall time (20% – 80 %): 23 ps typical
- Differential or single-ended I/O
- Power consumption: 1.65 W
- Output impedance: 300 ohms
- RoHS-6 compliant 5x5-mm QFN (MO-220) package



Device Diagram



Timing Diagram



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Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
VEE	Power supply voltage	-5.5	0	V
VIH	Input voltage level, high level	-1.5	1.5	V
VIL	Input voltage level, low level	-1.5	1.5	V
VC	Delay control voltage	-5.0	0	V
TA	Operating temperature range – die	-15	125	°C
TSTG	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
T_A	Operating temperature range – die	0		85	°C
V_{EE}	Power supply voltage		-5		V
VC	Delay control voltage	-3.0	-2.6	-2.2	V
V_{IH}	Input voltage level, high level (single ended)		0.0		V
V_{IL}	Input voltage level, low level (single ended)		-0.9		V
V_{INDC}	DC input voltage (with DC-coupled input)		-0.45		V

Electrical Characteristics

1. Electrical characteristics at ambient temperature.
2. In case of single-ended input, the unused pad must be tied to VINDC.
3. In case of single-ended output, the unused pad must be terminated with 50 ohms to ground.
4. Refer to timing diagram.

Symbol	Parameters	Min.	Typ.	Max.	Units
VEE	Power supply voltage	-4.5	-5.00	-5.25	V
VIH	Input voltage level, high level (single ended)		0.0		V
VIL	Input voltage level, low level (single ended)		-0.9		V
VINDC	DC input voltage (with DC-coupled input) (2)		-0.45		V
VOUT	Data output voltage amplidude (3)	0.8	0.9	1.0	V
TR	Output rise time (20% – 80%)		25		ps
TF	Output fall time (20% – 80%)		23		ps
TDH	Output delay low-high transition (4)		300		ps
TDL	Output delay high-low transition (4)		300		ps

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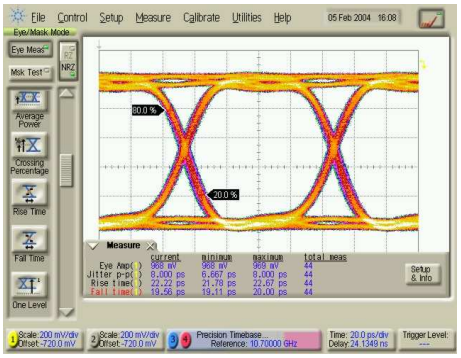
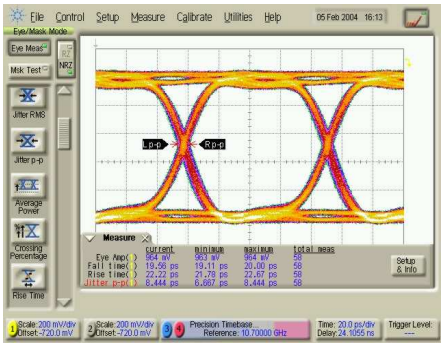
Electrical Characteristics (cont.)

Symbol	Parameters	Min.	Typ.	Max.	Units
T_{ADJ}	Output phase delay adjustment(4)		100		ps
F_{MAX}	Maximum clock frequency		10.7		GHz
J_{drms}	Jitter RMS degradation		1.5		ps
I_{EE}	Power supply current		330		mA
P_D	Power dissipation $J_{drms} = \sqrt{J_{meas}^2 - J_{thru}^2}$		1.65		W

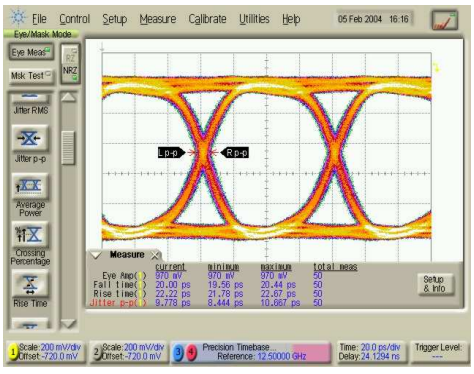
Eye Diagram Performance



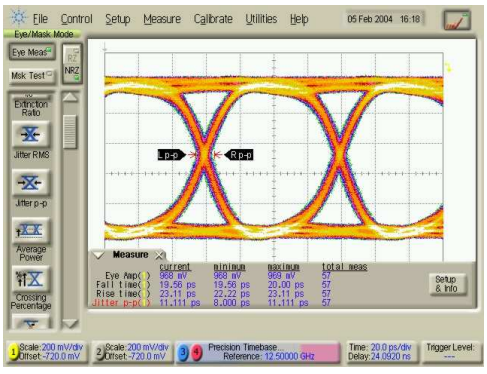
Evaluation board measurement
Vee: -5.0 V
Input data rate: 10.7 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCp = VCref, VCm =- 2.2 V



Evaluation board measurement
Vee: -5.0 V
Input data rate: 10.7 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCp = VCref, VCm = -3.0 V



Evaluation board measurement
Vee: -5.0 V
Input data rate: 12.5 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCp = VCref, VCm =- 2.2 V



Evaluation board measurement
Vee: -5.0 V
Input data rate: 12.5 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCp = VCref, VCm = -3.0 V

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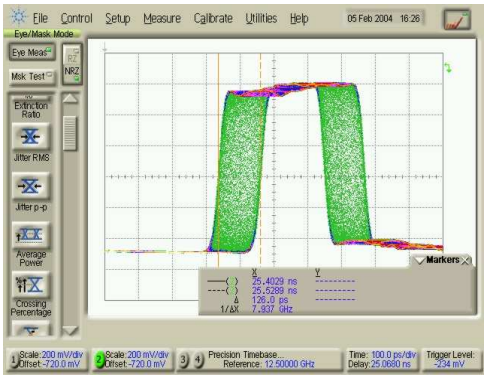
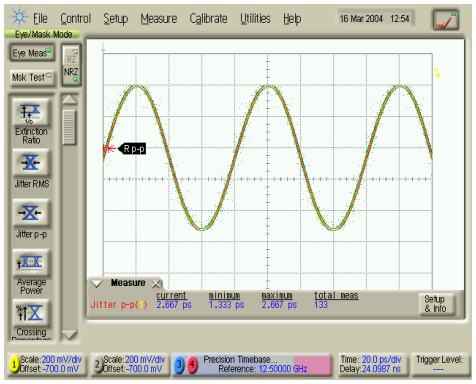
Eye Diagram Performance (cont.)

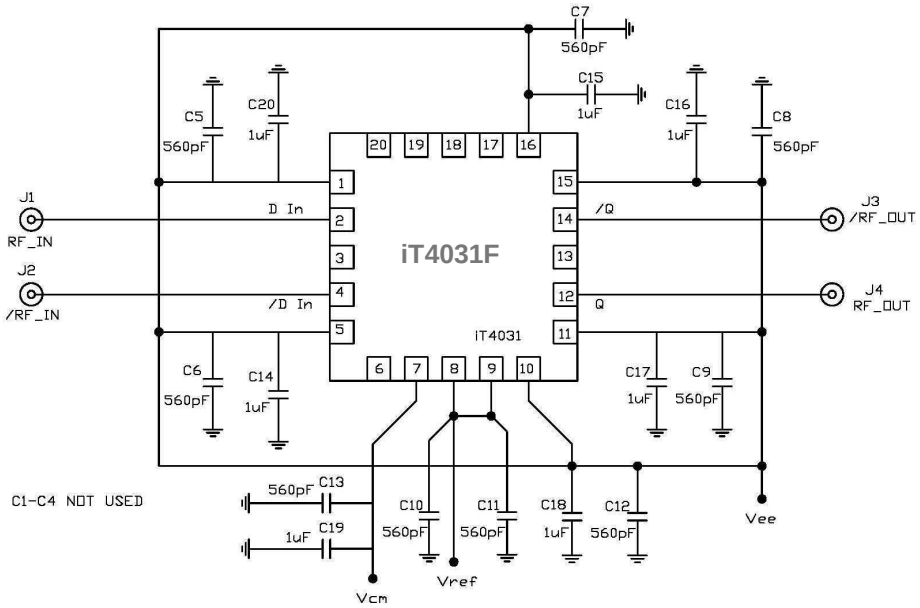


Evaluation board measurement
Vee: -5.0 V
Input data rate: 12.5 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCp = VCref,
VCm = -2.2 to -3.0 V (accumulating)



Evaluation board measurement
Vee: -5.0 V
Input CLK frequency: 12.5 GHz
Single-ended CLK input: +/-450 mVpp
Control voltage: VCp = VCref, VCm = -2.2 V

Recommended Operational Setup



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"F" Package Drawing, Pinouts, and Marking

Notes:

Dimensions in inches (mm) Tolerances are ±0.0039 in. (0.100 mm)

Package drawing encompasses JEDEC MO-220 Version VHHC-2

See iTerra Application Note 10 for recommended pad layout. RoHS parts are backward compatible if application note pad layout is followed.

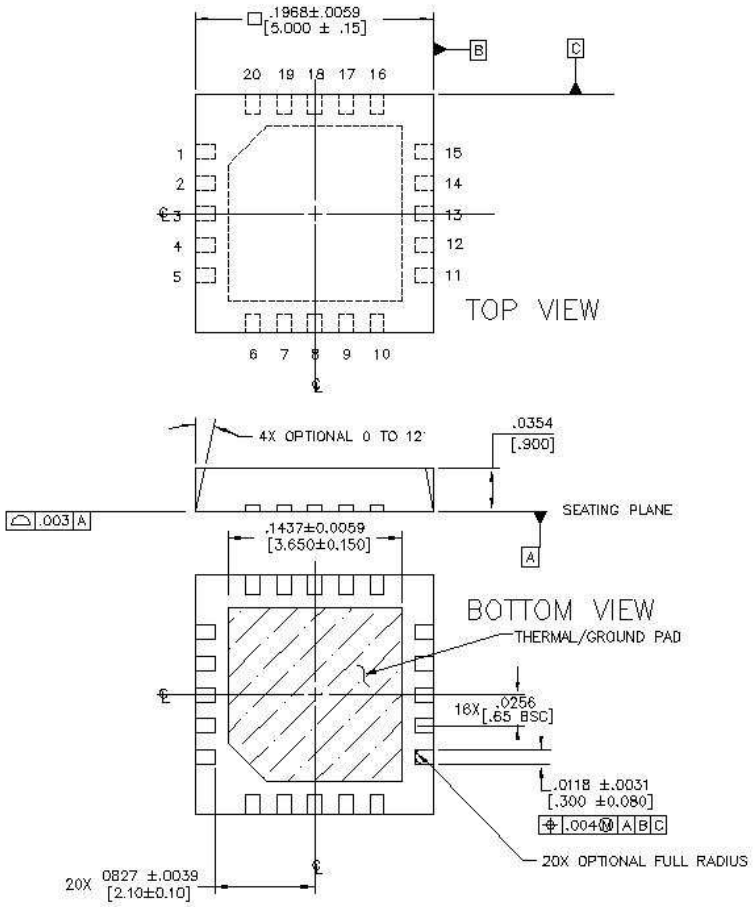
Lead frame material is copper alloy

Mold compound is UL94V0 compliant

Lead finish is NiPdAu

Marking Information
iTerra
MMMMFA
XXNNNN
LLYYWW

Where
MMMM = part number
F = Package Type
A = Temp. Range
XX = Wafer Lot
NNNN=Ser. No.
LLYYWW = MFG D/C



Pinouts

P1: Vee	P11: Vee
P2: Din	P12: Dout
P3: N/C	P13: N/C
P4: Din/	P14: Dout/
P5: Vee	P15: Vee
P6: N/C	P16: Vee
P7: VCm	P17: N/C
P8: VCp	P18: N/C
P9: Vcref	P19: N/C
P10: Vee	P20: N/C

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