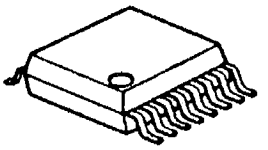
POCSAG PAGING DECODER

■ GENERAL DESCRIPTION

The **NJU5601** is a POCSAG Paging Decoder LSI in conformity to ITU-R RECOMMENDATION M.584-1 (POCSAG code). It provides three kinds of the battery power saving signal with the programmable output period of each signal as the RF block control signal (BS1), the RF block DC level adjustment signal (BS2) and the PLL SETUP signal (BS3). Therefore, it realizes the very low power operation in the pager system.

The **NJU5601** provides the serial interface to communicate data and commands with the outside CPU. It also provides the output buffers storing two User addresses and two User messages. Thus, it can reduce the load of operation in the outside CPU.

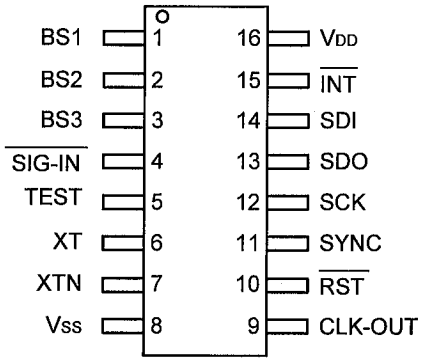
■ PACKAGE OUTLINE



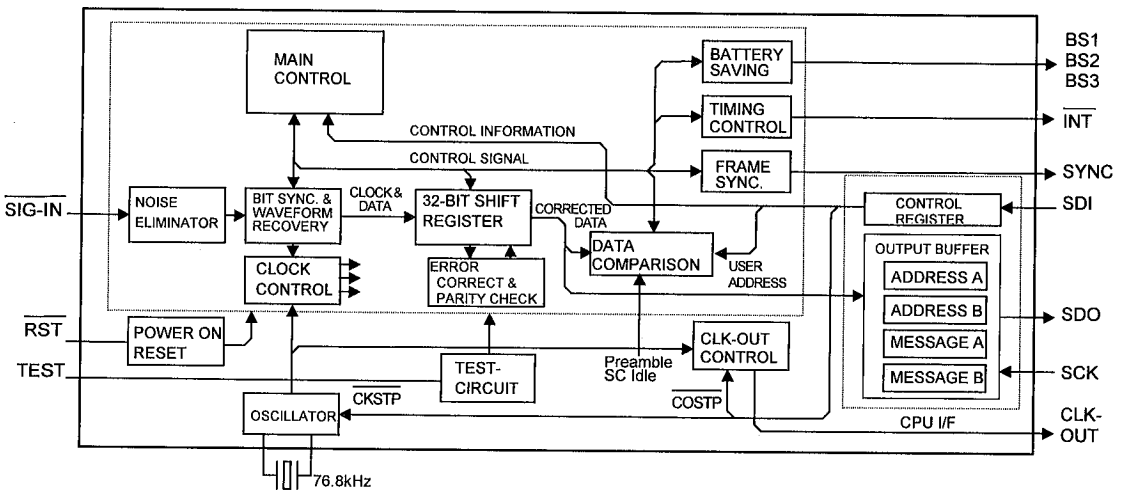
■ FEATURES

- POCSAG Paging Decoder in conformity to ITU-R RECOMMENDATION M.584-1
- Bit Rates : 512/1200/2400bps
- Battery Saving Signals (BS1,BS2,BS3) with Programmable Signal-Period
- User Address : 8
- User Frame : 2
- Random 2-bit Error Correction by BCH(31,21) Code
- Preamble Signal Duty Factor : 25%~75%
- 8-bit Serial Interface with 3 Wires
- Output Buffers storing two User Addresses and two User Messages
- Oscillator Circuit : 76.8kHz
- Noise Eliminator for the Input Signal($\overline{\text{SIG-IN}}$ terminal)
- Power On Reset Circuit
- Wide Operating Voltage Range : 2.6V to 3.4V
- Low Operating Current : 5 μA(TYP)
- C-MOS Technology
- Package Outline : SSOP16

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	INPUT/OUTPUT	FUNCTION
1	BS1	OUTPUT	RF Block Control Signal Output Terminal
2	BS2	OUTPUT	RF Block DC Level Adjustment Signal Output Terminal
3	BS3	OUTPUT	PLL Setup Signal Output Terminal
4	$\overline{\text{SIG-IN}}$	INPUT	FMIF-Signal Input Terminal. Programmable Active Level by the Control Register. Active Low after the Reset Operation.
5	TEST	INPUT	Test Terminal with Pull-down Resistance Normally Open
6	XT	–	Crystal Oscillator (76.8kHz) Connection Terminals
7	XTN	–	Built-in a Feedback Resistor (Rf) and two Load Capacitors (Cg and Cd)
8	V_{SS}	–	Power Source (0V)
9	CLK-OUT	OUTPUT	Reference Clock (76.8kHz) Pules Output Terminal
10	$\overline{\text{RST}}$	INPUT	Reset Terminal. Initializes the NJU5601 by Low level Signal.
11	SYNC	OUTPUT	Synchronization Codeword(SC) Detection Signal Output Terminal High Level Signal as Success of SC Detection.
12	SCK	INPUT	Serial Clock Input Terminal of Serial Interface
13	SDO	OUTPUT	Serial Data Output Terminal of Serial Interface
14	SDI	INPUT	Serial Data Input Terminal of Serial Interface
15	$\overline{\text{INT}}$	OUTPUT	Interrupt Request Signal Output Terminal Low Level Signal as Interrupt Request to the outside CPU
16	V_{DD}	–	Power Source (+2.6V to 3.4V)

■ THE POCSAG PAGING CODE

The POCSAG* code for the radio paging system is in conformity to ITU**-R RECOMMENDATION M.584-1 (POCSAG code) as shown in Fig.1 POCSAG code structure.

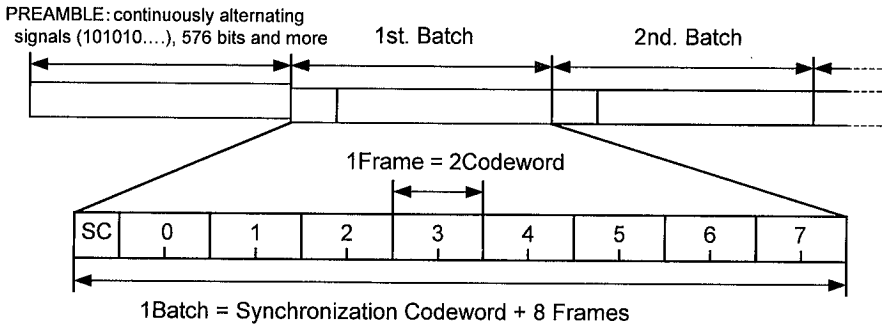


Fig.1 POCSAG code structure

* Post Office Code Standardization Advisory Group
**International Telecommunication Union

(1) Preamble

Preamble is the continuously alternating signals as 1,0,1,0,...., which are transmitted over 576 bits (a batch (544 bits) + a codeword (32 bits)) before the information in accordance with POCSAG.

(2) Batch

After the preamble, Synchronization Codeword (i.e. SC) and Batch consisting of 8 frames are transmitted. Each frame is consisted of two codewords. These 8 frames are numbered as 0 to 7 in order of transmission.

(3) Codeword

Codeword consisting of 32 bits as shown in Table-1 is transmitted with MSB first. The BCH(31,21) Code and the even parity check are adopted for the error correction.
There are four kinds of codeword as SC, Address codeword, Message and Idle.

Bit number	MSB 1	2~19	20~21	22~31	LSB 32
Address Codeword	Flag bit "0"	Address bits	Function bits	BCH check bits	Even parity bit
Message Codeword	Flag bit "1"	Message bits		BCH check bits	Even parity bit

※ When the flag bit is "0", transmitting data are Address Codeword or SC or Idle. When it is "1", transmitting data are only Message.

Table-1 Codeword structure

(3-1) Address Codeword

Address Codeword carries User Address to transmit data. When the codeword is the address codeword, the MSB as the flag bit is always "0" as shown in Table-1.

The upper side 18 bits in 21 bits converted to the binary data from 7 characters with decimal data of Pager (user) address are transmitted as the address bits. Although the remaining three bits are not transmitted, they correspond with the valid frame number to transmit the user address. For example, when an address codeword is transmitted in the third frame, the lower side three bits are "011".

The 20th bit and 21st are the function bits and they choose a function from four kinds of function prepared in the Pager system.

(3-2) Message Codeword

Message Codeword is a codeword to transmit the message to the address by the address codeword. When the codeword is the message, the MSB of codeword as the flag bit is always "1" as shown in Table-1. The message codeword always follows the address.

A message codeword transmits 20 bits message data. When the message is over 20 bits, multiple message codewords are transmitted continuously. However, SC transmission precedes against the message in the next frame after the 7th as shown in Fig.2.

After the message transmission, the address codeword or the idle is transmitted.

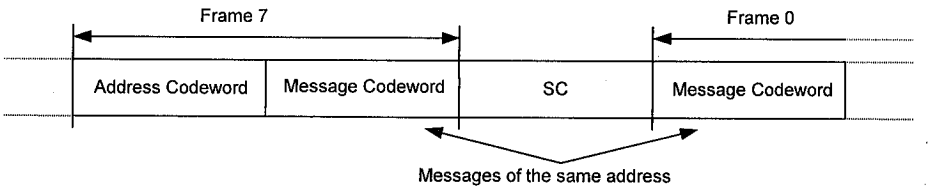


Fig.2 Message Codeword Continuously Transmission

(3-3) Synchronization Codeword (SC)

Synchronization Codeword (i.e. SC) is transmitted at the top of each batch to synchronize for each frame. The bit pattern of SC as shown in Table-2 must not be set as the address.

Bit number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bit	0	1	1	1	1	1	0	0	1	1	0	1	0	0	1	0
Bit number	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Bit	0	0	0	1	0	1	0	1	1	1	0	1	1	0	0	0

Table-2 SC structure

(3-4) Idle Codeword

Idle Codeword is transmitted when any address codewords and messages are not transmitted. The bit pattern of Idle as shown in Table-3 must not be set as the address.

Bit number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bit	0	1	1	1	1	0	1	0	1	0	0	0	1	0	0	1
Bit number	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Bit	1	1	0	0	0	0	0	1	1	0	0	1	0	1	1	1

Table-3 Idle Codeword

■ INTERNAL SYSTEM DESCRIPTION

(1) Internal system structure (refer **■BLOCK DIAGRAM**)

(1-1) Decoder

- Noise Eliminator
  Eliminates noises in the receiving signals from FMIF block.
- Bit Synchronization and Waveform Recovery
  Synchronizes between the receiving signal from FMIF and the internal system clock.
  Recovers the data and the clock.
- Main Control
  Generates the internal operation timing for the decoder sequence control.
- Error Correction
  Corrects Random 2-bit errors by the BCH(31,21) code and the even parity bit.
- Data Comparison
  Compares the input signal with Preamble, SC, User address, and Idle Codeword .
- Battery Saving
  Generates three kinds of Battery Saving signal as BS1, BS2 and BS3 controlling the outside RF block to reduce the power consumption of Radio Pager system.

(1-2) CPU Interface

- Control Register
  Stores the system information of the decoder from / to the outside CPU.
- Output Buffer
  Stores the received data to the outside CPU temporarily.

(1-3) Oscillator

Generates the system clock by connection of only external crystal resonator.

(1-4) Power on Reset

Initializes the system of NJU5601 automatically at the power on.

(2) FUNCTIONAL DESCRIPTION

※ The number of bit is counted in the bit rate.

(2-1) Initial state

The all of contents in the control register are initialized to "0" at the power on by the power on reset circuit. They are also set to "0" by the low level signal input to the RST terminal. In the mean time, On–chip oscillator does not operate. It starts the oscillation by writing "1" into the bit7 : CKSTP(refer (3)CPU INTERFACE) of the address 28 in the control register. Then the state goes to Rest state before Synchronization Achievement (refer (2-2)).

(2-2) Rest state before Synchronization Achievement

Until Synchronization Achievement, the **NJU5601** goes to Rest state during 512 bits counted with the bit rate clock for the power saving. In the mean time, all of the system except for the counter counting the number of bit rate clock is suspended, and BS1, BS2 and BS3 as the battery saving signals keep the "LOW" level.

After the rest state during 512 bits, the state goes to Preamble Search state 1 (refer (2-3)).

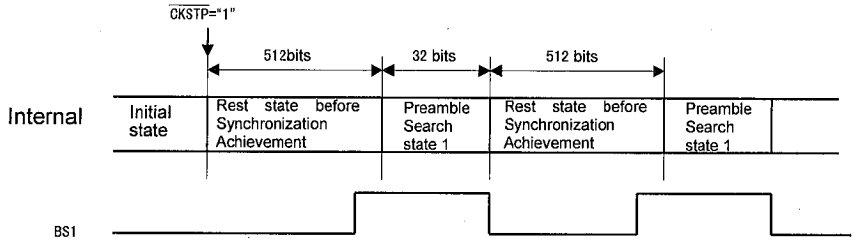


Fig.3 Rest state before Synchronization Achievement

(2-3) Preamble Search state 1

Preamble Search state 1 during 32 bits comes after the rest state before the synchronization achievement. When the preamble signals are not detected within this state, the rest state before synchronization comes again (refer Fig. 3). These two states operate alternately until the preamble is detected. This alternating operation realizes the intermittent signal receiving.

In the preamble search state 1, when the number of the input alternating signals as 1,0,1,0,.... programmed by bit 6 and 7 / PDL 1 and 0 of the address 25 in the control register are detected, the signals are recognized as Preamble signal. The duty ratio of the preamble signal is allowed 25% to 75%. When the preamble is detected, SC Search state before Synchronization Achievement comes after the preamble search state 1.

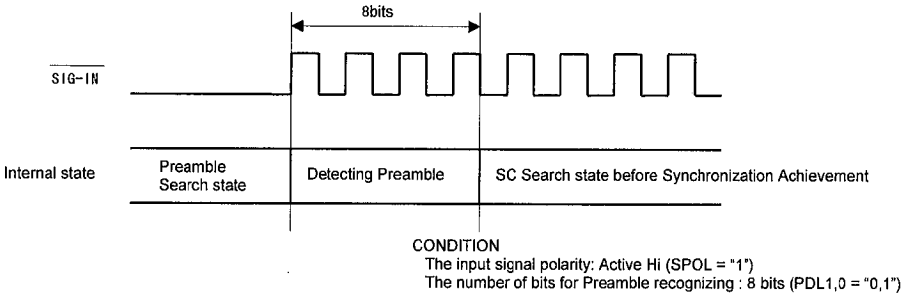


Fig.4 Preamble Detection

(2-4) SC Search state before Synchronization Achievement

When the preamble is detected, the intermittent signal receiving is stopped. BS1 terminal and BS3 output "H" level signals and the SC search is started. The input signals from the SIG-IN terminal are performed the error correction and the comparison with the bit pattern of SC. When the results of error correction in accordance with the receiving condition in Table-4 and comparison are available to receive them, the "H" level signal is output through the SYNC terminal as the sign of SC Recognition. And the bit-3: SYNC(refer (3)CPU Interface) of the address 0 in the output buffer is also set "1" (refer Fig.5).

In this state, the preamble is still checked. When the alternate signals as "1,0,1,0,1... is lost, the state goes to Preamble Search state 2 after that.

BCH(31,21)	Even Parity	Receiving
No error bit	No error	Available to receive
	Error	
1-bit error	No error	
	Error	
2-bit errors	No error	
	Error	Disable to receive
3 and more –bit errors	don't care	

Table-4 Operations at each Error Conditions

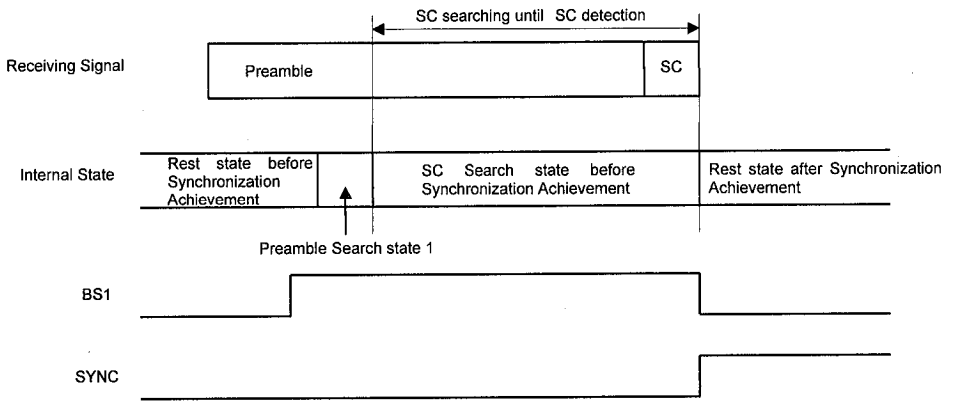


Fig.5 SC Search state before Synchronization Achievement

(2-5) Preamble Search state 2

In Preamble Search state 2, both of preamble signal and SC are searched. As same as Preamble Search state 1, when the number of the input alternating signals as 1,0,1,0,.... programmed by bit 6 and 7 / PDL 1 and 0 of the address 25 in the control register are detected, the signals are recognized as the preamble. After the preamble detection, the state goes to SC Search (refer Fig.6a) .

When both of the preamble signal and SC are not detected, the search of them is continued during 1-batch. Then, the state goes to Rest state before Synchronization Achievement (refer (2-2) and Fig.6b).

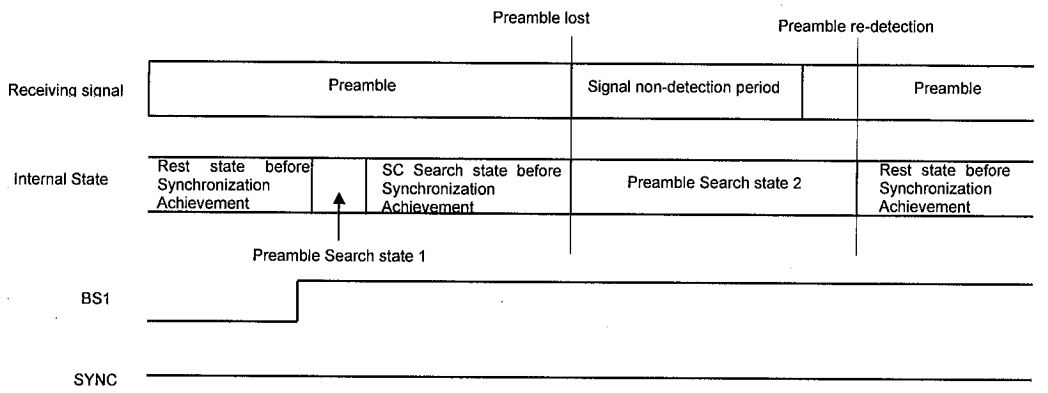


Fig.6a Preamble Search state 2 in case of success of Preamble detection

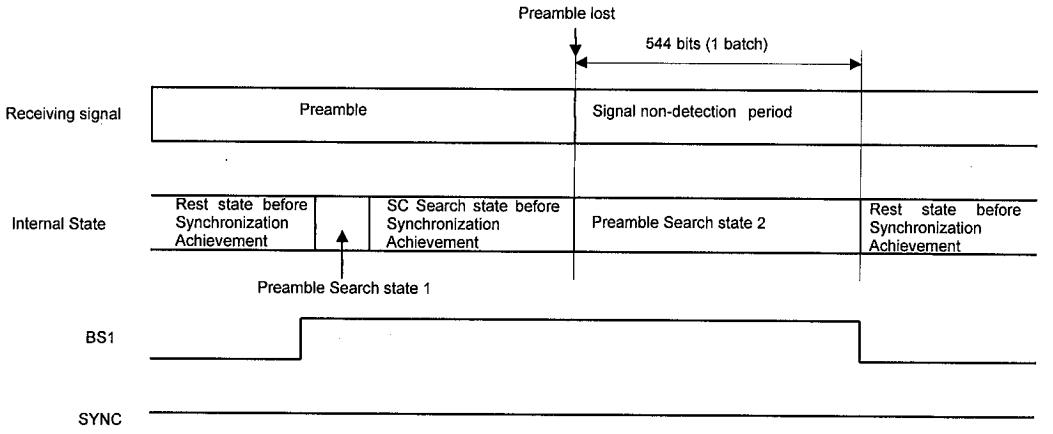


Fig.6a Preamble Search state 2 in case of failure of Preamble detection

(2-6) Rest state after Synchronization Achievement

When SC is detected, the state goes to Rest state after Synchronization Achievement until the frame number of received signal corresponds the user frame assigned to the user as a Paging system (refer Fig. 7). When the frame number of received signal corrosponds the user frame, the state goes to Address Codeword Search. But, when it is "0", the state goes to Address Code Word Search immediately after the success of SC detection.

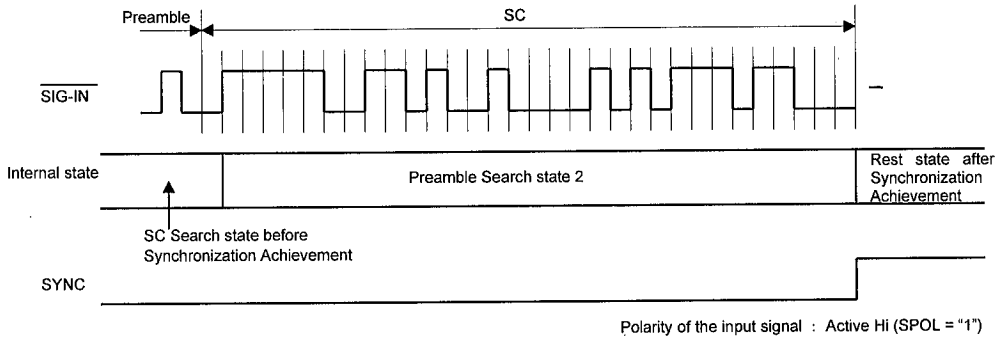


Fig.7 SC Detection - Rest state after Synchronization Achievement

(2-7) Address Codeword Search state

The frame number after SC as the starting point is counted in the internal system counter. When it corresponds to the user frame, the user address search is started. The error correction and the even parity check are performed for the received signals first. When the results of the error correction and the even parity check conform to the condition of Table-4, the data are compared with the user address. When the data corresponds to the user address, the number of address corresponding to the user address and the function are stored into the output buffer. And the request signal to read the data out from the output buffer is output to the outside CPU as the interrupt. Two output buffers to store the received data are prepared for reducing the load of the outside CPU.

When the user address is not detected in the user frame, the state goes to Rest state after Synchronization Achievement and the contents in the output buffers are not changed.

(2-8) Message Codeword Receiving (refer Fig.8a and b)

After the user address is detected, the message codeword is searched when the next period is SC receiving. When the next period is SC receiving, SC Search after Synchronization Achievement (refer (2-12)) is preceded. And the message codeword is searched after the next frame of SC detection.

The received codeword is performed the error correction and the even parity check. When the result conforms to the condition of Table-4 and the MSB as the flag bit of the received codeword is "1", the codeword is recognized as the message to the user address. The true message without each bits for the error correction and the even parity check, the flag bit and the information of the error correction are stored into the output buffer. Then, the request signal to read the data out from the output buffer is output as the interrupt to the outside CPU.

Although the result doesn't meet the condition of Table-4, the true message, the flag bit and the information of the error correction are stored into the output buffer. Then the request signal to read the data out from the output buffer is output as the interrupt to the outside CPU as same as the above operation. But the user application must decide weather the valid message or the invalid.

There are two kinds of way to finish the message receiving which are selected by bit 0 / EMR (refer (3)CPU INTERFACE) of an address 27 in the control register. In both of ways, EMSG bit in the output buffer is set to "1" when the message receiving is finished. EMSG bit is set to "0" when the user address is received again.

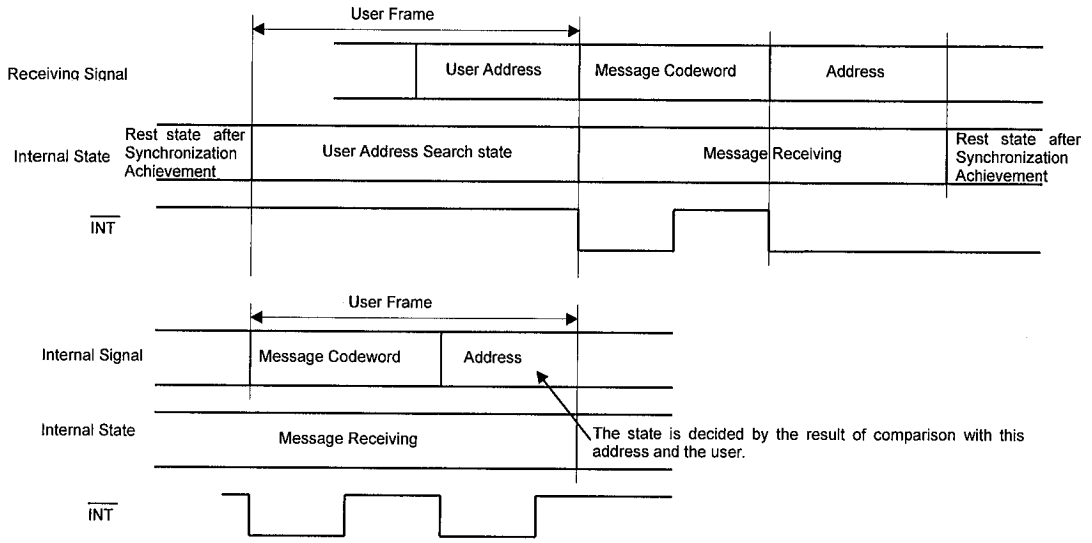


Fig.8a User Address Message Receiving in case of EMR = "0"

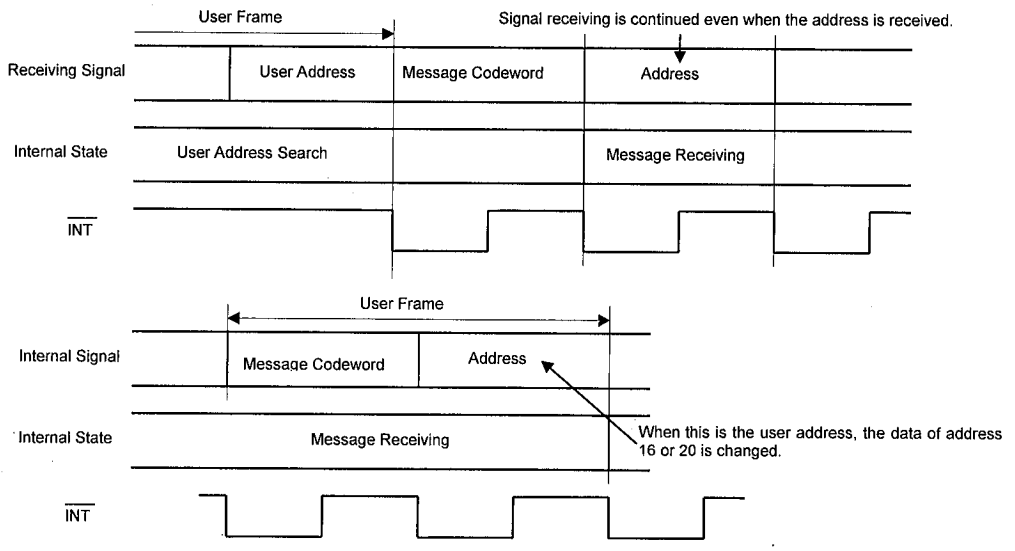


Fig.8b User Address Message Receiving in case of EMR = "1"

(2-8-1) In case of EMR = "0" (refer Fig. 8a)

In case of success of the error correction, when MSB is "0", the state is recognized as the end of the message receiving to the user address and the start of the address receiving for the next message or Idle codeword receiving. And the receiving operation is stopped until the period of next user frame. In this time, the EMSG bit is set to "1" as the sign of the end of data receiving and the interrupt signal is output through the $\overline{INT}$ terminal to the outside CPU. When the received frame is not the user frame, the state goes to Rest state after Synchronization Achievement (refer (2-6)). When it is the user frame, the state goes to Address Codeword search state(refer (2-7)).

Otherwise, the message receiving is also stopped by the data set to "1" into the bit 5 / RSUS (refer (3) CPU Interface) of the address 28 in the control register.

(2-8-2) In case of EMR = "1" (refer Fig.8b)

The message receiving is stopped by only the data set to "1" into the bit 5 / RSUS (refer (3) CPU Interface) of an address 28 in the control register. In this mode, when the addresses or Idle codeword is received, they are also stored into the output buffer and the interrupt signal is output through the $\overline{INT}$ terminal to the outside CPU.

(2-9) Error Correction

Each random two-bit errors of SC, Address Codeword or Idle are accepted (refer Table-4). When SC or User Address is detected, the sign flags as shown in Table-5a or 5c are written into the output buffer to notice the result of the error correction.

In case of Message Codeword Receiving state, all of receiving signals are accepted independent of the result of error correction. And the sign flags as shown in Table-5b or 5c are written into the output buffer to notice the result of the error correction

ECSC1~0,ECAA1~0,ECAB1~0	Result of error correction
00	no error
01	one error
10	two errors
11	-

Table-5a Result of Error Correction of SC and User Address

ECMA1~0,ECMB1~0	Result of error correction
00	no error
01	one error
10	two errors
11	three and more errors

Table-5b Result of Error Correction of Message

EPSC,EPAA,EPAB,EPMA,EPMB	Even Parity
0	no error
1	Error

Table-5c Result of Even Parity Check of SC and User Address

(2-10) Interrupt

The interrupt request to the outside CPU operates by the "L " level signal output through the $\overline{INT}$ terminal (refer Fig.8a and b). The period of "L" level depends on the bit rate as shown in Table-6.

Bit Rate(bps)	"L" level period of $\overline{INT}$(mSec)
512	31.3
1200	13.3
2400	6.67

Table-6 "L " level period of $\overline{INT}$

(2-11) Output buffer

The output buffer storing User Address and Message are prepared for each two codewords. When the data are received over two codewords, they are written on the former data in the output buffer in order of receiving (refer Fig.9a and b). The outside CPU must read the received data out from the output buffer within the period of two codewords receiving at the interrupt request (refer (3) CPU Interface).

LSB of the address 0 in the output buffer is the Busy Flag. During the data of Busy Flag is "1", the data in the output buffer is not valid why it is renewing.

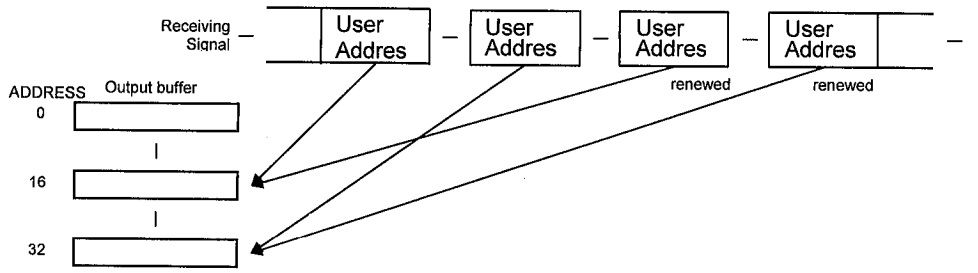


Fig. 9a User Address Renewal in the output buffer

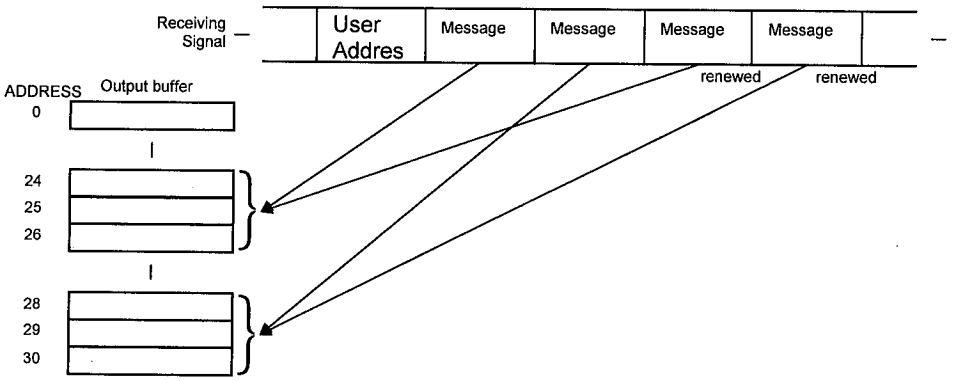


Fig. 9b Message Data Renewal in the output buffer

(2-12) SC Search state after Synchronization Achievement

SC is searched again after one batch operation. In this state, the SC appearance position is so foreseeable that a codeword at the SC appearance position is received and the received data is compared with SC after the error correction and the even parity check. The condition of SC detection is same as "(2-4) SC Search state before Synchronization Achievement". When the SC detection is failed and the synchronization is lost, the output from SYNC terminal is set to "L" and the bit 3 of an address 0 in the output buffer (refer (3) CPU Interface) is also set to "L". In the batch without SC detection, the user address is not searched at the user frame. SC search is performed at the period of next SC receiving.

When the message or the user address is received at the second codeword of the Frame 7, the next codeword after SC is searched without relationship of the result of SC detection. When an idle codeword or an address except for the user address is received, the receiving operation is stopped.

When the Messages come across SC, the receiving is continued without relationship of the SC detection. When the detection of SC sandwiched by the messages is failed, the message is received continuously. The output signal from SYNC terminal is set to "L" and the bit 3 / SYNC (refer (3) CPU Interface) of an address 0 in the output buffer is also set to "0" because the synchronization is lost. In this batch, the user address is not searched at the user frame (refer Fig. 10).

Although SC can not be detected after the synchronization achievement, SC detection or the preamble according to (2-13) is performed at the appearance position of SC in mode of the success of Synchronization Achievement.

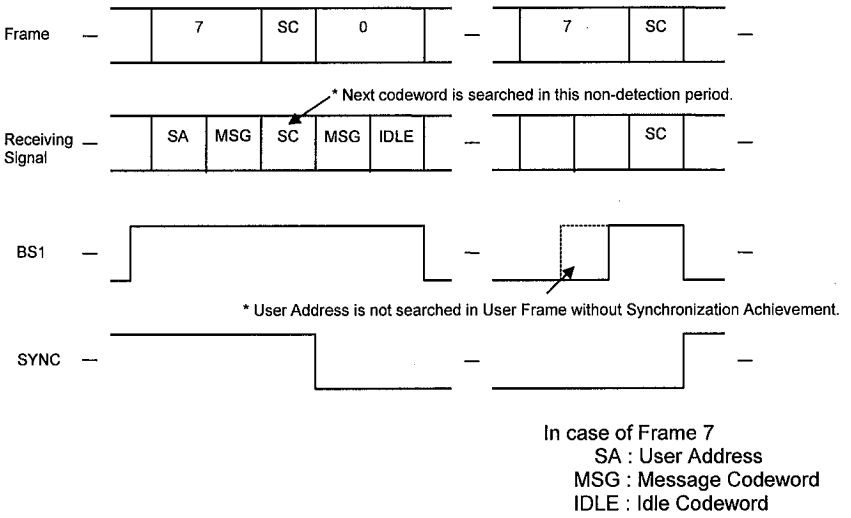


Fig. 10 SC in Message Receiving

(2-13) Preamble Detection during the period of User Frame or SC

When the alternating signals as "1,0,1,0,...." are detected 16 bits and more during the user address search state or SC period, those data are kept until the end of the codeword. When the error correction of the kept data is failed at the end of codeword, the kept data is recognized as the preamble. Therefore the state goes to Preamble Search state 1.

(2-14) Stop the receiving

When the bit 5 / RSUS of the address 28 in the control register is set to "1" in the address receiving or the message, the receiving is stopped and BS signals outputting "H" level are set to "L".

(3) CPU Interface

CPU Interface is shown in Fig. 11. Excepting for the busy state of data transmission, SDI terminal must be set to "H" and SCK must be set to "L".

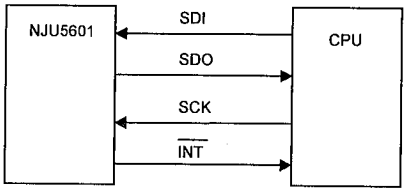


Fig. 11 CPU Interface

(3-1) START and STOP Commands for data transmission

Start command operation for data receiving is the signal transition from "H" to "L" into the SDI terminal when the SCK terminal is "H". Stop command operation is the signal transition from "L" to "H" into the SDI terminal when the SCK terminal is "H". For inputting data from the outside CPU to the **NJU5601**, the condition of SDI terminal must be changed when the SCK is "L". The condition of the SCK terminal must be set to "L" after the stop command (refer Fig. 12a).

Start command can be input without Stop command (refer Fig. 12b).

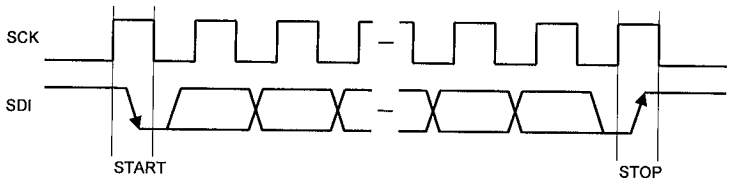


Fig. 12a Start and Stop commands

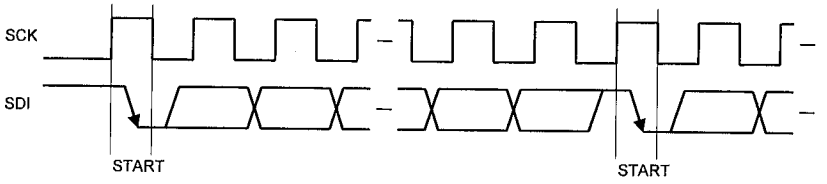


Fig. 12b Start commands in sequential input

(3-2) Writing into the Control Register

For writing data into the control register, "0" must be input at first from the outside CPU after the start command. And the top address of data to write must be input as second procedure. The address of the control register consists of 8 bits and its area is from "0" to "28". The upper 3 bits of the address must be set to "0". A data word consisting of 8 bits is written with MSB first. When the data is written over than 8 bits (, or a word), the address is increased automatically. A data word to write must consist of 8 bits. When the start or stop command is input before the end of operation to write one word, the data word is not written into the control register or an invalid data word is written.

The bit positions and the functions in the control register are shown in Table-7a and b.

(3-3) Reading from the Output Buffer

For reading data from the output buffer, "1" must be input at first from the outside CPU after the start command. And the top address of data to read must be input as second procedure. The address of the output buffer consists of 8 bits and its area is from "0" to "30". The upper 3 bits of the address must be set to "0". The SDO terminal outputs "0" after the address is input, and the data from the output buffer is output sequentially. The output data is synchronizing to the negative edge ("H" to "L") of the clock into the SCK terminal. When the data is read over than one word , the address is increased automatically. In case of the address 0 as the start point for reading data, the address is increased from 0 to 16, 20, 24, 25, 26, 28, 29, 30, and 0. The start or stop command is always allowed to input in reading data.

The bit positions and the functions in the output buffer are shown in Table-8a and b.

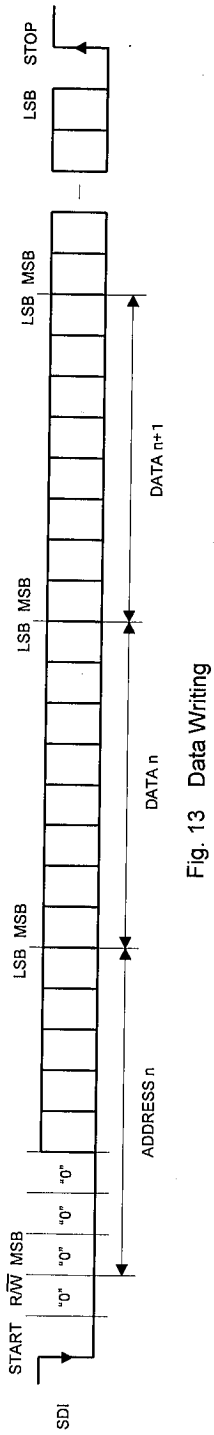


Fig. 13 Data Writing

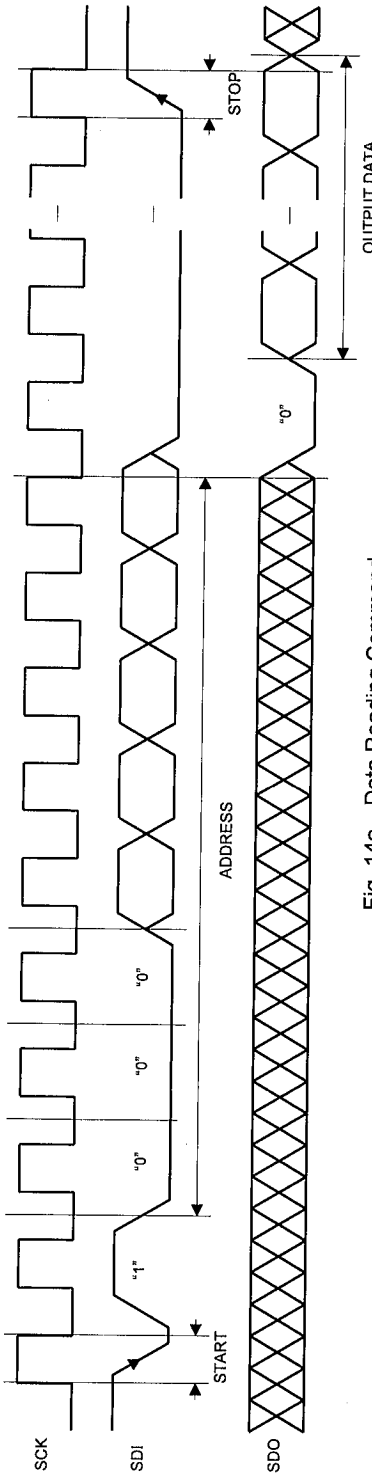
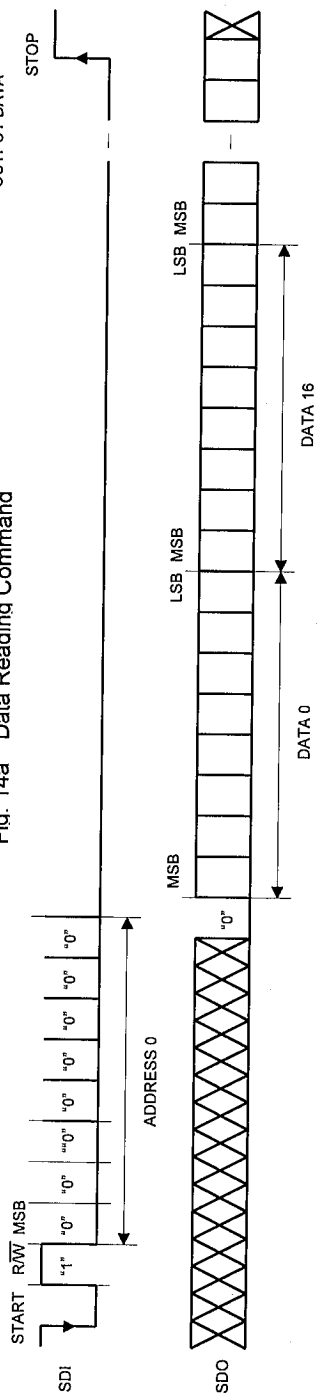


Fig. 14a Data Reading Command



In case of data read from address 0

Fig. 14b Data Reading

	MSB							LSB
Address	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
0	$\overline{AE}$	AFS	-	-	-	-	A17	A16
1	A15	A14	A13	A12	A11	A10	A9	A8
2	A7	A6	A5	A4	A3	A2	A1	A0
3	$\overline{BE}$	BFS	-	-	-	-	B17	B16
4	B15	B14	B13	B12	B11	B10	B9	B8
5	B7	B6	B5	B4	B3	B2	B1	B0
6	$\overline{CE}$	CFS	-	-	-	-	C17	C16
7	C15	C14	C13	C12	C11	C10	C9	C8
8	C7	C6	C5	C4	C3	C2	C1	C0
9	$\overline{DE}$	DFS	-	-	-	-	D17	D16
10	D15	D14	D13	D12	D11	D10	D9	D8
11	D7	D6	D5	D4	D3	D2	D1	D0
12	$\overline{EE}$	EFS	-	-	-	-	E17	E16
13	E15	E14	E13	E12	E11	E10	E9	E8
14	E7	E6	E5	E4	E3	E2	E1	E0
15	$\overline{FE}$	FFS	-	-	-	-	F17	F16
16	F15	F14	F13	F12	F11	F10	F9	F8
17	F7	F6	F5	F4	F3	F2	F1	F0
18	$\overline{GE}$	GFS	-	-	-	-	G17	G16
19	G15	G14	G13	G12	G11	G10	G9	G8
20	G7	G6	G5	G4	G3	G2	G1	G0
21	$\overline{HE}$	HFS	-	-	-	-	H17	H16
22	H15	H14	H13	H12	H11	H10	H9	H8
23	H7	H6	H5	H4	H3	H2	H1	H0
24	-	FR12	FR11	FR10	-	FR02	FR01	FR00
25	SPOL	BS2WF2	BS2WF1	BS2WF0	RATE1	RATE0	PDL1	PDL0
26	RFC3	RFC2	RFC1	RFC0	PSU3	PSU2	PSU1	PSU0
27	EMR	IGSC6	IGSC5	IGSC4	IGSC3	IGSC2	IGSC1	IGSC0
28	BS1	BS2	BS3	-	BFCL	RSUS	$\overline{COSTP}$	$\overline{CKSTP}$

-: don't care

Tbale-7a The bit positions in the control register

$\overline{AE}$,$\overline{BE}$,$\overline{CE}$,$\overline{DE}$, $\overline{EE}$,$\overline{FE}$,$\overline{GE}$,$\overline{HE}$	Enables User addresses from A to H by "0" Don't set multiple addresses written same value to enable in the mean time.
AFS,BFS,CFS,DFS, EFS,FFS.GFS,HFS	Selects the frame numbers of User addresses from A to H
A17~0,B17~0, C17~0,D17~0, E17~0,F17~0, G17~0,H17~0	User addresses from A to H
FR02~00,FR12~10	User frame number 0 and 1
SPOL	Selects the polarity of input signal to $\overline{SIG\text{-}IN}$ ("0": Active Low, "1": Active High)
RATE1~0	Bit rates("00": 512、"01": 1200、"10": 2400bps)
BS2WF2	Selects the condition of BS2 output as follows; BS2 is output only in case of the state before Synchronization Achievement or the failed result of the latest SC detection BS2 is output after Synchronization Achievement
BS2WF1~0	Selects the output form of BS2 (refer Fig. 15)
PDL1~0	Sets the bit-number to recognize the receiving data as Preamble
RFC3~0	Selects an output period of BS1 (RF block control signal) 0 to 8 as value can be set. The step is 0.83 mSec from 6.67 to 13.3 mSec
PSU3~0	Selects an output period of BS3 (PLL set up signal) 0 to A_H as value can be set. The step is 5 mSec from 10 to 60 mSec.
EMR	Selects a way of stop the message receiving By the address receiving or the RSUS input By only the RSUS input
IGSC6~0	Times of SC disregard (0: no disregard ... $7F_H$: 127 times of disregard
BS1、BS2、BS3	Outputs "H" from BS1, BS2 and BS3
BFCL	Clears the output buffer
$\overline{RSUS}$	Stops the receiving by "1"
$\overline{COSTP}$	Stops to output from CLK-OUT (0: stop, 1: output)
$\overline{CKSTP}$	Stops the internal oscillator (0: stop, 1: oscillating) The period which is from stop of oscillation to start again is required 200 μ sec and more.

Table-7b Functions of Control Register

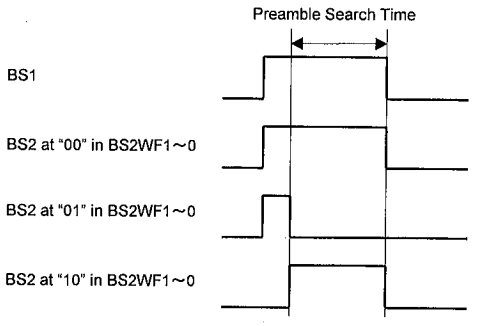


Fig. 15 BS2 Output Wave Form Selection

	MSB							LSB
Address	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
0	ECSC1	ECSC0	EPSC	SYNC	RCW1	RCW0	EMSG	BUSY
16	ECAA1	ECAA0	EPAA	AA2	AA1	AA0	FUNCA1	FUNCA0
20	ECAB1	ECAB0	EPAB	AB2	AB1	AB0	FUNCB1	FUNCB0
24	ECMA1	ECMA0	EPMA	FLGA	MA19	MA18	MA17	MA16
25	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8
26	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
28	ECMB1	ECMB0	EPMB	FLGB	MB19	MB18	MB17	MB16
29	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8
30	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

Table-8a Bit Positions in Output Buffer

ECSC1~0	Latest Result of Error Correction of SC (refer Table-2a)
EPSC	Latest Result of Even Parity Check of SC ("0":Success, "1":Fail)
SYNC	Latest Result of Detection of SC ("0":No Detection, "1":Detection)
RCW1~0	Receiving Code Words "00":Reciving Address A, "01": Receiving Address B "10":Massage A, "11":Massage B
EMSG	End of Massage Receiving ("1":End)
BUSY	Busy Flag ("1":busy)
AA2~0,AB2~0	Receiving Address A, B ("000":A~"111":H)
FUNCA1~0,FUNCB1~0	Receiving Function Bit A, B
ECAA1~0,ECAB1~0	Result of Error Correction of Receiving Address A, B (refer Table-5a)
ECMA1~0,ECMB1~0	Result of Error Correction of Massage A, B (refer Table-5b)
EPAA,EPAB	Result of Even Parity Check of Receiving Address A, B ("0":Success, "1":Fail)
EPMA,EPMB	Result of Even Parity Check of Massage A, B ("0":Success, "1":Fail)
FLGA,FLGB	Receiving Code Word Flag ("0":SC, Address, Idle, "1":Massage)
MA19~0,MB19~0	Receiving Massage A, B

Table-8b Functions of Output Buffer

(3-4) Reading Data from Output Buffer

The top addresses of the output buffers; A and B for the user addresses, and another A and B for the messages; are shown in Table-9.

bit0	bit1	bit2	bit3	Bit4	bit5	bit6	bit7
0	0	0	1	RCW1	RCW0	0	0

Table-9 The top addresses of output buffers; A and B for User addresses, and another A and B for Messages.

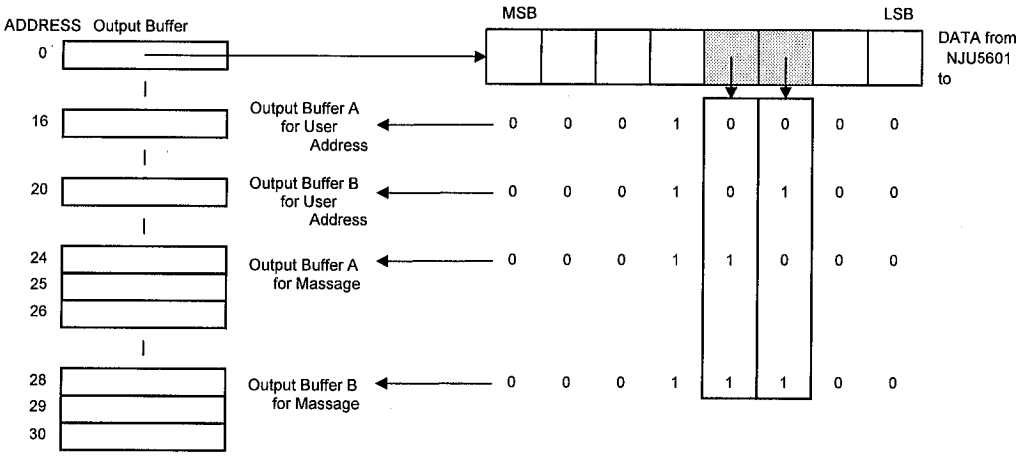


Fig.16 Reading data from Output Buffer

When the bit 4 and 5 (RCW1 and 0) as the result of reading data from the address 0 in the output buffer are "0" and "1", the contents in the output buffer B for the user address is in renewing. The read address of the output buffer in this time is shown in Tabl-10(When the bit7 (BUSY) is "1", the data is renewing).

bit0	bit1	bit2	bit3	Bit4	Bit5	bit6	bit7
0	0	0	1	0	1	0	0

Table-10 The read address of the output buffer B for User address

(4) Battery Saving Function

Very low power consumption system is realized by BS1 (for RF control), BS2 (for DC level control of RF) and BS3 (for PLL set up) which are controlled the output period and the output timing.

BS1 and BS3 versus SC after Synchronization Achievement based on the input signal from $\overline{\text{SIG-IN}}$ terminal is shown in Fig.17.

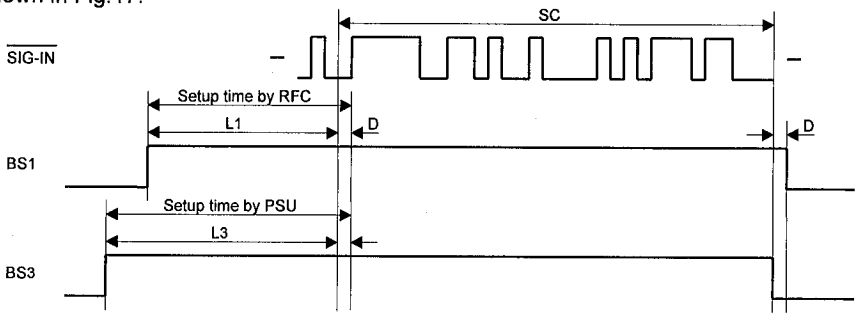


Fig.17 Input signal and BS signals

Bit rate(bps)	L1(μ sec)	L3(μ sec)	D(μ sec)
512	4714	8047	1953
1200	5833	9167	833
2400	6250	9583	417

D: Time for the internal operation (1 bit)

Table-11 The output periods of BS signals for the input signal

(4-1) Intermittent Receiving state before Synchronization Achievement

After initialization, the oscillator starts the operation and the preamble is searched intermittently for the power saving. The operation timings of each signal are shown in Fig.18 and Table-12.

The periods of A and C called as Pre-signals in Fig. 18 are controlled by RFC3 to 0 and PSU3 to 0 of the address 26 in the control register. The output wave form of BS2 is selected by BS2WF1 to 0 of the address 25 in the control register (refer (4-4) Output waveform of BS2).

The times of B in Table-12 are the conditions when the preamble is not detected in Preamble search state 1 (2-3).

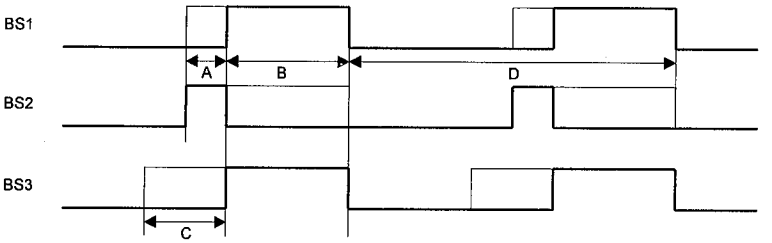


Fig.18 Battery Saving signals in the Intermittent Receiving state

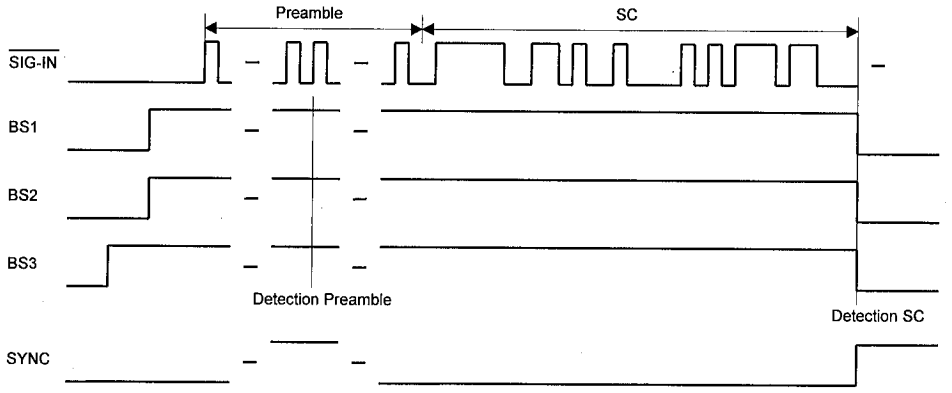
	512bps	1200bps	2400bps
A	6.67~13.3msec 0.83msec step		
B	62.5msec	26.7msec	13.3msec
C	10~60msec 5msec step		
D	1062.5msec	453.3msc	226.7msec

Table-12 Signal timings in the Intermittent Receiving state

(4-2) SC Detection

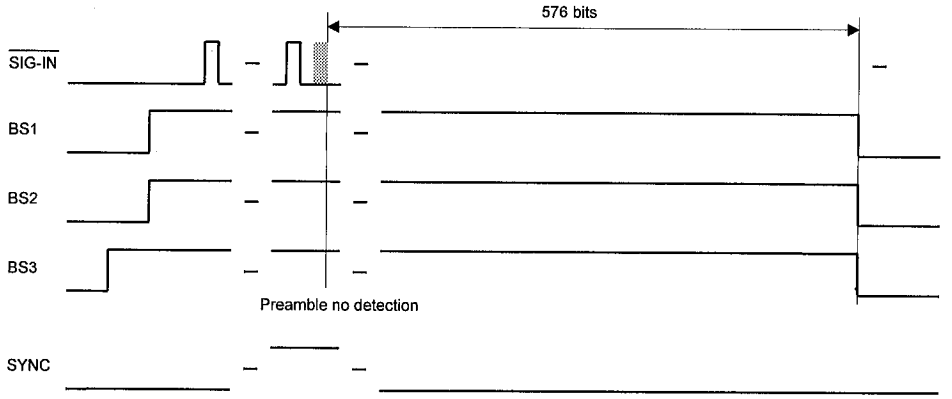
When the preamble is detected at the period of B in the intermittent receiving as shown in Fig.18, the outputs of BS1 and BS3 are kept with "H" and SC is searched. When SC is detected, "H" is output from SYNC terminal. Then, the outputs of BS1 to 3 set to "L" and the state goes to Intermittent Receiving state after Synchronization Achievement as shown in Fig.19a. However, when the user frame is set as the frame 0, the outputs of BS1 to 3 are continued the conditions as "H".

When both signals of Preamble and SC are not detected, the state goes back to Intermittent Receiving state before Synchronization Achievement after the period of one batch (576 bits) as shown in Fig.19b.



ex.SPOL="1",BS2WF1~0="00"

Fig.19a In case of success of Preamble and SC detection



ex.SPOL="1",BS2WF1~0="00"

Fig.19b In case of failure of Preamble and SC detection

(4-3) Intermittent Receiving state after Synchronization Achievement

When the frame number of the received signal is corresponded to User frame after SC detection, the outputs of BS1 to 3 are set to "H" and the user address is searched (refer Fig.20). The timings and the periods are shown in Fig.21 and Table-13.

The times of A and C are set by the address 26 / RFC3 to 0 and PSU3 to 0 in the control register. The times of B in Table-13 are shown in case of failure of the user address detection at all of a frame in Address Code Word Search state (2-7). In case of success of the user address or the message receiving, or the stop of receiving in the intermediate of the frame by the simple decision of address, the time of B is not fixed in accordance with Table-13.

The waveform of BS2 is selected by BS2WF1 to 0 of the address 25 in the control register (refer (4-4) Output waveform of BS2).

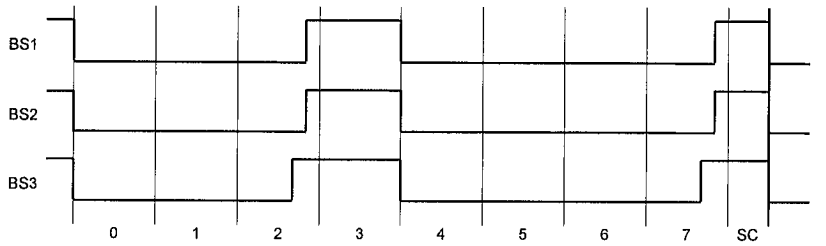


Fig.20 Receiving in User frame (in case of User frame 3)

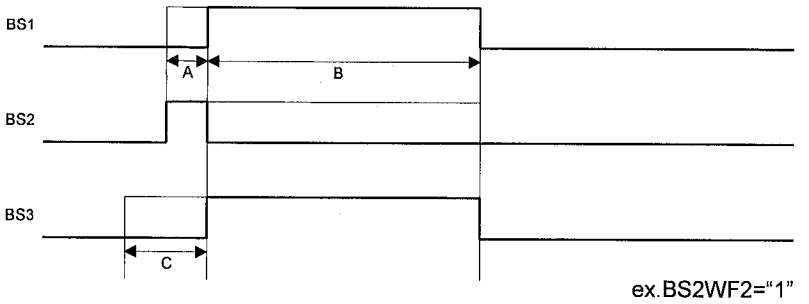


Fig.21 Battery Saving signals in Intermittent Receiving state after Synchronizing Achievement

	512bps	1200bps	2400bps
A	6.67～13.3msec 0.83msec step		
B	125msec	53.3msec	26.7msec
C	10～60msec 5msec step		

Table-13 Signal-timings in Intermittent Receiving sate after Synchronization Achievement

(4-4) Output Waveform of BS2

Output Waveform of BS2 can be changed by BS2WF1 to 0 of the address 25 in the control register. BS2 signal is output until the success of Bit Synchronization (at "L" output only from SYNC terminal) in Preamble Search state after Power on Reset. But BS2 is also output after Synchronization Achievement (at "H" output from SYNC terminal) by setting of BS2WF2 to "1".

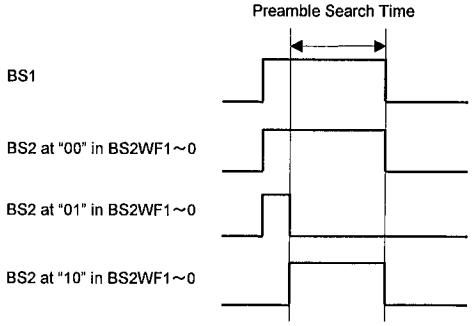
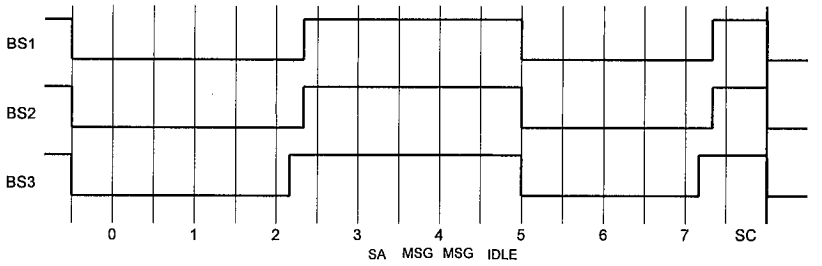


Fig.22 BS2 output waveform Selection

(4-5) Message Codeword

When the user address is detected, the outputs of BS1, BS2 and BS3 are kept "H" level for the message codeword receiving. When the address or Idle codeword is detected, BS1, BS2 and BS3 output "L". (refer Fig.23)



ex.BS2WF2="1",BS2WF1~0="00"
SA: User address
MSG: Message Codeword
IDLE: Address Codeword

Fig.23 Message codeword receiving

(4-6) Simple Decision of Address

When three illegal data are detected from the received data at the user address search, the received data is not recognized as the user address by the result of simple decision and the receiving is stopped. When the received data is even not the preamble, the power saving is realized by controlling the signals of BS1, BS2 and BS3. The following is an example of BS1, BS2 and BS3 in accordance with the conditions on Table-14.

Bit rate	1200bps
SPOL	"1"(Active "H")
BS2WF2	"0"
RFC3~0	0
PSU3~0	1
User frame	3
User address	$(25A5A)_H$
Receiving data	$(0B6B00BE)_H$

Table-14 Operational Condition

When the three illegal data are detected from the received data and the user address can not be detected in the received data as result of the simple decision, the receiving is stopped and BS1, BS2 and BS3 output "L" signals at the rear part (second codeword) of the frame if the next is not the user frame (refer Fig.24a).

When the result of simple decision is completed at the front part (first frame) of the frame, the signals of BS1, BS2 and BS3 are output in accordance with the condition in the control register because the simple decision of address is required at the rear part of the frame. When the result of simple decision is completed at the rear part (second frame) of the frame and the next is the user frame, the signals of BS1, BS2 and BS3 are also output in accordance with the condition in the control register

In case of the operational condition in Table-14, the output of BS1 is set to "L" at once when the simple decision of address is completed. Then, BS1 is output as shown in Fig.24b for the next codeword receiving. The output of BS3 is kept as "H" continuously because the pre-signal for the next codeword is already started when the simple decision of address is completed (refer Fig.24b).

When RFC is set to 6 and more, the output of BS1 is also "H" continuously as shown in Fig.24c.

The each length of pre-signals of BS1 and BS3 does not so depend on the bit rate that the transition of signal from "H" to "L" are not fixed relatively.

Preamble search operates in the mean time of the simple decision of address. Therefore, if illegal three bits are detected in the received data, the receiving operates continuously without the simple decision of address when the receiving data are alternating signals as "1,0,1,0,..". The simple decision of address is completed when the alternating signals can not be received. However, when these alternating signals is received continuously during 16 bits, the state goes to Preamble Detection state in User Frame and SC period (refer (2-13)) as the success of the preamble detection.

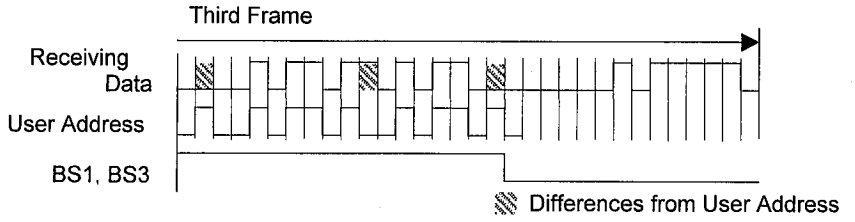


Fig.24a Simple Decision of Address without Next Codeword Receiving

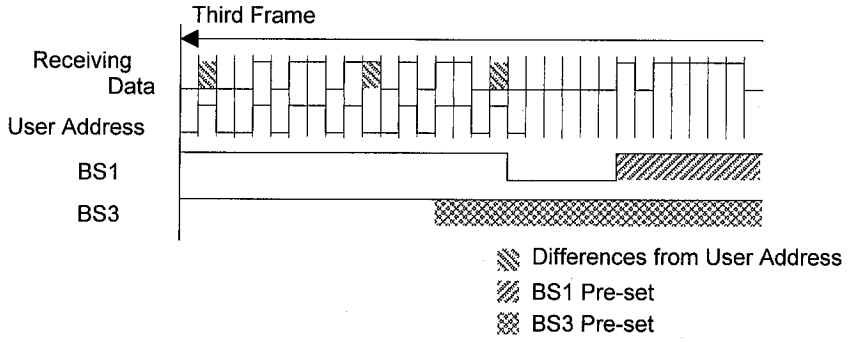


Fig.24b Simple Decision of Address with Next Codeword Receiving

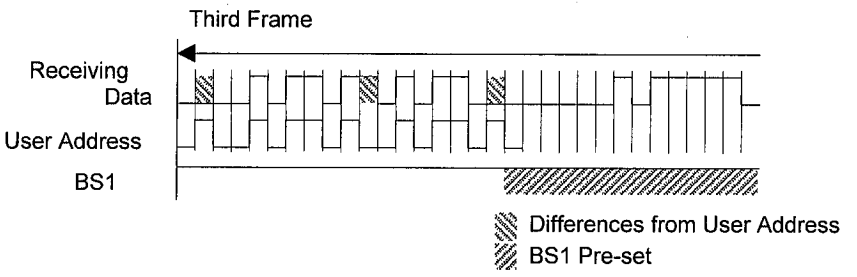


Fig.24c Simple Decision of Address with 6 or more in RFC

(4-7) SC Disregard

By disregarding SC after Synchronization Achievement, the power saving is realized to stop the outputs of BS1, BS2 and BS3. The times of SC disregard are set by IGSC6 to 0 in the control register. The maximum time of SC Disregard is for 127-batch.

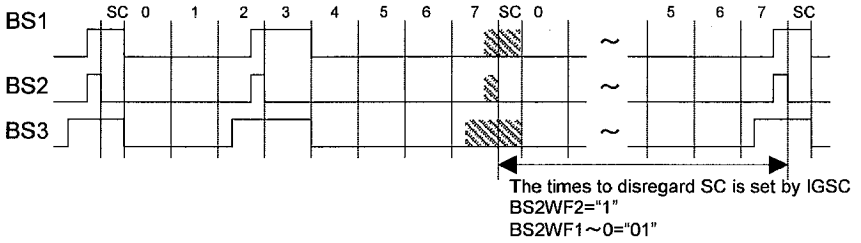


Fig.25a SC Disregard

In case of receiving the message sandwiching SC, SC is not disregarded.

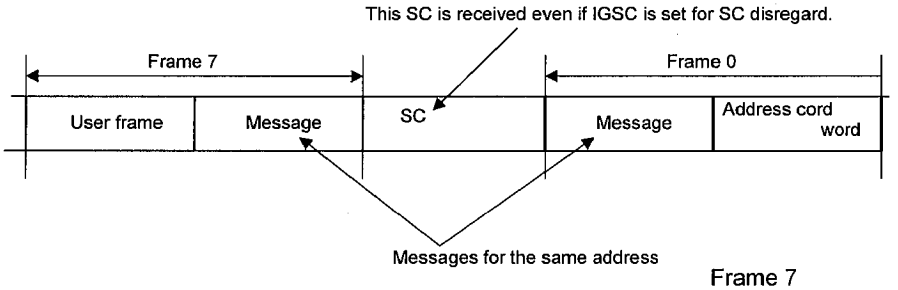


Fig.25b SC sandwiched by Messages

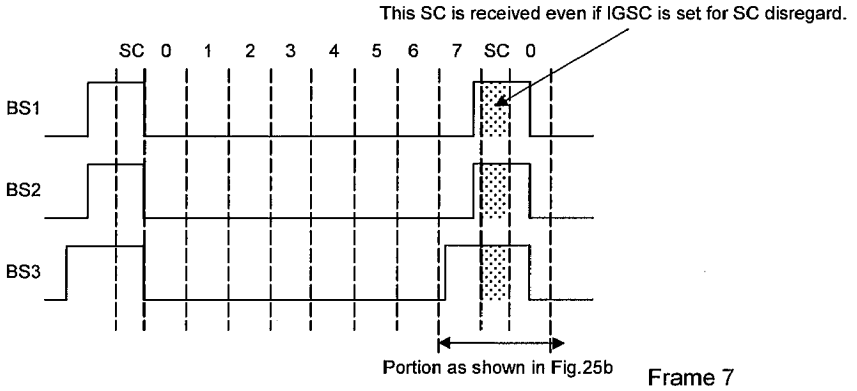


Fig.25c BS signal (BS2WF2 , 1 and 0 = 1, 0 and 0) when a signal as shown in Fig.25b is received

When the IGSC is set again to "0" in the receiving operation, the new condition of IGSC as "0" becomes effective immediately. When it is not "0", it dose not become effective until the sequence of SC Disregard in accordance with the former condition is completed. (refer Fig.26a and b)

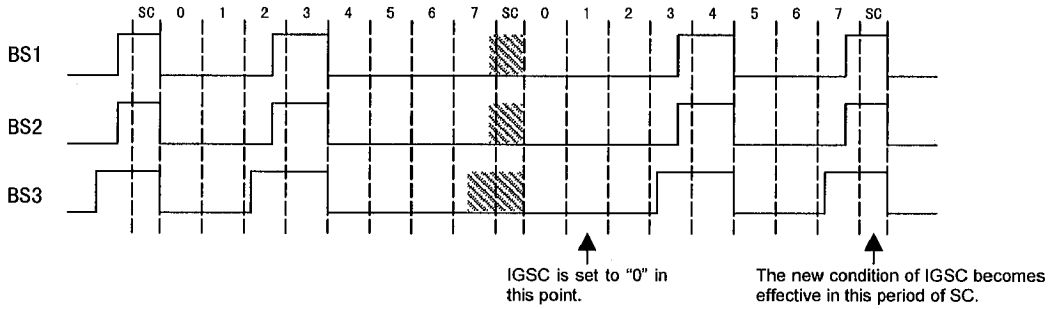


Fig.26a In case of IGSC re-setting to "0"

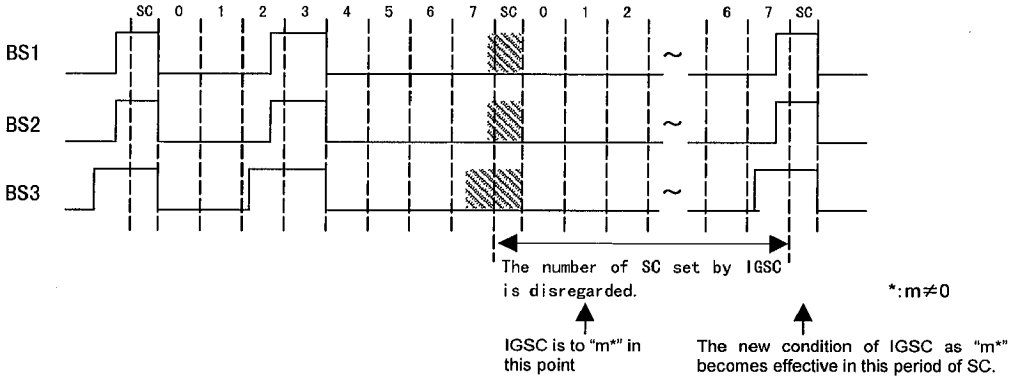


Fig.26b In case of IGSC re-setting to any number excepting for "0"

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3～+5.0	V
Input voltage	V_{IN}	-0.3～V_{DD}+0.3	V
Operating Temperature	T_{opr}	-20～+75	℃
Storage Temperature	T_{stg}	-55～+125	℃

Note) Decoupling capacitor should be connected between the V_{DD} terminal and the V_{SS} due to the stabilization of the operation.

■ ELECTRICAL CHARACTERISTICS

·DC CHARACTERISTICS

(V_{DD}=2.6～3.4V, V_{SS}=0V,Ta=-20～75℃)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		2.6	—	3.4	V
High-level Input Voltage	V_{IH}		0.8×V_{DD}	—	V_{DD}	V
Low-level Input Voltage	V_{IL}		V_{SS}	—	0.2×V_{DD}	V
High-level Output Current	I_{OH}	V_{DD}=3.0V, V_{OH}=V_{DD}-0.3V Excepting the XTN terminal	-400	-200	-100	μA
Low-level Output Current	I_{OL}	V_{DD}=3.0V, V_{OL}=0.3V Excepting the XTN terminal	100	200	400	μA
Input Leakage Current	I_{IN}		-1	—	1	μA
Pull-down resistance Current	I_P	Operating TEST terminal	12	25	38	μA
Stand-by Current	I_{DDQ}	Note.1	—	—	1.0	μA
Operating Current	I_{DD}	V_{DD}=3.0V, Note.2	—	5	8	μA
		V_{DD}=3.0V, Note.3	—	5.5	9	

Note.1) X'tal oscillator is stopped.
Note.2) The CLK-OUT terminal doesn't output the clock pulses.
Note.3) The CLK-OUT terminal outputs the clock pulses.

· X'tal Oscillator

(V_{DD}=2.6～3.4V,V_{SS}=0V,Ta=-20～75℃)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Built-in Feedback Resistance	R_f	Operating	—	10	—	MΩ
Load Capacitance	C_g,C_d	Operating	—	18	—	pF
Oscillation Frequency	F_O	Operating	—	76.8	—	kHz

■ ELECTRICAL CHARACTERISTICS

· AC CHARACTERISTICS

CPU INTERFACE (V_{DD}=2.6~3.4V,V_{SS}=0V,Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Operating Frequency	f_{OSC}	Fig.26	-250ppm	76.8	+250ppm	kHz
SCK Cycle Time	t_{SCKCYC}	Fig.26	10	—	—	μs
SCK Pulse High-level Width	t_{SCKH}	Fig.26	5	—	—	μs
SCK Pulse Low-level Width	t_{SCKL}	Fig.26	5	—	—	μs
SDO Output Delay Time	t_{SDOD}	Fig.26	—	—	5	μs
SDI Setup Time to SCK	t_{SDISU}	Fig.26	1	—	—	μs
SDI Hold Time to SCK	t_{SDIHD}	Fig.26	1	—	—	μs
Rise Time	t_{SR}	Fig.26	—	—	500	ns
Fall Time	t_{SF}	Fig.26	—	—	500	ns

CLK-OUT

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Cycle Time	t_{CKOCYC}	Fig.27	—	13.0	—	μs
Rise Time	t_{CKOR}	Fig.27	—	—	3	μs
Fall Time	t_{CKOF}	Fig.27	—	—	3	μs

RST

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reset Low-level Width	t_{RST}	The $\overline{RST}$ Terminal	1	—	—	ms

OSCILLATOR START-UP TIME

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Start-up Time	t_{STRT}	Fig.28	—	—	800	ms

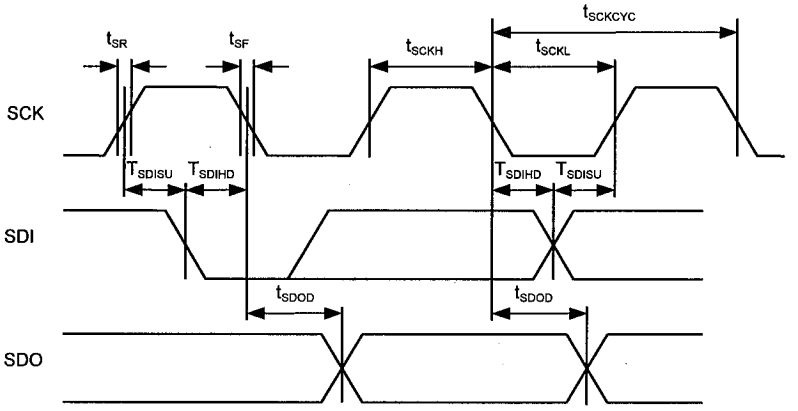


Fig.26 CPU INTERFACE TIMING CHART

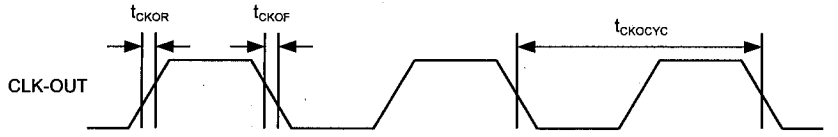


Fig.27 CLK-OUT WAVEFORM

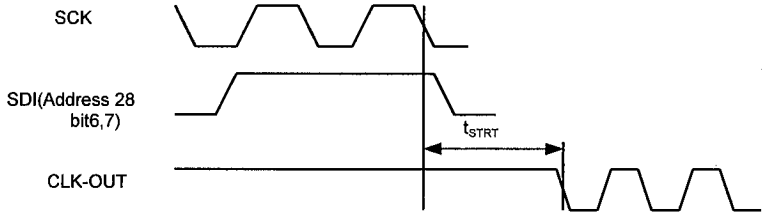
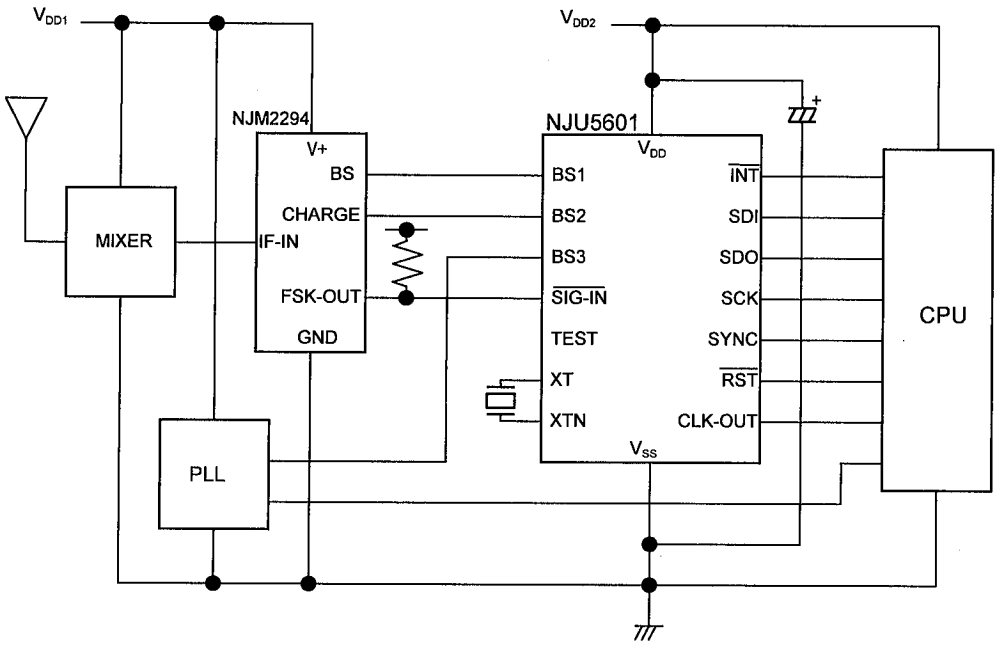


Fig.28 OSCILLATOR START-UP TIME

■ APPLICATION CIRCUITS



MEMO