LITTLE FOOT® TSSOP-8
The Next Step in Surface-Mount Power MOSFETs

Wharton McDaniel and David Oldham

When Vishay Siliconix introduced its LITTLE FOOT MOSFETs, it was the first time that power MOSFETs had been offered in a true surface-mount package, the SOIC. LITTLE FOOT immediately found a home in new small form factor disk drives, computers, and cellular phones.

The new LITTLE FOOT TSSOP-8 power MOSFETs are the natural evolutionary response to the continuing demands of many markets for smaller and smaller packages. LITTLE FOOT TSSOP-8 MOSFETs have a smaller footprint and a lower profile than LITTLE FOOT SOICs, while maintaining low $r_{DS(on)}$ and high thermal performance. Vishay Siliconix has accomplished this by putting one or two high-density MOSFET die in a standard 8-pin TSSOP package mounted on a custom leadframe.

THE TSSOP-8 PACKAGE

LITTLE FOOT TSSOP-8 power MOSFETs require approximately half the PC board area of an equivalent LITTLE FOOT device (Figure 1). In addition to the reduction in board area, the package height has been reduced to 1.1 mm.

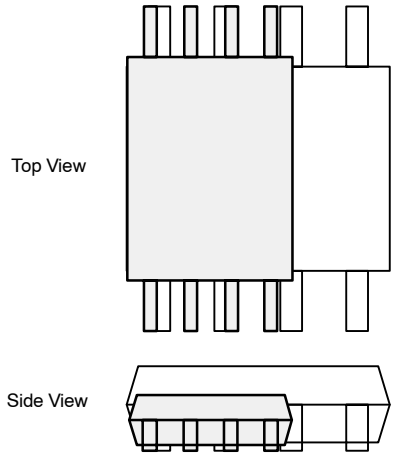


Figure 1. An TSSOP-8 Package Next to a SOIC-8 Package with Views from Both Top and Side

This is the low profile demanded by applications such as PCMCIA cards.

It reduces the power package to the same height as many resistors and capacitors in 0805 and 0605 sizes. It also allows placement on the “passive” side of the PC board.

The standard pinouts of the LITTLE FOOT TSSOP-8 packages have been changed from the standard established by LITTLE FOOT. This change minimizes the contribution of interconnection resistance to $r_{DS(on)}$ and maximizes the transfer of heat out of the package.

Figure 2 shows the pinouts for a single-die TSSOP. Notice that both sides of the package have Source and Drain connections, whereas LITTLE FOOT has the Source and Gate connections on one side of the package, and the Drain connections are on the opposite side.

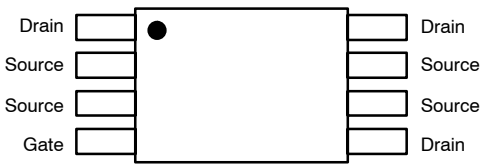


Figure 2. Pinouts for Single Die TSSOP

Figure 3 shows the standard pinouts for a dual-die TSSOP-8. In this case, the connections for each individual MOSFET occupy one side.

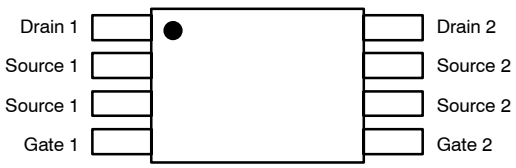
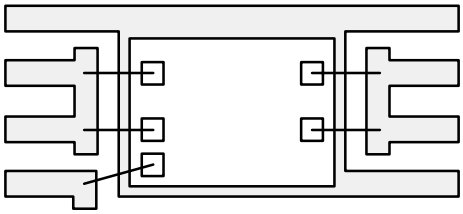


Figure 3. Pinouts for Dual-Die TSSOP

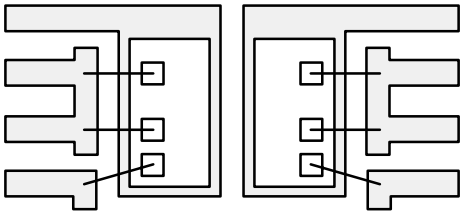
Because the TSSOP has a fine pitch foot print, the pad layout is somewhat more demanding than the layout of the SOIC. Careful attention must be paid to silkscreen-to-pad and soldermask-to-pad clearances. Also, fiduciary marks may be required. The design and spacing of the pads must be dealt with carefully. The pads must be sized to hold enough solder paste to form a good joint, but should not be so large or so placed as to extend under the body, increasing the potential for solder bridging. The pad pattern should allow for typical pick and place errors of 0.25 mm. See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286), for the recommended pad pattern for PC board layout.

THERMAL ISSUES

LITTLE FOOT TSSOP MOSFETs have been given thermal ratings using the same methods used for LITTLE FOOT. The maximum thermal resistance junction-to-ambient is 83°C/W for the single die and 125°C/W for dual-die parts. TSSOP relies on a leadframe similar to LITTLE FOOT to remove heat from the package. The single- and dual-die leadframes are shown in Figure 4.



a) 8-Pin Single-Pad TSSOP



b) 8-Pin Dual-Pad TSSOP

Figure 4. Leadframe

The MOSFETs are characterized using a single pulse power test. For this test the device mounted on a one-square-inch piece of copper clad FR-4 PC board, such as those shown in Figure 5. The single pulse power test determines the maximum amount of power the part can handle for a given pulse width and defines the thermal resistance junction-to-ambient. The test is run for pulse widths ranging from approximately 10 ms to 100 seconds. The thermal resistance at 30 seconds is the rated thermal resistance for the part. This rating was chosen to allow comparison of packages and leadframes. At longer pulse widths, the PC board thermal charateristics become dominant, making all parts look the same.

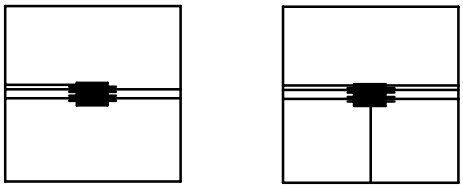


Figure 5.

The actual test is based on dissipating a known amount of power in the device for a known period of time so the junction temperature is raised to 150°C. The starting and ending junction temperatures are determined by measuring the forward drop of the body diode. The thermal resistance for that pulse width is defined by the temperature rise of the junction above ambient and the power of the pulse, ΔTja/P.

Figure 6 shows the single pulse power curve of the Si6436DQ laid over the curve of the Si9936DY to give a comparison of the thermal performance. The die in the two devices have equivalent die areas, making this a comparison of the packaging. This comparison shows that the TSSOP package performs as well as the SOIC out to 150 ms, with long-term performance being 0.5 W less. Although the thermal performance is less, LITTLE FOOT TSSOP will operate in a large percentage of applications that are currently being served by LITTLE FOOT.

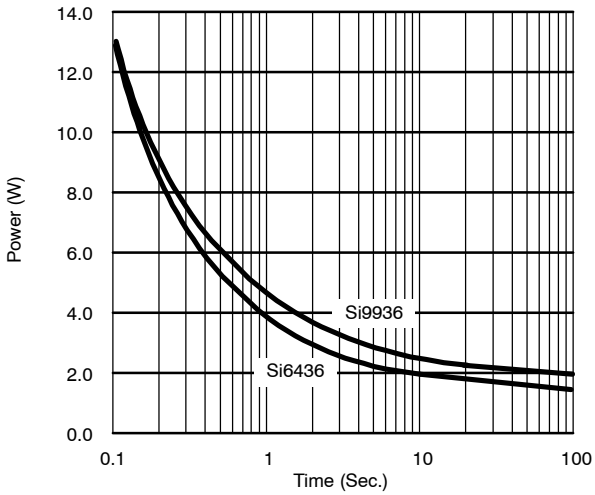


Figure 6. Comparison of Thermal Performance

CONCLUSION

TSSOP power MOSFETs provide a significant reduction in PC board footprint and package height, allowing reduction in board size and application where SOICs will not fit. This is accomplished using a standard IC package and a custom leadframe, combining small size with good power handling capability.

For the TSSOP-8 package outline visit:
http://www.vishay.com/doc?71201
For the SOIC-8 package outline visit:
http://www.vishay.com/doc?71192