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L64765
Color and Raster-Block Converter

Logo

Introduction

The L64765 Color and Raster-Block Converter performs two main functions: color conversion among RGB, YCbCr, and Y-only formats; and reformatting between raster-ordered and block-ordered image data. The L64765 can be used either as a preprocessor in image encoding systems, or a reconstructor in decoding systems.

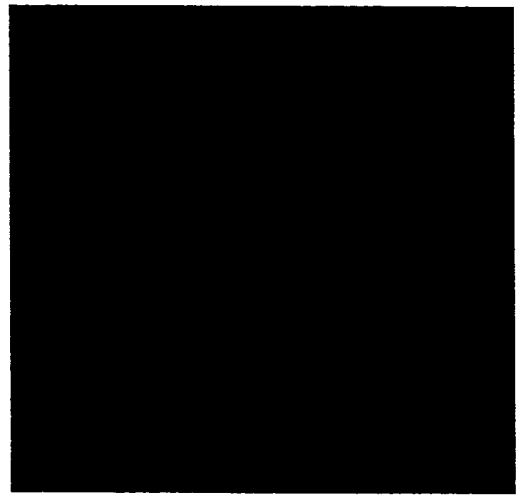
Image data can be supplied to the L64765 in nine formats to ensure compatibility with most standard video devices.

Three internal correction tables apply a transformation to each color at the RGB interface. This transformation is typically a gamma correction. Data in the correction tables is downloaded to the L64765.

The color conversion is performed by a fixed digital matrix defined to convert between RGB and YCbCr as defined by the CCIR Recommendations 601, Mod F. A range limiter forces out-of-range data values into the usable range. Color conversion can be bypassed.

The L64765 includes internal resampling filters that downsample YCbCr data into a 2:1:1 ratio in the encoder direction and reconstruct the data in the decoder direction.

The raster-block reformatting uses an external strip memory to store eight scan lines. The L64765 includes an internal buffer RAM to assist in the reformatting process. The L64765 supports an 8x8 block format, and can process scan lines up to 8192 pixels wide. Raster-block reformatting can be bypassed.



L64765 Die Photograph

The L64765 is a member of the JPEG image compression chipset, which also includes the L64735 DCT Processor and the L64745 JPEG Coder. These three devices provide a complete solution for compression or decompression of digital raster-scanned RGB data to coded bit stream. When combined with a small number of external memory and support devices, these chips implement a complete still-image compression and decompression system.

Features

- Performs raster-to-block or block-to-raster conversion
- Performs color space conversions in either direction:
  - RGB-to-YCbCr or YCbCr-to-RGB
  - RGB-to-Y-only or Y-only-to-RGB
  - YCbCr-to-Y-only or Y-only-to-YCbCr
- Applies gamma correction from user-defined internal gamma correction tables
- Supports nine image data formats
- Support eight scan lines up to 8192 active pixels wide
- Supports user-programmable active window area synchronized to video sync signals
- Interfaces directly to LSI Logic L64735 DCT Processor
- Implements CCIR Recommendation 601, Mod F, for color space conversion
- Supports 2:1:1 downsampling with decimation and interpolation
- Operates at 27 MHz clock speed
- Is supplied in 100-pin ceramic pin-grid array (CPGA) package

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System Applications

Figure 1 shows a typical system application of the L64765. This system design supports encoding and decoding applications. The example shows the use of the other members of the JPEG chipset, the L64735 DCT Processor and the L64745 JPEG Coder. The text following the figure describes the function of the devices in the example.

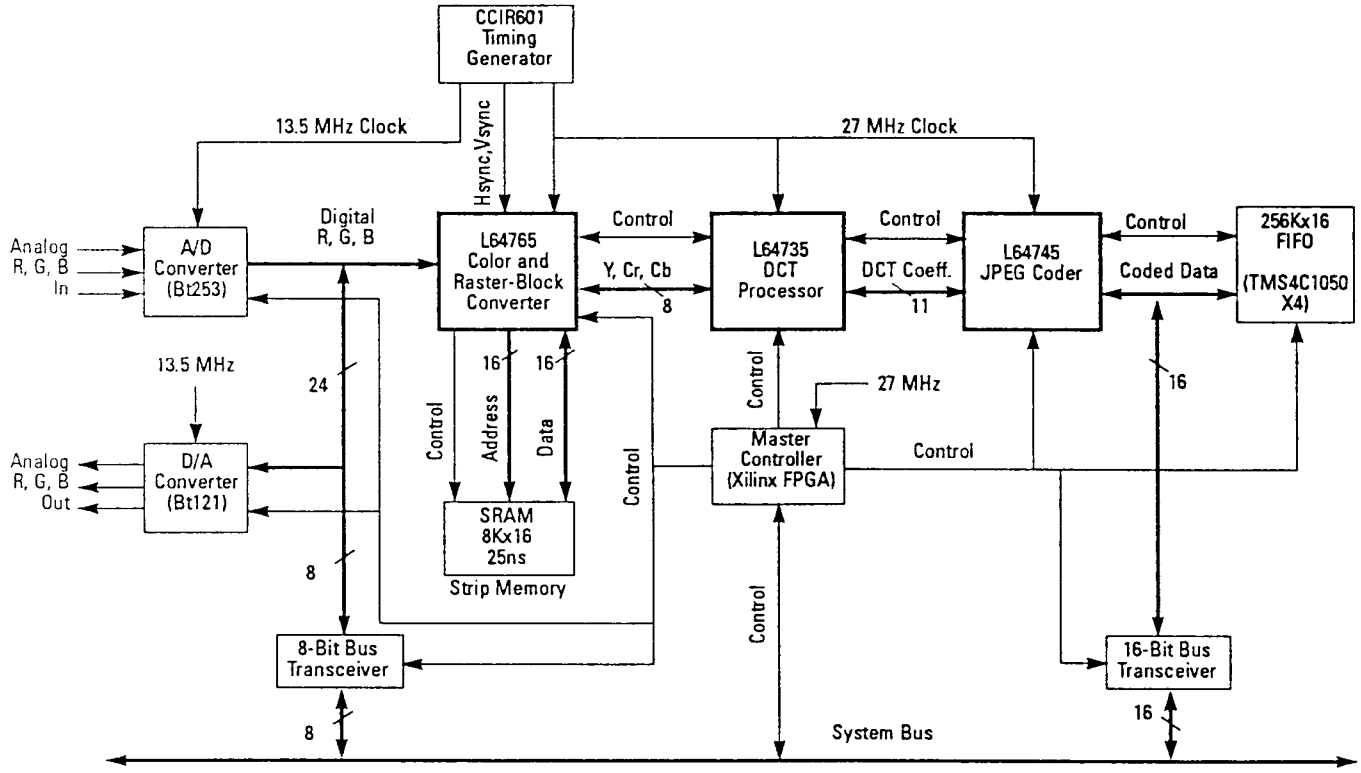

Figure 1. Typical Video Real-Time Image Processing Application

In encoding applications, the *A/D Converter* converts analog input RGB data into 24-bit digital RGB data for input to the L64765. The L64765 converts RGB values to luminance (Y) and chrominance (C_b, C_r) components and arranges the raster image into 8x8 blocks. The *Strip Memory* buffers eight lines of the raster-scanned image to assist in the raster-to-block conversion. The *L64735 DCT Processor* performs a discrete cosine transform on the 8x8 blocks to produce DCT coefficients. The *L64745 JPEG Coder* quantizes and encodes the DCT coefficients into a compressed data stream.

The *FIFO* stores the compressed data stream. In the application shown, the FIFO provides 512 Kbytes of storage for the compressed image. At a typical 24:1 compression ratio, this memory can store an image as large as 12 Mbyte, or 16 NTSC images (512 X 480 X 24).

The *Master Controller* provides all control signals and performs the handshaking between the host and the L64745, and the host and the FIFO. The Master Controller initializes all three chips in the chipset and controls the transfer of data between the L64745 and the FIFO, and the FIFO and the system bus.

In decoding applications, the data flow is reversed. The *D/A Converter* converts the digital RGB image data from the L64765 into analog RGB data.

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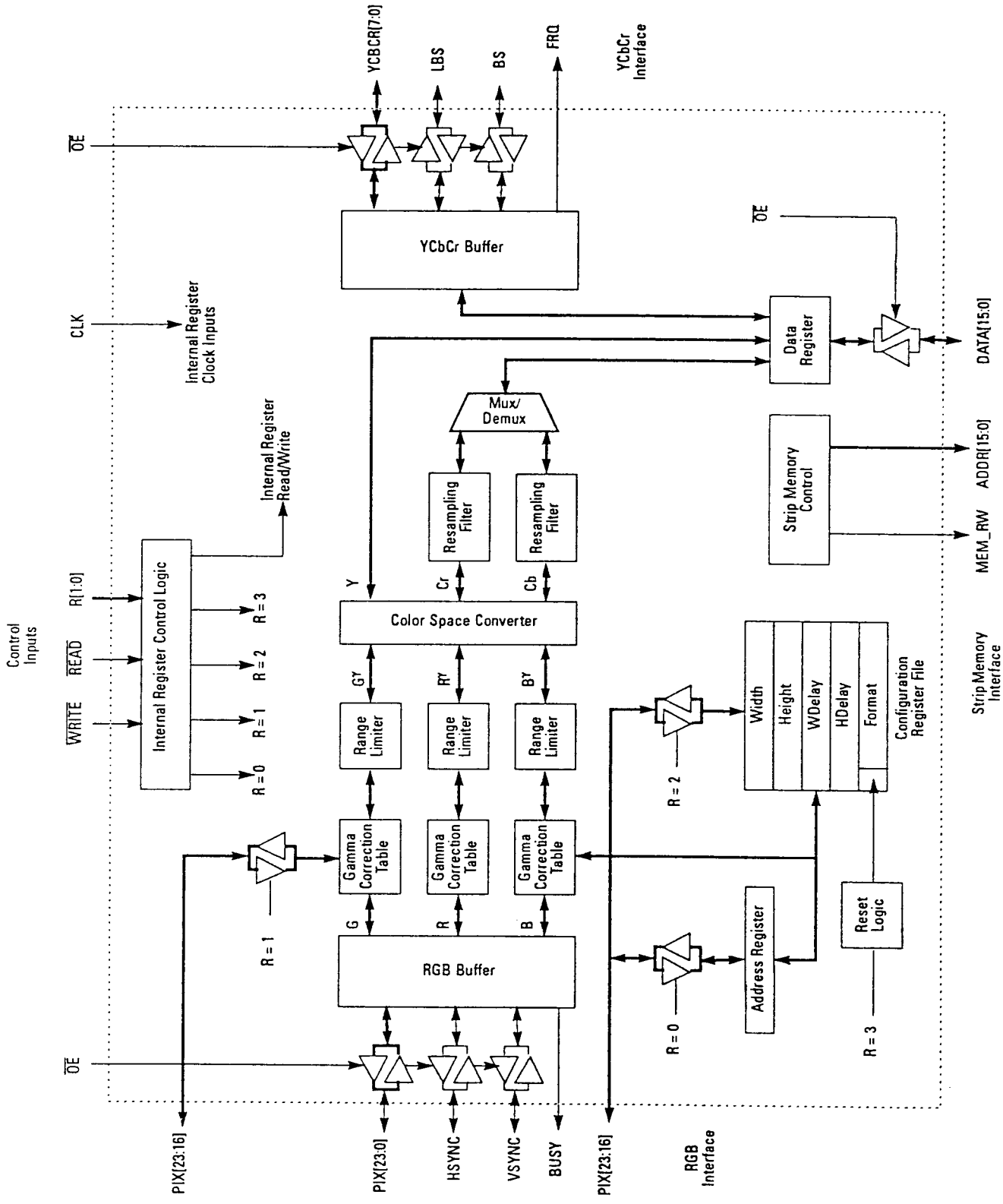

Figure 2. L64765 Internal Block Diagram

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Functional Overview

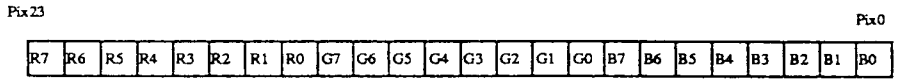
Figure 2 is a block diagram showing major functional blocks of the L64765. Bold lines indicate buses (more than one signal).

RGB Interface

The RGB interface operates at a sample rate of at least 13.5MHz. These bidirectional lines are configured as either inputs or outputs depending on the direction of the conversion. The RGB interface reads or writes data in one of the data formats described below. The data format used by the L64765 is set in the Format Register described later in "Control Registers."

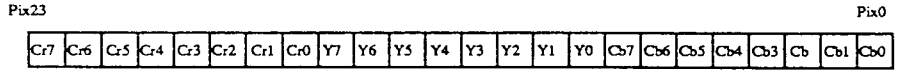
- 24 bit RGB

  Twenty four bits of RGB data (8 bits each) are transferred on the RGB interface at rates up to 13.5 M samples/sec.The original source signal is assumed to be band-limited and in the range 0-255 for each component.



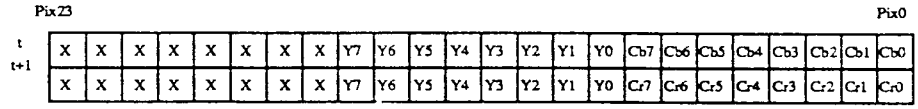
- 24 bit YCbCr

  Twenty four bits of YCbCr data (8 bits each) are transferred on the RGB interface. The sample rate of the signal is 13.5MHz or greater. Y,Cr and Cb are all unsigned, Cr and Cb being level shifted by +128. The original source signal is assumed to be band-limited and in the range 0-255 for each component.



- 16 bit YCbCr (4:2:2 or 2:1:10

  This mode is compatible with the Phillips SAA7151 and SAA7197 digital television decoders and Brooktree VideoNet transceivers. The Cr and Cb data is time multiplexed onto the same eight pins since it is already sampled at half the frequency of Y. Cr and Cb are level shifted and range limited as above. The first active pixel on each scan line is always a Y-Cb pair.



- 16 Bit RGB

  Three 16-bit RGB formats are commonly implemented in graphics systems. In RGB order these are (X,5,5,5), (6,6,4) and (5,6,5).

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(X,5,5,5)

X	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(6,6,4)

X	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B3	B2	B1	B0

(5,6,5)

X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

- 32 Bit RGB

Two 32-bit RGB formats are supported. In each case, each pixel is represented by eight bits; the most significant eight bits are always unused. These modes differ from the 24-bit RGB mode in that the data is multiplexed onto the lower 16 bits of the RGB interface on alternate cycles.

RGB

t	X	X	X	X	X	X	X	X	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0
t+1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B7	B6	B5	B4	B3	B2	B1	B0

BGR

t	X	X	X	X	X	X	X	X	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
t+1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	R2	R1	R0

Gamma Correction Tables

Each channel can be transformed by a user-defined function, e.g., gamma correction. The function is stored in an independent 256 X 8 lookup table for each channel. The lookup tables can be read or written as described later in "Initialization and Control."

Color Space Converter

Color space conversion is performed by a digital matrix. To allow the same matrix to be used for CCIR-compatible YCbCr data streams and RGB data streams, data in either form must be in the range 16-235. If input data falls outside this range, the range limiters clamp the data to the appropriate boundary value.

The color conversion matrix may be bypassed in either direction to allow systems with images already in YCbCr space to use the raster to block conversion function.

The RGB-to-YCbCr and YCbCr-to-RGB matrices are defined in the CCIR601 specification. The matrices for these conversions are shown in Figure 3 and Figure 4 below.

$$Y = (77/256)R + (150/256)G + (29/256)B$$
$$Cr = (131/256)R - (110/256)G - (21/256)B + 128$$
$$Cb = (-44/256)R - (87/256)G + (131/256)B + 128$$

Figure 3. RGB-to-YCbCr Matrix

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$$R = Y + 1.370\,(Cr - 128)$$
$$G = Y - 0.698\,(Cr - 128) - 0.336\,(Cb - 128)$$
$$B = Y + 1.730\,(Cb - 128)$$

Figure 4. YCbCr-to-RGB Matrix

Resampling Filters
The resampling filters implement one of two built-in transfer functions depending on the direction of the conversion. In the forward (RGB-to-YCbCr) direction, the filters downsample the RGB components in a 2:1:1 ratio. The built-in forward transfer function H uses the values of the current pixel Z_0 and the two adjacent pixels Z_{-1} and Z_1. The first and last pixel in each scan line are not filtered. Figure 5 shows the forward transfer function.

$$H(Z) = (128/256)\,Z^0 + (64/256)\,(Z^{-1} + Z^1)$$

Figure 5. Resampling Filter Forward Transfer Function

In the reverse (YCrCB-to-RGB) direction, the pixel value is reconstructed based on the values of the adjacent pixels. The first and last pixel in each scan line require no reconstruction. Figure 6 shows the reverse transfer function.

$$H(Z) = (128/256)\,(Z^{-1} + Z^1)$$

Figure 6. Resampling Filter Reverse Transfer Function

In some pixel formats, the resampling filters are automatically bypassed. See "Control Registers" for more information on pixel formats.

Strip Memory Interface
Raster data is stored in an external strip memory to facilitate raster-to-block conversion. Since a 16 bit YCr/Cb pixel must be read and written every 74 ns at 13.5 MHz, the strip memory interface is 16 bits wide for a cycle time of 37 ns. 25ns RAMs can be used in the strip memory. In sustained operation a pixel is first read from the memory before a new raster sample is written to the same address. After eight scan lines have been written, the process is repeated. The read-then-write scheme reduces the number of addressing operations and increases the utilization of the strip memory.

The 16-bit address bus can access up to 64K pixels. This memory addressing range is enough to support eight 17-inch scan lines at 300 dpi (40,800 pixels). However, the system configuration need only include the amount of memory that will actually be used. The L64765 always uses the minimum amount of memory as shown in the equation below, where *M* is the memory size in 16-bit words and *width* is the width of the active window in pixels:

$$M = 8 \times width$$

For example, an image 512 pixels wide requires a strip memory of 4K (4,196) 16-bit words.

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Addresses are always generated starting at zero after reset.

The memory access cycle is optimized for static RAMS. The read/write cycle occurs every 2 CLK cycles. The memory cycle is fully synchronous with respect to the device clock. Figure 7 shows the memory access cycle.

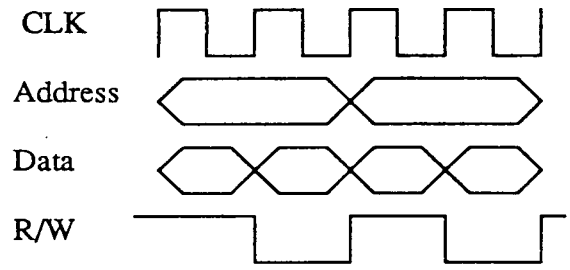

Figure 7. Memory Access Timing

The active image area is restricted to contain only complete MCUs (minimum coded units). In the L64765, an MCU contains two data blocks of the luminance component and one data block each of the two chrominance components (2:1:1). An MCU is 8 pixels high by 16 pixels wide.

YCbCr Interface

The YCbCr interface transfers the reformatted and subsampled data to and from the L64735 DCT Processor. The 8-bit wide data bus is organized in 8x8 blocks for the L64735 DCT Processor. An optional Y only mode is supported by forcing the Cr and Cb components to zero. This allows the YCbCr interface to operate at the same rate regardless of mode. The sustained data transfer rate is 2x(sample frequency). The raster to block conversion function and 2:1:1 data reformatting may be optionally bypassed. In this case data on the YCbCr interface is in the format YCbYCr; i.e. a time-multiplexed raster-ordered signal similar to the one described in CCIR 601.

External Interface

The external interface to the L64765 consists of the signals shown in Figure 8. Each signal is described in the text following the figure.

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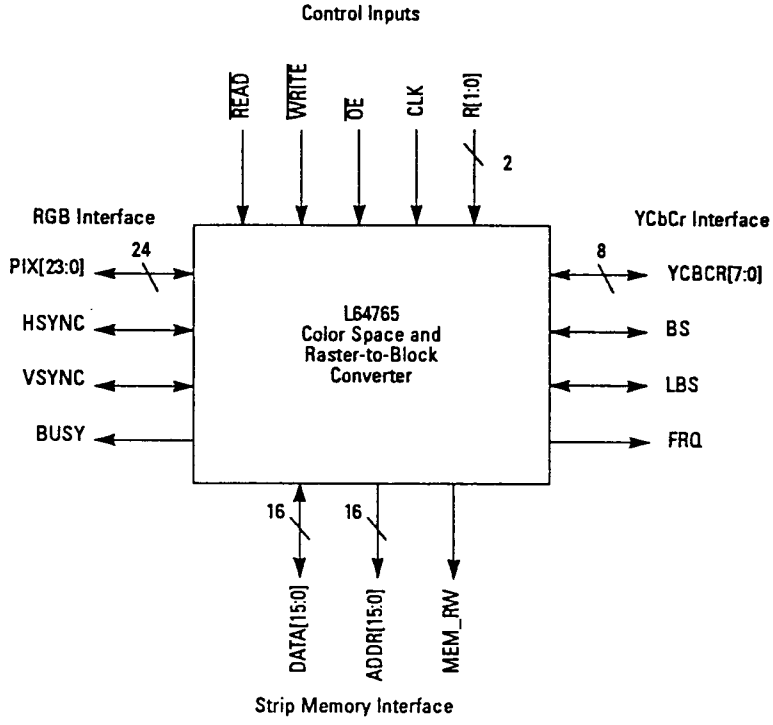

Figure 8. L64765 Logic Symbol

RGB Interface Signals
These signals comprise the interface to the digital RGB signals.

PIX[23:0]

24 bit RGB interface data I/O. In encode mode, PIX[23:0] are inputs. In decode mode, PIX[23:0] are outputs. Data on PIX[23:0] is translated according to the control bits in the format control register.The upper 8 bits of this bus, PIX[23:16], are used to read from and write to the internal control registers. See "Control Registers" for more information.

HSYNC

A positive-going pulse indicates to the L64765 that the input data source has reached the beginning of a scan line. HDelay is measured from HSYNC going HIGH. HSYNC is synchronous with respect to the device clock CLK. HSYNC is allowed to go low before all the pixels in a scan are sampled so that images without a line flyback interval may be handled. HSYNC is an input in both encode and decode mode, except in decode raster mode when HSYNC is an output. In block decode mode the L64765 uses inputs HSYNC and VSYNC to sync the device to the external video source.

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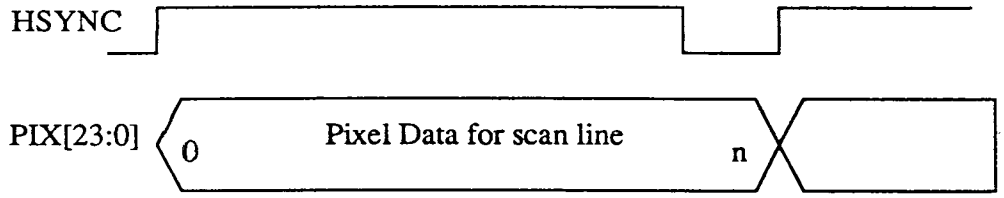

Figure 9. HSYNC Timing for Image with No Horizontal Flyback Interval

VSYNC

A positive-going input pulse indicates that the beginning of a frame has been reached. VDelay is measured from VSYNC going high. The L64765 uses a combination of VSYNC and the active display area to determine when LBS is to be asserted. As above, VSYNC may be asserted before the last scanline of the image is reached to deal with the case of image scanners with no vertical retrace interval. VSYNC is assumed synchronous with respect to the device clock, and is an input in both encoder and decoder mode, except decode raster mode where it is an output.

BUSY

In encoder operation, the L64765 asserts BUSY (HIGH) to inhibit the input of data on the PIX bus.

Strip Memory Interface
These signals comprise the interface between the L64765 and the external 16-bit wide strip memory.

DATA[15:0]

16 bit bidirectional data bus. DATA[15:0] are used to read and write data to the strip memory.

ADDR[15:0]

16 bit address output bus. ADDR[15:0] selects the address of the strip memory.

MEM_R/W

Read/Write output. MEM_R/W designates a strip memory operation as a read or write cycle. MEM_R/W is asserted HIGH for read operations and deasserted LOW for Write.

YCbCr Interface
These signals comprise the interface between the L64765 and the portion of the system that processes YCbCr data. In a typical system such as the one shown previously in "System Applications," these signals interface directly to the L64735 DCT Processor.

YCBCR[7:0]

8 bit subsampled data I/O bus. Data on this bus is presented in the 2:1:1 format used by the L64735 in JPEG blocking mode, or in YCbYCr time-multiplexed format in raster mode. YCBCR[7:0] are bidirectional, operating as outputs in encoder mode and as inputs in decoder mode.

BS

Block Start. BS indicates the beginning of a new block of input or output samples on YCBCR[7:0] during JPEG blocking mode. BS is always coincident with the first pixel of the block. In raster mode it is a copy of HSYNC, delayed by the pipeline delay of the L64765.

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LBS

Last Block Strobe. LBS indicates that the last block of an image was just passed over YCBCR[7:0]. LBS is asserted on the first sample *after* the last pixel in the active window is presented on YCBCR[7:0]. In encode mode, LBS is generated by the L64765 after processing of the last block in the image window. In decode mode, LBS is typically generated by the L64745. In raster mode, LBS is a copy of VSYNC delayed by the pipeline delay of the L64765 in both the encode and decode direction

FRQ

Freeze Request output. FRQ controls the optional external gating of the device clocks to the L64735 and L64745 so that data flow is correctly controlled during horizontal and vertical blanking intervals.

Control Inputs
These input signals comprise the control interface to the L64765.

R[1:0]

Register address input bits. R[1:0] set the internal register or table being accessed during a read or write operation as shown in Table 1.

$\overline{\text{READ}}$

Active low signal. When READ is asserted, the L64765 initiates a read operation from the internal register or table indicated by R[1:0]. Reading from the Gamma Table or Initialization Table registers causes the data pointed to by the current value of the address register to be read. The address register increments after each read.

$\overline{\text{WRITE}}$

Active low signal. Data is written to the control register indicated by R[1:0] on the rising edge of $\overline{\text{WRITE}}$.

$\overline{\text{OE}}$

Active low output enable pin. When $\overline{\text{OE}}$ is LOW, PIX[23:0] and YCBCR[7:0] are 3-stated.

CLK

The L64765 is clocked on the rising edge of CLK.

Control Registers

The L64765 uses PIX[23:16], the eight most significant bits of the PIX bus, to access the internal control registers. An external eight-bit bidirectional buffer is required to prevent contention between the external bus and the 8 most significant bits of the PIX bus (PIX[23:16]) during normal operation. Register loading is asynchronous with respect to the L64765 clock. The register select inputs [R0,R1] select the internal register or table to be accessed as shown in Table 1. The access is performed when $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ are asserted.

Table 1. R[1:0] Meaning

R[1:0]	Accesses:
00	Address Register
01	Gamma Correction Tables
10	Configuration Register File
11	Reset

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Address Register
The Address Register functions as a pointer to an internal location. The control inputs R[1:0] determine whether the Address Register points to an entry in a gamma table or a register in the configuration register file. To write a new value into the Address Register:

1. Place the address value on PIX[23:16].
2. Set R[1:0] to 00. (Steps 1 and 2 can be done in either order).
3. Assert $\overline{\text{WRITE}}$. The address value is stored in the Address Register on the rising edge of $\overline{\text{WRITE}}$.

Gamma Correction Tables
The L64765 has three separate gamma correction tables, one each for the R,G, and B digital inputs. Each table holds 256 entries. The Address Register points to a gamma address when R[1:0] is set to 01. The data written to a gamma address must be written in order: Red, Green, then Blue. Once the Blue value has been written, the Address Register automatically increments. The sequence for writing the complete gamma tables is:

1. Set the address register to 0x00 as described earlier in "Address Register."
2. Set R[1:0] to 01. The address register now points to address 00 of the R gamma table.
3. Place the Red value on PIX[23:16] and assert $\overline{\text{WRITE}}$ for one CLK cycle. This writes the value into the Red gamma table.
4. Write the Green value in the same way as the Red.
5. Write the Blue value in the same way as the Red. Once the Blue value is written, the Address Register automatically increments to 0x01.
6. Repeat steps 3, 4, and 5 until all 256 entries (address = 0xFF) have been written to all three tables.

Partial write operations are allowed: the Address Register can be set to any gamma table address, and the write operation does not have to go to the highest address (0xFF). However, for each gamma table address, the write operation must begin with Red.

Configuration Registers
The L64765 contains five internal configuration registers. The Format Register sets the format of the input RGB data on the PIX bus and controls other aspects of device operation. The four window control registers, Width, Height, WDelay, and HDelay, control the active window area of the image.

The configuration registers are addressed in the same manner as the correction tables. For all registers except the Format register, two load operations are required to write the full contents of the register. The less significant byte is always written first to the address shown in Table 2. The more significant byte is written to the next address. The address of each configuration register is shown in Table 2.

Table 2. Configuration Register Addresses

Address	Register	# of Loads Required
XXXX0000	Width	2
XXXX0010	Height	2
XXXX0100	WDelay	2
XXXX0110	HDelay	2
XXXX1XXX	Format	1

Format Register
The Format Register is accessed by any address with PIX.19 set to 1 and R[1:0] equal to 10_2. Figure 10 shows the content of the Format Register. Descriptions of the meaning of each field follow the figure.

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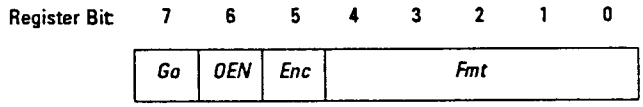

Figure 10. Format Register

Go **Go Control**
Go controls the start of frame processing. *Go* must be set before frame processing can begin.

In encode mode, the L64765 is enabled for frame processing when *Go* is set to one. The L64765 waits for the first pixel of the active window to begin processing.

In decode mode, the L64765 starts sampling the BS pin and filling the strip memory as appropriate. Once the strip memory is filled the L64765 waits until the first pixel of the active window before outputting the data on the PIX bus.

If *Go* is cleared to zero, the FRQ pin is reset to LOW. In encode mode, BS and LBS are deasserted to LOW. In decode mode, BS and LBS are ignored.

OEN **Output Enable Control**
OEN controls the state of all bidirectional signals. When *OEN* is set to one, all bidirectional signals are disabled. The $\overline{OE}$ input pin also disables the bidirectional signals; see "Pin Descriptions." For the bidirectional signals to be enabled, both *OEN* must be set to zero, and the $\overline{OE}$ pin must be deasserted (HIGH).

Enc **Code Operation Control**
Enc controls the direction of data flow. When *Enc* is set to one, the data input is from the PIX bus, and data output is on the YCBCR bus. When *Enc* is reset to zero, the dat input is from the YCBCR bus, and data output is on the PIX bus.

Fmt **Format Control**
Fmt is a five-bit field that controls how the L64765 interprets the PIX and YCBCR buses. Table 3 shows the meaning of the *Fmt* field.

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Table 3. FMT[4:0] Meaning

FMT[4:0]	PIX[23:0]	Order	YCBCR[7:0]	Filter	
10000	16-bit YCbCr	Raster	YCbYCr	No Filter	YCbCr Modes
00000	16-bit YCbCr	Block	YYCbCr	No Filter	
10001	24-bit YCbCr	Raster	YCbYCr	Filter	
00001	24-bit YCbCr	Block	YYCbCr	Filter	
11001	16/24-bit YCbCr	Raster	YCbYCr[1]	No Filter	
01001	16/24-bit YCbCr	~~Raster~~ Block	YCbYCr[1]	No Filter	
10010	(8,8,8) RGB	Raster	YCbYCr	Filter	1 cycle RGB Modes
00010	(8,8,8) RGB	Block	YYCbCr	Filter	
10011	(5,5,5) RGB	Raster	YCbYCr	Filter	
00011	(5,5,5) RGB	Block	YYCbCr	Filter	
10100	(6,6,4) RGB	Raster	YCbYCr	Filter	
00100	(6,6,4) RGB	Block	YYCbCr	Filter	
10101	(5,6,5) RGB	Raster	YCbYCr	Filter	
00101	(5,6,5) RGB	Block	YYCbCr	Filter	
11010	(8,8,8) RGB	Raster	YCbYCr[1]	Filter	
01010	(8,8,8) RGB	Block	YYCbCr[1]	Filter	
10110	(X,8,8,8) RGB	Raster	YCbYCr	Filter	2 cycle RGB Modes
00110	(X,8,8,8) RGB	Block	YYCbCr	Filter	
10111	(X,8,8,8) BGR	Raster	YCbYCr	Filter	
00111	(X,8,8,8) BGR	Block	YYCbCr	Filter	

Note:
1. In these formats, Cb and Cr data are set to zeroes.

Window Control Registers
The Window Control registers contain the values of four parameters: Width, Height, WDelay, and HDelay. Each Window Control register is 16 bits wide. The bits that are not used return zeros when read. Figure 11 shows the format of each register. The fields are defined in the text following the figure.

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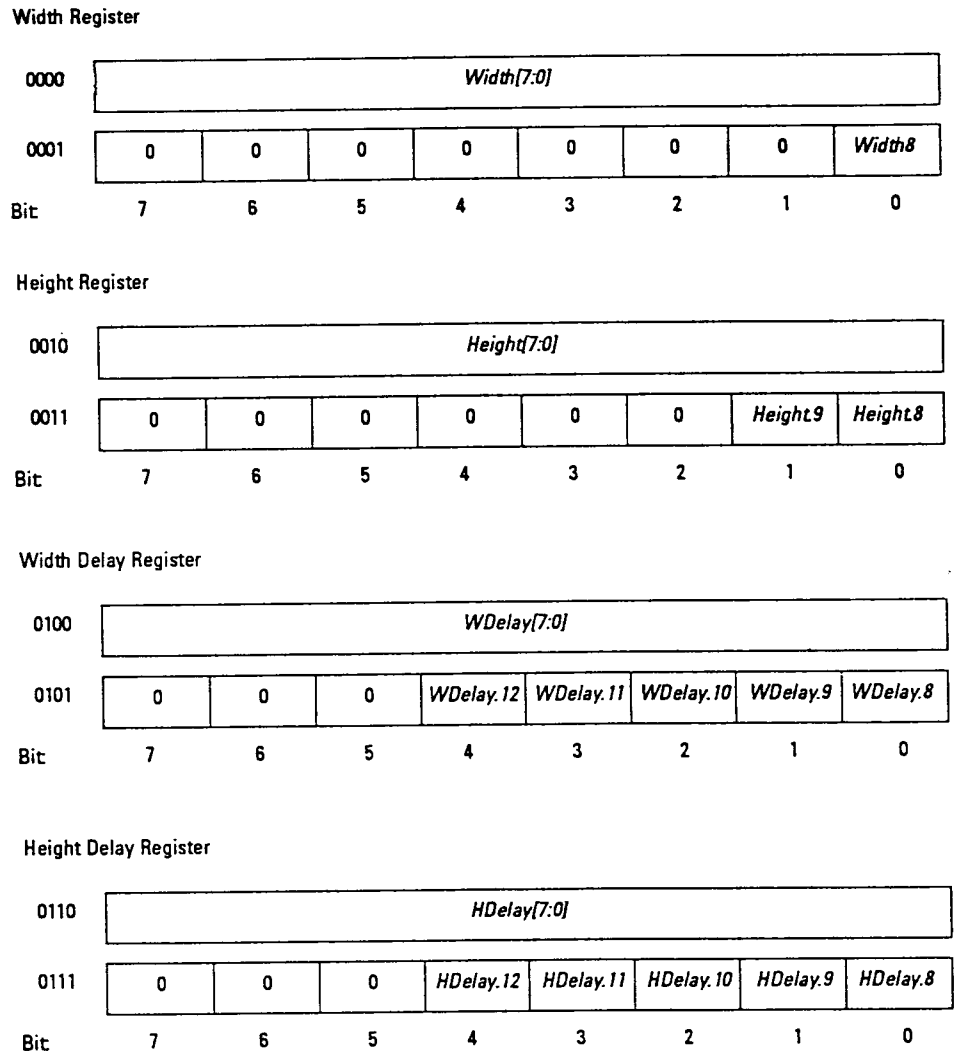

Figure 11. Window Control Registers

Width[8:0] **Image Width**
The width of the active image area in multiples of 16 pixels. The L64765 supports images up to 8192 pixels or 512 MCUs wide (1 MCU is 16 pixels wide).

Height[9:0] **Image Height**
The height of the active image area in multiples of 8 pixels. The L64765 supports images up to 8192 pixels 1024 MCUs high (1 MCU is 8 pixels high).

WDelay[12:0] **Width Delay**
The delay in pixels from the horizontal sync pulse to the first active pixel. *WDelay[12:0]* is in the range 0 to 8191.

HDelay[12:0] **Height Delay**
The delay in scan lines from the vertical sync pulse to the first active scan line. *HDelay[12:0]* is in the range 0 to 8191.

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The four parameters described above define the active image area as shown in Figure 12.

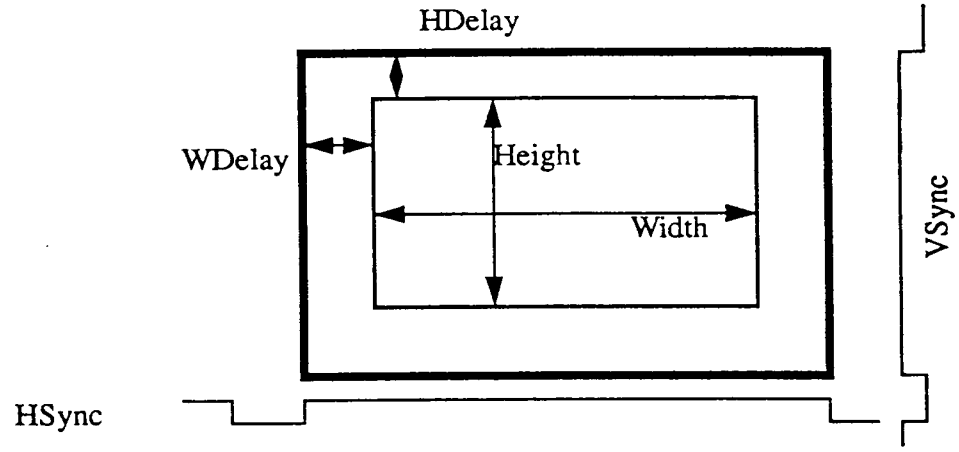

Figure 12. Active Image Area Defined by Window Parameters

Reset
A write operation to the Reset Register performs a reset operation on the L64765. (The value written is ignored). A reset operation clears the *Go* bit in the Format Register but does not otherwise affect the state of the L64765. The contents of the gamma correction tables and the configuration registers are unchanged after a reset operation.

Initialization

When the L64765 is powered on, the contents of the internal registers is undefined. Before the device is put into operation, this initialization sequence should be performed.

1. Set the values of Width, Height, WDelay, and HDelay as described earlier in "Window Control Registers."
2. Set the values of the operating parameters in the Format Register as described earlier in "Format Register." Do not set the *Go* bit yet.
3. Load the gamma correction into the tables as described earlier in "Gamma Correction Tables."
4. Perform a reset operation as described earlier in "Reset."
5. Set the *Go* bit. The L64765 is now ready for operation.

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Functional Waveforms

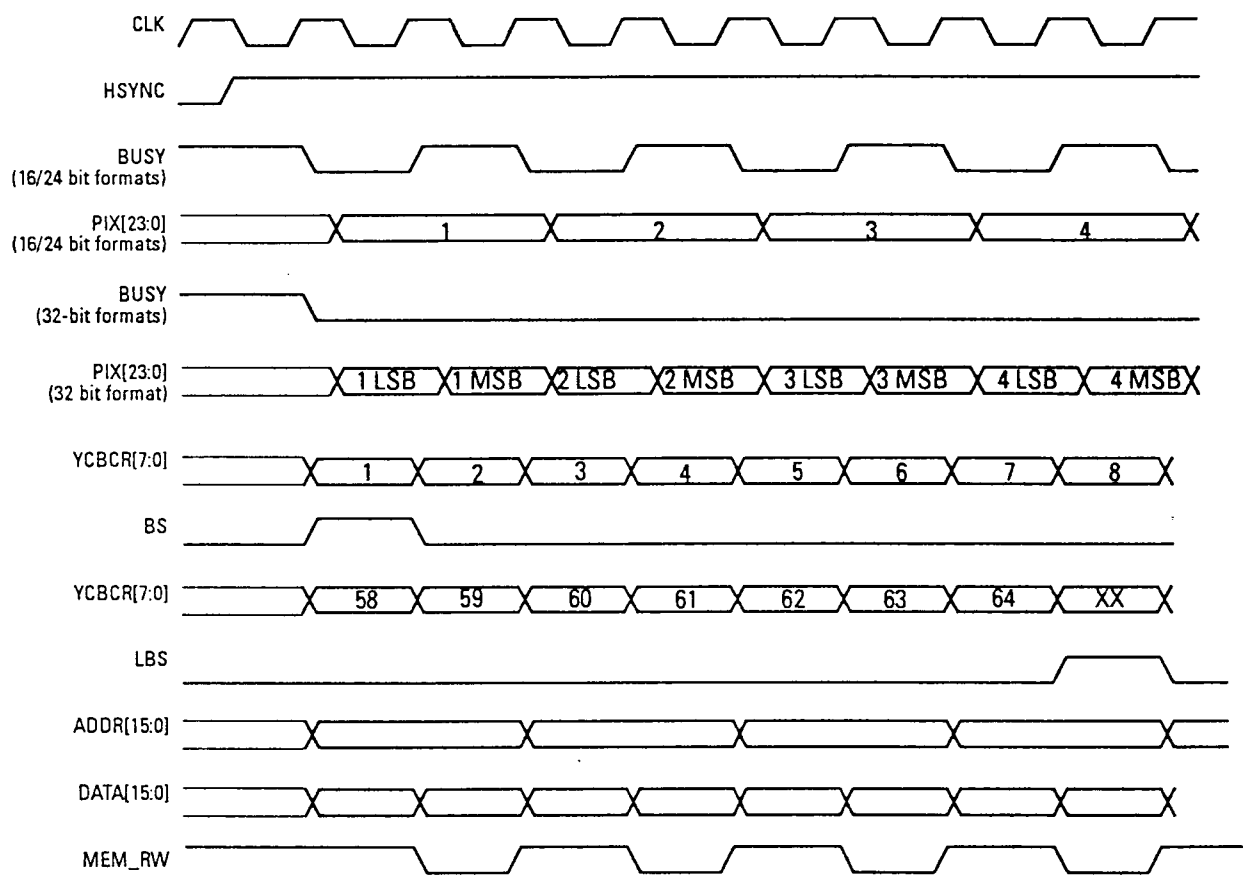

Figure 13. Functional Waveforms

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AC Timing

This section presents the AC timing information for the L64765, including:

- Table 4, AC Timing Values
- Figure 16, Write Timing Waveforms
- Figure 14, Read Timing Waveforms
- Figure 15, AC Timing Waveforms

All parameters in Table 4 are measured for T_A = 0 to 70 C, V_{DD} = 4.75 to 5.25 volts.

Table 4. AC Timing Values

Symbol	Parameter	27 MHz				Units
		Min	Max			
t_{cycle}	CLK cycle time	37				ns
t_{setup}	Input signal setup	10				ns
t_{hold}	Input signal hold	6				ns
t_{bsod}	BS, LBS output delay[1]		24			ns
t_{od}	Output delay[1,3]		22			ns
t_{mdsu}	Memory data setup	0				ns
t_{mdod}	Memory data output delay[1]		20			ns
t_{maod}	Memory address output delay[2]		11			ns
t_{mwhl}	MEM_RW High-to-Low delay[2]		9			ns
t_{mwlh}	MEM_RW Low-to-High delay[2]		8			ns
t_{frqod}	FRQ output delay[2]		12			ns
t_{rsu}	R[1:0] setup	11				ns
t_{rhld}	R[1:0] hold	11				ns
t_{cdsu}	Control data (PIX[23:16]) setup	11				ns
t_{cdhld}	Control data (PIX[23:16]) hold	5				ns
t_{cdod}	Control data (PIX[23:16]) output delay[1]		19			ns
t_{oez}	Output tri-state delay from $\overline{OE}$ active		18			ns

Notes:
1. Output loading = 85 pF.
2. Output loading = 50 pF.
3. t_{od} applies to output signals YCBCR[7:0], HSYNC, VSYNC, BUSY, and PIX[23:0] except when PIX[23:16] are used for control read and write operations.

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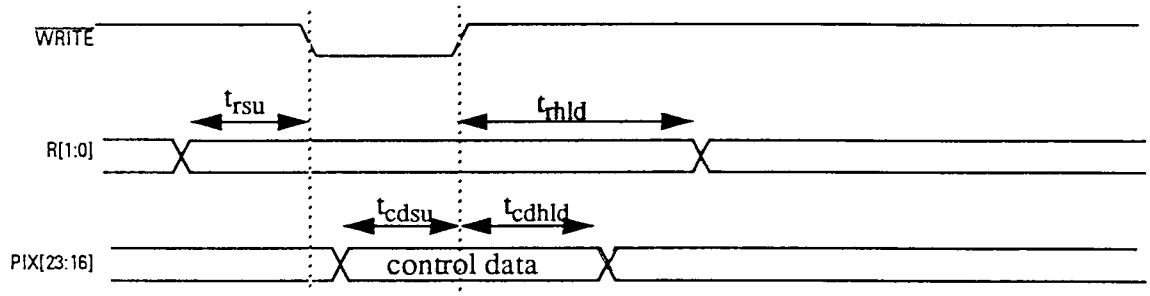

Figure 14. Write Timing Waveforms

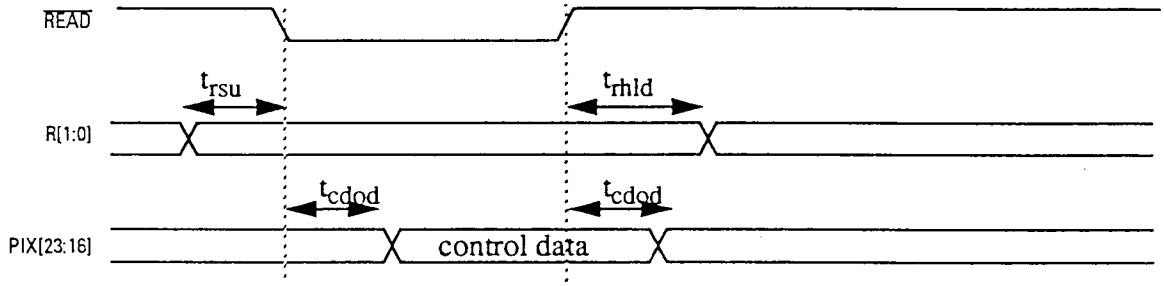

Figure 15. Read Timing Waveforms

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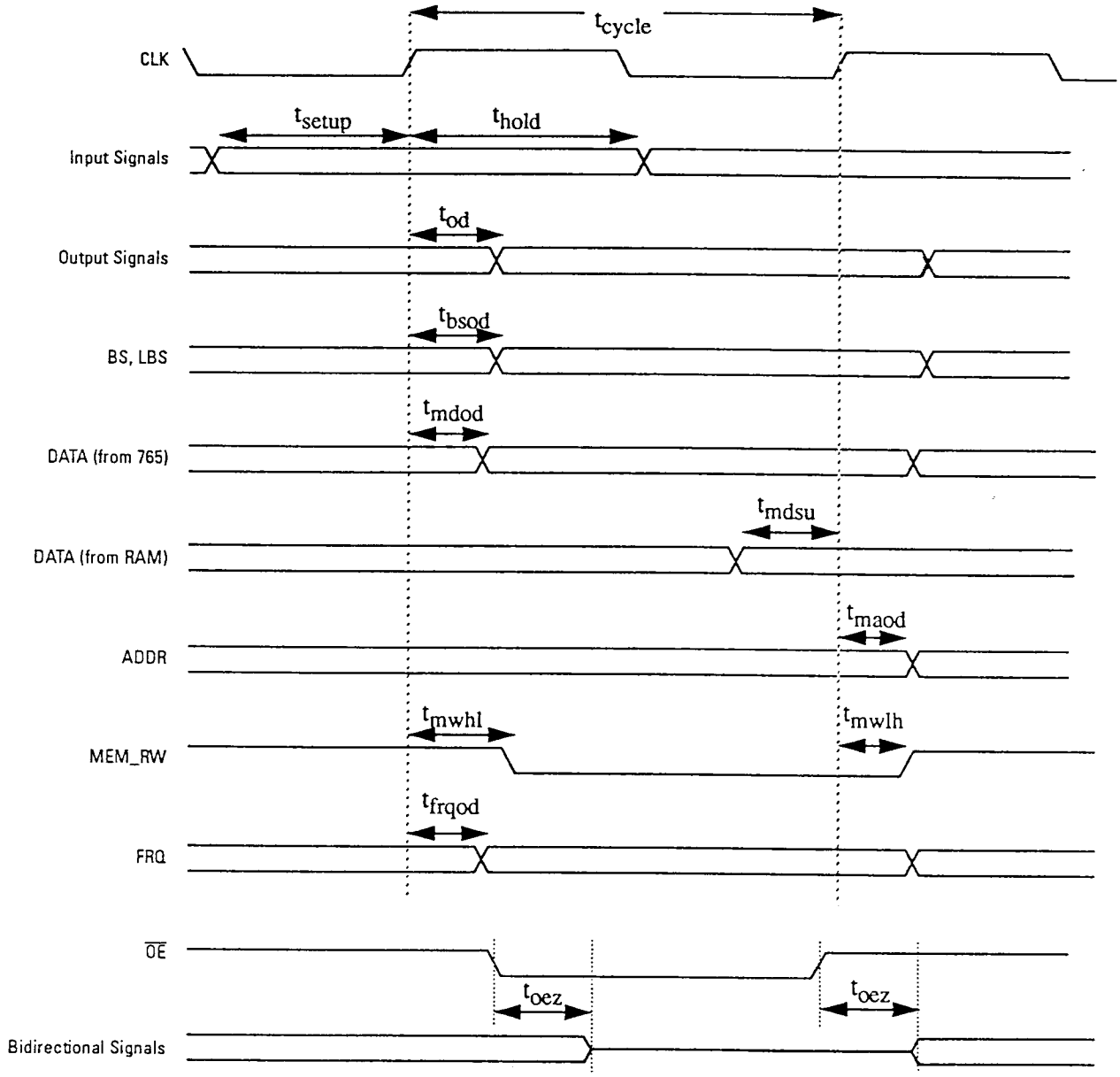

Figure 16. AC Timing Waveforms

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Electrical Characteristics

This section presents the electrical characteristics of the L64745:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- DC Characteristics

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature	TSTG	-65 to +150	°C

Table 6. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	+3 to +6	V
Operating ambient Temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

Table 7. DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
VIL	LOW input voltage				0.8	V
VIH	HIGH input voltage					
	Commercial[2]		2.0			V
	Military[2]		2.25			V
IIN	Input current	VIN = VDD	-100	-30	-8	µA
VOL	LOW output voltage					
	Commercial	IOL = -4 mA		0.2	0.4	V
	Military	IOL = -3.2 mA		0.2	0.4	V
VOH	HIGH output voltage					
	Commercial	IOH = -4 mA	2.4	2.5		V
	Military	IOH = -3.2 mA	2.4	2.5		V
IOS	Output short-circuit current[3]	VDD = Max, VO = VDD	15		130	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current			200		mA
CIN	Input capacitance	Any input		5		pF
COUT	Output capacitance	Any output		10		pF

Notes:
1. All DC characteristics are specified for VDD = 5 V over the specified temperature and voltage ranges.
2. See "Recommended Operating Conditions" for commercial and military temperature ranges.
3. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

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Packaging

The L64745 is supplied in a 100-pin ceramic pin-grid array (CPGA). This section provides the following following information:

- Pin number to signal name correspondance
- Signal name to pin number correspondance
- Pin diagram for 100-pin CPGA package
- Mechanical dimensions

Table 8. Signal Name to Pin Number Correspondance

Signal Name	*Pin No.*	*Signal Name*	*Pin No.*	*Signal Name*	*Pin No.*	*Pin No.*	*Signal Name*
ADDR.0	J1	DATA.7	M4	PIX.12	B9	VDD	N13
ADDR.1	H3	DATA.8	N3	PIX.13	A9	VSS	C1
ADDR.2	H2	DATA.9	M3	PIX.14	C8	VSS	C7
ADDR.3	H1	DATA.10	N2	PIX.15	B8	VSS	C12
ADDR.4	G2	DATA.11	M1	PIX.16	A8	VSS	G3
ADDR.5	F1	DATA.12	L1	PIX.17	A7	VSS	G11
ADDR.6	F2	DATA.13	K2	PIX.18	A6	VSS	L2
ADDR.7	F3	DATA.14	K1	PIX.19	B6	VSS	L7
ADDR.8	E1	DATA.15	J2	PIX.20	C6	VSS	M11
ADDR.9	E2	FRQ	H12	PIX.21	A5	VSYNC	F12
ADDR.10	D1	HSYNC	G13	PIX.22	B5	$\overline{\text{WRITE}}$	H11
ADDR.11	D2	LBS	M8	PIX.23	A4	YCBCR.0	L13
ADDR.12	C2	MEM_RW	B4	R.0	J12	YCBCR.1	L12
ADDR.13	B3	$\overline{\text{OE}}$	K12	R.1	K13	YCBCR.2	N12
ADDR.14	A2	PIX.0	F11	$\overline{\text{READ}}$	J13	YCBCR.3	N11
ADDR.15	A3	PIX.1	E13	VDD	A1	YCBCR.4	M10
BS	N8	PIX.2	E12	VDD	A13	YCBCR.5	N10
BUSY	F13	PIX.3	D13	VDD	B2	YCBCR.6	M9
CLK	H13	PIX.4	D12	VDD	B7	YCBCR.7	N9
DATA.0	M7	PIX.5	C13	VDD	B12	*Reserved*[1]	B1
DATA.1	N6	PIX.6	B13	VDD	G1	*Reserved*[1]	C3
DATA.2	M6	PIX.7	A12	VDD	G12	*Reserved*[1]	L8
DATA.3	L6	PIX.8	B11	VDD	M2	*Reserved*[1]	M12
DATA.4	N5	PIX.9	A11	VDD	M13		
DATA.5	M5	PIX.10	B10	VDD	N1		
DATA.6	N4	PIX.11	A10	VDD	N7		

Notes:

1.Reserved pins must be left unconnected for normal operation.

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Table 9 . Pin Number to Signal Name Correspondance

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	VDD	C1	VSS	G12	VDD	M4	DATA.7
A2	ADDR.14	C2	ADDR.12	G13	HSYNC	M5	DATA.5
A3	ADDR.15	C3	*Reserved*[1]	H1	ADDR.3	M6	DATA.2
A4	PIX.23	C6	PIX.20	H2	ADDR.2	M7	DATA.0
A5	PIX.21	C7	VSS	H3	ADDR.1	M8	LBS
A6	PIX.18	C8	PIX.14	H11	$\overline{\text{WRITE}}$	M9	YCBCR.6
A7	PIX.17	C12	VSS	H12	FRQ	M10	YCBCR.4
A8	PIX.16	C13	PIX.5	H13	CLK	M11	VSS
A9	PIX.13	D1	ADDR.10	J1	ADDR.0	M12	*Reserved*[1]
A10	PIX.11	D2	ADDR.11	J2	DATA.15	M13	VDD
A11	PIX.9	D12	PIX.4	J12	R.0	N1	VDD
A12	PIX.7	D13	PIX.3	J13	$\overline{\text{READ}}$	N2	DATA.10
A13	VDD	E1	ADDR.8	K1	DATA.14	N3	DATA.8
B1	*Reserved*[1]	E2	ADDR.9	K2	DATA.13	N4	DATA.6
B2	VDD	E12	PIX.2	K12	$\overline{\text{OE}}$	N5	DATA.4
B3	ADDR.13	E13	PIX.1	K13	R.1	N6	DATA.1
B4	MEM_RW	F1	ADDR.5	L1	DATA.12	N7	VDD
B5	PIX.22	F2	ADDR.6	L2	VSS	N8	BS
B6	PIX.19	F3	ADDR.7	L6	DATA.3	N9	YCBCR.7
B7	VDD	F11	PIX.0	L7	VSS	N10	YCBCR.5
B8	PIX.15	F12	VSYNC	L8	*Reserved*[1]	N11	YCBCR.3
B9	PIX.12	F13	BUSY	L12	YCBCR.1	N12	YCBCR.2
B10	PIX.10	G1	VDD	L13	YCBCR.0	N13	VDD
B11	PIX.8	G2	ADDR.4	M1	DATA.11		
B12	VDD	G3	VSS	M2	VDD		
B13	PIX.6	G11	VSS	M3	DATA.9		

Notes:

1.Reserved pins must be left unconnected for normal operation.

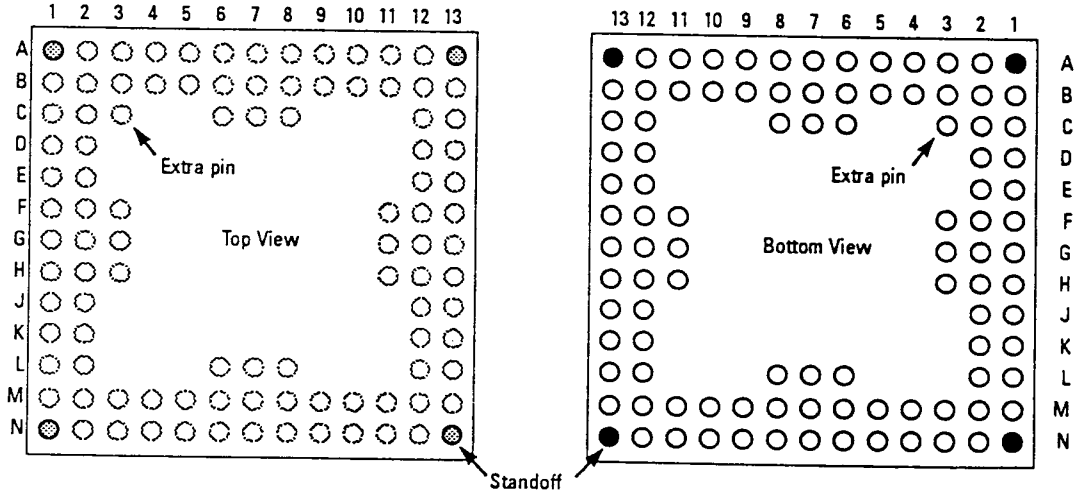

Figure 17. 100-Pin CPGA Pin Layout

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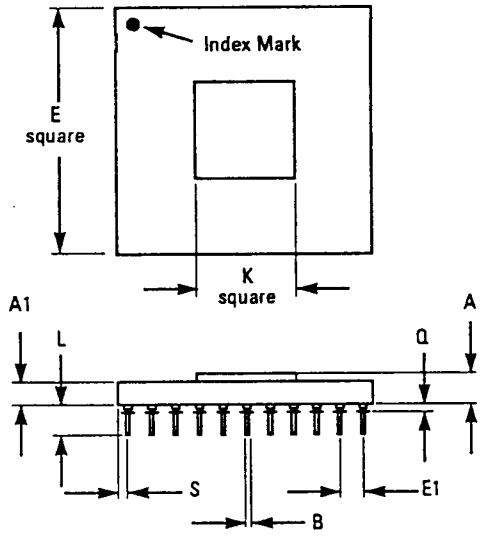

Dimension		100-pin CPGA
A	Max	0.117 (2.972)
A1	Ref	0.080 (2.032)
B	Min	0.016 (0.406)
	Max	0.020 (0.508)
E	Min	1.308 (33.22)
	Max	1.332 (33.83)
E1	Min	0.095 (2.413)
	Max	0.105 (2.667)
L	Min	0.170 (4.318)
	Max	0.190 (4.826)
Q	Ref	0.050 (1.270)
S	Ref	0.060 (1.524)
K	Ref	0.673 (17.09)

Figure 18. 100-Pin CPGA Mechanical Dimensions

Ordering Information

To order products or for more information, contact any LSI Logic sales office shown on the back cover.

L64765 Ordering

Figure 19 shows an example of a valid part number for ordering the L64765 and the codes for other options. The part number shown, L64765G M-27, designates an L64765 in a 100-pin ceramic pin-grid array (CPGA) rated for the military temperature range and a maximum clock speed of 27MHz.

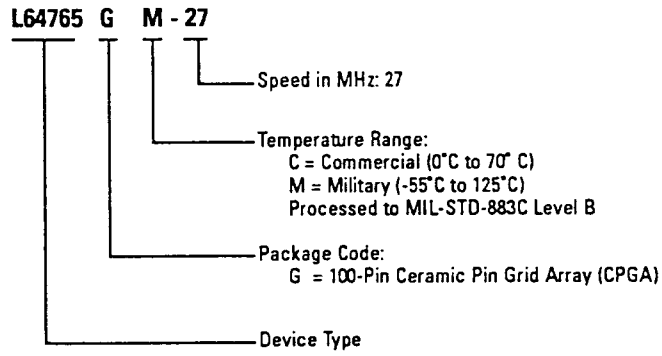

Figure 19. L64765 Part Number Designation

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