PHK31NQ03LT

N-channel TrenchMOS logic level FET

Rev. 02 — 20 December 2010 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

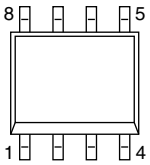
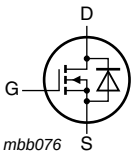
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	30	V
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	-	-	30.4	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2	-	-	6.9	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 5	-	3.45	4.4	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5$ V; $I_D = 25$ A; $V_{DS} = 12$ V; see Figure 6	-	7.7	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain	SOT96-1 (SO8)	
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

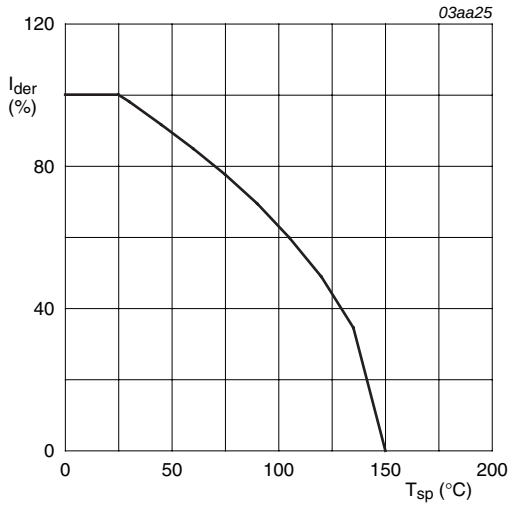
Type number	Package		
	Name	Description	Version
PHK31NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

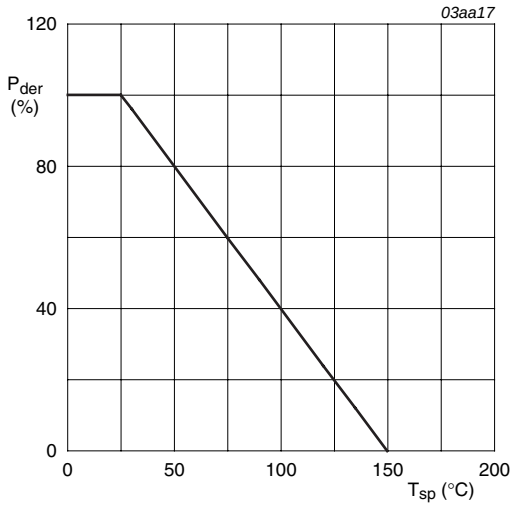
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20$ kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 100$ °C; $V_{GS} = 10$ V; see Figure 1	-	17.2	A
		$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	-	30.4	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs	-	121.8	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2	-	6.9	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25$ °C	-	5.7	A
I_{SM}	peak source current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs	-	23.1	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 35$ A; $V_{sup} \leq 25$ V; unclamped; $t_p = 0.16$ ms; $R_{GS} = 50$ Ω	-	120	mJ



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point		-	-	18	K/W

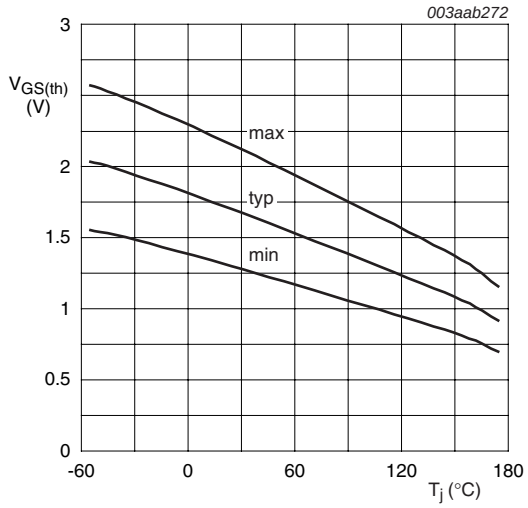
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 3; see Figure 4	0.8	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 3; see Figure 4	-	-	2.6	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 3; see Figure 4	1.3	1.7	2.15	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; see Figure 5	-	5.85	7.5	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 5	-	4.25	5.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 5	-	3.45	4.4	mΩ
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
R_G	gate resistance	f = 1 MHz	-	1.2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 6	-	33	-	nC
Q_{GS}	gate-source charge		-	13.6	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	6.5	-	nC
Q_{GS2}	post-threshold gate-source charge		-	7.1	-	nC
Q_{GD}	gate-drain charge		-	7.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 12 V; see Figure 6	-	2.85	-	V
C_{iss}	input capacitance	V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	4900	-	pF
		V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	4235	-	pF
C_{oss}	output capacitance		-	840	-	pF
C_{rss}	reverse transfer capacitance		-	370	-	pF

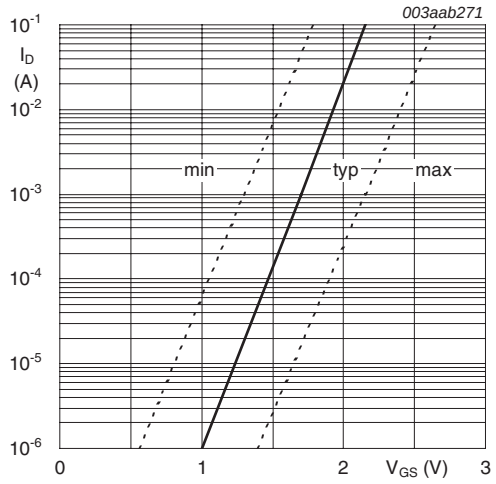
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5.6 Ω	-	37	-	ns
t_r	rise time		-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	54	-	ns
t_f	fall time		-	26	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C	-	0.94	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	52	-	ns
Q_r	recovered charge	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V	-	30	-	nC



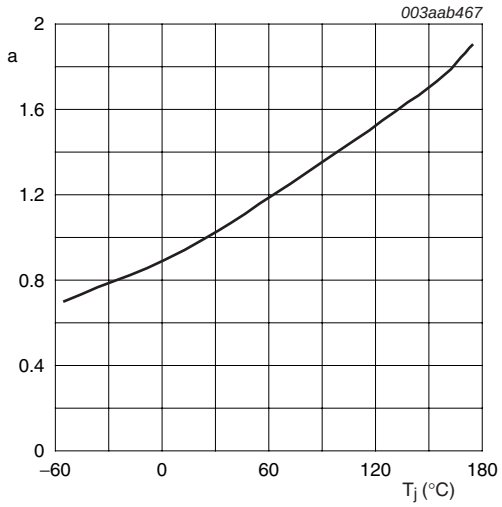
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 3. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\,°C; V_{DS} = 5V$

Fig 4. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 5. Normalized drain-source on-state resistance factor as a function of junction temperature

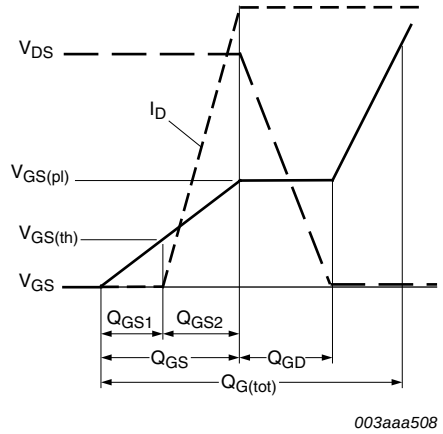
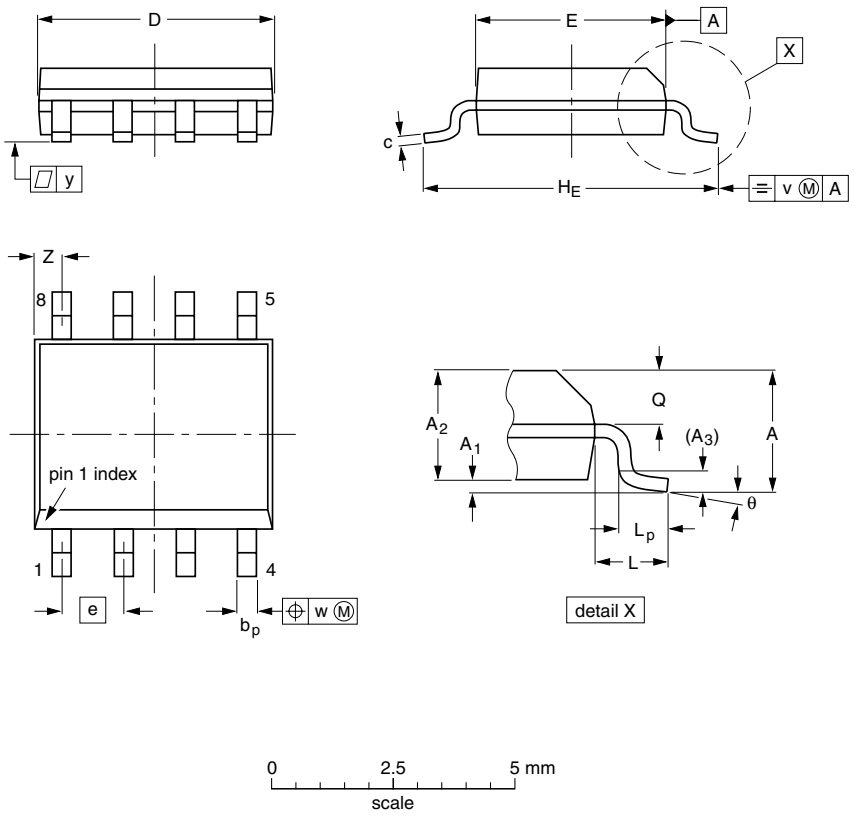


Fig 6. Gate charge waveform definitions

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK31NQ03LT v.2	20101220	Product data sheet	-	PHK31NQ03LT v.1
Modifications:	• Various changes to content.			
PHK31NQ03LT v.1	20061218	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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