

NTGS1135P

Power MOSFET

-8 V, -5.8 A, Single P-Channel, TSOP-6

Features

- Ultra Low $R_{DS(on)}$
- 1.2 V $R_{DS(on)}$ Rating
- This is a Pb-Free Device

Applications

- Load Switch
- Battery Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DS}	-8.0	V	
Gate-to-Source Voltage	V_{GS}	± 6.0	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-4.6	A
		$T_A = 85^\circ\text{C}$	-3.3	
		$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	0.97	W
			$t \leq 5 \text{ s}$	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-9.2	A
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$
Source Current (Body Diode)	I_S	-1.0		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size. (Cu area = 0.0751 in sq)

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	128	$^\circ\text{C/W}$
Junction-to-Ambient - $t = 5 \text{ s}$ (Note 1)	$R_{\theta JA}$	78	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	188	

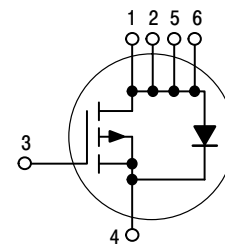


ON Semiconductor®

<http://onsemi.com>

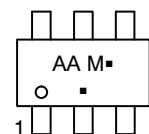
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-8 V	31 m Ω @ -4.5 V	-4.6 A
	38 m Ω @ -2.5 V	
	57 m Ω @ -1.8 V	
	300 m Ω @ -1.2 V	

P-Channel



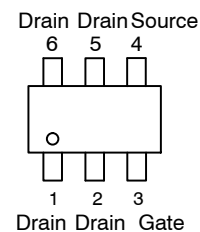
1
TSOP-6
CASE 318G
STYLE 1

MARKING DIAGRAM



AA = Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS1135PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTGS1135P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-8.0			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$, Ref to 25°C		-8.4		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -6\text{ V}$			-1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 6\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.35	-0.57	-0.85	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.8		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.6\text{ A}$		22	31	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$		28	38	
		$V_{GS} = -1.8\text{ V}, I_D = -2.0\text{ A}$		37	57	
		$V_{GS} = -1.5\text{ V}, I_D = -1.0\text{ A}$		47	73	
		$V_{GS} = -1.2\text{ V}, I_D = -0.1\text{ A}$		100	300	
Forward Transconductance	g_{FS}	$V_{DS} = -4.0\text{ V}, I_D = -3.0\text{ A}$		1.2		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -6.0\text{ V}$		2200		pF
Output Capacitance	C_{OSS}			400		
Reverse Transfer Capacitance	C_{RSS}			200		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -8.0\text{ V};$ $I_D = -2.5\text{ A}$		21		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.9		
Gate-to-Source Charge	Q_{GS}			2.8		
Gate-to-Drain Charge	Q_{GD}			3.9		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -8.0\text{ V},$ $I_D = -2.5\text{ A}, R_G = 6.2\ \Omega$		10		ns
Rise Time	t_r			16		
Turn-Off Delay Time	$t_{d(OFF)}$			128		
Fall Time	t_f			71		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$		-0.6	-1.0	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = -1.0\text{ A}$			25		ns
Charge Time	t_a				11		
Discharge Time	t_b				14		
Reverse Recovery Charge	Q_{RR}				13		nC

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
- Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

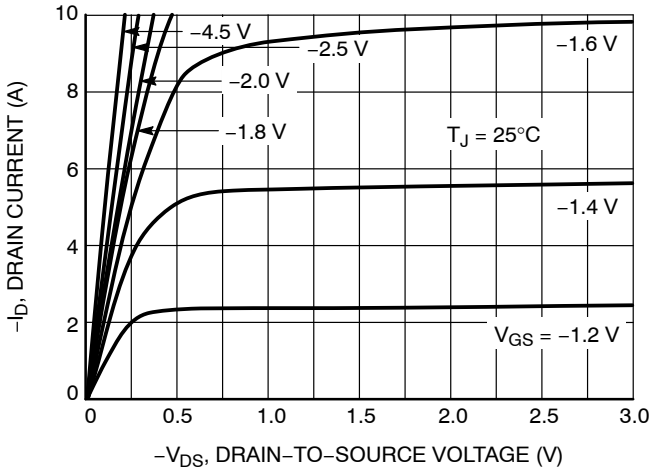


Figure 1. On-Region Characteristics

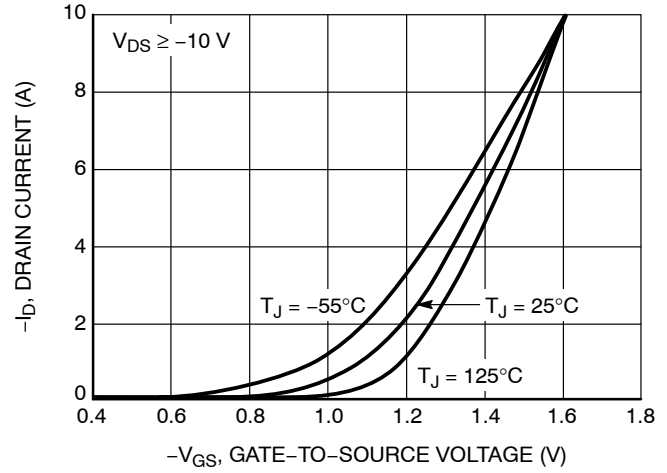


Figure 2. Transfer Characteristics

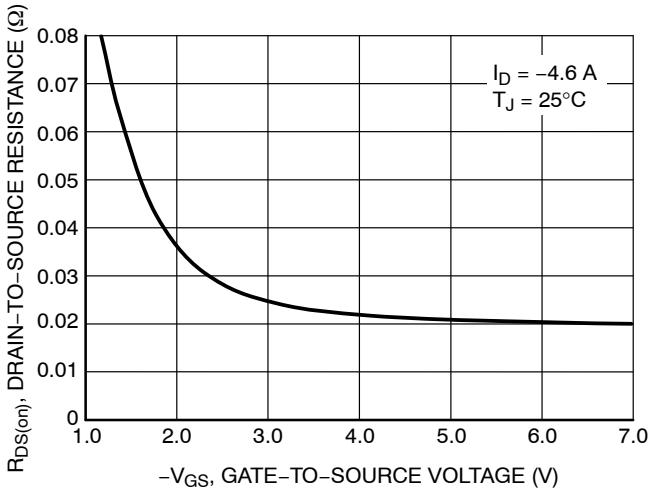


Figure 3. On-Resistance vs. Gate Voltage

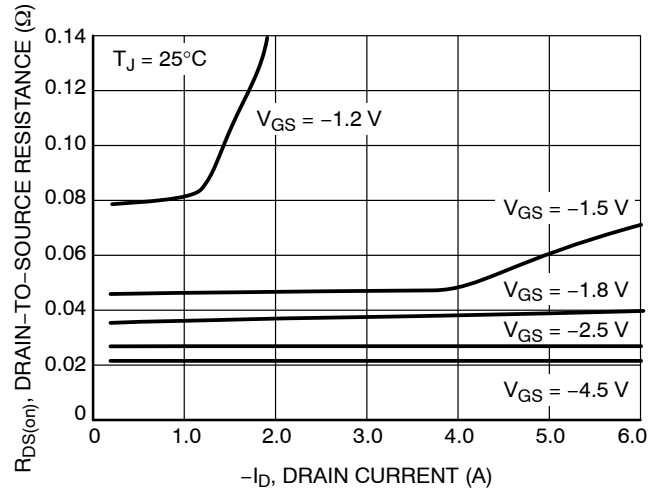


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

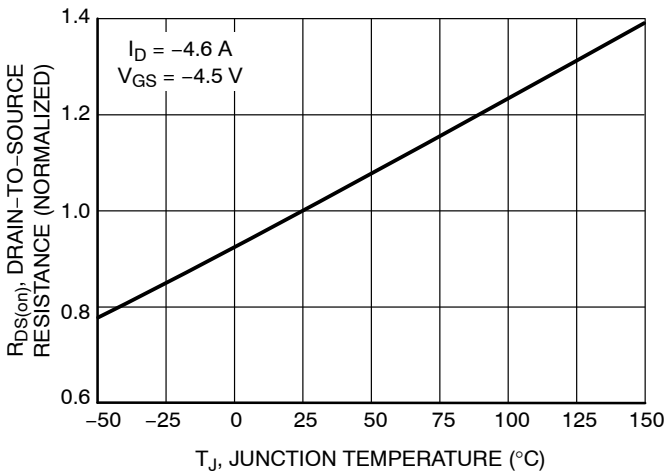


Figure 5. On-Resistance Variation with Temperature

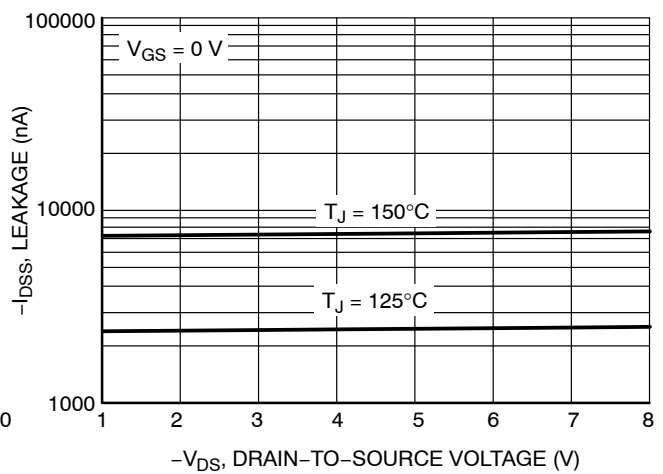


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

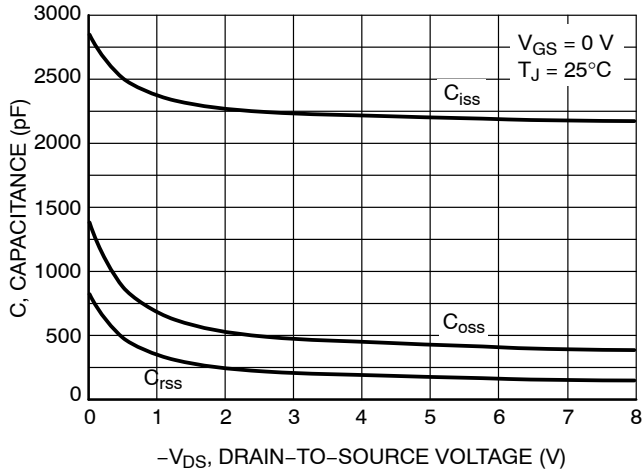


Figure 7. Capacitance Variation

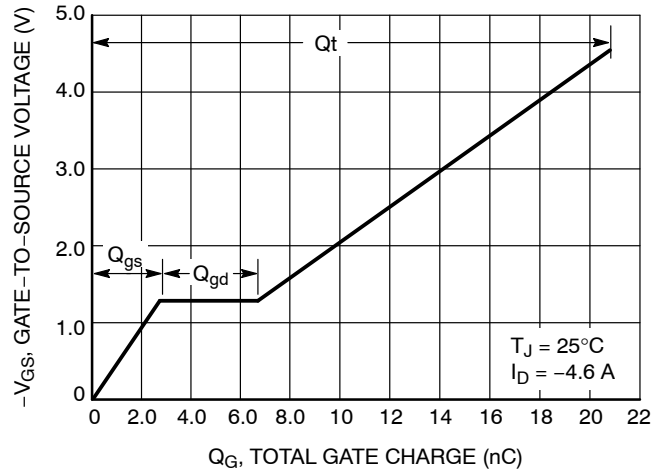


Figure 8. Gate-to-Source Voltage vs. Total Charge

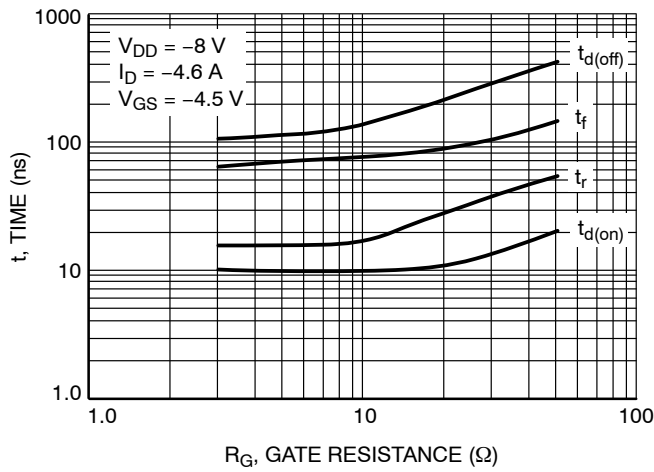


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

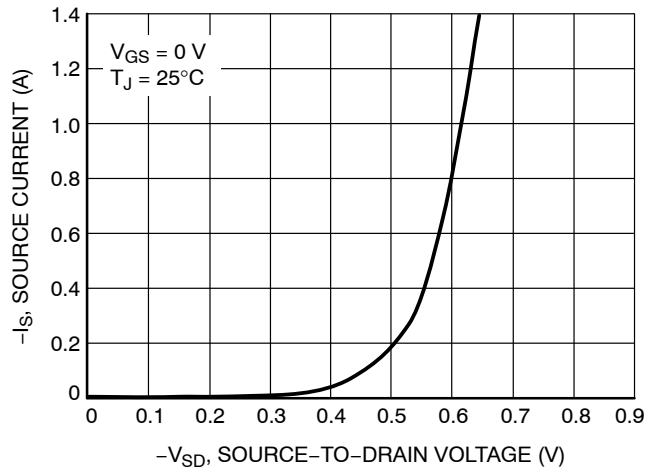
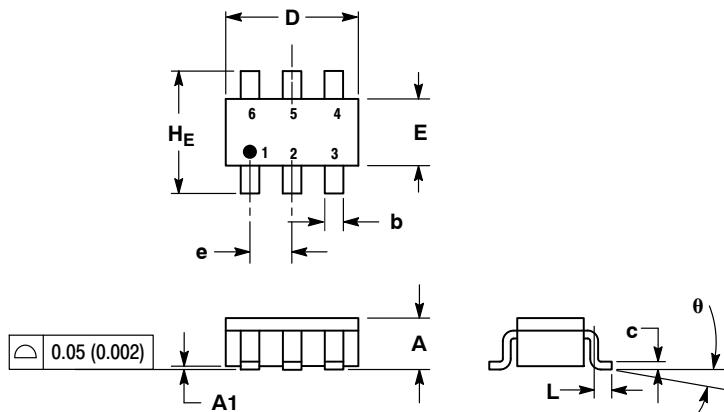


Figure 10. Diode Forward Voltage vs. Current

NTGS1135P

PACKAGE DIMENSIONS

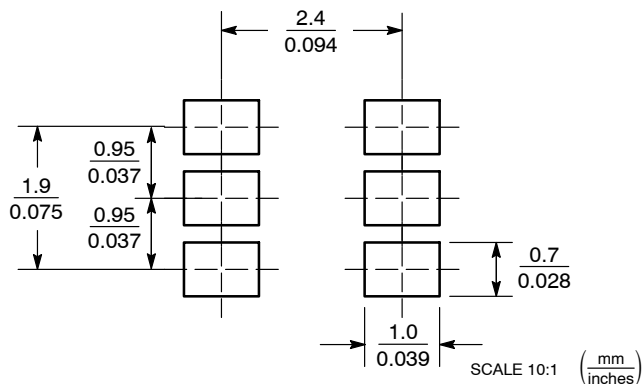
TSOP-6 CASE 318G-02 ISSUE S



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative