Fiber optic receiver applications note AN4003

I. A NEW FIBER OPTIC RECEIVER CHIP SET FOR 100Mb/s FDDI DATA LINKS

- SA5222 Transimpedance Amplifier.
- NE/SA5224 and NE/SA5225 Post Amplifiers

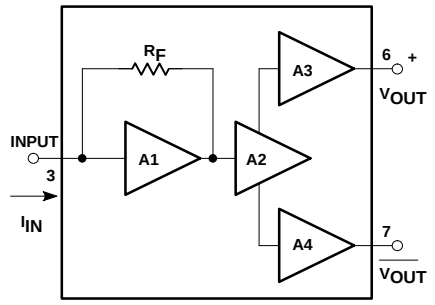


Figure 1. SA5222 Low Power Transimpedance Amplifier

The 140MHz Transimpedance Amplifier (Figure 1)

Designed specifically to meet the requirements of the ANSI Fiber Distributed Data Interface (FDDI) 100Mb/s LAN systems, the SA5222 is a new addition to Philips Semiconductors family of fiber optic devices. Table 1 shows a comparison of the features of this device in relation to the existing transimpedance amplifiers.

Particular attention has been paid to improving the power supply rejection ratio (PSRR). This reduces the chance of oscillation due to coupling onto the supply line. The PSRR specification, as noted in Table 1, is 57dB. In addition the supply current is reduced to 9mA, a particular advantage in remote, high density applications.

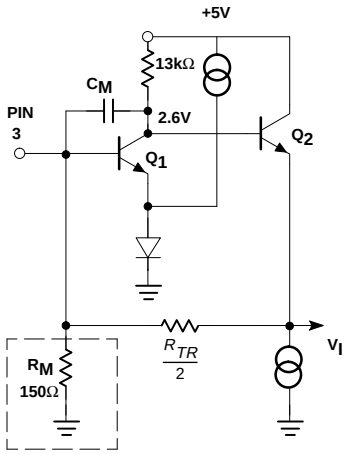


Figure 2. SA5222 Input Stage (Simplified)

Table 1.

	Differential Transresistance	Bandwidth	i_n	Input Max μA	I_{CC}	PSRR
SA5222	16.6kΩ	140MHz	1.8pA/√Hz	±115μA	9mA	57dB
NE5212	14kΩ	140MHz	2.5pA/√Hz	±120μA	26mA	33dB
NE5211	28kΩ	180MHz	1.8pA/√Hz	±60μA	24mA	32dB
NE5210	7kΩ	280MHz	3.5pA/√Hz	±240μA	26mA	36dB

Theory of Operation – SA5222

The SA5222 is an all-bipolar amplifier with a -3dB bandwidth of 140MHz. The device operates in the inverting mode with the first stage loop closed by a shunt feedback resistance (see Figure 2). The advantage in this topology is its inherent insensitivity to shunt capacitance at the input. The node at Pin 3 of the amplifier acts to sum the input current from the photo or PIN diode with the negative feedback from the shunt resistance. The input node is dominated by the Miller feedback capacitance from the collector-base junction of Q1 (C_M). This capacitance in conjunction with the Miller resistance ($R_M = R_{IN}$), acts to set the upper frequency bandwidth of the amplifier.

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}}$$

The first stage Miller capacitance is approximately 7pF and the Miller resistance is equal to the rated input resistance of 150Ω.

The upper 3dB bandwidth is then

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot 150 \cdot 7 \cdot 10^{-12}\ F} = 150MHz$$

which agrees with the device specifications.
The virtual capacitance now dominates the frequency response of the amplifier desensitizing it to small values of input shunt capacitance.

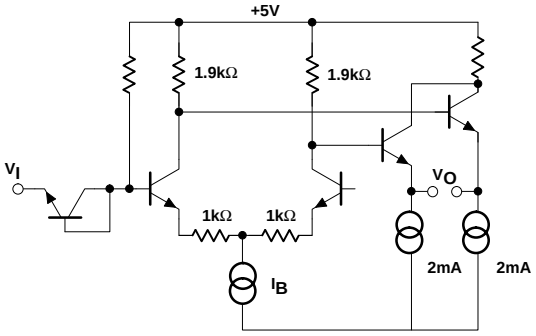


Figure 3. SA5222 Differential Output Stage (Simplified)

The major advantage of this configuration over a cascade amplifier with FET input is that the input frequency response limit is stabilized and the noise gain is not drastically affected by the external circuit capacitances.

For example, with the rated 1pF package capacitance plus 1pF of external capacitance combined with 150Ω, the input bandwidth is approximately 120MHz. This demonstrates the amplifier's intolerance to shunt capacitance. Adding external shunt

capacitance *will lower* the input stage bandwidth. This will also *increase* the noise gain, however. The shunt capacitance acts inversely with increasing frequency to increase the gain of the amplifier to internal noise currents.

The input stage is followed by a differential buffer driver which provides the necessary interface and level shifting for the output emitter followers (see Figure 3). The second stage converts the single-ended input signal to a differential signal raised to a common mode voltage of 3.2V. The amplifier has a source/sink output capability of 2mA. The second stage provides a gain of slightly over two. NPN current sources are bandgap referenced to provide highly stable biasing in the amplifier giving it an advantage in power supply rejection and linearity.

The SA5222 differential output resistance is typically 60Ω and is, therefore, capable of driving low impedance circuitry. However, the output voltage of the SA5222 is 3.2V which limits the external DC load resistance to ground to a value which does not draw more than the rated 2mA of sink current. It is typically necessary to include capacitive coupling between the SA5222 and the post amplifier in order to allow the threshold comparators to automatically detect the bit amplitude and provide proper level conversion independent of preamp DC offset.

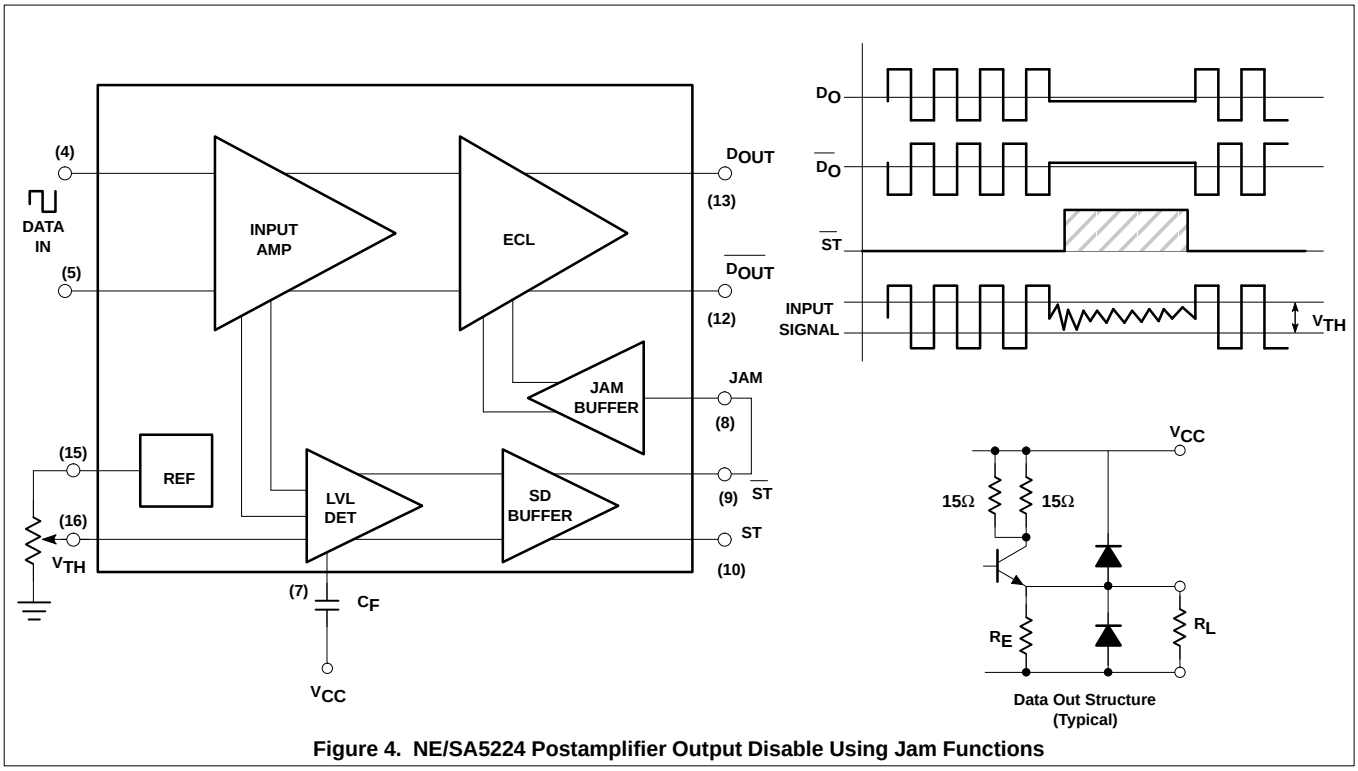


Figure 4. NE/SA5224 Postamplifier Output Disable Using Jam Functions

Input Sensitivity and Signal-to- Noise Ratio

Example of Optical Conversion gain.

Consider a 10µW optical signal incident upon a 0.45A/Watt responsivity PIN diode. This corresponds to –20dB optical relative to 1mW (-20dBmo*). The current generated at the input node of the SA5222 is 4.5µA. The resultant differential output voltage is

$$4.5\ A \cdot 16.6k \quad = 75mV_{P-P}$$

between Pins 6 and 7.

The dynamic signal-to-noise ratio at this level is calculated below using the rated 1.8pA/√Hz over a 150MHz bandwidth

$$20 \log \frac{(75 \cdot 10^{-3})\ V_{P-P}}{(1.8 \cdot 10^{-12})\ \overline{150 \cdot 10^{6} \cdot 16.6K}} = 47dB$$

Whereas, a 1µW (–30dBmo) input into a typical 0.3A/Watt responsivity photo diode or PIN will result in a theoretical signal-to-noise ratio of

$$20 \log \frac{5 \cdot 10^{-3}\ V_{P-P}}{(22 \cdot 10^{-9} A_{RMS})\ 16.6k\ \ V_{RMS}} = 23dB$$

This does not include the optical noise of the fiber or the receiver diode. In this case the SA5222 output voltage due to the 1µW optical input signal is $5mV_{P-P}$. (NOTE: A 12:1 ratio or 21.6dB corresponds to a BER of 10^{-9}.)

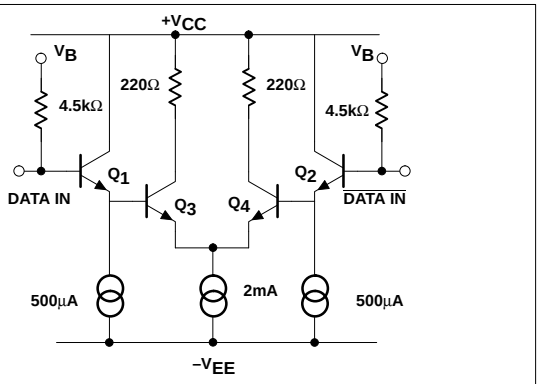
*NOTE: dBmo = dBm optical relative to 1mW.

Postamplifier Selection (NE/SA5224 and 5225)

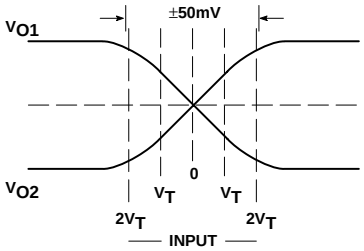
In selecting the correct signal interface to meet user data communications system specifications, two different devices are available to the designer. For the Fiber Data Distributed Interface (FDDI), the NE/SA5224 is recommended. This device provides 100k ECL compatibility for the differential data output, Status output and Jam input.

For industrial fiber communications applications, the NE/SA5225 is recommended. It provides 10k ECL compatibility. With the

exception of different hysteresis specifications, the two devices are fully pin-for-pin compatible.



a. NE/SA5224, 5225 Simplified Input Stage Data



b. NE/SA5224 Input Stage Transfer Functions

Figure 5.

Theory of Operation*

Referring to the Operational Block Diagram in Figure 4, the device consists of a main signal path that is fully differential from input to output. The input amplifier consists of a differential pair limited to an I_{CC} of 2mA (see Figure 5a). The amplifier is a limiting type with gain reduction above 2 V_t, or about 100mV_{P-P}. The input common mode voltage is approximately 2.9V with a V_{CC} of 5V. The input resistance of the device is typically 4.5kΩ. This, then, allows the calculation of the minimum coupling capacitor for the lowest data frequency component. (See Figure 5b.)

The NE/SA5224 Postamplifier

The NE/SA5224 is designed to operate within the FDDI specification data rate of 125Mb/s using the 4B/5B format. At 100Mb/s this requires the data clock to operate at 62.5MHz and presumes the use of an NRZ format. The NE/SA5224 is rated to operate over a frequency range of 1kHz to 120MHz, but will operate higher in frequency with some loss of sensitivity.

The first stage input capacitance is on the order of 1.5pF including the ESD diode junction capacitance plus the input device and package contributions.

Following the first stage are the intermediate gain stages from which a sample of the amplified signal is fed to the level detector.

(*Unless stated, also applies to NE/SA5225.)

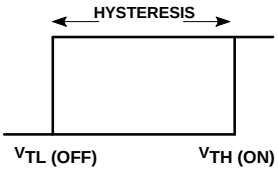


Figure 6.

Level Detector

This section provides the programmable threshold function of the device. Adjustment of the voltage on Pin 16 determines the point at which the input signal decision level occurs. The threshold levels are rated for the single-ended voltage trip level of 2 to 12mV_{P-P} which corresponds to twice this value or 4 to 24mV_{P-P} differentially (see Table 2).

Threshold sensing may be combined with the output signal function through use of the data out Jam functions). This allows you to force the output to a fixed state when the input falls below the predetermined level as programmed on Pin 16. This function is provided by connecting Pins 8 and 9 together.

Table 2.

V_{SET}	V_{TL}	V_{TH}	$V_{P-P(avg)}$	R_1	R_2
0.5V	3.6mV	6.4mV	5.0mV	4050Ω	950Ω
1.0V	7.2mV	12.8mV	10.0mV	3110Ω	1890Ω
1.5V	10.8mV	19.2mV	15.0mV	2160Ω	2840Ω
2.0V	14.4mV	26.0mV	20.0mV	1210Ω	37900Ω

The signal level detector controls the status detector, which has complimentary outputs at Pins 9 and 10. Pin 9 is forced to a high state whenever the input to the NE/SA5224 falls below the user determined voltage threshold as set on Pin 16 (V_{SET}) (see Figure 4). In the Jam state, the ECL data outputs are forced into predetermined states, D_{OUT} = low and $\overline{D_{OUT}}$ = high. The complimentary ST output at Pin 10 may be used as a system status enable providing an ECL high when the input signal level is above the threshold level.

The status circuit operates on the basis of a full wave rectifier averaging detector with a nominal response time of 1μs. Additional filtering may be added at Pin 7, (C_F pin) which has characteristic internal resistance of 24kΩ. This allows the user to select the time constant of the low-pass filter to meet a specific application by adding external capacitance at this pin. Note that the capacitor is returned to the plus V_{CC} line.

The hysteresis characteristic of the NE/SA5224 is fixed internally between 4 and 6dB. The plot in Figure 6 shows how this relates to the threshold levels discussed above. The typical value in dB is determined by taking 20 times the log of the ratio of V_{TH} (on) to V_{TL} (off) and for the NE/SA5224 this equals 5dB. The NE/SA5225, however, has a typical hysteresis value of 3dB with a tested range of 2 to 4dB.

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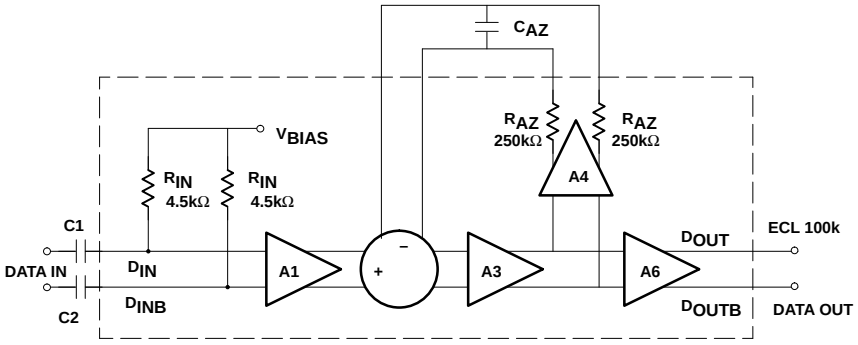

Figure 7. NE/SA5224 Forward Gain Path Including Auto-Zero

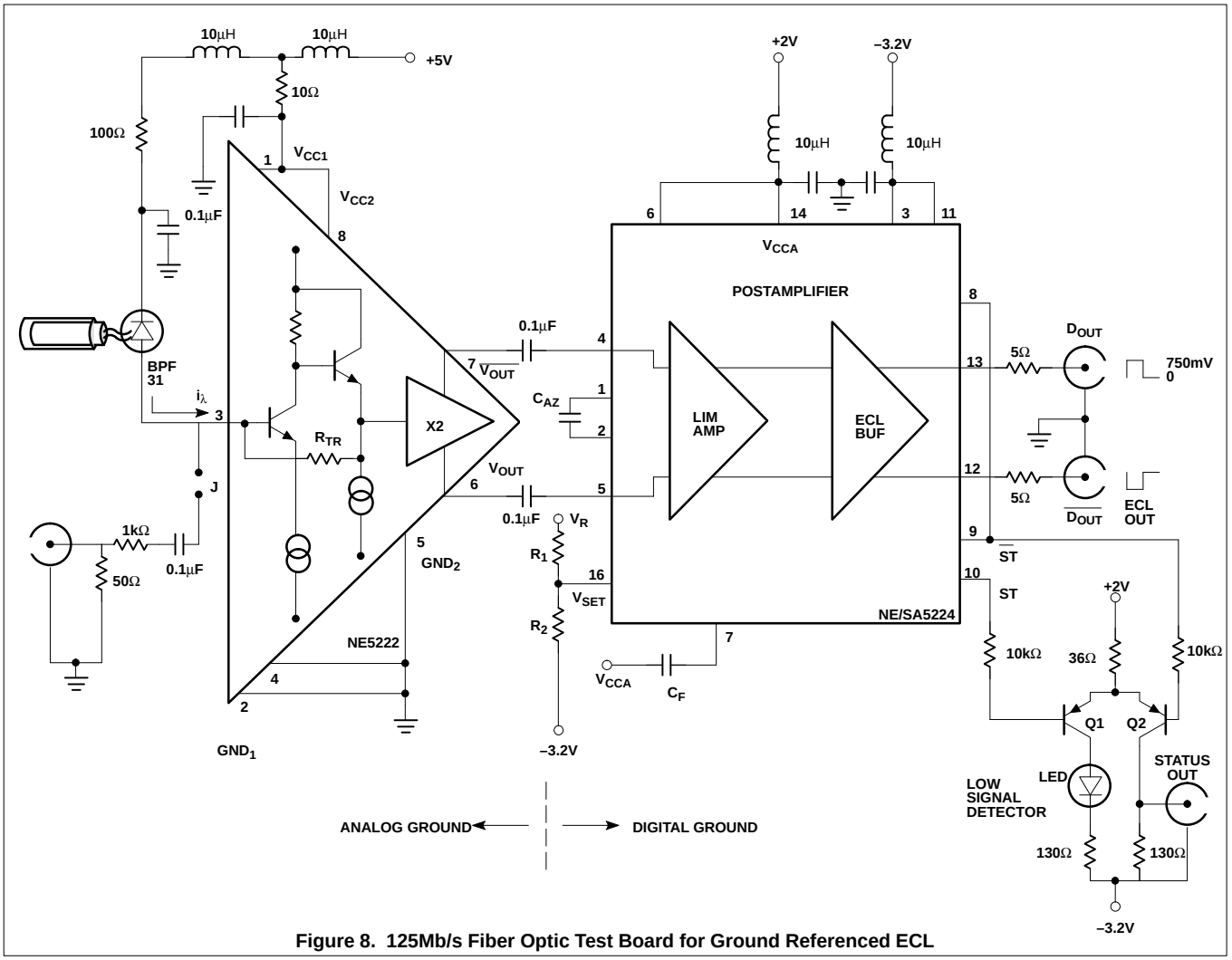

Figure 8. 125Mb/s Fiber Optic Test Board for Ground Referenced ECL

The Auto-Zero Loop

The auto-zero circuit provides closed loop feedback inside the NE/SA5224 which cancels the offset voltage of the forward signal path (Figure 7).

Essentially, the auto-zero circuit acts to cancel bias errors at the comparator due to component offsets and the data's average DC bias. The circuit is capable of cancelling the offset effect of long strings of zeros in transmission preventing a drift to a false output logic level.

The C_{AZ} capacitor is determined according to the relationship

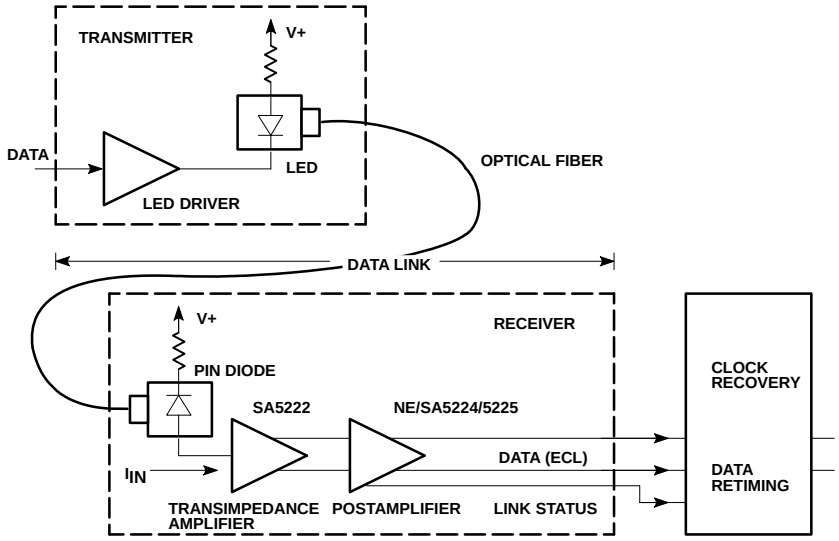

Figure 9. Fiber Optic-based Point-to-Point Communication Link

$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is specified by the data sheet.

For example if a 0.1uF capacitor is used for C_{AZ}, and R_{AZ} = 250kΩ.

$$f_{-3dB} = \frac{150}{2\pi \cdot 250x10^{3} \cdot 1x10^{-7}farad} = 1kHz$$

The lowest data frequency component must be above the –3dB frequency by an order of magnitude in order to reliably be reproduced at the ECL output. Lower frequencies will be filtered out by the AZ loop. The customer is referred to AN1443 for a more in-depth discussion of data rate response time versus the auto-zero function.

Setting The Threshold Level

A user programmable signal level detector is provided in both the NE/SA5224 and 5225. This circuit allows you to inhibit input signals which are below the predefined level as desired to provide a high quality output ECL signal, free of baseband noise. Setting the threshold is simply a matter of choosing a resistor divider ratio, R_1:R_2 as shown in Table 2 above, which connects from V_{REF}, Pin 15 to V_{SET}, Pin 16 (see Figure 4).

This provides the level detector with a threshold reference voltage. A scaled, rectified and filtered copy of the input signal is then compared to this threshold voltage. The programmable range is 4–24mV_{P-P} at the input and is a function of V_{SET}/100, a value which represents the average of V_{THIGH} and V_{TLOW}.

The actual threshold levels are:

$$V_{Tlow} = \frac{V_{SET}}{139} \quad \text{where } R_1 \text{ is constant} \quad R_2 = 5k$$

$$V_{Thigh} = \frac{V_{SET}}{78}$$

For example for V_{SET} = 1.2V, V_{TL} = 8.6mV and V_{TH} = 15.4mV. Table 2 shows various combinations of R_1 and R_2 with corresponding values of V_{SET} and threshold voltages.

$V_{HYST} = V_{TH} – V_{TL}$

Threshold levels as low as 4mV_{P-P} can be reliably set up for signal detection at the NE/SA5224,25 input. For sufficiently high signal levels the threshold may be maintained at an elevated clipping plateau allowing good rejection of incoming baseband noise.

(NOTE: 4mV_{P-P} corresponds to ≅ –33dBmo for an input PIN diode conversion efficiency of 0.45A/W.)

II. A TYPICAL RECEIVER TEST BOARD WITH ECL OUTPUT

The circuit shown in Figure 8 represents a simple printed circuit receiver capable of 100MB/s data processing from fiber.

The input photo optic device is a Philips BPF31 PIN diode optimized for a wavelength of 850nm.

The various waveforms (Figures 11–18) show signal levels produced within the receiver, for different optical power and data rates.

Supply voltages have been set for 5V on the SA5222 and +2V; –3.2V on the SA5224. This allows grounded 50Ω loads to be used at the output of the receiver.

The differential output of the transimpedance preamplifier is AC coupled to the NE5224 postamplifier to prevent any DC bias offset in the preamp from affecting the threshold accuracy of the output stage.

The coupling capacitors are made sufficiently large (0.1μF) in order to pass the lowest frequency data component.

The threshold voltage is set to 1.0V by R_1 and R_2 at Pin 16 of the NE5224 postamplifier. As noted in Table 2 this sets the threshold level, Vth, at 12.8mV_{P-P}.

This corresponds to an input current on Pin 3 of the SA5222 of

$$I_{IN} = \frac{12.8mV}{16.6 \times 10^3} = 0.75 \text{ A}$$

or $$P_{OPT} = \frac{0.75 \cdot 10^{-6}A}{0.45A \text{ W}} = 1.7 \text{ W}$$

or –28dBmo, minimum.

C|AZ| is 0.1µF for a low frequency data limit of 1KHz.

The status detector allows visual output to determine when the input signal level is above the receiver threshold described above. The light is on when signal level is below threshold. (Figure 8).

The Optical Receiver Board Construction (Figure 19)

Supply decoupling is obtained by splitting up the various parts of the receiver with 10µH chokes combined with low inductance chip capacitors placed in close proximity to the IC supply pin and grounded to wide ground plane copper areas.

Observe that the top and bottom of the printed circuit board is covered with copper ground plane within which the circuit traces are embedded. In addition, the bottom and top planes are tied together with connecting pins (soldered carefully) and placed at numerous points around the board. In particular this must be done where critical ground returns such as ground 1 and 2 of the SA5222 are brought out of the SMD device. A good rule is to place top to bottom ground plane pins every half inch in critical areas.

The supply is isolated between the input preamplifier, SA5222 and the post amplifier, SA5224. Ground traces are also separated into input stage (analog) and output stage (digital) grounds. This technique provides a more stable circuit, in addition to allowing ground referenced ECL signal into 50Ω loads at the output.

Noise Immunity

Level detection is set to automatically block reception when input signals fall below the threshold.

If left disconnected the JAM function is inactive. The NE/SA5224 (100K ECL output) and the NE/SA5225 (10K ECL output) easily provide sufficient signal detection and level translation accuracy for 100MB/s signal reproduction.

The signal-to-noise ratio is primarily determined by the receiver input stage so that equivalent input noise versus input signal current and signal bandwidth sets the limits on the signal-to-noise ratio of the combined receiver.

The noise immunity of the receiver proper, including the PC board, is determined by how well the layout is done. Ground plane construction of the signal preamplifier and post amplifier (with regard to RF technique) is required. No high level signal traces should be returned near the input sections in order to prevent feedback oscillation. The overall gain of preamplifier and post amplifier is in excess of 100dB with very wide bandwidth. This makes physical as well as electrical layout critical but reasonable once the rules are understood. Good bypassing of the V_{CC} lines, a low inductance ground plane and high quality passive components are required.

Note that 1” of copper trace 1/16th” wide is equivalent to 15nH of inductance. Wide traces on all V_{CC} and ground bus connections are mandatory. The same applies to the PIN diode signal traces at the input stage.

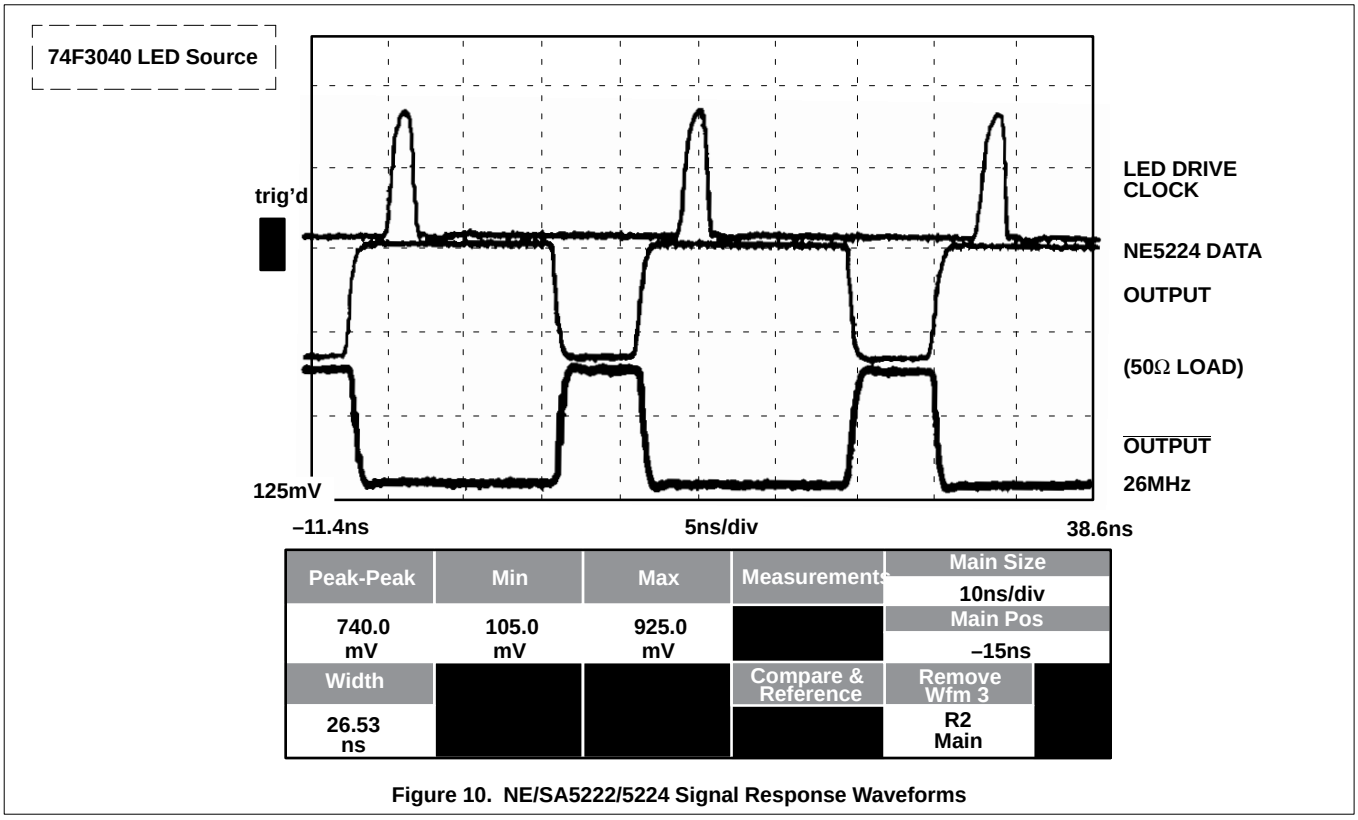

Figure 10. NE/SA5222/5224 Signal Response Waveforms

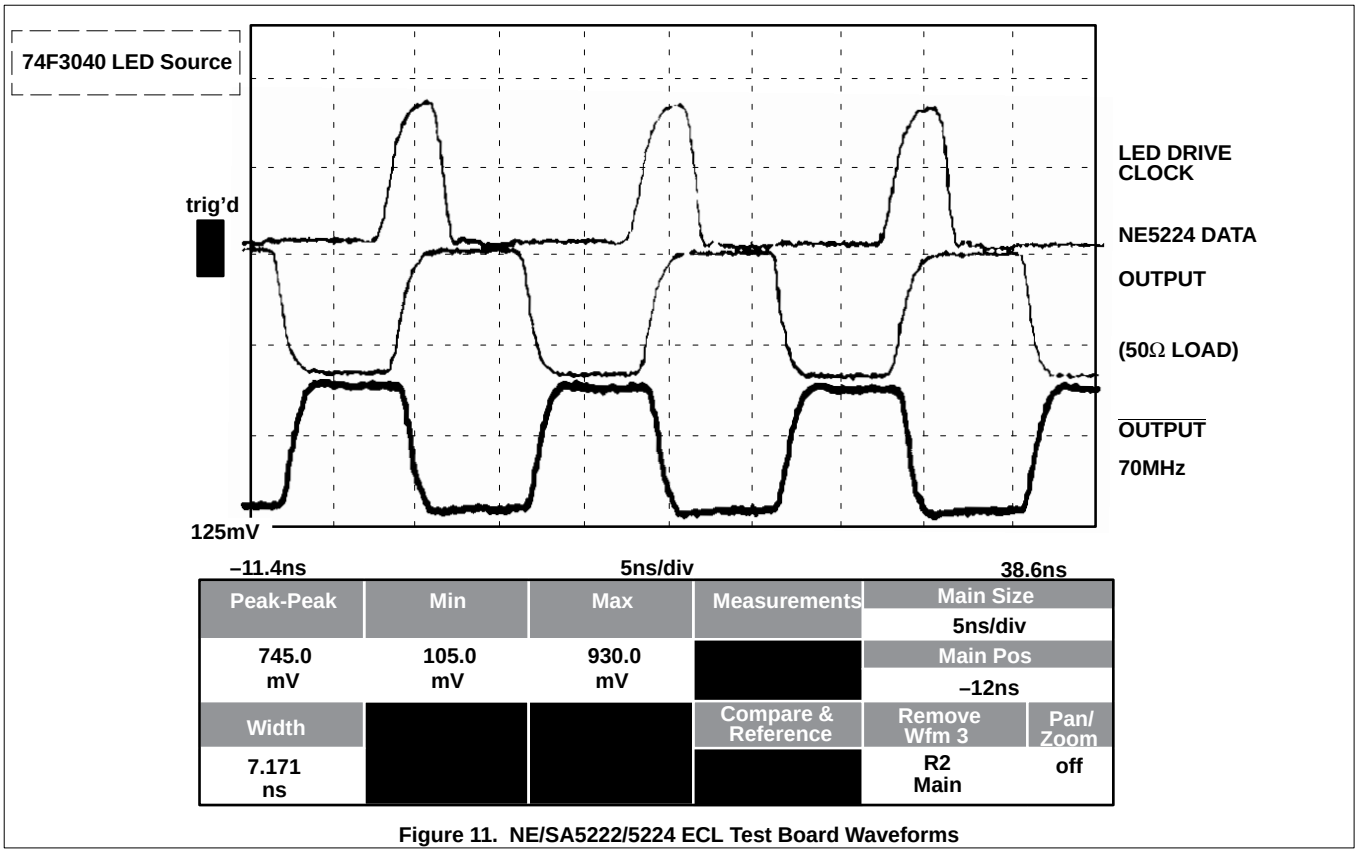

Figure 11. NE/SA5222/5224 ECL Test Board Waveforms

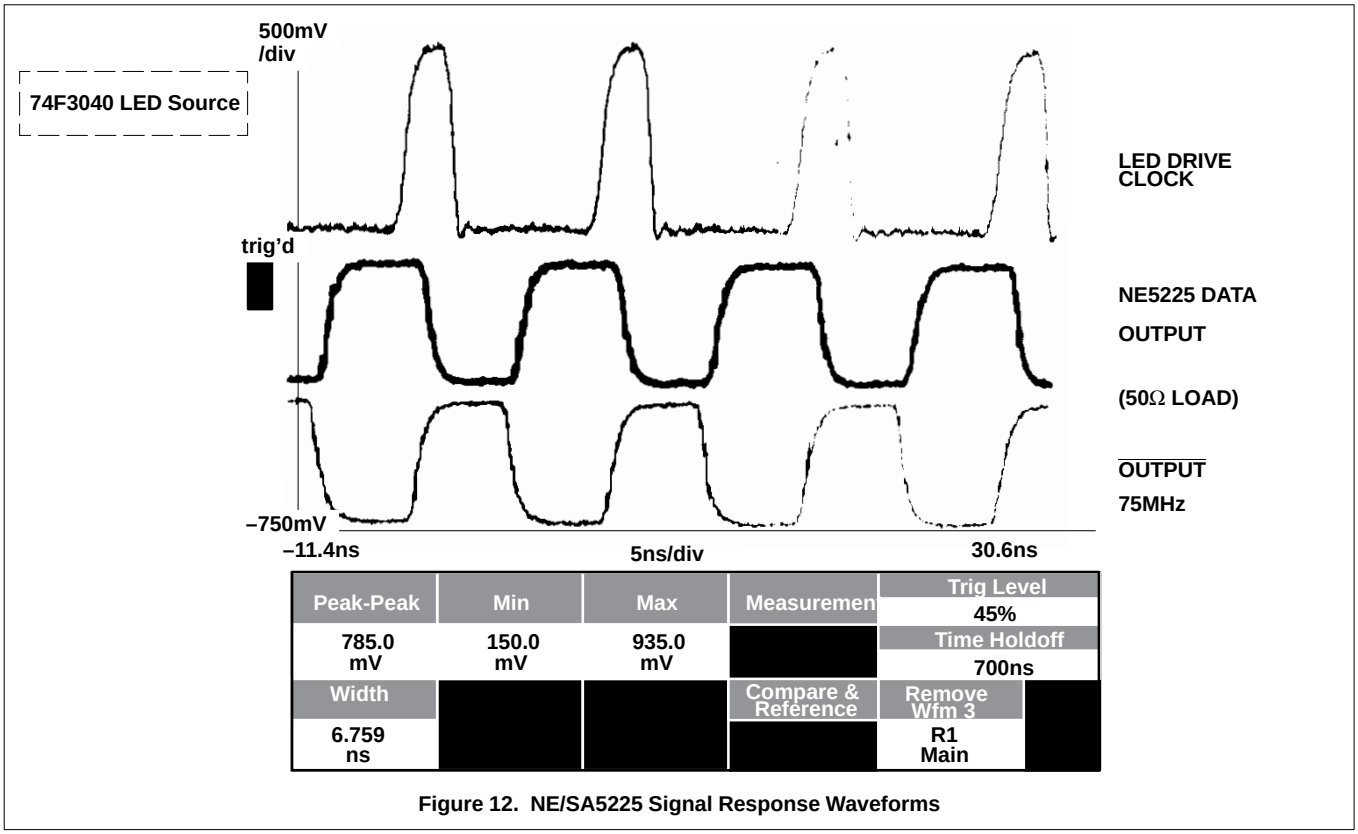

Figure 12. NE/SA5225 Signal Response Waveforms

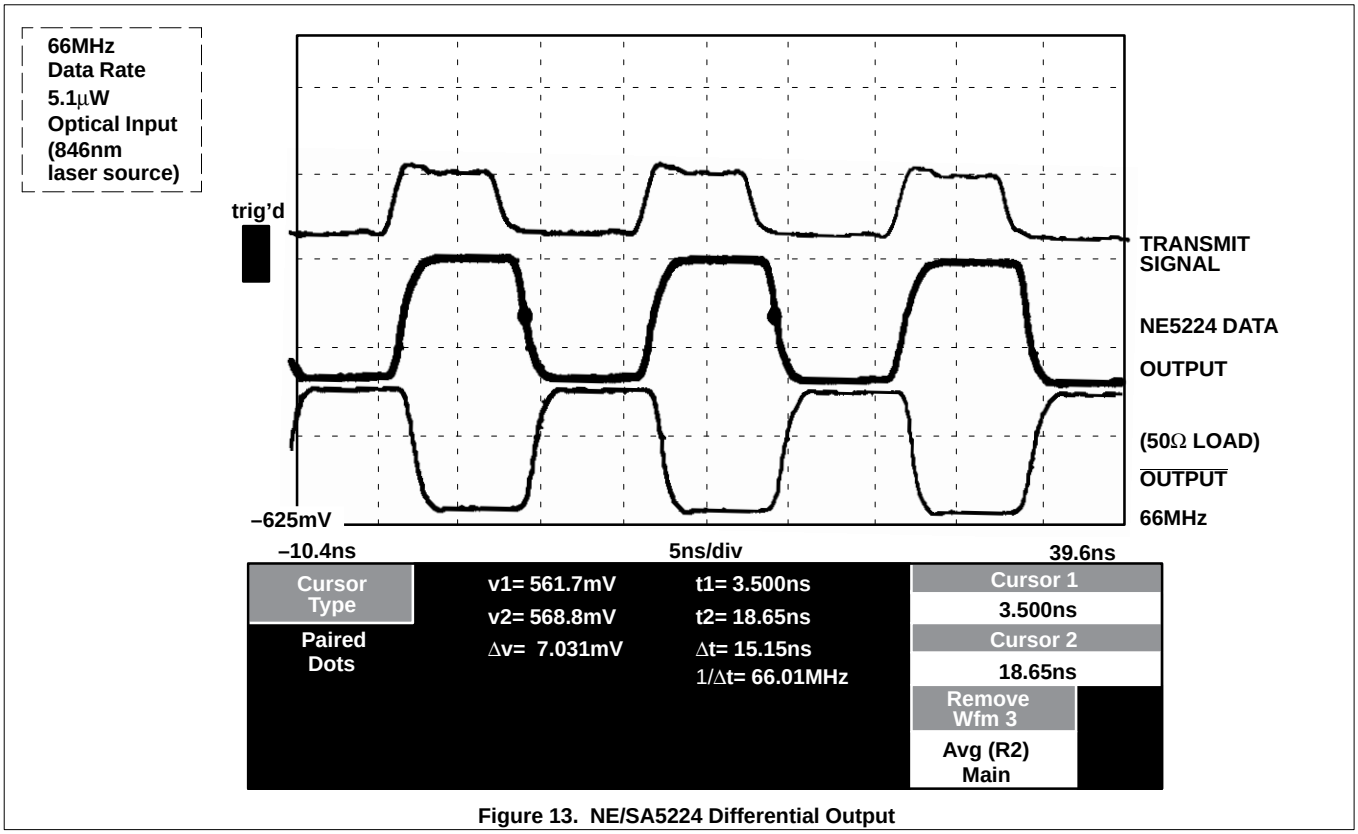

Figure 13. NE/SA5224 Differential Output

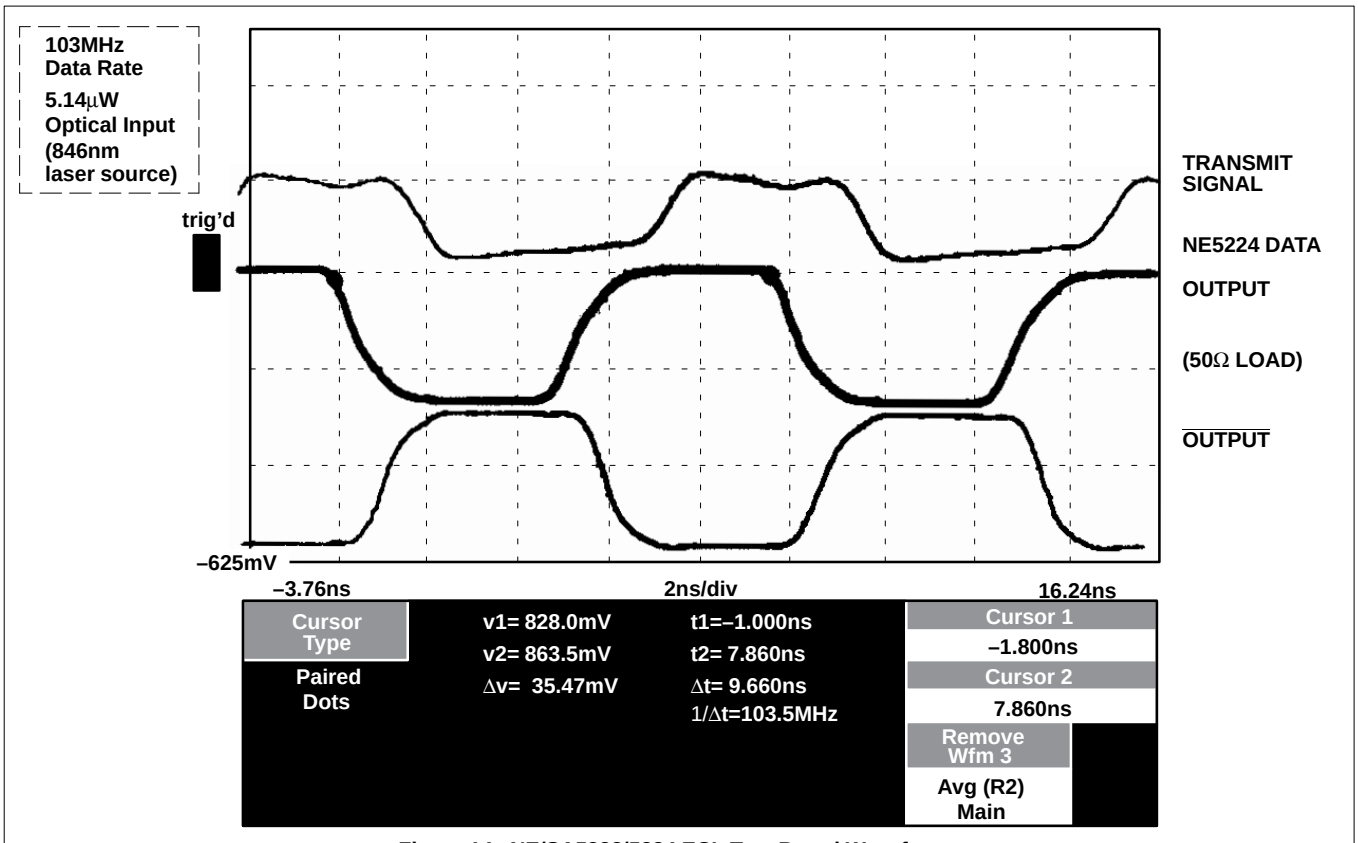

Figure 14. NE/SA5222/5224 ECL Test Board Waveforms

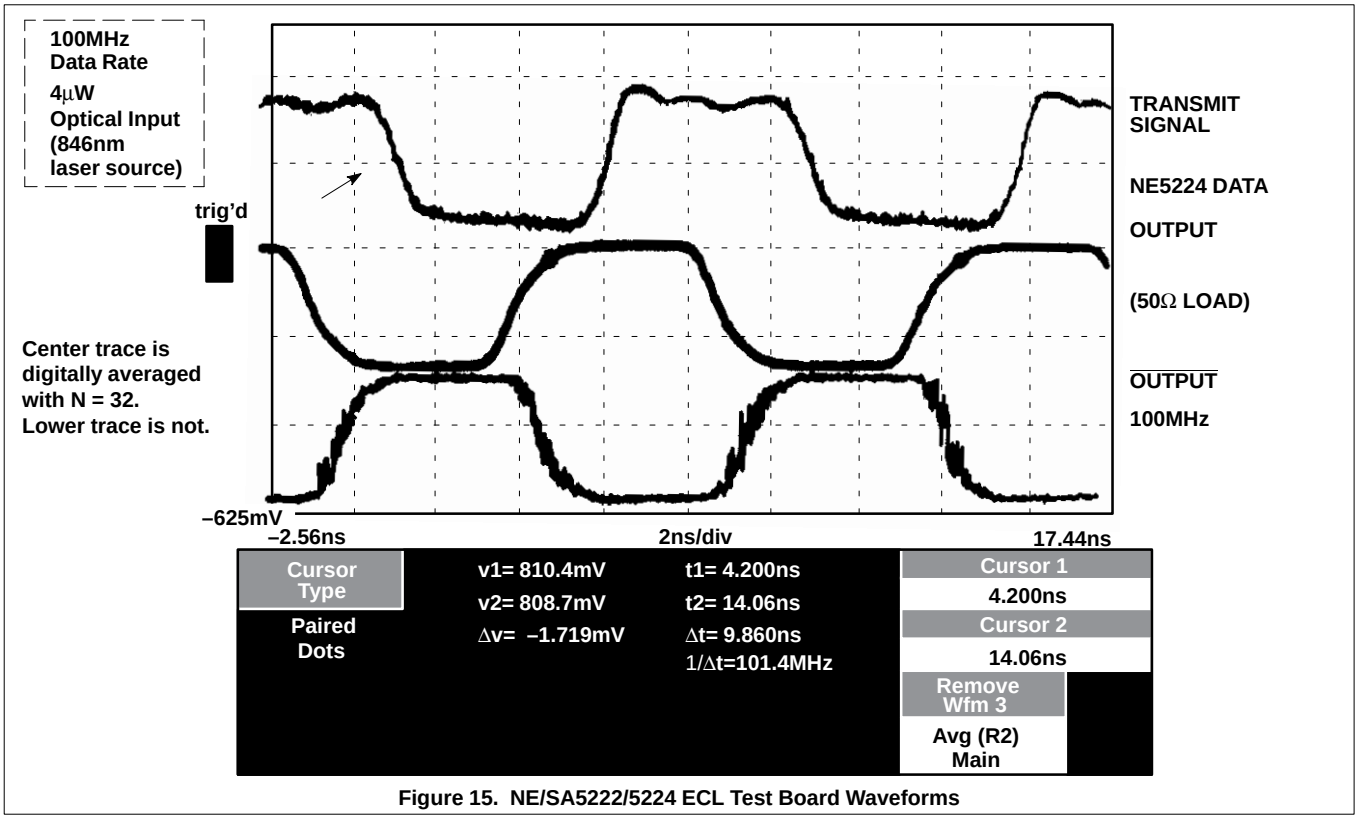

Figure 15. NE/SA5222/5224 ECL Test Board Waveforms

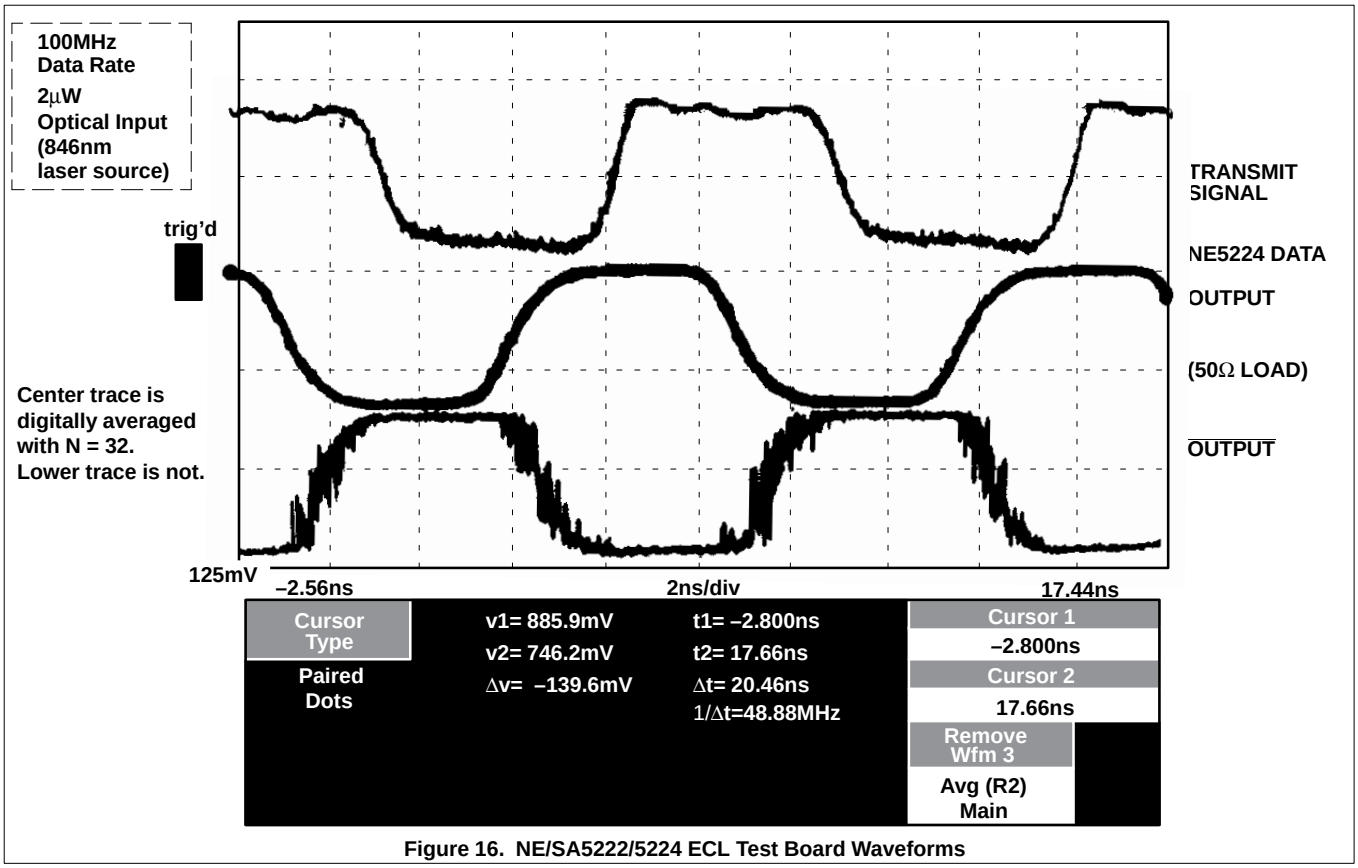

Figure 16. NE/SA5222/5224 ECL Test Board Waveforms

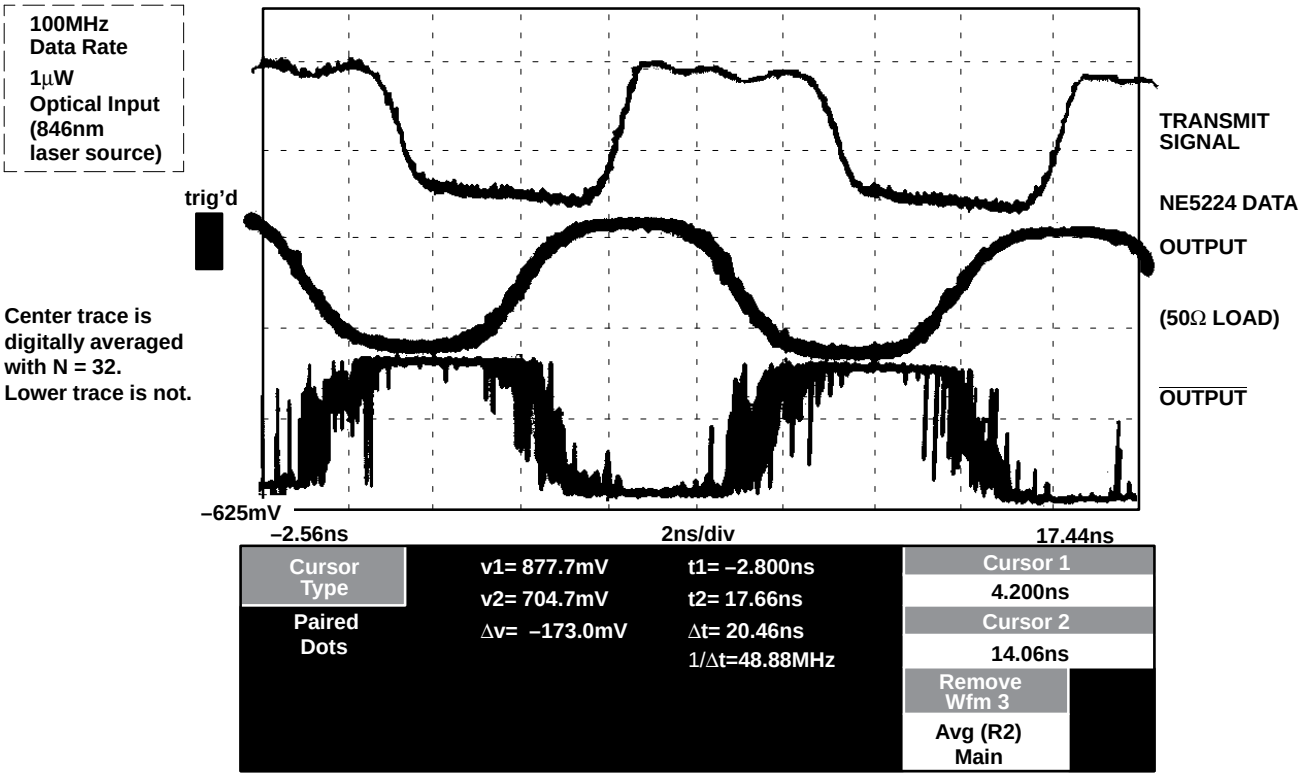

Figure 17. NE/SA5222/5224 ECL Test Board Waveforms

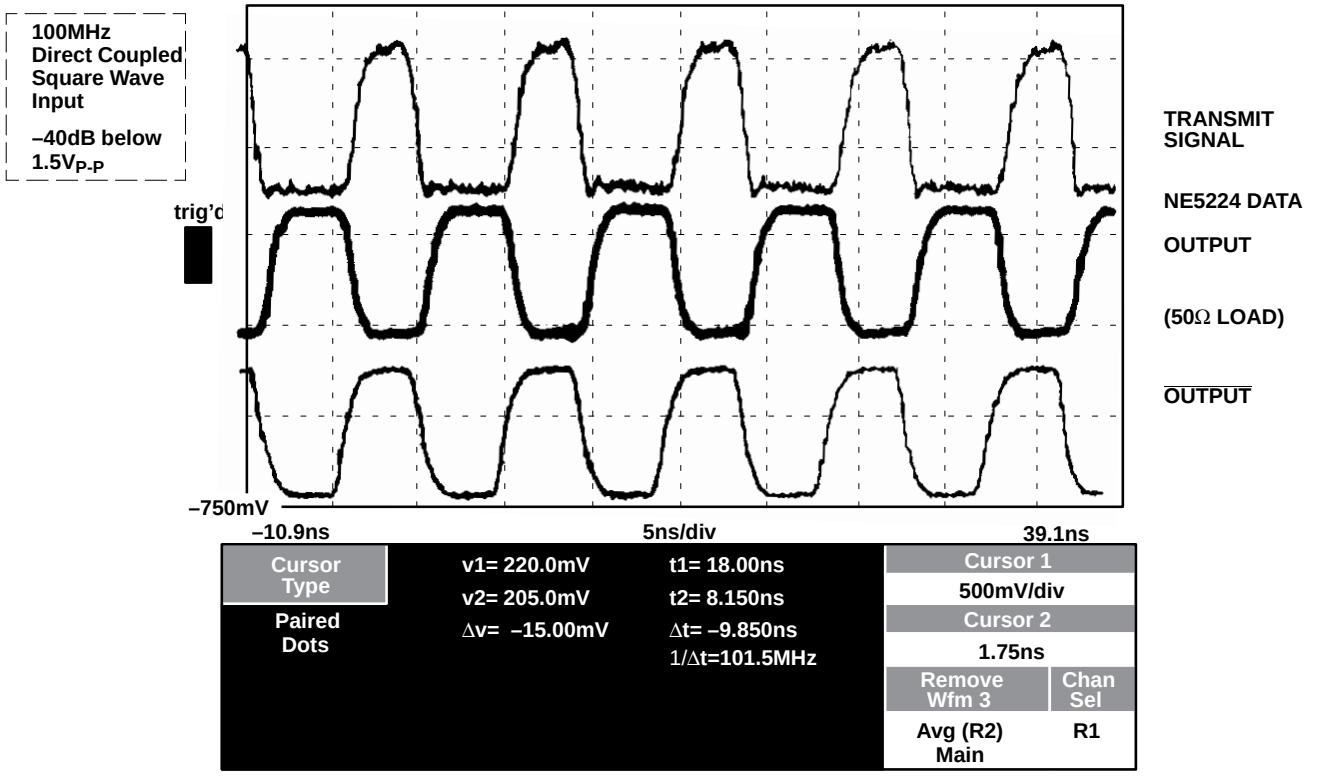

Figure 18. NE/SA5222/5224 ECL Test Board Waveforms

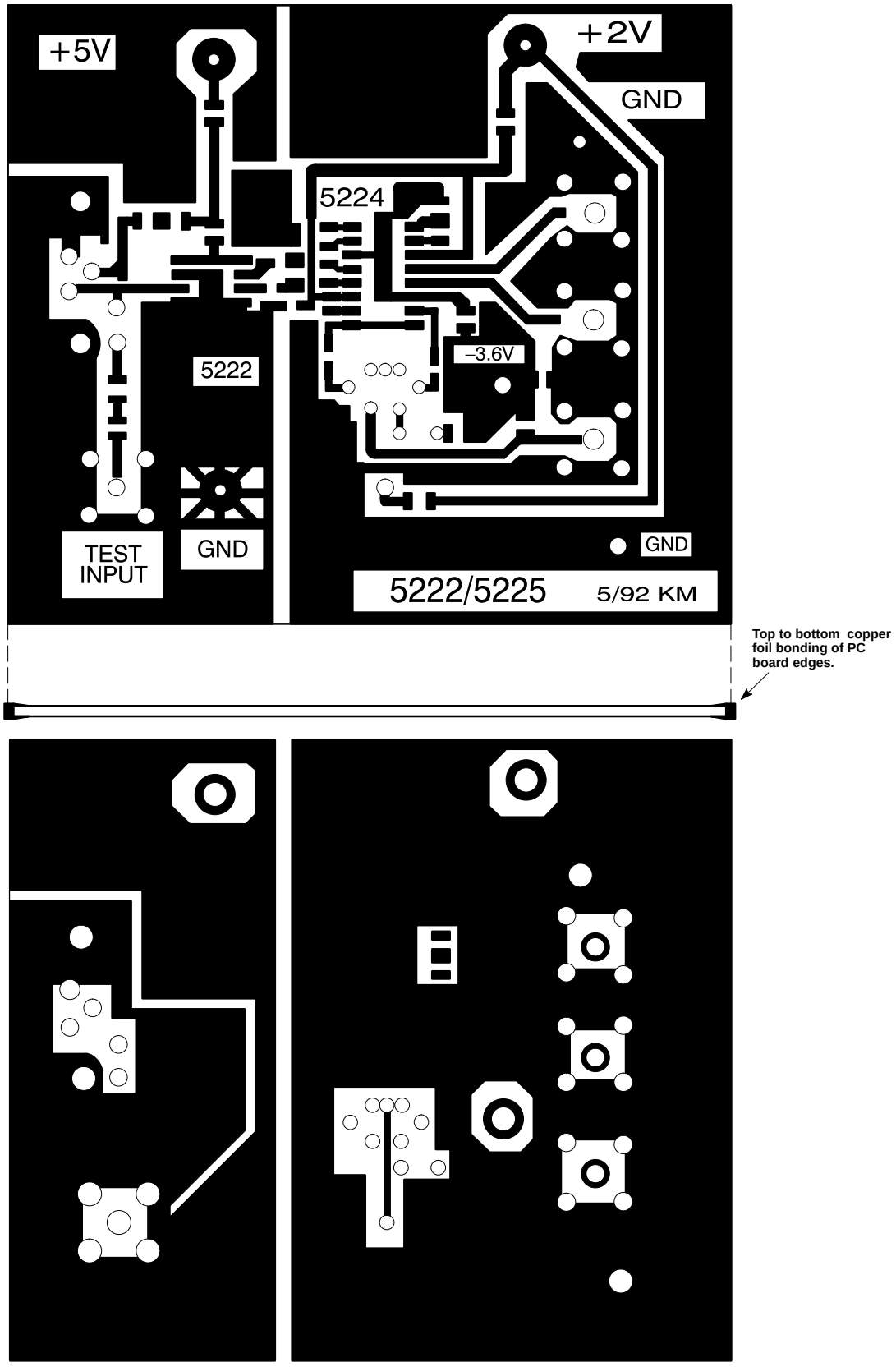

Figure 19. PC Board Layout