

Silicon NPN Power Transistors

2SD772 2SD772A 2SD772B

DESCRIPTION

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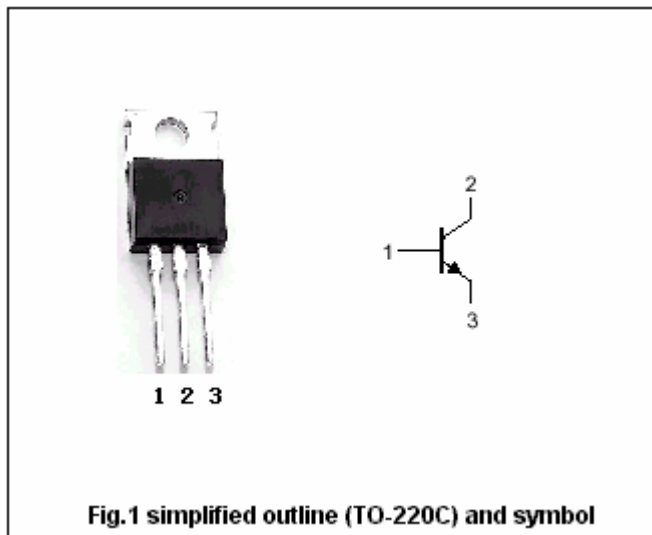
- With TO-220C package
- High breakdown voltage
- High speed switching

APPLICATIONS

- For power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter



Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	2SD772	150	V
		2SD772A	200	
		2SD772B	250	
V _{CEO}	Collector-emitter voltage	Open base	80	V
V _{EBO}	Emitter-base voltage	Open collector	6	V
I _C	Collector current (DC)		5	A
I _{CM}	Collector current-Peak		10	A
P _C	Collector dissipation	T _C =25°C	40	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-50~150	°C

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CHARACTERISTICS

T_j=25°C unless otherwise specified

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =0.2A; L=25mH	80			V	
V _{CEsat}	Collector-emitter saturation voltage	I _C =5A; I _B =1A			1.6	V	
V _{BE}	Base-emitter on voltage	I _C =5A; V _{CE} =4V			1.5	V	
I _{CBO}	Collector cut-off current	2SD772			1.0	mA	
		2SD772A					V _{CB} =150V; I _E =0
		2SD772B					V _{CB} =200V; I _E =0
I _{EBO}	Emitter cut-off current	V _{EB} =6V; I _C =0			0.1	mA	
h _{FE}	DC current gain	I _C =5A; V _{CE} =4V	14				
t _f	Fall time	I _C =5A; V _{EB} =-5V, I _{B1} =0.8A			1	μs	
f _T	Transition frequency	I _C =0.5A; V _{CE} =10V		40		MHz	

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PACKAGE OUTLINE

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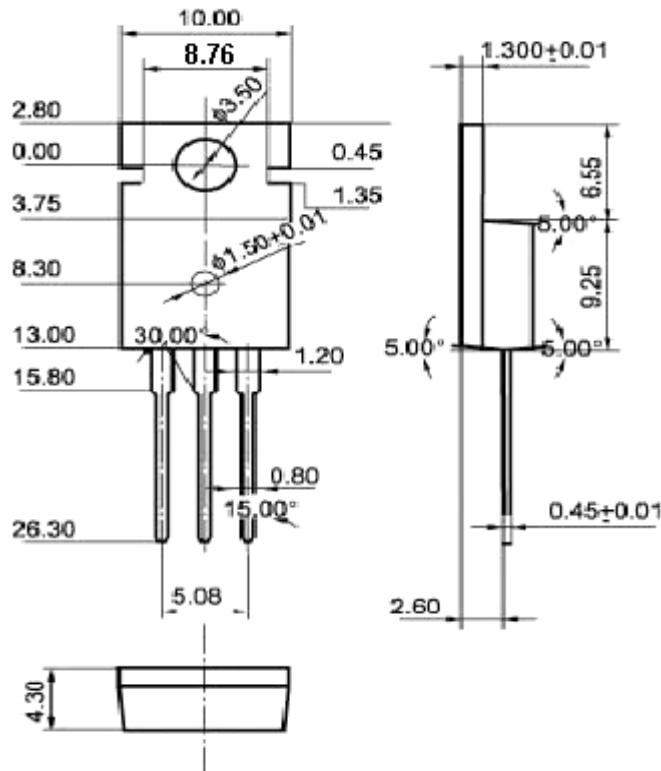


Fig.2 Outline dimensions (unindicated tolerance:±0.10mm)