

PHX18NQ11T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 13 February 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a fully isolated plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Isolated mounting base
- Fast switching
- Low thermal resistance

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

1.4 Quick reference data

- $V_{DS} \leq 110 \text{ V}$
- $I_D \leq 12.5 \text{ A}$
- $P_{tot} \leq 31.2 \text{ W}$
- $R_{DS(on)} \leq 90 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT186A (TO-220F), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	source (s)		
3	drain (d)		
mb	mounting base; isolated	SOT186A (TO-220F)	



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHX18NQ11T	TO-220F	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220AB 'full pack'	SOT186A

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	110	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	110	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_h = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	[1] -	12.5	A
		$T_h = 100\text{ °C}$; $V_{GS} = 10\text{ V}$ Figure 2	[1] -	7.9	A
I_{DM}	peak drain current	$T_h = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	[1] -	50.2	A
P_{tot}	total power dissipation	$T_h = 25\text{ °C}$; Figure 1	[1] -	31.2	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

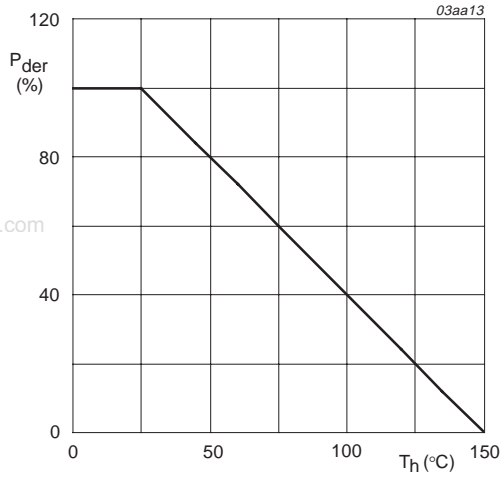
Source-drain diode

I_S	source (diode forward) current (DC)	$T_h = 25\text{ °C}$	[1] -	12.5	A
I_{SM}	peak source (diode forward) current	$T_h = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1] -	50.2	A

Avalanche ruggedness

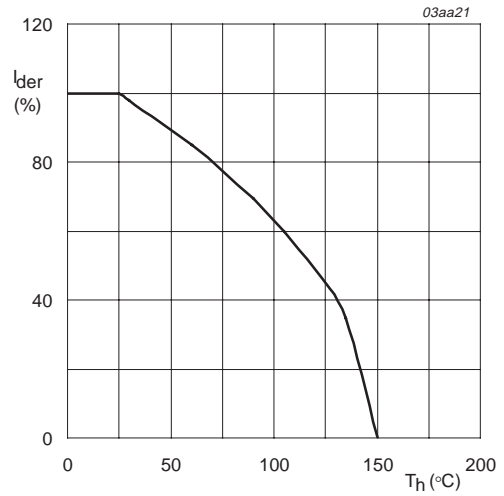
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 7.5\text{ A}$; $t_p = 0.09\text{ ms}$; $V_{DD} \leq 15\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	56	mJ
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[1] External heatsink connected to mounting base.



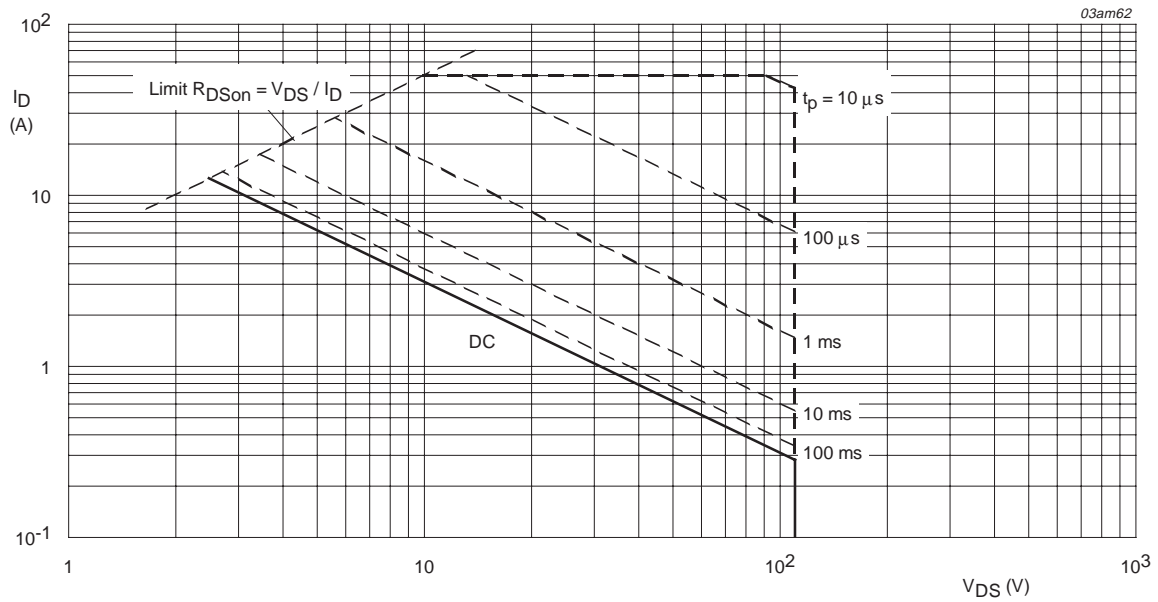
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of heatsink temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of heatsink temperature.



T_h = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	Figure 4	[1]	-	4	K/W

[1] External heatsink connected to mounting base.

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5.1 Transient thermal impedance

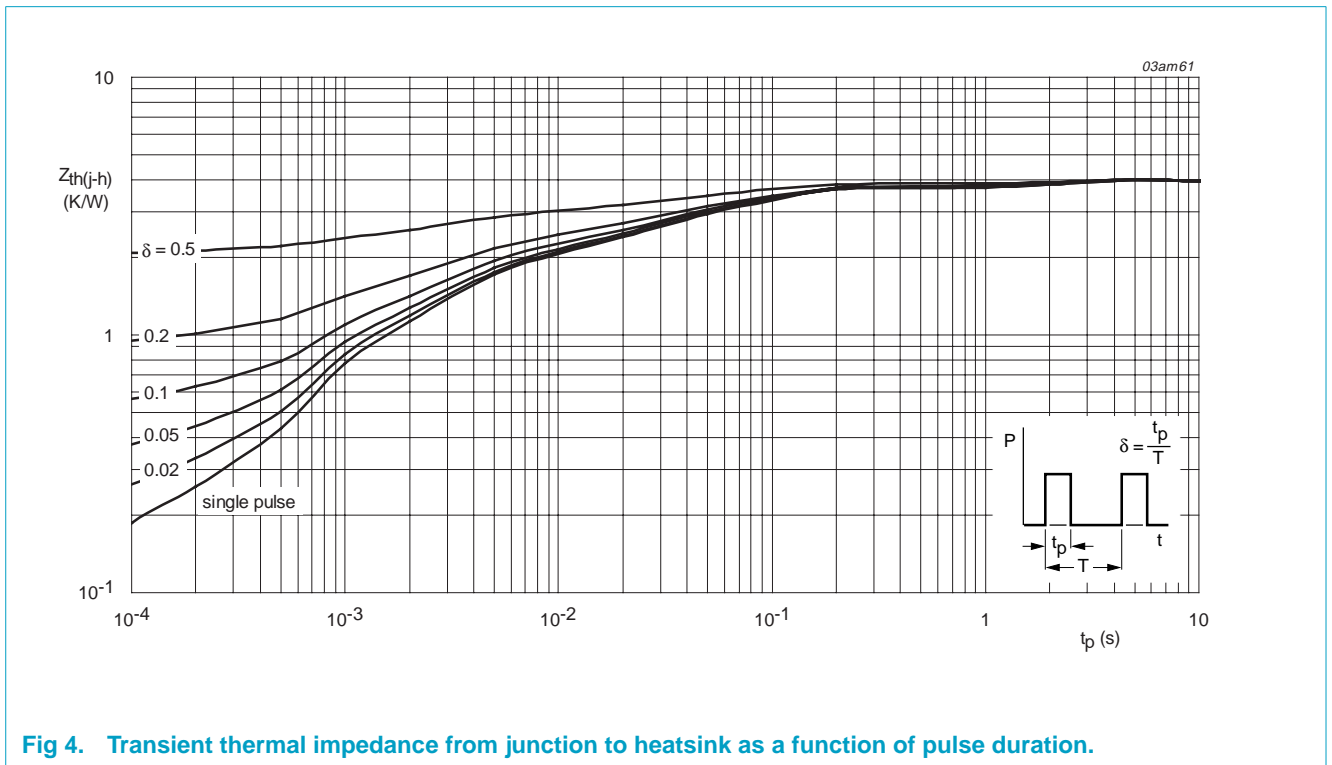
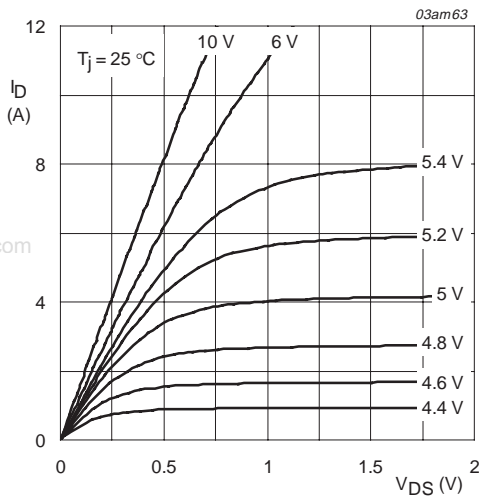


Fig 4. Transient thermal impedance from junction to heatsink as a function of pulse duration.

6. Characteristics

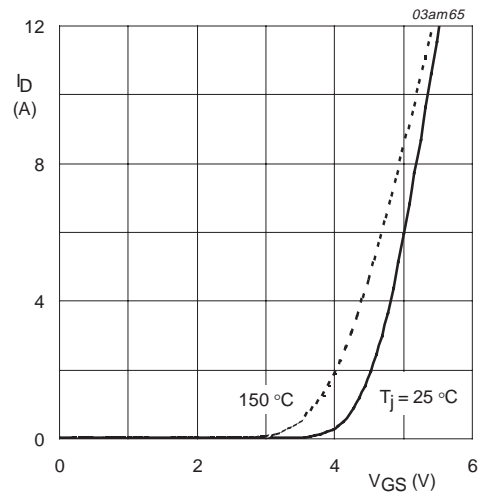
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	110	-	-	V
		$T_j = -55\text{ °C}$	99	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 100\ \text{V}$; $V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 150\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 9\ \text{A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	67	90	m Ω
		$T_j = 150\text{ °C}$	-	148	198	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 3\ \text{A}$; $V_{DD} = 80\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 13	-	21	-	nC
Q_{gs}	gate-source charge		-	2.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	8	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	635	-	pF
C_{oss}	output capacitance		-	105	-	pF
C_{rss}	reverse transfer capacitance		-	60	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 50\ \text{V}$; $R_L = 15\ \Omega$; $V_{GS} = 10\ \text{V}$; $R_G = 5.6\ \Omega$	-	6	-	ns
t_r	rise time		-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	10	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 12\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.87	1.2	V
t_{rr}	reverse recovery time	$I_S = 12\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	55	-	ns
Q_r	recovered charge		-	135	-	nC



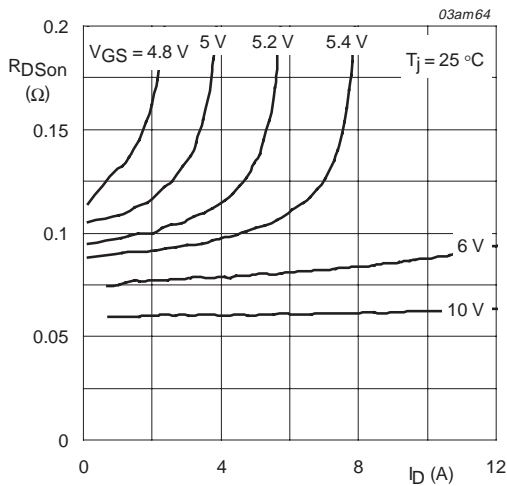
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



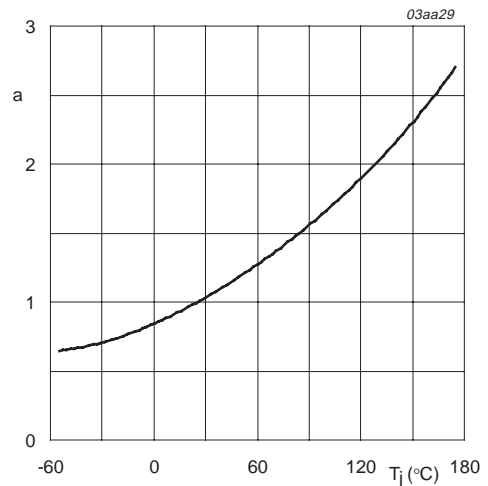
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



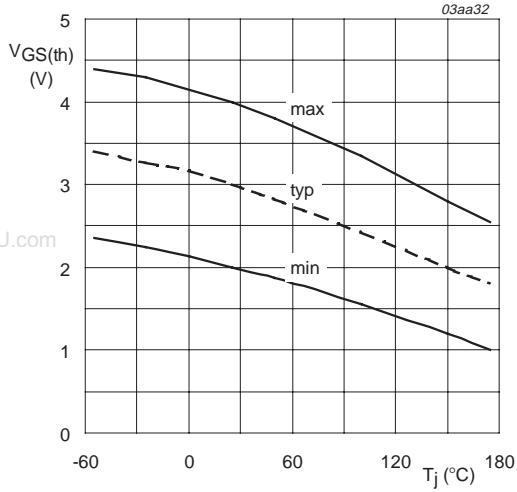
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



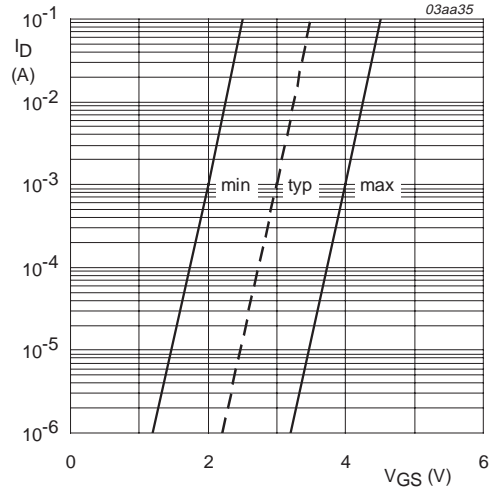
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



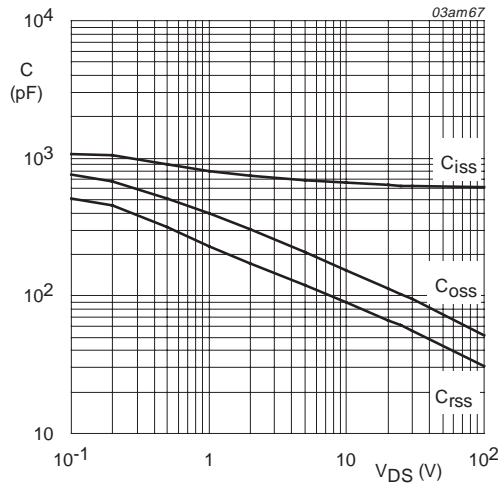
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



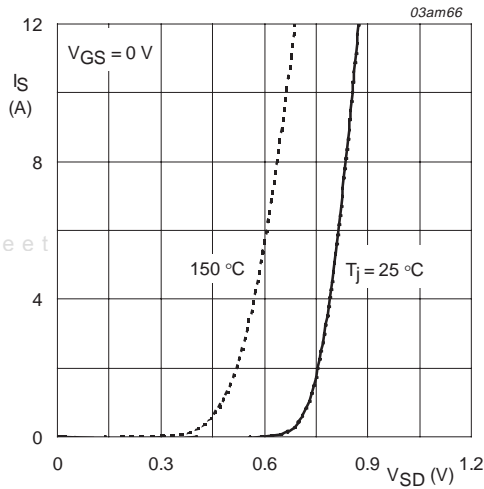
$T_j = 25 \text{ }^{\circ}C$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



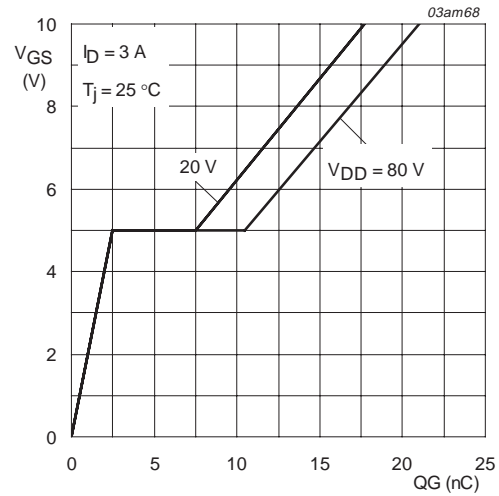
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 3\text{ A}$; $V_{DD} = 20\text{ V}$ and 80 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Isolation characteristics

Table 6: Isolation characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(isol)RMS}$	RMS isolation voltage from all three terminals to external heatsink	$f = 50\text{-}60\text{ Hz}$; sinusoidal waveform; $RH \leq 65\%$; clean and dust-free.	-	-	2500	V
$C_{(d-h)}$	Capacitance from drain to external heatsink		-	10	-	pF

8. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 'full pack'

SOT186A

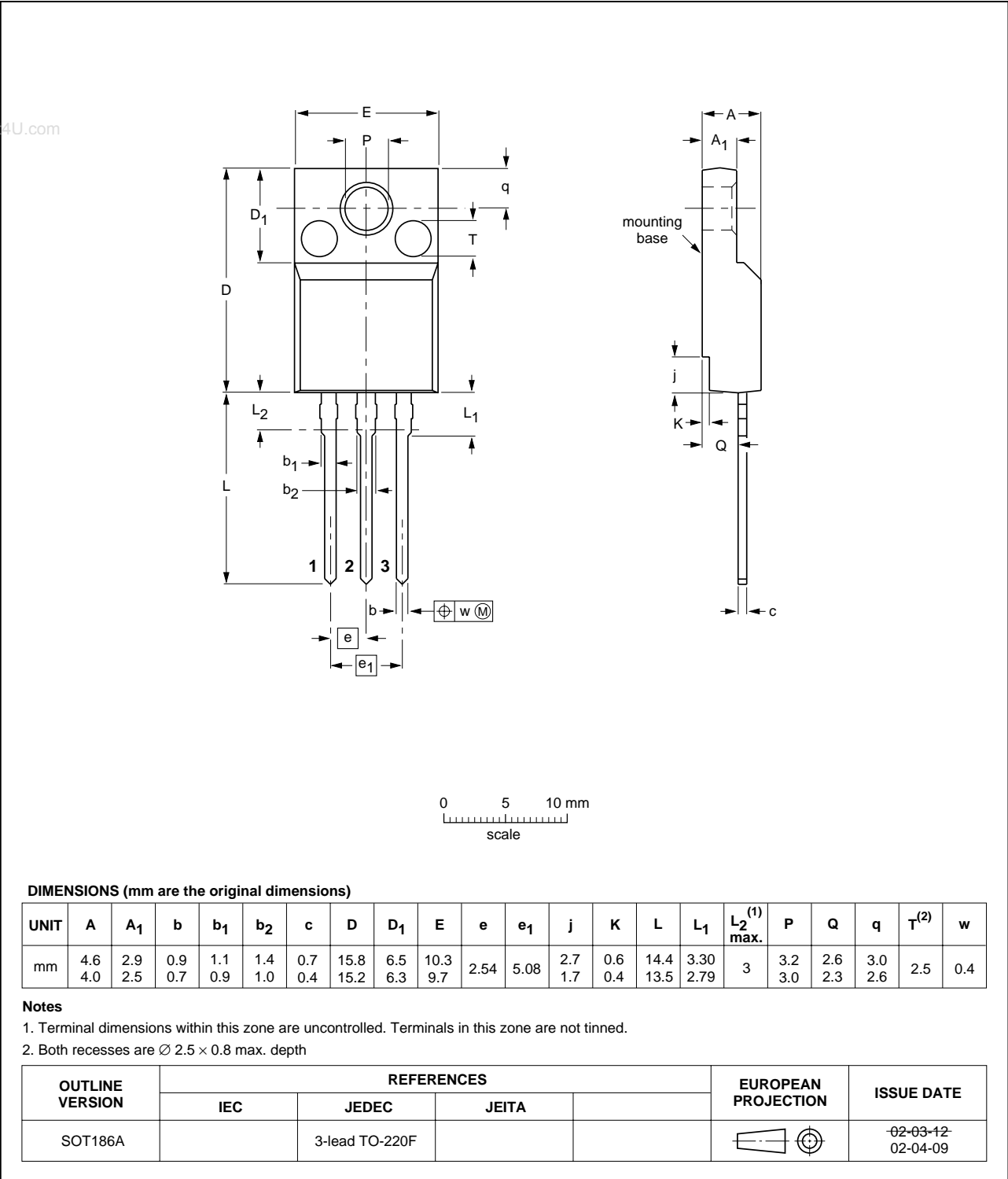


Fig 14. SOT186A (TO-220F).

9. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
01	20040213	-	Product data (9397 750 12915)

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
5.1	Transient thermal impedance	4
6	Characteristics	5
7	Isolation characteristics	8
8	Package outline	9
9	Revision history	10
10	Data sheet status	11
11	Definitions	11
12	Disclaimers	11
13	Trademarks	11

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