

SILICON GATE BICMOS

131,072 WORD x 8 BIT BiCMOS STATIC RAM

Description

The TC55B8128P/J is a 1,048,576 bit high speed BiCMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B8128P/J features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access.

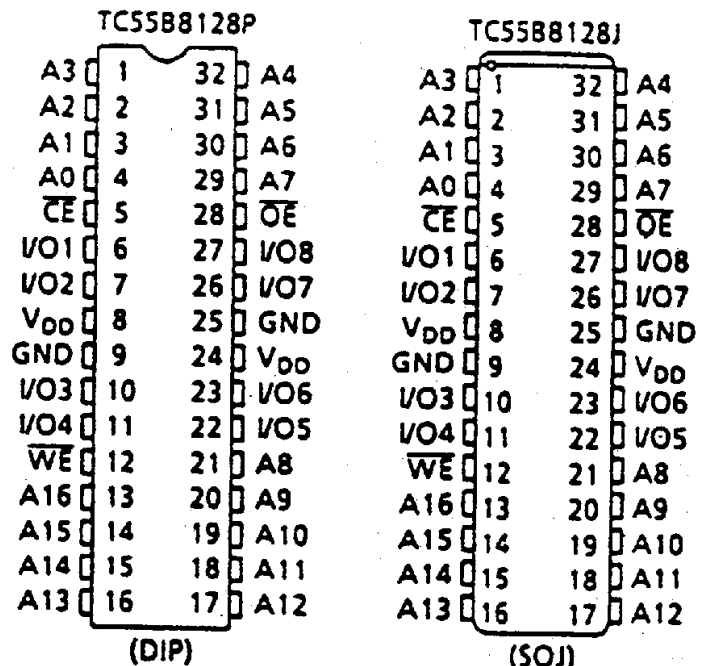
The TC55B8128P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B8128P/J is available in a 400mil width, 32-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55B8128P/J-12 12ns (max.)
 - TC55B8128P/J-15 15ns (max.)
 - TC55B8128P/J-20 20ns (max.)
- Low power dissipation
 - Operation:
 - TC55B8128P/J-12 150mA (max.)
 - TC55B8128P/J-15 150mA (max.)
 - TC55B8128P/J-20 150mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: 5V \pm 10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B8128P: DIP32-P-400
 - TC55B8128J: SOJ32-P-400A

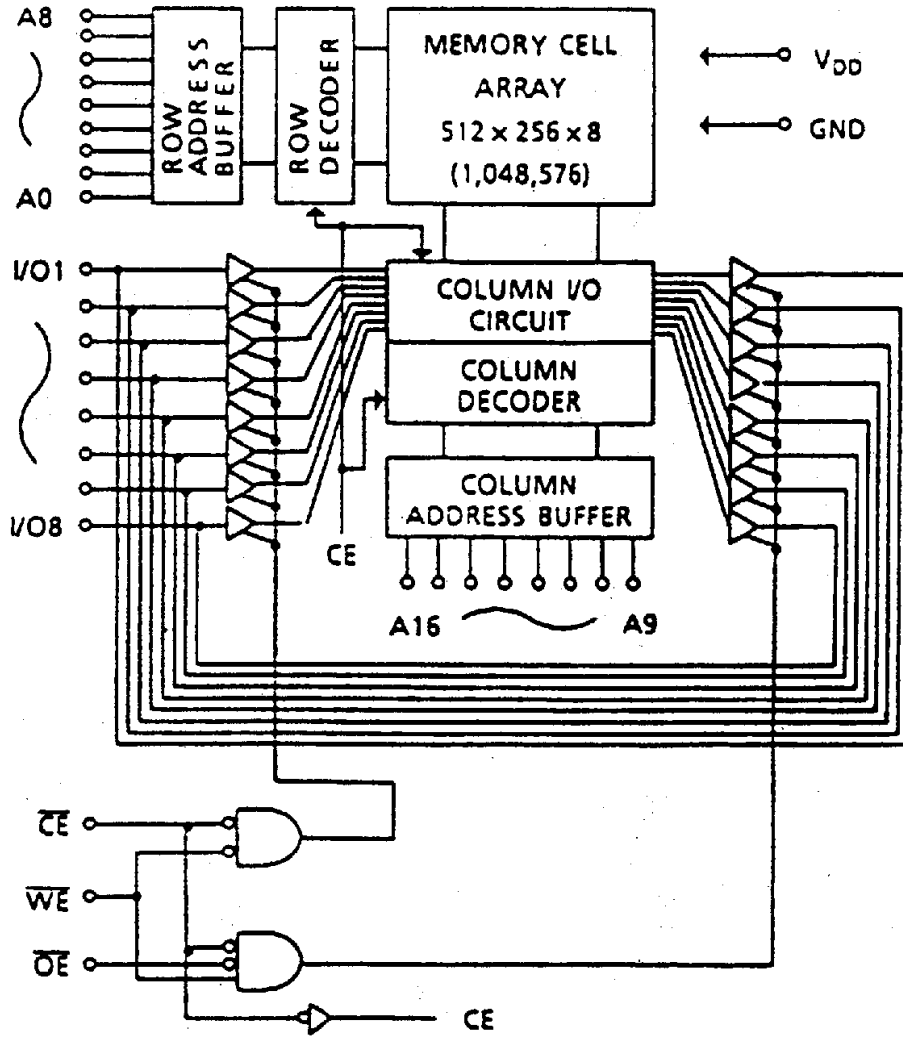
Pin Connection (Top View)



Pin Names

A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O	POWER
Read		L	L	H	Output	I_{DDO}
Write		L	*	L	Input	I_{DDO}
Output Disabled		L	H	H	High-Z	I_{DDO}
Standby		H	*	*	High-Z	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	900	mW
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* 3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	-	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	-	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	-	-	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	-	-	150	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$, Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	-	-	15	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B8128P/J-12		TC55B8128P/J-15		TC55B8128P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	-	15	-	20	-	ns
t_{ACC}	Address Access Time	-	12	-	15	-	20	
t_{CO}	Chip Enable Access Time	-	12	-	15	-	20	
t_{OE}	Output Enable Access Time	-	7	-	8	-	10	
t_{COE}	Output Enable Time from \overline{CE}	4	-	4	-	4	-	
t_{COD}	Output Disable Time from \overline{CE}	-	6	-	7	-	8	
t_{OEE}	Output Enable Time from \overline{OE}	0	-	0	-	0	-	
t_{ODO}	Output Disable Time from \overline{OE}	-	5	-	6	-	7	
t_{OH}	Output Data Hold Time from Address Change	4	-	4	-	4	-	

Write Cycle

SYMBOL	PARAMETER	TC55B8128P/J-12		TC55B8128P/J-15		TC55B8128P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	-	15	-	20	-	ns
t_{WP}	Write Pulse Width	8	-	9	-	10	-	
t_{AW}	Address Valid to End of Write	9	-	10	-	11	-	
t_{CW}	Chip Enable to End of Write	8	-	9	-	10	-	
t_{AS}	Address Setup Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	1	-	
t_{OEW}	Output Enable Time from \overline{WE}	1	-	1	-	1	-	
t_{ODW}	Output Disable Time from \overline{WE}	-	6	-	7	-	8	
t_{DS}	Data Setup Time	7	-	8	-	9	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

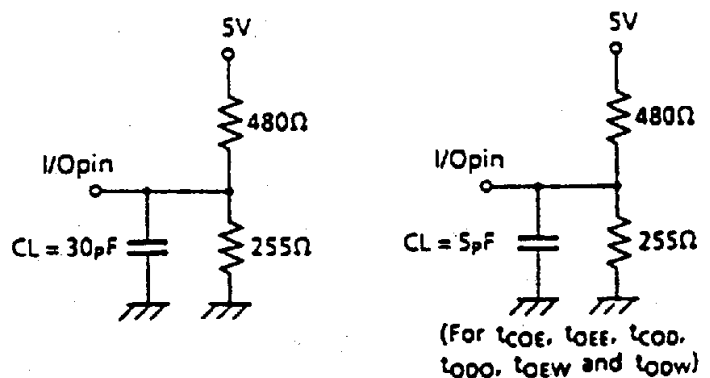
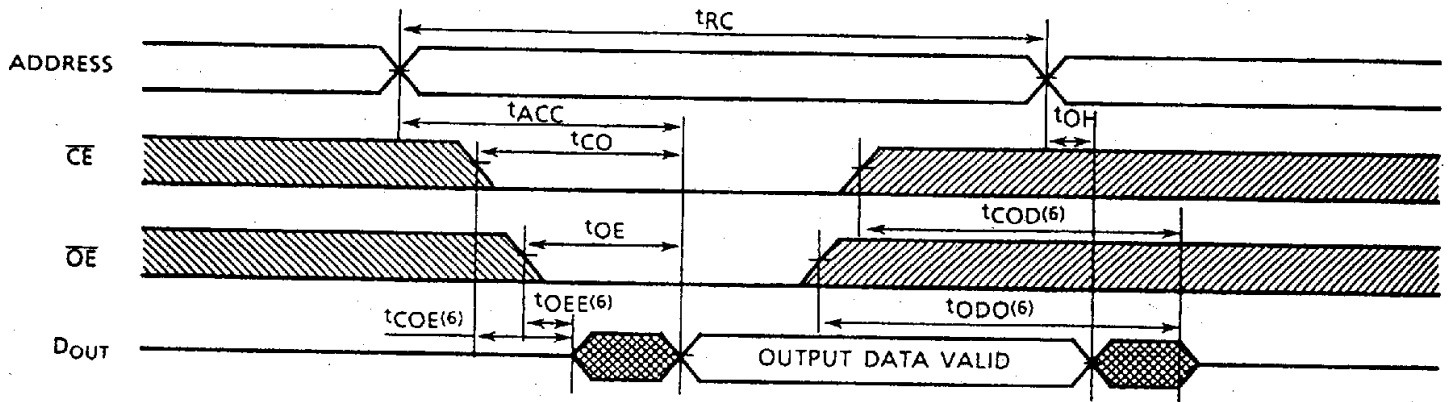


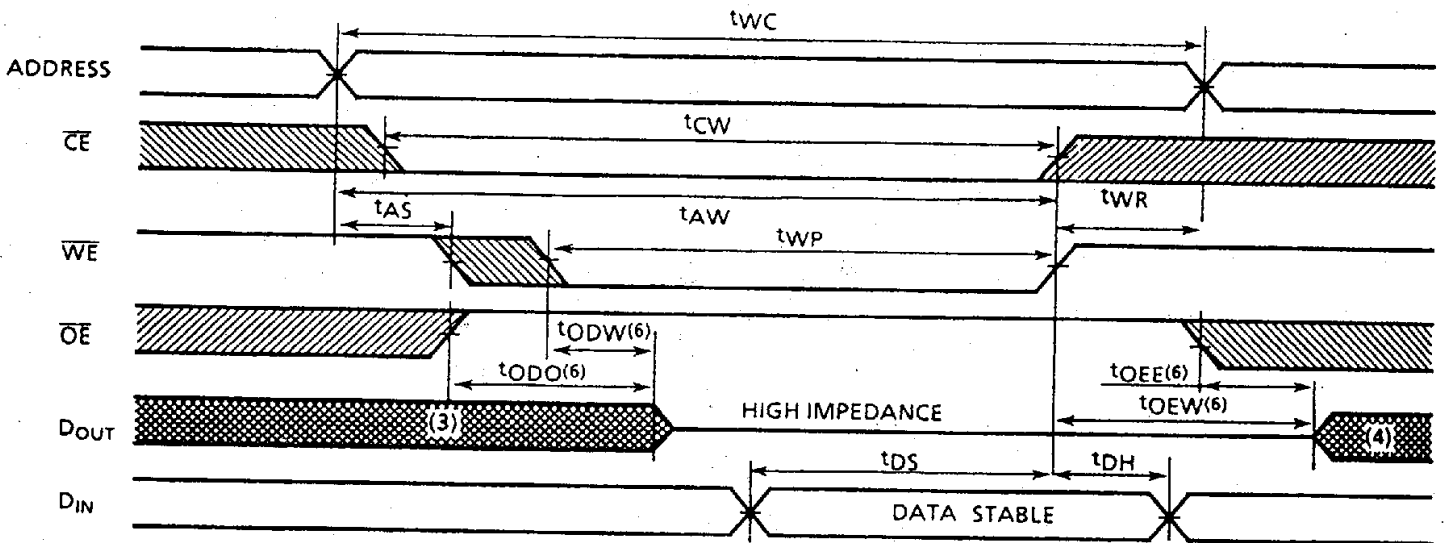
Figure 1.

Timing Waveforms

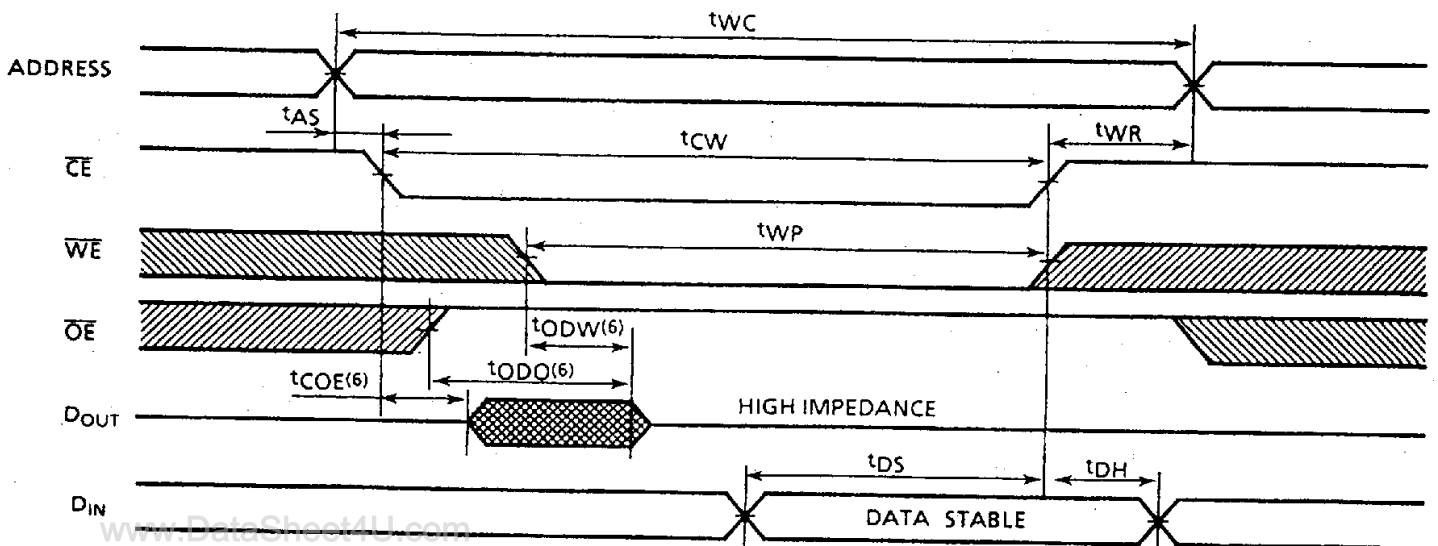
Read Cycle (2)



Write Cycle 1 (5) (\overline{WE} Controlled Write)



Write Cycle 2 (5) (\overline{CE} Controlled Write)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{OE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{OE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time

