

576-BIT BIPOLAR RAM (64 × 9)

82S09/82S19 (O.C.)

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DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/19 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

The 82S09/19 is available in the commercial and military temperature ranges. For the commercial temperature ranges (0°C to +75°C) specify N82S09/19, F or N and for the military temperature range (-55°C to +125°C) specify S82S09/19 I, R or F.

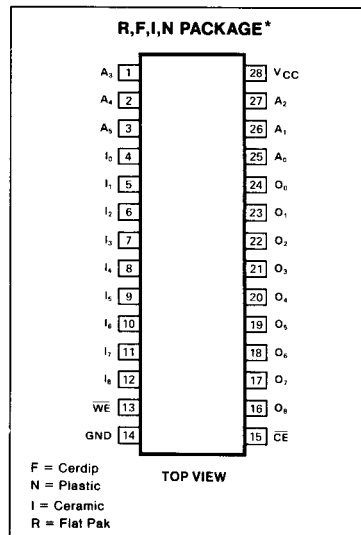
FEATURES

- **Address access time:**
 N82S09: 45ns max
 S82S09: 80ns max
 N82S19: 35ns max
 S82S19: 60ns max
- **Write cycle time:**
 N82S09/19: 45ns max
 S82S09: 80ns max
 S82S19: 70ns max
- **Power dissipation:** 1.3mW/bit typ
- **Input loading:**
 N82S09/19: -100µA max
 S82S09/19: -150µA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- 82S09 Output is Non-Blanked During Write
- 82S19 Output is Blanked During Write

APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

PIN CONFIGURATION

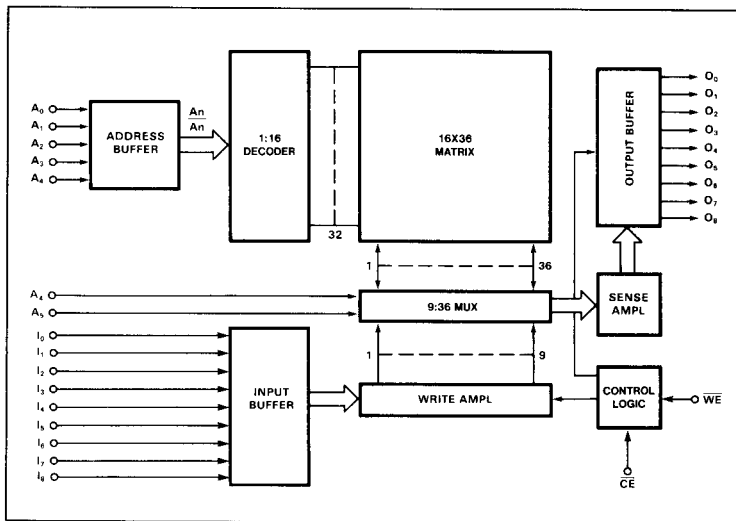


TRUTH TABLE

MODE	CE	WE	I _N	O _N	
				82S09	82S19
Read	0	1	X	Complement of data stored	
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	1
Disabled	1	X	X	1	1

X = Don't care

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

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PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	V _{dc}
V _{IN}	Input voltage	+5.5	V _{dc}
	Output voltage		V _{dc}
V _{OH}	High	+5.5	
T _A	Temperature range		°C
	Operating	0 to +75	
	N82S09/19	-55 to +125	
	S82S09/19	-65 to +150	
T _{STG}	Storage		

DC ELECTRICAL CHARACTERISTICS^{1,7}N82S09/19: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25VS82S09/19: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER ¹	TEST CONDITIONS	N82S09/19			S82S09/19			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp ²			.85	2.2		.80	V
		2.0		-1.5			-1.5	
V _{OL}	Output voltage Low ³			0.5			0.5	V
I _{IL} I _{IH}	Input current Low High			-100 25			-150 40	μA
I _{OLK}	Output current Leakage ⁴			40			60	μA
I _{CC}	V _{CC} supply current ⁵			190			200	mA
C _{IN} C _{OUT}	Capacitance Input Output		5 8			5 8		pF

Refer to notes on next page.

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AC ELECTRICAL CHARACTERISTICS⁷

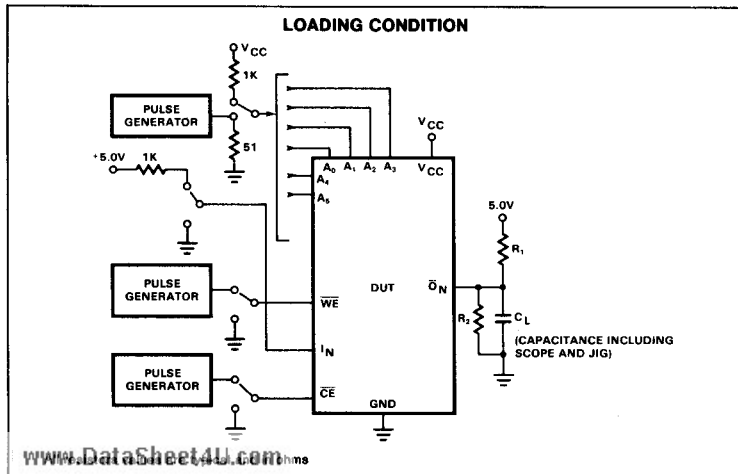
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, for 82S09
 $R_1 = 510\Omega$, $R_2 = 750\Omega$, $C_L = 30pF$, for 82S19
 N82S19: $0^\circ \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$
 S82S19: $-55^\circ C \leq T_A \leq +125^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S09			S82S09			N82S19			S82S19			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T _{AA} T _{CE}	Access time				45			80			35			60	ns
	Address				30			50			25			40	
T _{CD} T _{WD} T _{WR}	Disable time	Output			30			50			25			35	ns
	Valid time	Output			50			80			25			50	
	Write recovery time	Output	Chip enable											50	
T _{WSA} T _{WHA}	Setup and hold time	Write enable	Address	Setup time	5		10			5		10		ns	
	Hold time			5		20		5		10					
T _{WSD} T _{WHD}	Setup time	Write enable	Data in	Setup time	35		50			30		45	ns		
	Hold time			5		5		5		5					
T _{WSC} T _{WHC}	Setup time	Write enable	CE	Setup time	5		10			5		10	ns		
	Hold time			5		10		5		10					
T _{WP}	Pulse width			Write enable ⁶	35		50			35		50	ns		

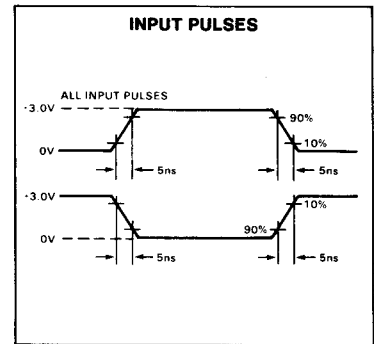
NOTES

- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
- Measured with V_{IH} applied to CE.
- I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
- Minimum required to guarantee a Write into the slowest bit.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



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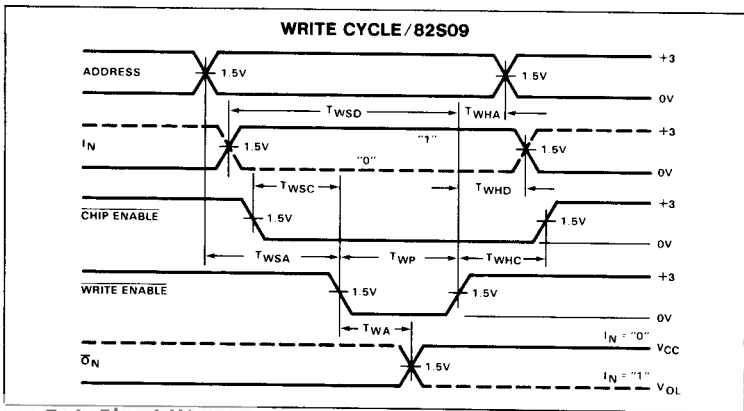
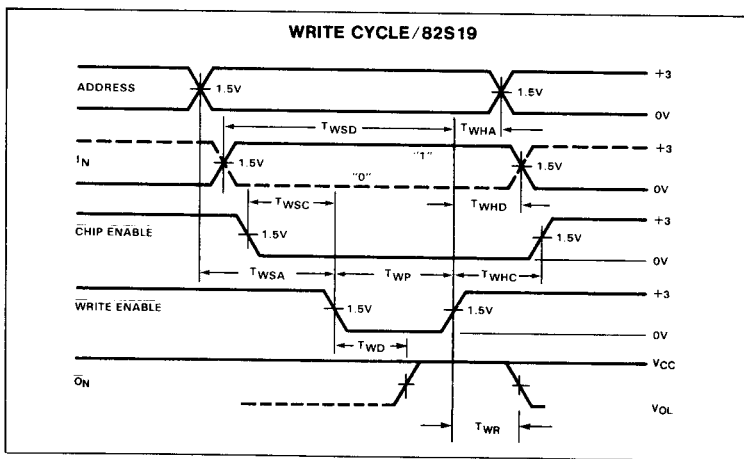
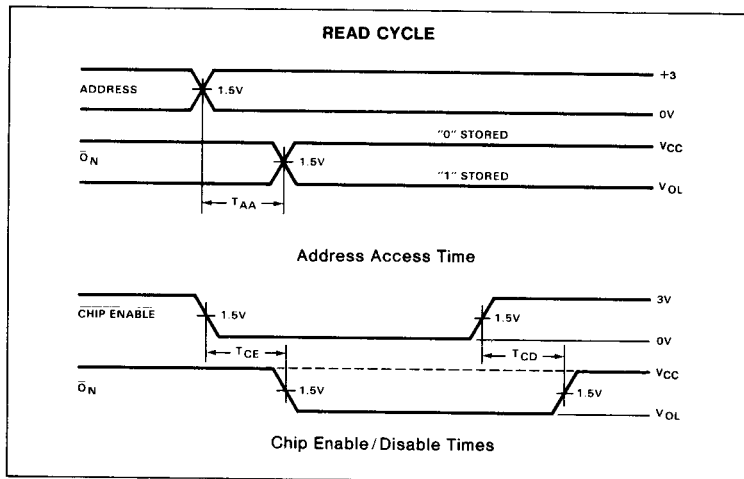
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TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{CE}** Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{CD}** Delay between when Chip Enable becomes high and Data Output is in off state.
- T_{AA}** Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC}** Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD}** Required delay between end of Write Enable pulse and end of valid Input Data.
- T_{WP}** Width of Write Enable pulse.
- T_{WSA}** Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD}** Required delay between beginning of valid Data Input and end of Write Enable pulse.
- T_{WD}** Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
- T_{WHC}** Required delay between end of Write Enable pulse and end of Chip Enable.
- T_{WHA}** Required delay between end of Write Enable pulse and end of valid Address.
- T_{WR}** Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
- T_{WA}** Delay between beginning of Write Enable pulse and when data output reflects complement of data input.