

K1526B & K1536B Series

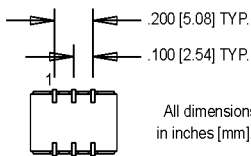
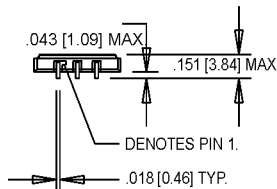
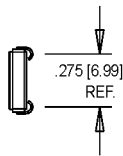
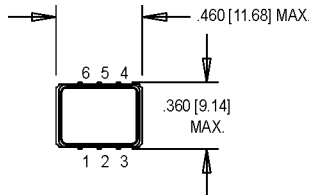
9x11 mm, 5.0 or 3.3 Volt, CMOS/TTL, VCXO



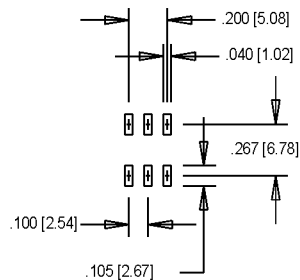
Ordering Information

	K15X6BX	X	X	00.0000 MHz
Product Series	K1526B = 5.0 Volt K1536B = 3.3 Volt			
Model Selection:	See Electrical Specs			
Temperature Range	Blank: 0°C to +70°C M: -40°C to +85°C			
Symmetry/Logic Compatibility	Blank: TTL/CMOS 40%/60% C: CMOS 45%/55% T: TTL 45%/55%			
Frequency (customer specified)				

- Former **Champion Technologies, Inc.** Product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Voltage Control
2	Tristate
3	Ground & Gnd Plane
4	Output
5	N/C
6	+Vdd

PARAMETER	Symbol				Units		
		K1526BA K1536BA	K1526BD K1536BD	K1526BE			
Model		K1526BA K1536BA	K1526BD K1536BD	K1526BE			
Frequency Range	F	2 to 55	55.1 to 80	2 to 55	2 to 40	MHz	
Frequency Stability: Overall	$\Delta F/F$	Inclusive of Calibration, Temperature, Voltage, Load, and Aging					
0°C to +70°C		±25	±40	±25	±32	ppm	
-40°C to +85°C		±50	±60	±50	±50	ppm	
Pullability Minimum		±100	±80	±80	±200	ppm	
Maximum		±150	±160	±130		ppm	
PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Operating Temperature	T _A	(See Ordering Information)					
Storage Temperature	T _s	-40		+125	°C		
Aging 1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz	
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz	
Control Voltage	V _c	0.5 0.3 0	2.5 1.65	4.5 3.0 5.0	V	K1526B K1536B K1526BE	
Linearity				10	%	Positive Monotonic Slope	
Modulation Bandwidth	f _m	20			kHz	+3 dB	
Input Impedance	Z _{in}	50k			Ohms	@ 10 kHz	
Input Voltage	V _{dd}	4.5 3.0	5.0 3.3	5.5 3.6	V	K1526B K1536B	
Input Current	I _{dd}			30	mA		
Output Type						CMOS/TTL	
Load				15	pF	HCMOS	
Symmetry (Duty Cycle)		(See Ordering Information)					
Logic "1" Level	V _{oh}	V _{dd} -0.5			V		
Logic "0" Level	V _{ol}			0.5	V		
Output Current				20	mA		
Rise/Fall Time	T _r /T _f			5	ns	20% to 80% V _{dd} , CL = 15 pF	
Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z					
Start up Time				10	ms		
Phase Jitter @ 26 MHz	φ _J		4		ps RMS	Integrated 12 kHz - 20 MHz	
Phase Noise (Typical) @ 26 MHz		100 Hz -65	1 kHz -95	10 kHz -115	100 kHz -130	100 kHz -140	Offset from carrier dBc/Hz

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