INTRODUCTION

The KS0711 is an LCD driver LSI for liquid crystal dot-matrix graphic display systems. It incorporates 198 driver circuits for 132 segments, 64 commons an icon-driving common, 65 × 132 × 2 bit-map RAM, and 4-level gray scale controller for enhanced graphics. It is capable of interfacing the microprocessor, accepting serial or 8-bit parallel display data directly from the microprocessor, and storing data in an on-chip display data RAM. In addition, the KS0711 can read and write display data RAM with minimum current consumption, as it does not require any external operation clocks. It also has LCD driving voltage generation circuits, such as the voltage converter, voltage regulator and voltage follower to reduce power consumption.

FEATURES

- **4-level (white, light gray, dark gray, black) gray scale display 9/12/15 PWM and 3/4 FRC method**

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Dark

(Accessible Column Address, n = 0, 1, 2,....., 129, 130, 131)

- **Driver outputs**
  - — Common outputs: 65 common
  - — Segment outputs: 132 segment
- **On-chip display data RAM**
  - — capacity: 65 × 132 × 2 = 17,160 bits
- **Multi-chip operation (master, slave) available**
- **Applicable duty-ratio**

Duty Ratio	Applicable LCD Bias	Maximum Display Area
1/65	1/9 or 1/7	65 × 132
1/49	1/8 or 1/6	49 × 132
1/33	1/7 or 1/5	33 × 132

- **Microprocessor interface**
  - — 8-bit parallel bidirectional interface with 6800-series or 8080-series
  - — Serial interface (only write operation) available
- **On-chip oscillator circuit**
- **On-chip low power supply for LCD driving voltage generation**
  - — Voltage converter (×2 / ×3 / ×4 / ×5)
  - — Voltage regulator (selective temperature coefficient)
  - — Voltage follower
- **On-chip electronic contrast control functions (64 steps)**

- **Operating voltage range**
  - — Supply voltage (V_{DD}): 2.4V to 5.5V
  - — LCD driving voltage (V_{LCD} = V0 – V_{SS}): 4.0V to 15.0V
- **Low power consumption**
  - — 150μA Max. (operation)
  - — 10μA Max. (standby mode)
- **Wide operating temperature range**
  - — Ta = – 40°C to 85°C
- **CMOS process**
- **Package**
  - — Slim chip for COG, and TCP available

BLOCK DIAGRAM

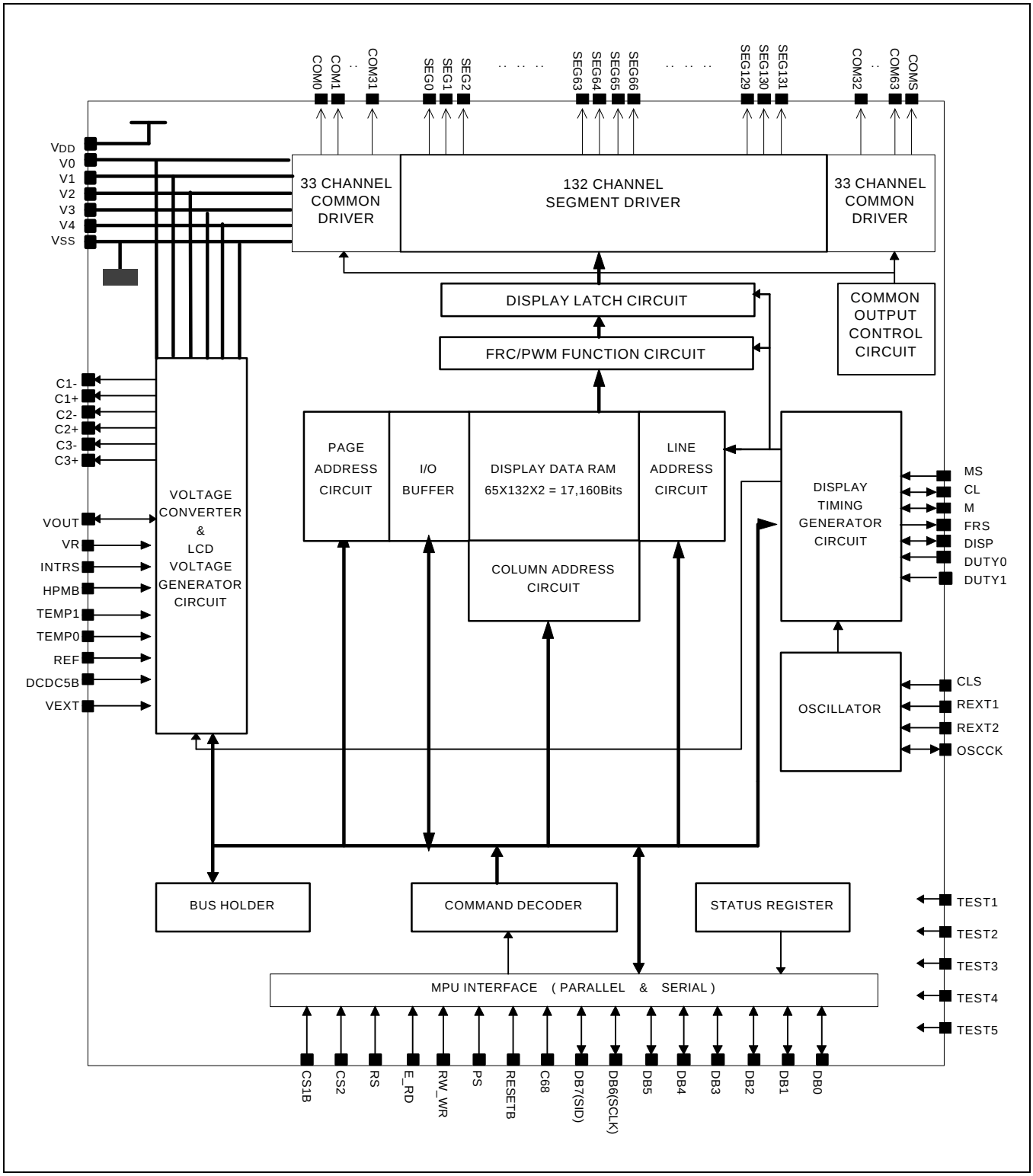


Figure 1. Block Diagram

PAD CONFIGURATION

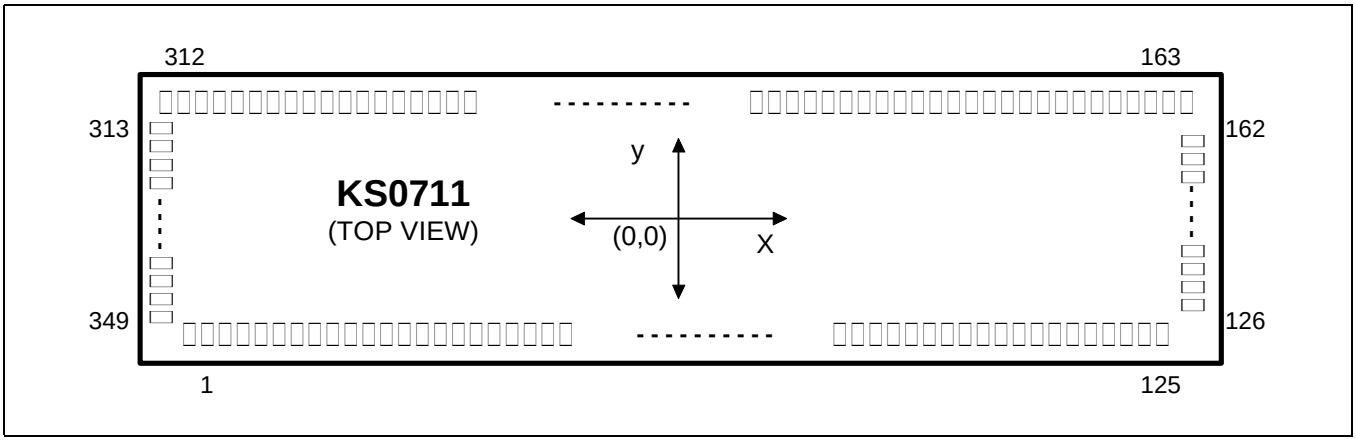


Figure 2. Pad Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	–	11690	3420	μm
Pad pitch	1 to 125	90		
	126 to 349	70		
Bumped pad size	1 to 125	56	114	
	126 to 162	108	50	
	163 to 312	50	108	
	313 to 349	108	50	
Bumped pad height	All pad	17 (Typ.)		

PAD LOCATION (NOT FIXED)

Table 1. Pad Location

[unit: μm]

Pad No	Pad Name	Coordinate		Pad No	Pad Name	Coordinate		Pad No	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	DUMMY	-5580	-1586	46	V_{SS}	-1530	-1586	91	VR	2520	-1586
2	DUMMY	-5490	-1586	47	V_{SS}	-1440	-1586	92	VR	2610	-1586
3	DUMMY	-5400	-1586	48	V_{SS}	-1350	-1586	93	V0	2700	-1586
4	DUMMY	-5310	-1586	49	V_{SS}	-1260	-1586	94	V0	2790	-1586
5	FRS	-5220	-1586	50	V_{SS}	-1170	-1586	95	V0	2880	-1586
6	M	-5130	-1586	51	V_{SS}	-1080	-1586	96	V0	2970	-1586
7	CL	-5040	-1586	52	V_{SS}	-990	-1586	97	V1	3060	-1586
8	DISP	-4950	-1586	53	V_{DD}	-900	-1586	98	V1	3150	-1586
9	V_{SS}	-4860	-1586	54	V_{DD}	-810	-1586	99	V2	3240	-1586
10	CS1B	-4770	-1586	55	V_{DD}	-720	-1586	100	V2	3330	-1586
11	CS2	-4680	-1586	56	V_{DD}	-630	-1586	101	V3	3420	-1586
12	V_{DD}	-4590	-1586	57	V_{DD}	-540	-1586	102	V3	3510	-1586
13	RESETB	-4500	-1586	58	V_{DD}	-450	-1586	103	V4	3600	-1586
14	RS	-4410	-1586	59	V_{DD}	-360	-1586	104	V4	3690	-1586
15	V_{SS}	-4320	-1586	60	V_{DD}	-270	-1586	105	V_{SS}	3780	-1586
16	RW_WR	-4230	-1586	61	VOUT	-180	-1586	106	V_{SS}	3870	-1586
17	E_RD	-4140	-1586	62	VOUT	-90	-1586	107	OSCCK	3960	-1586
18	V_{DD}	-4050	-1586	63	VOUT	0	-1586	108	DCDC5B	4050	-1586
19	C68	-3960	-1586	64	VOUT	90	-1586	109	V_{DD}	4140	-1586
20	PS	-3870	-1586	65	C3+	180	-1586	110	HPMB	4230	-1586
21	V_{SS}	-3780	-1586	66	C3+	270	-1586	111	INTRS	4320	-1586
22	REF	-3690	-1586	67	C3+	360	-1586	112	V_{SS}	4410	-1586
23	DUMMY	-3600	-1586	68	C3+	450	-1586	113	TEMP0	4500	-1586
24	DUMMY	-3510	-1586	69	C3-	540	-1586	114	TEMP1	4590	-1586
25	V_{DD}	-3420	-1586	70	C3-	630	-1586	115	V_{DD}	4680	-1586
26	DB0	-3330	-1586	71	C3-	720	-1586	116	REXT1	4770	-1586
27	DB1	-3240	-1586	72	C3-	810	-1586	117	REXT2	4860	-1586
28	DB2	-3150	-1586	73	C1+	900	-1586	118	VSS	4950	-1586
29	DB3	-3060	-1586	74	C1+	990	-1586	119	TEST3	5040	-1586
30	DB4	-2970	-1586	75	C1+	1080	-1586	120	TEST4	5130	-1586
31	DB5	-2880	-1586	76	C1+	1170	-1586	121	TEST5	5220	-1586
32	DB6	-2790	-1586	77	C1-	1260	-1586	122	DUMMY	5310	-1586
33	DB7	-2700	-1586	78	C1-	1350	-1586	123	DUMMY	5400	-1586
34	V_{SS}	-2610	-1586	79	C1-	1440	-1586	124	DUMMY	5490	-1586
35	TEST1	-2520	-1586	80	C1-	1530	-1586	125	DUMMY	5580	-1586
36	TEST2	-2430	-1586	81	C2+	1620	-1586	126	DUMMY	5669	-1330
37	V_{DD}	-2340	-1586	82	C2+	1710	-1586	127	DUMMY	5669	-1260
38	DUTY0	-2250	-1586	83	C2+	1800	-1586	128	DUMMY	5669	-1190
39	DUTY1	-2160	-1586	84	C2+	1890	-1586	129	COMS	5669	-1120
40	V_{SS}	-2070	-1586	85	C2-	1980	-1586	130	COM0	5669	-1050
41	MS	-1980	-1586	86	C2-	2070	-1586	131	COM1	5669	-980
42	CLS	-1890	-1586	87	C2-	2160	-1586	132	COM2	5669	-910
43	V_{DD}	-1800	-1586	88	C2-	2250	-1586	133	COM3	5669	-840
44	VEXT	-1710	-1586	89	V_{SS}	2340	-1586	134	COM4	5669	-770
45	V_{SS}	-1620	-1586	90	V_{SS}	2430	-1586	135	COM5	5669	-700

Table 1. Pad Location (Continued)

[unit: μm]

Pad No	Pad Name	Coordinate		Pad No	Pad Name	Coordinate		Pad No	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
136	COM6	5669	-630	186	SEG14	3605	1534	236	SEG64	105	1534
137	COM7	5669	-560	187	SEG15	3535	1534	237	SEG65	35	1534
138	COM8	5669	-490	188	SEG16	3465	1534	238	SEG66	-35	1534
139	COM9	5669	-420	189	SEG17	3395	1534	239	SEG67	-105	1534
140	COM10	5669	-350	190	SEG18	3325	1534	240	SEG68	-175	1534
141	COM11	5669	-280	191	SEG19	3255	1534	241	SEG69	-245	1534
142	COM12	5669	-210	192	SEG20	3185	1534	242	SEG70	-315	1534
143	COM13	5669	-140	193	SEG21	3115	1534	243	SEG71	-385	1534
144	COM14	5669	-70	194	SEG22	3045	1534	244	SEG72	-455	1534
145	COM15	5669	0	195	SEG23	2975	1534	245	SEG73	-525	1534
146	COM16	5669	70	196	SEG24	2905	1534	246	SEG74	-595	1534
147	COM17	5669	140	197	SEG25	2835	1534	247	SEG75	-665	1534
148	COM18	5669	210	198	SEG26	2765	1534	248	SEG76	-735	1534
149	COM19	5669	280	199	SEG27	2695	1534	249	SEG77	-805	1534
150	COM20	5669	350	200	SEG28	2625	1534	250	SEG78	-875	1534
151	COM21	5669	420	201	SEG29	2555	1534	251	SEG79	-945	1534
152	COM22	5669	490	202	SEG30	2485	1534	252	SEG80	-1015	1534
153	COM23	5669	560	203	SEG31	2415	1534	253	SEG81	-1085	1534
154	COM24	5669	630	204	SEG32	2345	1534	254	SEG82	-1155	1534
155	COM25	5669	700	205	SEG33	2275	1534	255	SEG83	-1225	1534
156	COM26	5669	770	206	SEG34	2205	1534	256	SEG84	-1295	1534
157	COM27	5669	840	207	SEG35	2135	1534	257	SEG85	-1365	1534
158	COM28	5669	910	208	SEG36	2065	1534	258	SEG86	-1435	1534
159	COM29	5669	980	209	SEG37	1995	1534	259	SEG87	-1505	1534
160	COM30	5669	1050	210	SEG38	1925	1534	260	SEG88	-1575	1534
161	COM31	5669	1120	211	SEG39	1855	1534	261	SEG89	-1645	1534
162	DUMMY	5669	1190	212	SEG40	1785	1534	262	SEG90	-1715	1534
163	DUMMY	5215	1534	213	SEG41	1715	1534	263	SEG91	-1785	1534
164	DUMMY	5145	1534	214	SEG42	1645	1534	264	SEG92	-1855	1534
165	DUMMY	5075	1534	215	SEG43	1575	1534	265	SEG93	-1925	1534
166	DUMMY	5005	1534	216	SEG44	1505	1534	266	SEG94	-1995	1534
167	DUMMY	4935	1534	217	SEG45	1435	1534	267	SEG95	-2065	1534
168	DUMMY	4865	1534	218	SEG46	1365	1534	268	SEG96	-2135	1534
169	DUMMY	4795	1534	219	SEG47	1295	1534	269	SEG97	-2205	1534
170	DUMMY	4725	1534	220	SEG48	1225	1534	270	SEG98	-2275	1534
171	DUMMY	4655	1534	221	SEG49	1155	1534	271	SEG99	-2345	1534
172	SEG0	4585	1534	222	SEG50	1085	1534	272	SEG100	-2415	1534
173	SEG1	4515	1534	223	SEG51	1015	1534	273	SEG101	-2485	1534
174	SEG2	4445	1534	224	SEG52	945	1534	274	SEG102	-2555	1534
175	SEG3	4375	1534	225	SEG53	875	1534	275	SEG103	-2625	1534
176	SEG4	4305	1534	226	SEG54	805	1534	276	SEG104	-2695	1534
177	SEG5	4235	1534	227	SEG55	735	1534	277	SEG105	-2765	1534
178	SEG6	4165	1534	228	SEG56	665	1534	278	SEG106	-2835	1534
179	SEG7	4095	1534	229	SEG57	595	1534	279	SEG107	-2905	1534
180	SEG8	4025	1534	230	SEG58	525	1534	280	SEG108	-2975	1534
181	SEG9	3955	1534	231	SEG59	455	1534	281	SEG109	-3045	1534
182	SEG10	3885	1534	232	SEG60	385	1534	282	SEG110	-3115	1534
183	SEG11	3815	1534	233	SEG61	315	1534	283	SEG111	-3185	1534
184	SEG12	3745	1534	234	SEG62	245	1534	284	SEG112	-3255	1534
185	SEG13	3675	1534	235	SEG63	175	1534	285	SEG113	-3325	1534

Table 1. Pad Location (Continued)

[unit: μm]

Pad No	Pad Name	Coordinate		Pad No	Pad Name	Coordinate		Pad No	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
286	SEG114	-3395	1534	308	DUMMY	-4935	1534	330	COM48	-5669	0
287	SEG115	-3465	1534	309	DUMMY	-5005	1534	331	COM47	-5669	-70
288	SEG116	-3535	1534	310	DUMMY	-5075	1534	332	COM46	-5669	-140
289	SEG117	-3605	1534	311	DUMMY	-5145	1534	333	COM45	-5669	-210
290	SEG118	-3675	1534	312	DUMMY	-5215	1534	334	COM44	-5669	-280
291	SEG119	-3745	1534	313	DUMMY	-5669	1190	335	COM43	-5669	-350
292	SEG120	-3815	1534	314	COMS	-5669	1120	336	COM42	-5669	-420
293	SEG121	-3885	1534	315	COM63	-5669	1050	337	COM41	-5669	-490
294	SEG122	-3955	1534	316	COM62	-5669	980	338	COM40	-5669	-560
295	SEG123	-4025	1534	317	COM61	-5669	910	339	COM39	-5669	-630
296	SEG124	-4095	1534	318	COM60	-5669	840	340	COM38	-5669	-700
297	SEG125	-4165	1534	319	COM59	-5669	770	341	COM37	-5669	-770
298	SEG126	-4235	1534	320	COM58	-5669	700	342	COM36	-5669	-840
299	SEG127	-4305	1534	321	COM57	-5669	630	343	COM35	-5669	-910
300	SEG128	-4375	1534	322	COM56	-5669	560	344	COM34	-5669	-980
301	SEG129	-4445	1534	323	COM55	-5669	490	345	COM33	-5669	-1050
302	SEG130	-4515	1534	324	COM54	-5669	420	346	COM32	-5669	-1120
303	SEG131	-4585	1534	325	COM53	-5669	350	347	DUMMY	-5669	-1190
304	DUMMY	-4655	1534	326	COM52	-5669	280	348	DUMMY	-5669	-1260
305	DUMMY	-4725	1534	327	COM51	-5669	210	349	DUMMY	-5669	-1330
306	DUMMY	-4795	1534	328	COM50	-5669	140				
307	DUMMY	-4865	1534	329	COM49	-5669	70				

PIN DESCRIPTIONS

Table 2. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship:

V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS

When the internal power circuit is active, these voltages are generated as shown in the following table, according to the state of LCD Bias.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 Bias</td><td>(8/9) V0</td><td>(7/9) V0</td><td>(2/9) V0</td><td>(1/9) V0</td></tr>
<tr><td>1/8 Bias</td><td>(7/8) V0</td><td>(6/8) V0</td><td>(2/8) V0</td><td>(1/8) V0</td></tr>
<tr><td>1/7 Bias</td><td>(6/7) V0</td><td>(5/7) V0</td><td>(2/7) V0</td><td>(1/7) V0</td></tr>
<tr><td>1/6 Bias</td><td>(5/6) V0</td><td>(4/6) V0</td><td>(2/6) V0</td><td>(1/6) V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>C1–</td><td>I</td><td>Capacitor 1– negative connection pin for voltage converter</td></tr>
<tr><td>C1+</td><td>I</td><td>Capacitor 1+ positive connection pin for voltage converter</td></tr>
<tr><td>C2–</td><td>I</td><td>Capacitor 2– negative connection pin for voltage converter</td></tr>
<tr><td>C2+</td><td>I</td><td>Capacitor 2+ positive connection pin for voltage converter</td></tr>
<tr><td>C3–</td><td>I</td><td>Capacitor 3– negative connection pin for voltage converter</td></tr>
<tr><td>C3+</td><td>I</td><td>Capacitor 3+ positive connection pin for voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter output</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjust pin which is valid only when on-chip registers are not used</td></tr>
<tr><td>DCDC5B</td><td>I</td><td>5-times boosting circuit enable input pin. When this pin is low in 4-times boosting circuit, the 5-times boosted voltage appears at VOUT</td></tr>
<tr><td>REXT1,
REXT2</td><td>I</td><td>When using an internal clock oscillator, connect a register between REXT1 and REXT2.</td></tr>
<tr><td>VEXT</td><td>I</td><td>External VREF input terminal for the LCD power supply voltage regulator.</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">System Control</td></tr>
<tr><td>MS</td><td>I</td><td>Master/slave mode select input. Master makes some signals for display, and slave receives them. This is for display synchronization.
MS = “H”: Master mode
MS = “L”: Slave mode

<table><tr><th>MS</th><th>OSC Circuit</th><th>Power Supply Cicuit</th><th>CL</th><th>M</th><th>DISP</th></tr><tr><td>H</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td></tr><tr><td>L</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Input</td></tr></table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin.
CLS = “H”: Enable
CLS = “L”: Disable (External display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output. When KS0711 is used in master/slave mode (multi-chip), the CL pins must be connected to each other.
MS = “H”: output
MS = “L”: input</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input / input. When KS0711 is used in master/slave mode (multi-chip), the M pins must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver output. This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output. When KS0711 is used in master/slave mode (multi-chip), the DISP pins must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>REF</td><td>I</td><td>Selects the external VREF voltage via the VEXT terminal.
REF = “H”: using the Internal VREF
REF = “L”: using the external VREF</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal Resistor Select.

This pin selects the resistors for adjusting V0 voltage level and is available only in master mode.
INTRS = “H”: using built-in resistors,
INTRS = “L”: not using built-in resistors. V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power control pin of the power supply circuit for LCD driver.
HPMB = “L”: High power mode
HPMB = “H”: Normal mode

This pin is available only in master mode.</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>TEMP1
TEMP0</td><td>I</td><td>Selects the temperature coefficient of the reference voltage.
<table>
<tr><th>TEMP1</th><th>TEMP0</th><th>Temperature Coefficient</th></tr>
<tr><td>H</td><td>H</td><td>TBD</td></tr>
<tr><td>H</td><td>L</td><td>TBD</td></tr>
<tr><td>L</td><td>H</td><td>TBD</td></tr>
<tr><td>L</td><td>L</td><td>TBD</td></tr>
</table></td></tr>
<tr><td>DUTY1
DUTY0</td><td>I</td><td>The LCD driver duty ratio depends on the following table.
<table>
<tr><th>DUTY1</th><th>DUTY0</th><th>Duty Ratio</th></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L</td><td>1/65</td></tr>
<tr><td>H</td><td>H</td><td>1/65</td></tr>
</table></td></tr>
<tr><td>OSCCK</td><td>I/O</td><td>Oscillator clock input / output.
<table>
<tr><th>MS</th><th>CLS</th><th>OSCCK</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td></tr>
<tr><td>L</td><td>Input</td></tr>
<tr><td>L</td><td>–</td><td>Input</td></tr>
</table></td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Microprocessor Interface</td></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin. When RESETB is low, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel/Serial data input select input
<table>
<tr><th>PS</th><th>Operating Mode</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data Input/Output</th><th>Read/ Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RD, RW_WR</td><td>–</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>DB7(SID)</td><td>Write Only</td><td>DB6 (SCLK)</td></tr>
</table>
NOTE: In serial mode, it is impossible to read data from the on-chip RAM. DB0 to DB5 is high impedance and E_RD and RW_WR must be fixed on high or low.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor interface select input in parallel mode.
C68 = “H”: 6800-series MPU interface
C68 = “L”: 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select inputs.

Data input / output is enabled only when CS1B is low and CS2 is high. When chip select is non-active, DB0 to DB7 will be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input.
RS = “H”: Then data on DB0 to DB7 is display data
RS = “L”: Then data on DB0 to DB7 is control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>When interfacing to a 6800-series MPU, Read/Write is enable.
RW_WR = “H”: Read
RW_WR = “L”: Write

When interfacing to a 8080-series MPU, RW_WR is enable at low.</td></tr>
<tr><td>E_RD</td><td>I</td><td>When interfacing to a 6800-series MPU: Active High.
This is used as an enable clock input pin of the 6800-series MPU.

When interfacing to an 8080-series MPU: Active Low.
This input connects the RD signal of the 8080-series MPU. While this signal is low, KS0711 data bus output is enabled.</td></tr>
<tr><td>DB0 to DB7</td><td>I/O</td><td>8-bit bidirectional data bus. It is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”):
DB7: Serial input data (SID)
DB6: Serial input clock (SCLK)
DB0 to DB5: High impedance.

When chip select is not active, DB0 to DB7 will be high impedance.</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">LCD Driver Outputs</td></tr>
<tr><td>SEG0 to SEG131</td><td>O</td><td>LCD driver output for segment. The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td></tr>
<tr><td>COM0 to COM63</td><td>O</td><td>LCD driver output for segment. The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th>Display Data</th><th>M</th><th>COMs Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons. The output signals of two pins are the same. When not used, these pins should be left open. In multi-chip (master / slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
<tr><td colspan="3">Test Pin</td></tr>
<tr><td>TEST1 to TEST5</td><td>I</td><td>IC test pins
TEST1 to TEST2 pins: High
TEST3 to TEST5 pins: Open</td></tr>
</table>

FUNCTION DESCRIPTION

MICROPROCESSOR INTERFACE

CHIP SELECT INPUT

There are CS1B and CS2 pins for chip selection. The KS0711 can interface with a microprocessor only when CS1B is low and CS2 is high. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. Also, in the case of serial interface, the internal shift register and the counter are reset.

PARALLEL / SERIAL INTERFACE

The KS0711 has three types of interface with MPU, one serial and two parallel. This parallel or serial interface is determined by PS pin as shown in Table 3.

Table 3. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C68	Interface Mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	(NOTE)	Serial-mode

NOTE: Don't care

Parallel Interface (PS = "H")

The 8-bit bidirectional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in Table 4. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 5.

Table 4. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU Bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	RD	WR	DB0 to DB7	8080-series

Table 5. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (RD)	RW_WR (WR)	
H	H	H	L	H	Display data read
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (Instruction)

Serial Interface (PS = "L")

When KS0711 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. When not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of the serial clock going into DB6 and is processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easily affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

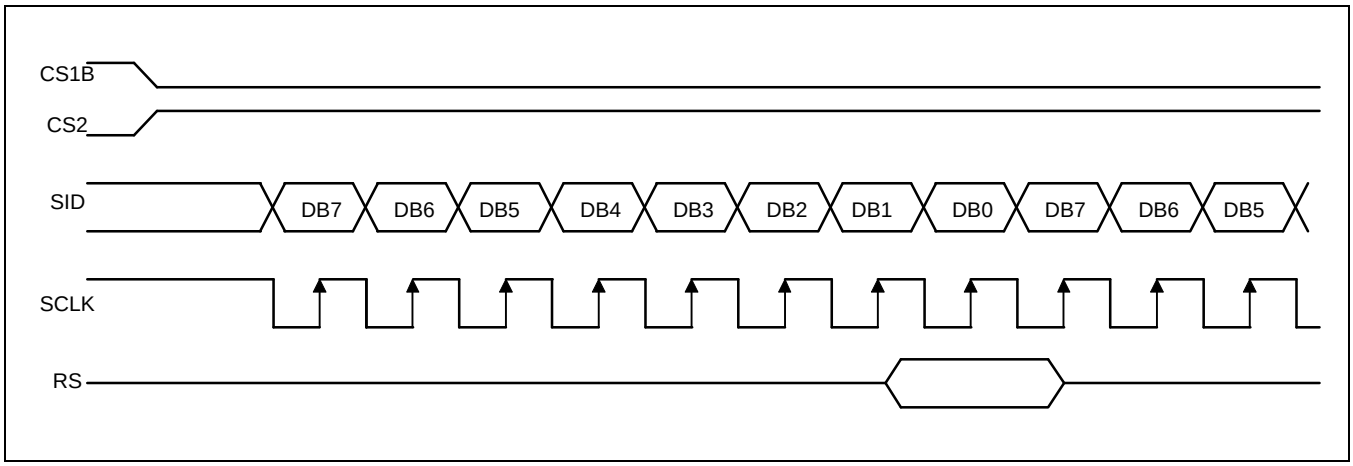


Figure 3. Serial Interface Timing

BUSY FLAG

The busy flag indicates whether the KS0711 is operating or not. When DB7 is high in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor does not need to check this flag before each instruction, which improves microprocessor performance.

DATA TRANSFER

The KS0711 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to the on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure4. When reading data from the on-chip RAM to MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and MPU reads this stored data from the bus holder for the next data read cycle, as shown in Figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

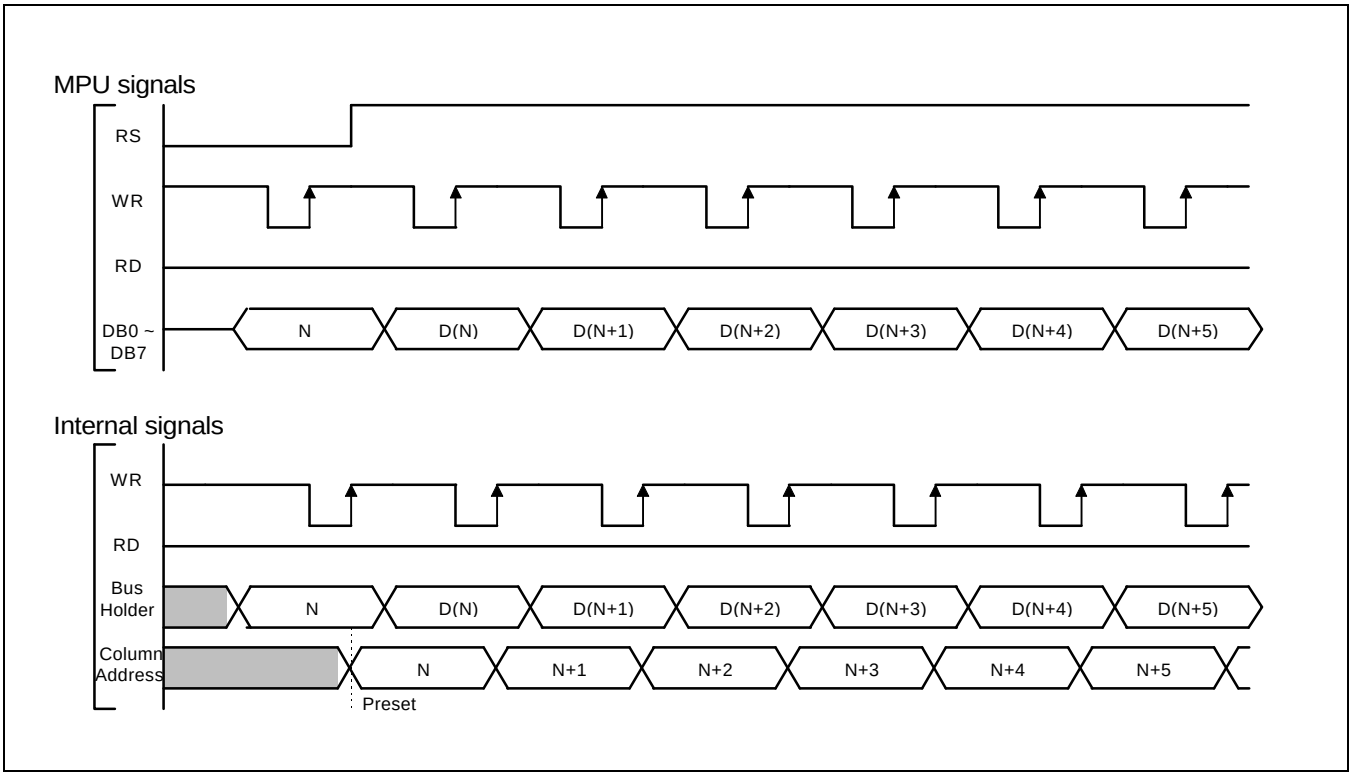


Figure 4. Write Timing

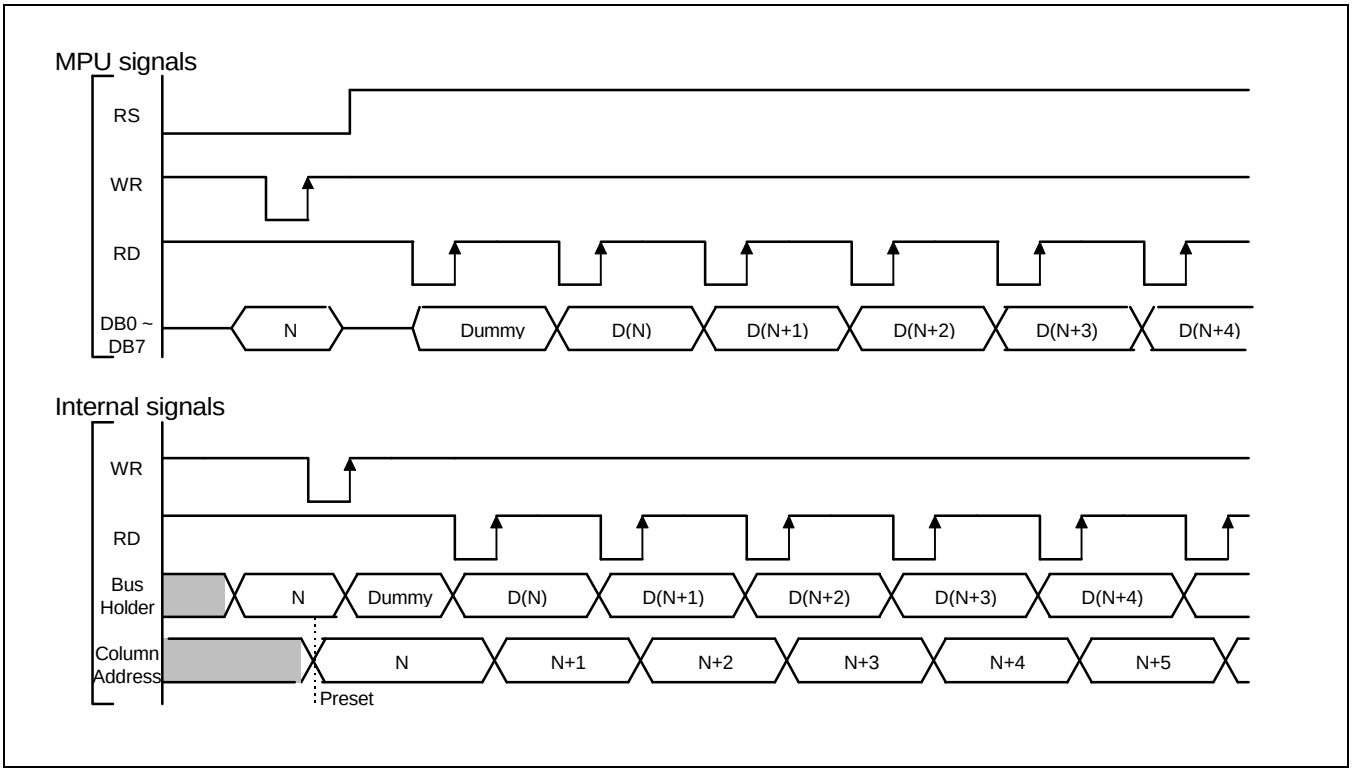


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The display data RAM stores pixel data for the LCD. It is a 65-row ((8 page by 8 bits) + 1) by 264-column addressable array. Each pixel can be selected when the page and column address is specified. The 65 rows are divided into 8 pages with 8 lines each, and a ninth page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines.

The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as when data is being displayed, without causing the LCD to flicker.

PAGE ADDRESS CIRCUIT

This circuit is for providing a page address to the display data RAM shown in Table 7. It incorporates a 4-bit page address register changed only by the set page instruction. Page address 8 (DB3 is high, but DB2, DB1 and DB0 are low) is a special RAM area for icons, and only display data DB0 is valid. When page address is above 8, it is impossible to access the on-chip RAM.

LINE ADDRESS CIRCUIT

This circuit assigns DDRAM a line address corresponding to the first line (COM1) of the display. Therefore, by setting the line address repeatedly, it is possible to scroll the screen and switch the page without changing the contents of the on-chip RAM (refer to Table 7). It incorporates a 6-bit Line Address register which can only be changed by the Initial display line instruction and a 6-bit counter circuit. At the beginning of each LCD frame, the contents of a register are copied to the line counter which is increased by the CL signal, and generates the line address for transferring the 264-bit RAM data to the 100 display data latch circuit. However, display data of icons are not scrolled because the microprocessor cannot access the line address of icons.

COLUMN ADDRESS CIRCUIT

The column address circuit has a 9-bit preset counter that provides the column address to the display data RAM (Shown in Table 7). When set column address MSB / LSB instruction is issued, 8 bits [Y8:Y1] are set and lowest bit, Y0 is set to “0”. Since this address is increased by 1 at every read or write data instruction, the microprocessor can access the display data continuously. However, the counter is not increased and locked for a non-existing address above 108H. It is unlocked if a column address is set again by the set column address MSB / LSB instruction. The column address counter is independent of the page address register.
ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. Refer to Table 6.

Table 6. Segment Output Direction According to ADC

SEG Output	**SEG 0**		**SEG 1**		**SEG 2**		**SEG 3**		**.....**	**SEG 128**		**SEG 129**		**SEG 130**		**SEG 131**	
Column address [Y8:Y1]	00H		01H		02H		03H		.....	80H		81H		82H		83H	
Internal column address [Y8:Y1]	000 HEX	001 HEX	002 HEX	003 HEX	004 HEX	005 HEX	006 HEX	007 HEX	.....	100 HEX	101 HEX	102 HEX	103 HEX	104 HEX	105 HEX	106 HEX	107 HEX
Display data (ADC=0)	1	1	1	0	0	0	0	1	.....	1	0	1	1	0	0	0	1
LCD panel display									.....								
ADC=1	0	1	0	0	1	1	1	0	.....	0	1	0	0	1	0	1	1
LCD panel display																	

Table 7. Display Data RAM Addressing

Page Address P3, P2, P1, P0				Data	Column Address													Line Address (HEX)	Common Output (1/65)	Common Output (1/49)	Common Output (1/33)
0	0	0	0	DB0							Page0							00	COM36	COM36	–
				DB1														01	COM37	COM37	–
				DB2														02	COM38	COM38	–
				DB3														03	COM39	COM39	–
				DB4														04	COM40	COM40	–
				DB5														05	COM41	COM41	–
				DB6														06	COM42	COM42	–
				DB7														07	COM43	COM43	–
0	0	0	1	DB0							Page1							08	COM44	COM44	–
				DB1														09	COM45	COM45	–
				DB2														0A	COM46	COM46	–
				DB3														0B	COM47	COM47	–
				DB4														0C	COM48	–	–
				DB5														0D	COM49	–	–
				DB6														0E	COM50	–	–
				DB7														0F	COM51	–	–
0	0	1	0	DB0							Page2							10	COM52	–	–
				DB1														11	COM53	–	–
				DB2														12	COM54	–	–
				DB3														13	COM55	–	–
				DB4														14	COM56	–	–
				DB5														15	COM57	–	–
				DB6														16	COM58	–	–
				DB7														17	COM59	–	–
0	0	1	1	DB0							Page3							18	COM60	–	–
				DB1														19	COM61	–	–
				DB2														1A	COM62	–	–
				DB3														1B	COM63	–	–
				DB4														1C	COM0	COM0	COM0
				DB5														1D	COM1	COM1	COM1
				DB6														1E	COM2	COM2	COM2
				DB7														1F	COM3	COM3	COM3
0	1	0	0	DB0							Page4							20	COM4	COM4	COM4
				DB1														21	COM5	COM5	COM5
				DB2														22	COM6	COM6	COM6
				DB3														23	COM7	COM7	COM7
				DB4														24	COM8	COM8	COM8
				DB5														25	COM9	COM9	COM9
				DB6														26	COM10	COM10	COM10
				DB7														27	COM11	COM11	COM11
0	1	0	1	DB0							Page5							28	COM12	COM12	COM12
				DB1														29	COM13	COM13	COM13
				DB2														2A	COM14	COM14	COM14
				DB3														2B	COM15	COM15	COM15
				DB4														2C	COM16	COM16	COM16
				DB5														2D	COM17	COM17	COM17
				DB6														2E	COM18	COM18	COM18
				DB7														2F	COM19	COM19	COM19

Table 7. Display Data RAM Addressing (Continued)

Page Address P3, P2, P1, P0				Data	Column Address												Line Address (HEX)	Common Output (1/65)	Common Output (1/49)	Common Output (1/33)
0	1	1	0	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page6							30 31 32 33 34 35 36 37	COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27	COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27	COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27
0	1	1	1	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page7							38 39 3A 3B 3C 3D 3E 3F	COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35	COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35	COM28 COM29 COM30 COM31 – – – –
1	0	0	0	DB0							Page8								COMS	COMS	COMS
Column Address [HEX]				ADC = 0	00		01		02		MPU Accessible column address (Y8~Y1)	81		82		83					
					000	001	002	003	004	005	Internal column address (Y8~Y0)	102	103	104	105	106	107				
				ADC = 1	83		82		81		MPU Accessible column address (Y8~Y1)	02		01		00					
					106	107	104	105	102	103	Internal column address (Y8~Y1)	004	005	002	003	000	001				
LCD OUTPUT					SEG 0		SEG 1		SEG 2		–	SEG 129		SEG 130		SEG 131					

NOTE: When the initial display line address is 1CH.

LCD DRIVING CIRCUIT

OSCILLATOR

This is a completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

DISPLAY TIMING GENERATOR CIRCUIT

This circuit generates some signals to be used in the LCD. The display clock CL generates a clock to the line counter and a latch signal to the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL) and the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. 2-frame AC driver waveforms and the internal timing signal are shown in Figure 6.

When KS0711 is used in multi-chip mode, the slave chip needs to receive the M, CL, DISP signals from the master. Table 8 shows the M, CL, and DISP status.

Table 8. Master and Slave Timing Signal Status

Operation Mode	Oscillator ON / OFF	M	CL	DISP
Master	ON (Internal clock used)	Output	Output	Output
	OFF (External clock used)	Output	Input	Output
Slave	–	Input	Input	Input

DISPLAY DATA LATCH CIRCUIT

This latch circuit temporarily stores the output display data from the display data RAM to the LCD driver in each instruction period. This latch circuit is controlled by the display ON / OFF, Reverse display ON / OFF and entire display ON / OFF instructions, and the data in the display data RAM remains unchanged.

FRC (FRAME RATE CONTROL) AND PWM (PULSE WIDTH MODULATION) FUNCTION CIRCUIT

The KS0711 incorporates an FRC function and a PWM function circuit to display a four-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The KS0711 provides 4 4-bit palette-registers to assign the desired gray level. These registers are set by the instructions and RESETB.

— Gray scale table of 4 FRC (Frame Rate Control)

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

— Gray scale table of 3 FRC (Frame Rate Control)

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	X X X X	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	X X X X	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	X X X X	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	X X X X	3rd FR (FR3)

— Gray scale table of 15 PWM (Pulse Width Modulation)

	Hex	4-Bits	PWM (on width)	Note
0	00	0000	0 (0/15)	
1	01	0001	1/15	
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	
11	0B	1011	11/15	
12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1(15/15)	

— Gray scale table of 12 PWM (Pulse Width Modulation)

	Hex	4-Bits	PWM (on width)	Note
0	00	0000	0 (0/12)	
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	

	Hex	4-Bits	PWM (on width)	Note
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1(12/12)	
13	0D	1101	0/12	(NOTE)
14	0E	1110	0/12	(NOTE)
15	0F	1111	0/12	(NOTE)

NOTE: This area is selected to off level (0/12 level).

— Gray scale table of 9 PWM (Pulse Width Modulation)

	Hex	4-Bits	PWM (on width)	Note
0	00	0000	0 (0/9)	
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1(9/9)	
10	0A	1010	0/9	(NOTE)
11	0B	1011	0/9	(NOTE)
12	0C	1100	0/9	(NOTE)
13	0D	1101	0/9	(NOTE)
14	0E	1110	0/9	(NOTE)
15	0F	1111	0/9	(NOTE)

NOTE: This area is selected to off level (0/9 level).

Duty Ratio: 1/65

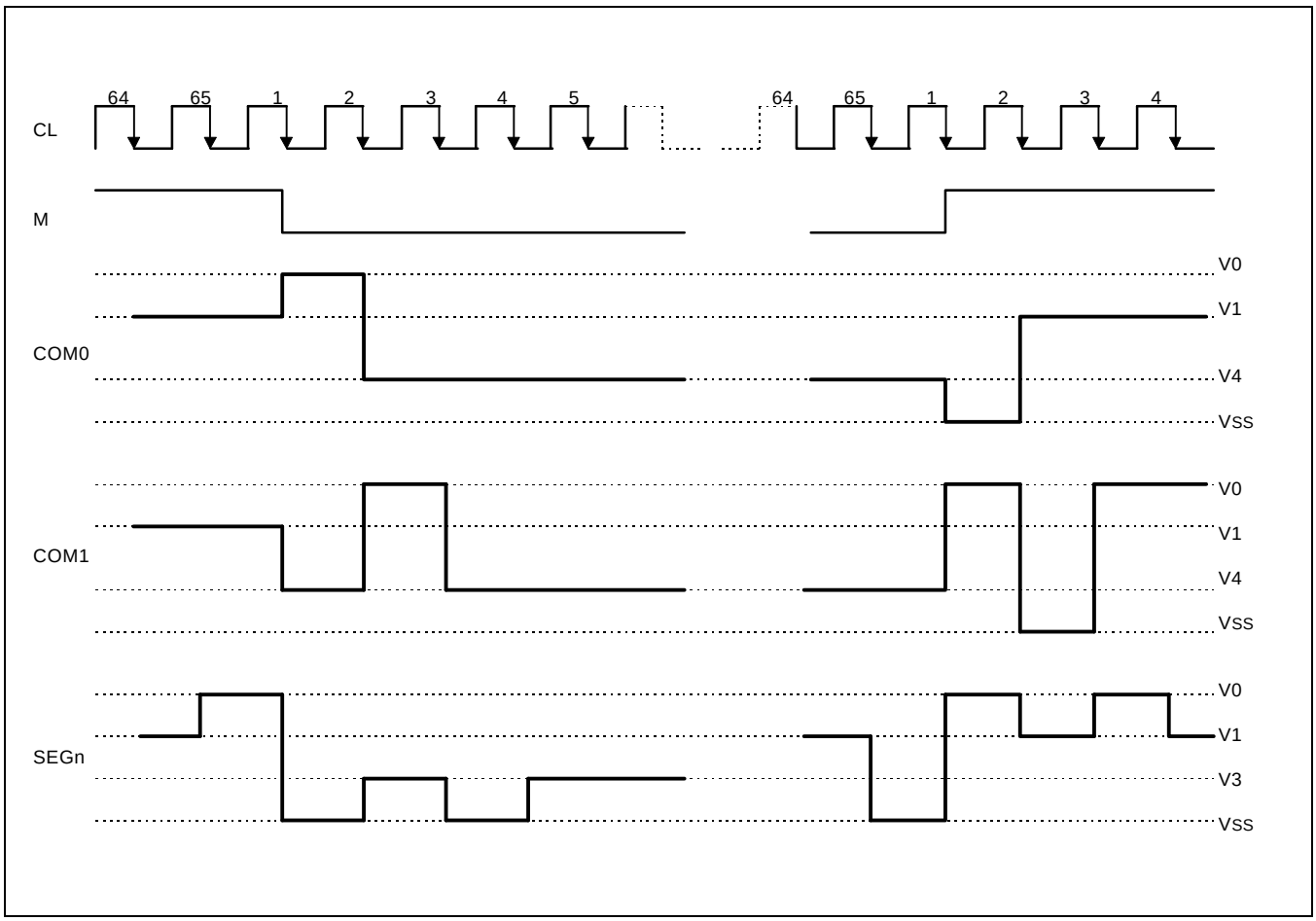


Figure 6. 2-Frame AC Driving Waveform

COMMON OUTPUT CONTROL CIRCUIT

This circuit controls the relationship between the number of common outputs and the specified duty ratio. SHL Select instruction specifies the scanning direction of the common output pins.

Table 9. The Relationship Between Duty Ration and Common Output

Duty	SHL	Common Output Pins						
		COM[0:15]	**COM[16:23]**	**COM[24:31]**	**COM[32:39]**	**COM[40:47]**	**COM[48:63]**	**COMS**
1/33	0	COM[0:15]					COM[16:31]	COM[32]
		COM[31:16]					COM[15:0]	COM[32]
1/49	0	COM[0:23]				COM[24:47]		COM[48]
	1	COM[47:24]				COM[23:0]		COM[48]
1/65	0	COM[0:63]						COM[64]
	1	COM[63:0]						COM[64]

LCD DRIVER CIRCUIT

This driver circuit is configured by a 65-channel common driver and a 132-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

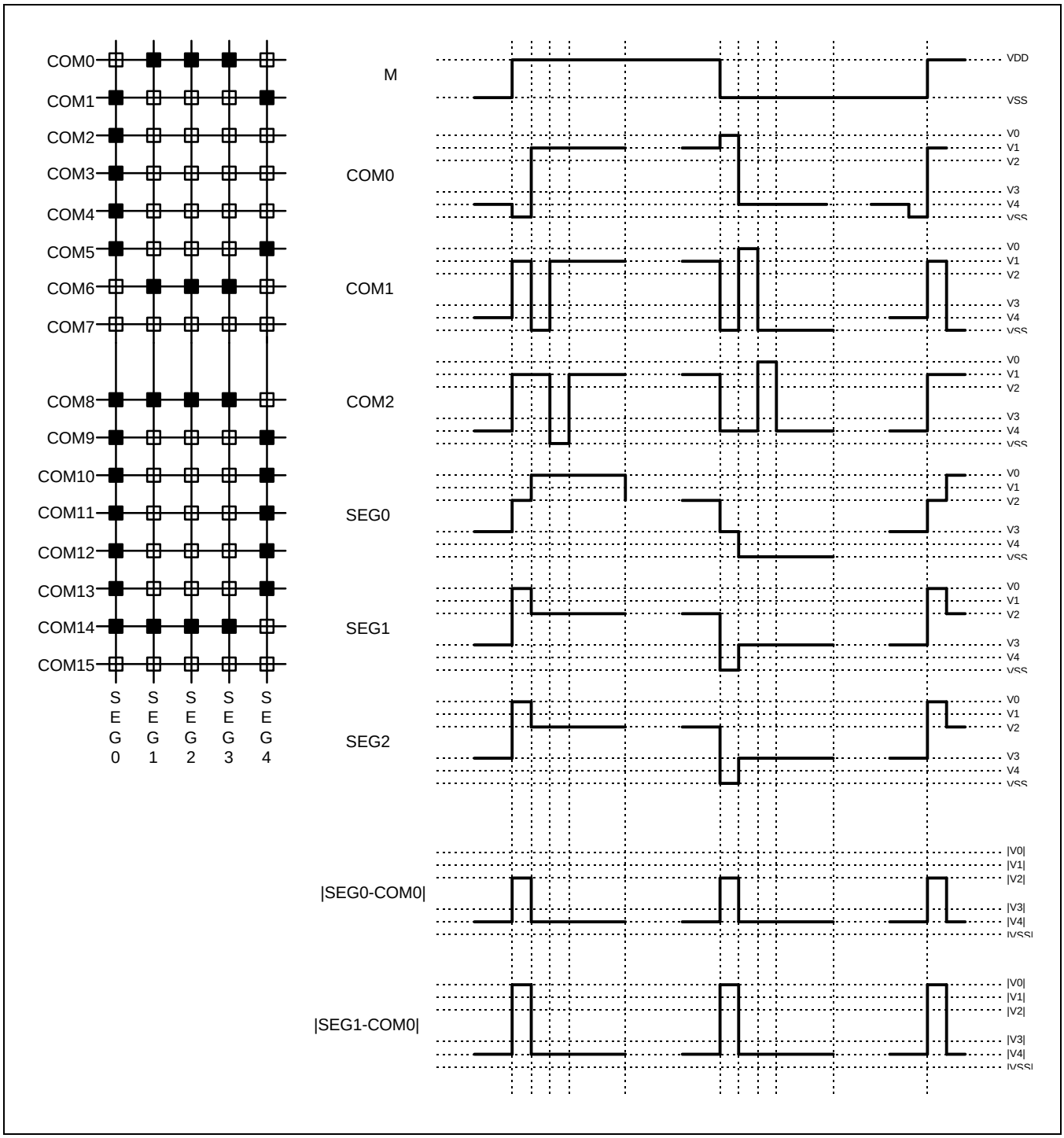


Figure 7. Segment and Common Timing

POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and are controlled by power control instruction. For details, refers to “Instruction Description”. Table 10 shows the referenced combinations in using power supply circuits.

Table 10. Recommended Power Supply Combinations

User Setup	PoWer Control Register [VC, VR, VF]	V/C Circuits	V/R Circuits	V/F Circuits	VOUT Pin	V0 Pin	V1–V4 Pin
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

VOLTAGE CONVERTER CIRCUITS

These circuits multiply the electric potential between V_{DD} and V_{SS} to 4 or 5 times toward the positive side. Boosted voltage is output from the VOUT pin.

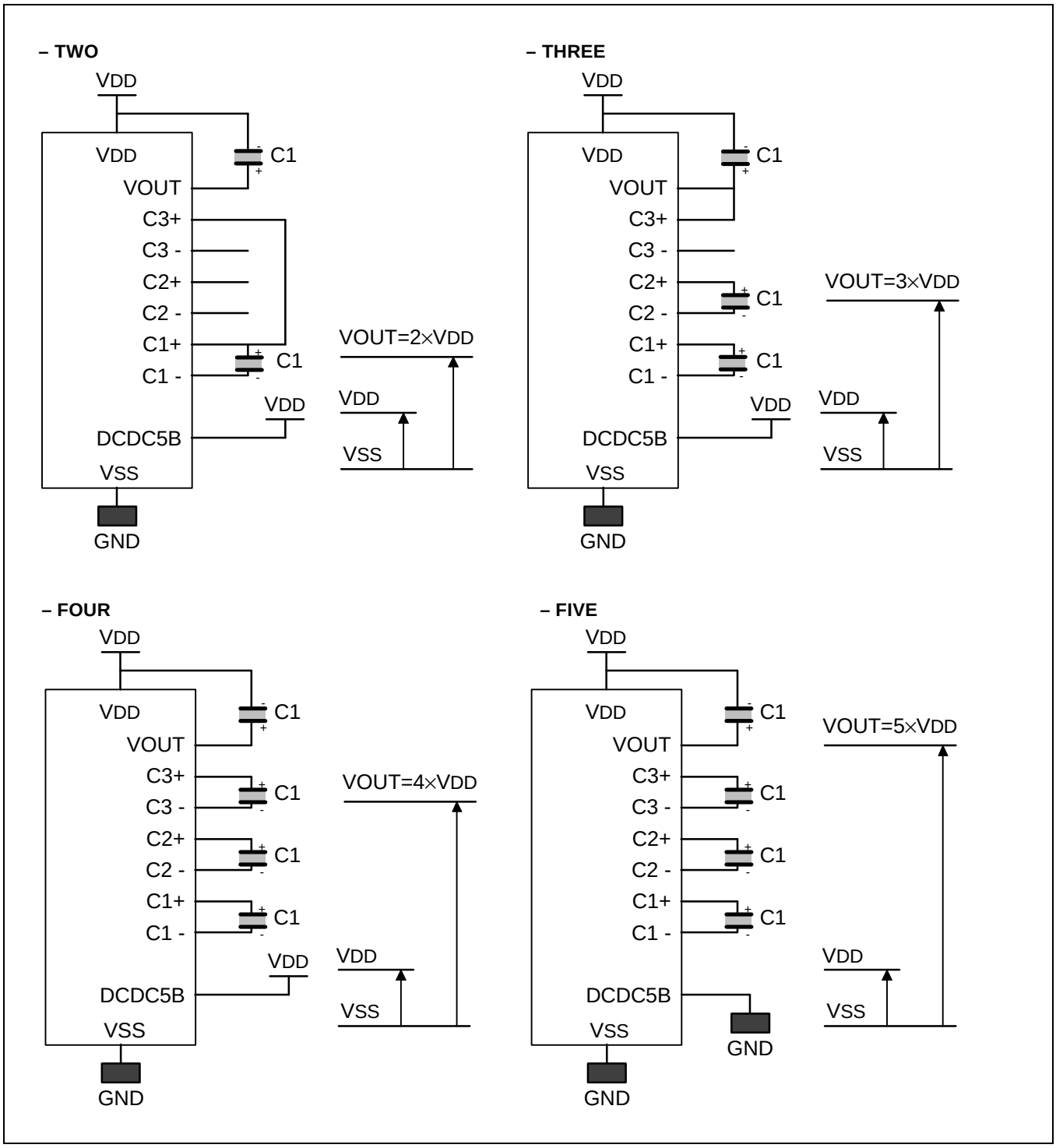


Figure 8. Two / Three / Four / Five Times Boosting Circuit

VOLTAGE REGULATOR CIRCUITS

The function of the internal voltage regulator circuits is to determine the liquid crystal operating voltage, V0, by adjusting the resistors Ra and Rb within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of the operational-amplifier circuits shown in Figure 9, it is necessary to apply it either internally or externally.
For Equation 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} (voltage of electronic volume) is determined by Equation 2, where the parameter is the value selected by the instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in Table 11.

<Equation 1>

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V]$$

<Equation 2>

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162}\right) \times V_{REF} \quad [V]$$

Table 11. V_{REF} Voltage at Ta = 25°C

TEMP1	TEMP0	Temp. Coefficient	V_{REF} [V]
H	H	TBD	TBD
H	L	TBD	TBD
L	H	TBD	TBD
L	L	TBD	TBD

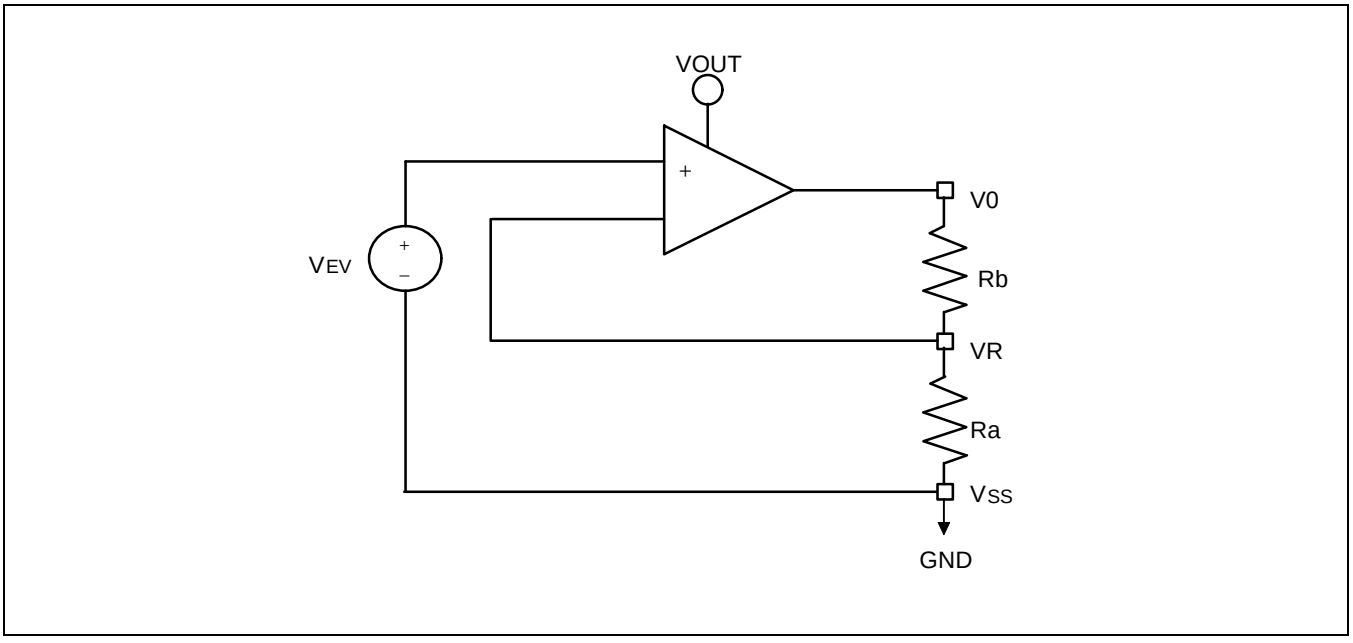


Figure 9. Internal Voltage Regulator Circuit

1) In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is high, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 12. Internal Rb/Ra Ratio Depending on 3-Bit Data (R2 R1 R0)

	3-Bit Data Settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb/Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

Figure 10. shows V0 voltage measured by adjusting the internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25°C.

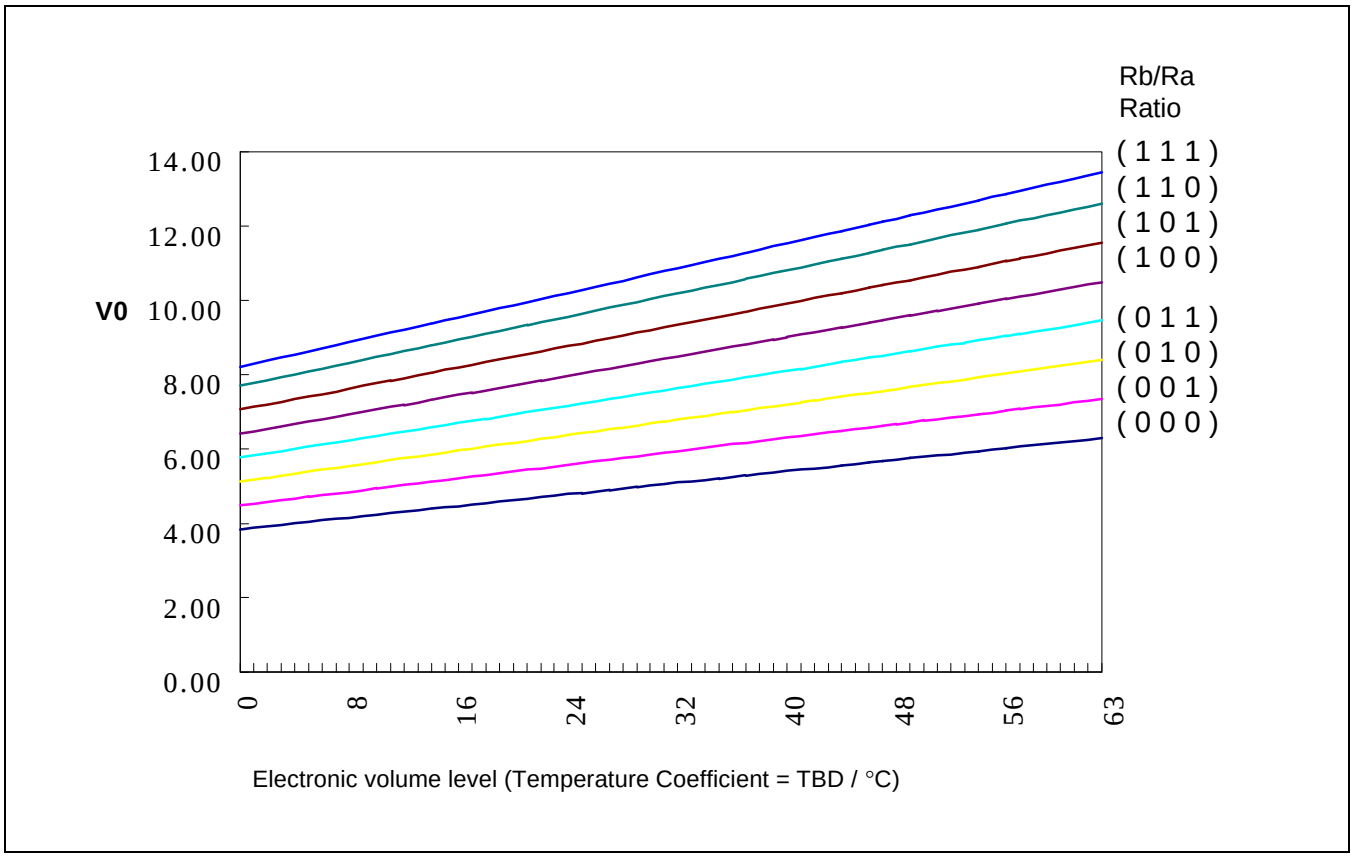


Figure 10. V0 Voltage

2) In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is low, it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements,

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1μA

<Equation 3> From Equation 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V]$$

<Equation 4> From Equation 1

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 = 1.698 \ [V]$$

<Equation 5> From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \ [\mu A]$$

From equations Equation 3, 4 and 5:

Ra = 1.69 [Ω]

Rb = 8.31 [Ω]

Table 13. shows the range of V0 depending on the above requirements.

Table 13. The Range of V0 Depending

	Electronic Volume Level				
	0	.....	32	.....	63
V0	7.59	.....	10.00	.....	12.43

VOLTAGE FOLLOWER CIRCUITS

V_{LCD} voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedances are converted by the voltage follower for increasing drive capability.

REFERENCED POWER SUPPLY CIRCUIT FOR DRIVING LCD PANEL

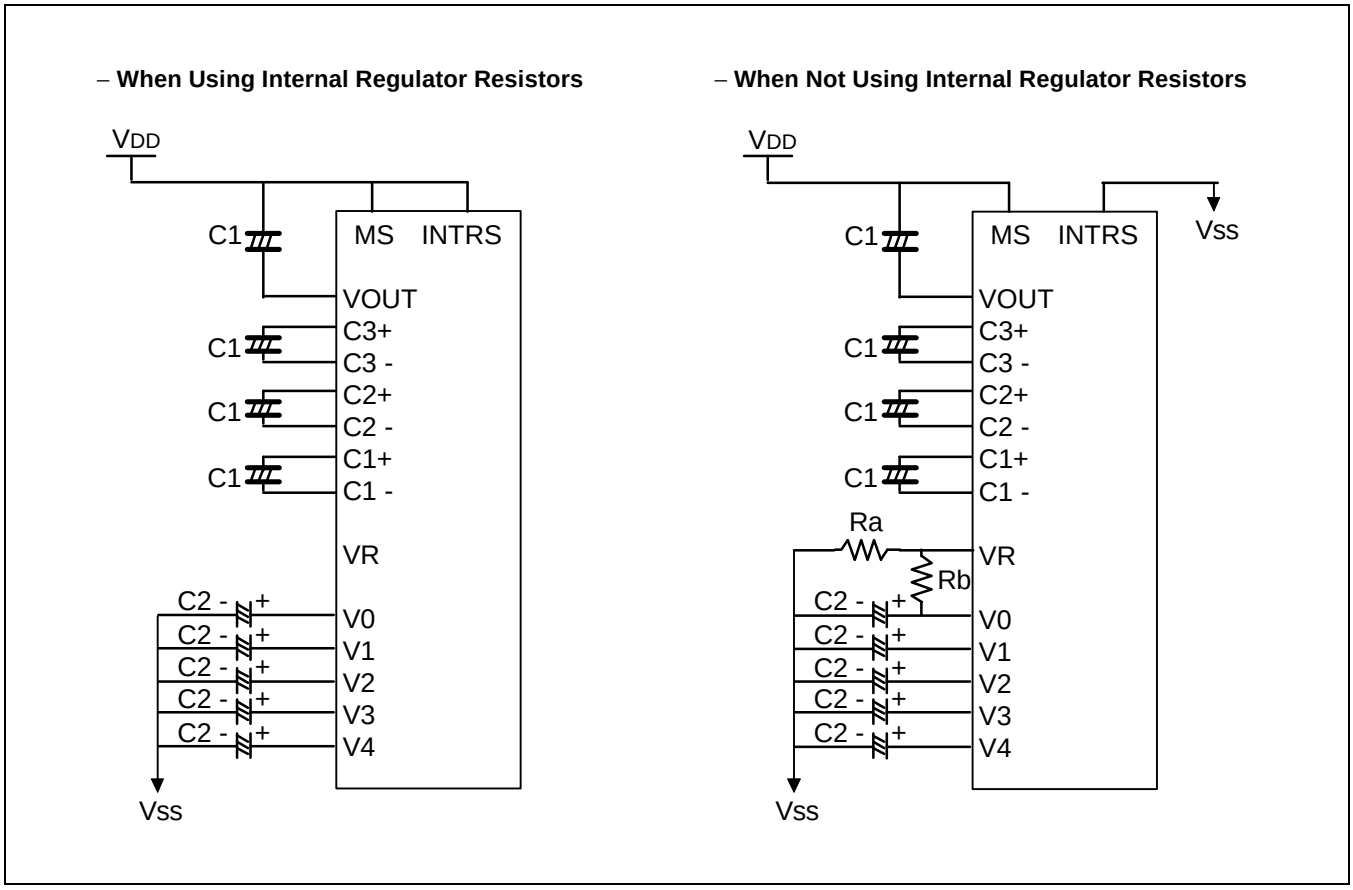


Figure 11. When Using All LCD Power Circuits (4-Times, V/R: On, V/F: On)

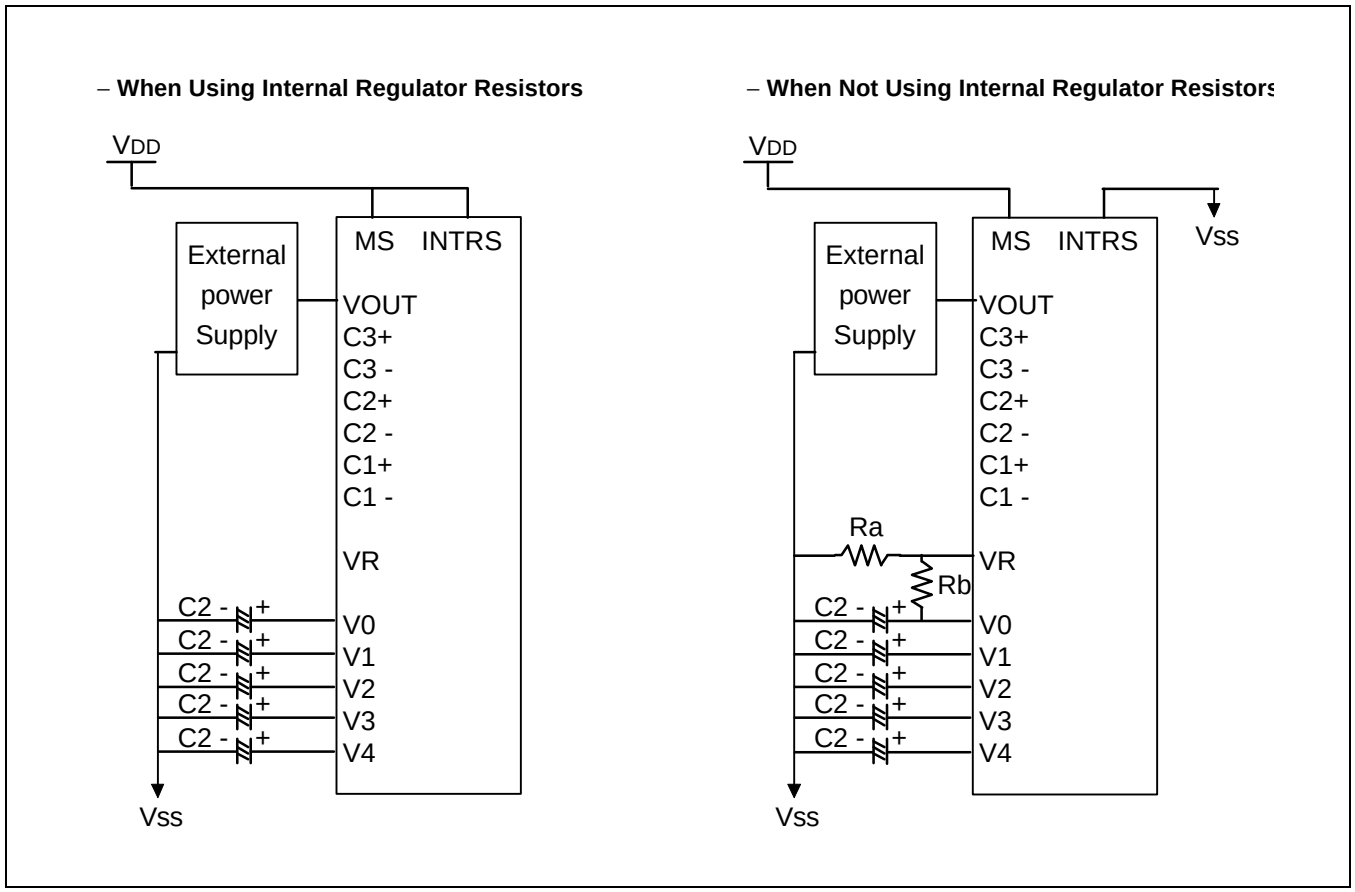


Figure 12. When Using Some LCD Power Circuits (V/C: Off, V/R: On, V/F: On)

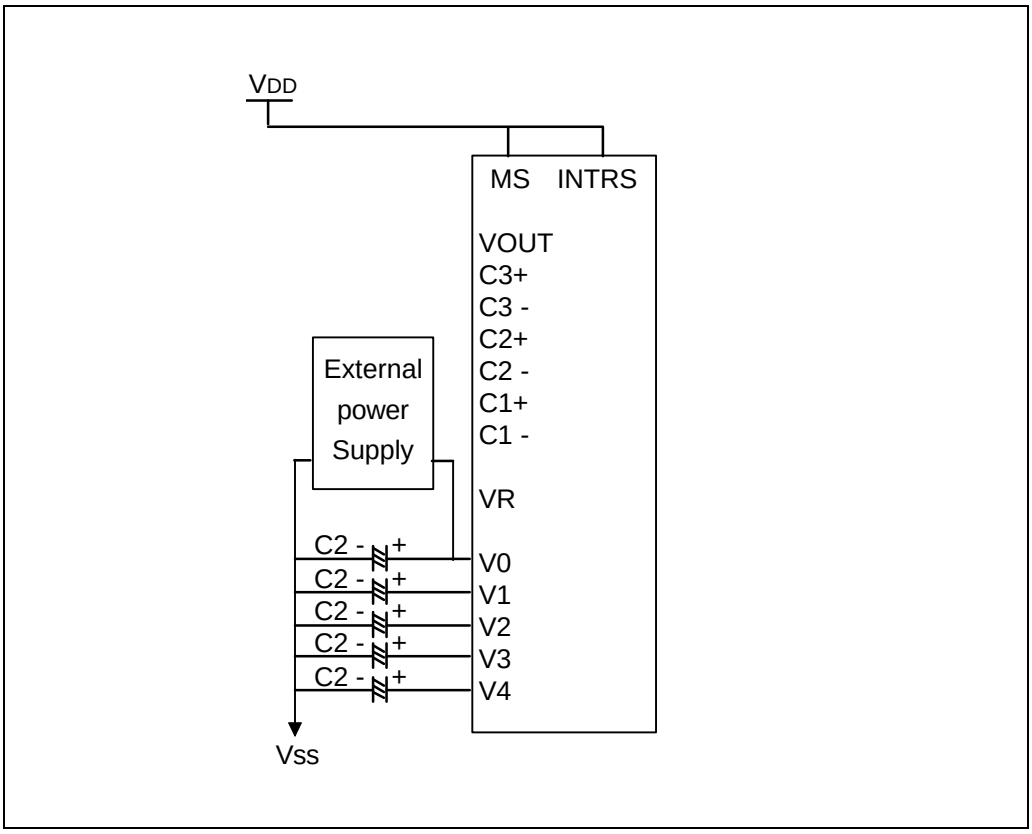


Figure 13. When Using Some LCD Power Circuits (V/C: Off, V/R: Off, V/F: On)

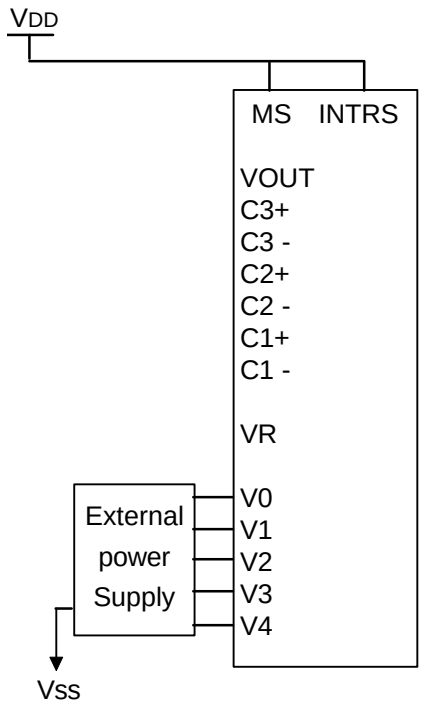


Table 14. Value of External Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	

Figure 14. When Not Using Any Internal LCD Power Circuits (V/C: Off, V/R: Off, V/F: Off)

RESET CIRCUIT

Internal function can be initialized by setting RESETB to low or Reset instruction.

When RESETB becomes low, following procedure occurs.

- Display ON / OFF:OFF
- Entire display ON / OFF: OFF (Normal)
- ADC select: OFF (Normal)
- Reverse display: OFF (Normal)
- Power control register (VC, VR, VF) = (0, 0, 0)
- LCD bias ratio: 1/9 (1/65 Duty), 1/8 (1/49 Duty), 1/7 (1/33 Duty)
- Modify-Read: OFF
- SHL select: 0
- Static indicator mode: OFF
  Static indicator register: (S1, S0) = (0, 0)
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
- Reference voltage set: OFF,
  Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
- White mode set: OFF
- White palette register (WG4, WG3, WG2, WG1, WG0) = (0, 0, 0, 0, 0)
- Light gray mode set: OFF
- Light gray palette register (LG4, LG3, LG2, LG1, LG0) = (0, 1, 0, 1, 0)
- Dark gray mode set: OFF
- Dark gray palette register (DG4, DG3, DG2, DG1, DG0) = (1, 0, 1, 0, 1)
- Black mode set: OFF
- Black palette register (BG4, BG3, BG2, BG1, BG0) = (1, 1, 1, 1, 1)

When RESET instruction is issued, following procedure is occurs.

- Modify-read: OFF
- Static indicator mode: OFF
  Static indicator register: (S1, S0) = (0, 0)
- SHL select: 0 (Normal)
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
- Reference voltage set: OFF
  Reference voltage control register (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
- White mode set: OFF
- White palette register (WG4, WG3, WG2, WG1, WG0) = (0, 0, 0, 0, 0)
- Light gray mode set: OFF
- Light gray palette register (LG4, LG3, LG2, LG1, LG0) = (0, 1, 0, 1, 0)
- Dark gray mode set: OFF
- Dark gray palette register (DG4, DG3, DG2, DG1, DG0) = (1, 0, 1, 0, 1)
- Black mode set: OFF
- Black palette register (BG4, BG3, BG2, BG1, BG0) = (1, 1, 1, 1, 1)

No instruction except read status can be accepted, while RESETB is low or reset instruction is being executed. Reset status appears at DB4. After DB4 becomes low, any instruction can be accepted.

RESETB pin must be connected to the reset pin of MPU. Initialize the MPU and this LSI at the same time. The initialization by RESETB pin is essential before use.

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON/ OFF	RESETB	0	0	0	0	Read the internal status
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON/OFF LCD panel When DON=0, display is OFF When DON=1, display is On
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y8	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC=0 normal direction (SEG0 → SEG131) When ADC=1 reverse direction (SEG131 → SEG0)
Normal / Reverse display	0	0	1	0	1	0	0	1	1	REV	Select normal/reverse display When REV=0 normal When REV=1 reverse
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	Select normal display / entire display ON When EON=0, normal display When EON=1, entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias When bias=0, 1/7 When bias=1, 1/9
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL=0 normal direction (COM0 → COM63) When SHL=1 reverse direction (COM63 → COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select resistance ratio of the regulator resistor

Table 15. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode When SM=0, OFF When SM=1, ON
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	–	–	–	–	–	–	–	–	–	–	Compound command of display OFF and entire display ON
Set white mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	0	0	0	Set white mode and 1st/2nd frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	Set white 1st/2nd register
Set white mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	0	0	1	Set white mode and 3rd/4th frame
	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	Set white 3rd/4th register
Set light gray mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	0	1	0	Set light gray mode and 1st/2nd frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	Set light gray 1st/2nd register
Set light gray mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	0	1	1	Set light gray mode and 3rd/4th frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	Set light gray 3rd/4th register
Set dark gray mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	1	0	0	Set dark gray mode and 1st/2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	Set dark gray 1st/2nd register
Set dark gray mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	1	0	1	Set dark gray mode and 3rd/4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	Set dark gray 3rd/4th register
Set black mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	1	1	0	Seg black mode 1st/2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	Seg black 1st/2nd register
Set black mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	1	1	1	Set black mode and 3rd/4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	Set black 3rd/4th register
Set FRC and PWM mode	0	0	1	1	1	1	0	FRC	PWM 1	PWM 0	FRC (1: 3FRC, 0: 4FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM

NOTE: "×" = Don't care

READ DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**1**	**Read Data**							

You can read the 8-bit data from display data RAM, specified by the column address and page address, using this instruction. As the column address is increased by 1 automatically after each instruction, the microprocessor can read data from the addressed page continuously. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

WRITE DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**0**	**Write Data**							

You can write the 8-bit data of display data from the microprocessor to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can write data to the addressed page continuously.

READ STATUS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**BUSY**	**ADC**	**ON/OFF**	**RESETB**	**0**	**0**	**0**	**0**

Indicates the internal status conditions.

Flag	Description
BUSY	The device is busy when in internal operation or reset. Any instruction is rejected until BUSY goes Low. 0 = Chip is active. 1 = Chip is busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0 = Reverse direction (SEG131 → SEG0), 1 = Normal direction (SEG0 → SEG131)
ON/OFF	Indicates display ON/OFF status. 0 = Display ON 1 = Display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0 = Chip is active. 1 = Chip is being reset.

DISPLAY ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**DON**

Turns the display ON or OFF

DON	
1	Display ON
0	Display OFF

INITIAL DISPLAY LINE

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM0) of the LCD panel.

ST5	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

REFERENCE VOLTAGE SELECT

Set reference voltage mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set reference voltage register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**´**	**´**	**SV5**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

Instruction consists of two bytes. The first byte sets the reference voltage mode, and the second one updates the contents of the reference voltage register. After the second instruction, the reference voltage mode is released.

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage (a)
0	0	0	0	0	0	0
:	:	:	:	:	:	:
1	1	1	1	1	1	63

SET PAGE ADDRESS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**1**	**P3**	**P2**	**P1**	**P0**

Sets the page address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the display RAM to write or read display data. Changing the page address doesn't affect the display status.

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:			:
0	1	1	1	7
1	0	0	0	8

SET COLUMN ADDRESS

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**Y8**	**Y7**	**Y6**	**Y5**

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**Y4**	**Y3**	**Y2**	**Y1**

Sets the column address of display RAM from the microprocessor into the column address register. Along with the page address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased, starting with the address stored in the column address register and continuously rotating right.

Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	2
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	260
1	0	0	0	0	0	1	1	262

ADC SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**ADC**

Changes the relationship between the RAM column address and segment driver. The direction of segment driver output pins can be reversed by software, making the IC layout flexible in an LCD module assembly.

ADC	
0	Normal direction (SEG0 → SEG131)
1	Reverse direction (SEG131 → SEG0)

REVERSE DISPLAY ON / OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**REV**

Reverses the display status on the LCD panel without rewriting the contents of the display data RAM.

REV	RAM Bit Data = “1”	RAM Bit Data = “0”
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

ENTIRE DISPLAY ON / OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**EON**

Forces whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

EON	
0	Normal display
1	Entire display on

LCD BIAS SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**BIAS**

Selects the LCD bias ratio of the voltage required for driving the LCD.

DUTY Ratio	LCD BIAS	
	BIAS = 1	BIAS = 0
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5

SET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

This instruction stops the automatic increment of the column address by read display data instruction, but the column address is still increased by the write display data. It also reduces the load of the microprocessor when the data of a specific area is repeatedly changed during cursor blinking or at other times. This mode is cancelled by the reset modify-read instruction.

RESET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This instruction cancels the modify read mode, and makes the column address return to its initial value just before the set modify read instruction starts.

RESET

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This instruction resets the initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of the display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

SHL SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**0**	**0**	**SHL**	×	×	×

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

SHL	
0	Normal direction (COM0 → COM63)
1	Reverse direction (COM63 → COM0)

POWER CONTROL

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**1**	**VC**	**VR**	**VF**

Selects one of eight power circuit functions by using a 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

VC, VR, VF	**Indicates whether the voltage converter / regulator / follower turns on or not**
0	Off
1	On

REGULATOR RESISTOR SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**1**	**R2**	**R1**	**R0**

Selects the resistance ratio of the resistor used in the Voltage Regulator. See the Voltage Regulator section in Power Supply Circuit.

R2 - 0			**[Rb/Ra] Ratio**
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

SET STATIC INDICATOR STATE

— Set static indicator mode (On/Off)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**SM**

Instruction consists of two bytes. The first byte instruction (Set Static Indicator Mode) enables the second byte instruction (Set Static Indicator Register) to be valid. The first byte sets the static indicator on/off. When it is on, the second byte updates the contents of the static indicator register without issuing any other instruction, and this static indicator state is released after setting the data of the indicator register.

SM	
0	Static indicator OFF
1	Static indicator ON

— Set static indicator register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	´	´	´	´	´	´	**S1**	**S0**

S1	**S0**	**Status of Static Indicator Output**
0	0	OFF
1	1	ON (Always ON)

POWER SAVE (COMPOUND INSTRUCTION)

If the entire display ON / OFF instruction is issued during the display OFF state, KS0711 enters the power save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to either sleep mode or. When static Indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power save mode is released by the display ON & entire display OFF instruction.

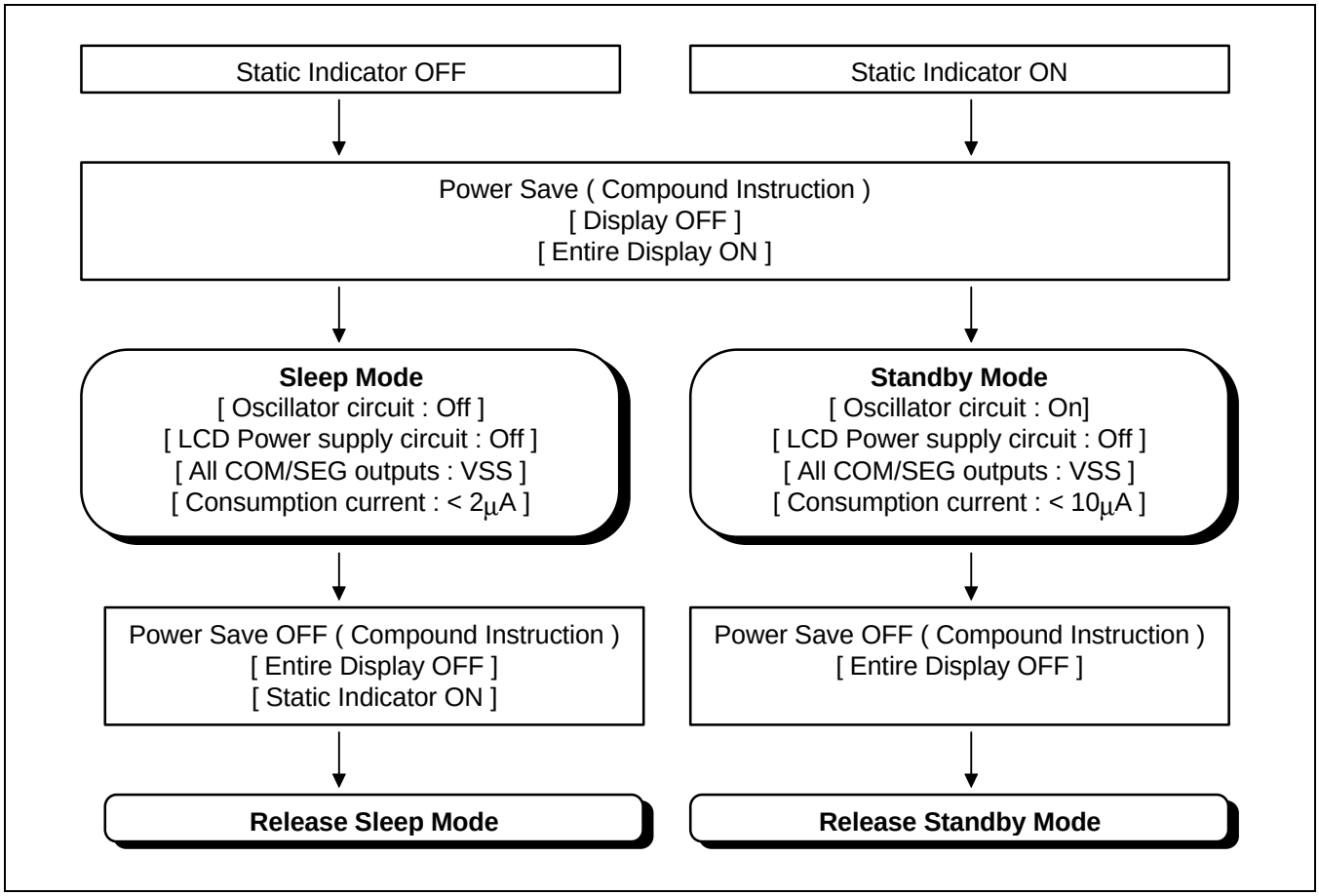


Figure 15. Power Save (Compound Instruction)

SET GRAY SCALE MODE & REGISTER

Set gray scale mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**1**	**1**	**GM2**	**GM1**	**GM0**

Instruction consists of two bytes. The first byte sets gray scale mode, and the second one updates the contents of the gray scale register without issuing any other instruction.

GM2, GM1, GM0

0	0	0	In case of setting white mode and 1st/2nd frame
0	0	1	In case of setting white mode and 3rd/4th frame
0	1	0	In case of setting light gray mode and 1st/2nd frame
0	1	1	In case of setting light gray mode and 3rd/4th frame
1	0	0	In case of setting dark gray mode and 1st/2nd frame
1	0	1	In case of setting dark gray mode and 3rd/4th frame
1	1	0	In case of setting black mode and 1st/2nd frame
1	1	1	In case of setting black mode and 3rd/4th frame

Set gray scale register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**GB3**	**GB2**	**GB1**	**GB0**	**GA3**	**GA2**	**GA1**	**GA0**
0	**0**	**GD3**	**GD2**	**GD1**	**GD0**	**GC3**	**GC2**	**GC1**	**GC0**

GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Degree of Contrast
0	0	0	0	White
0	0	0	1	:
:	:	:	:	:
1	1	1	0	:
1	1	1	1	Black

NOTE:

1. GA3=WA3, LA3, DA3, BA3, GA2=WA2, LA2, DA2, BA2, GA1=WA1, LA1, DA1, BA1, GA0=WA0, LA0, DA0, BA0
2. GB3=WB3, LB3, DB3, BB3, GB2=WB2, LB2, DB2, BB2, GB1=WB1, LB1, DB1, BB1, GB0=WB0, LB0, DB0, BB0
3. GC3=WC3, LC3, DC3, BC3, GC2=WC2, LC2, DC2, BC2, GC1=WC1, LC1, DC1, BC1, GC0=WC0, LC0, DC0, BC0
4. GD3=WD3, LD3, DD3, BD3, GD2=WD2, LD2, DD2, BD2, GD1=WD1, LD1, DD1, BD1, GD0=WD0, LD0, DD0, BD0

SET PWM & FRC

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**1**	**0**	**FRC**	**PWM1**	**PWM0**
FRC (1: 3FC, 0: 4FRC), PWM1 PWM0 (00: 9PWM, 01: 9PWM, 10: 12PWM, 11: 15PWM)									

REFERENTIAL INSTRUCTION SETUP FLOW

— Initializing with the built-in power supply circuits

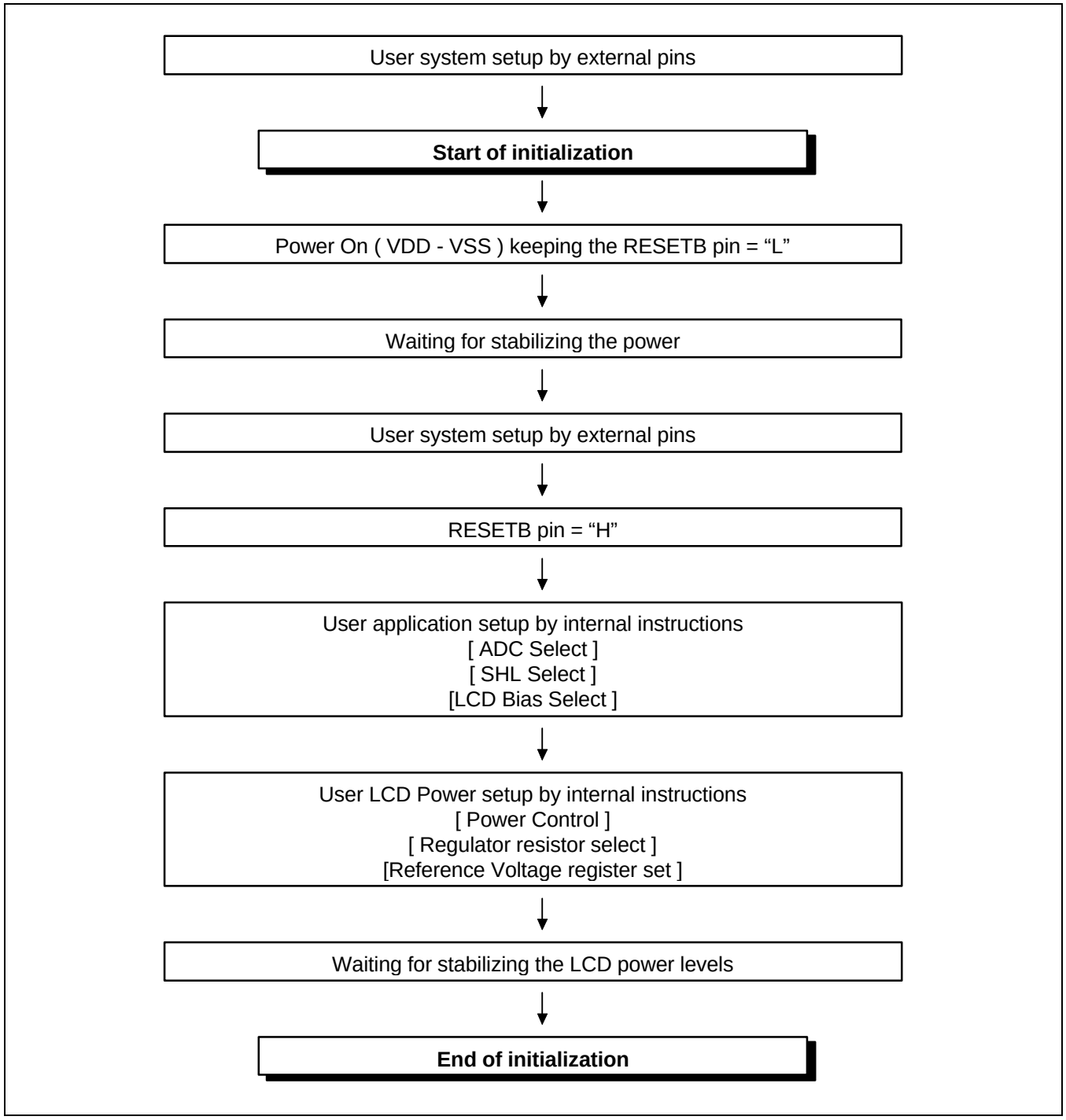


Figure 16. Initializing with the Built-in Power Supply Circuits

— Initializing without the built-in power supply circuits

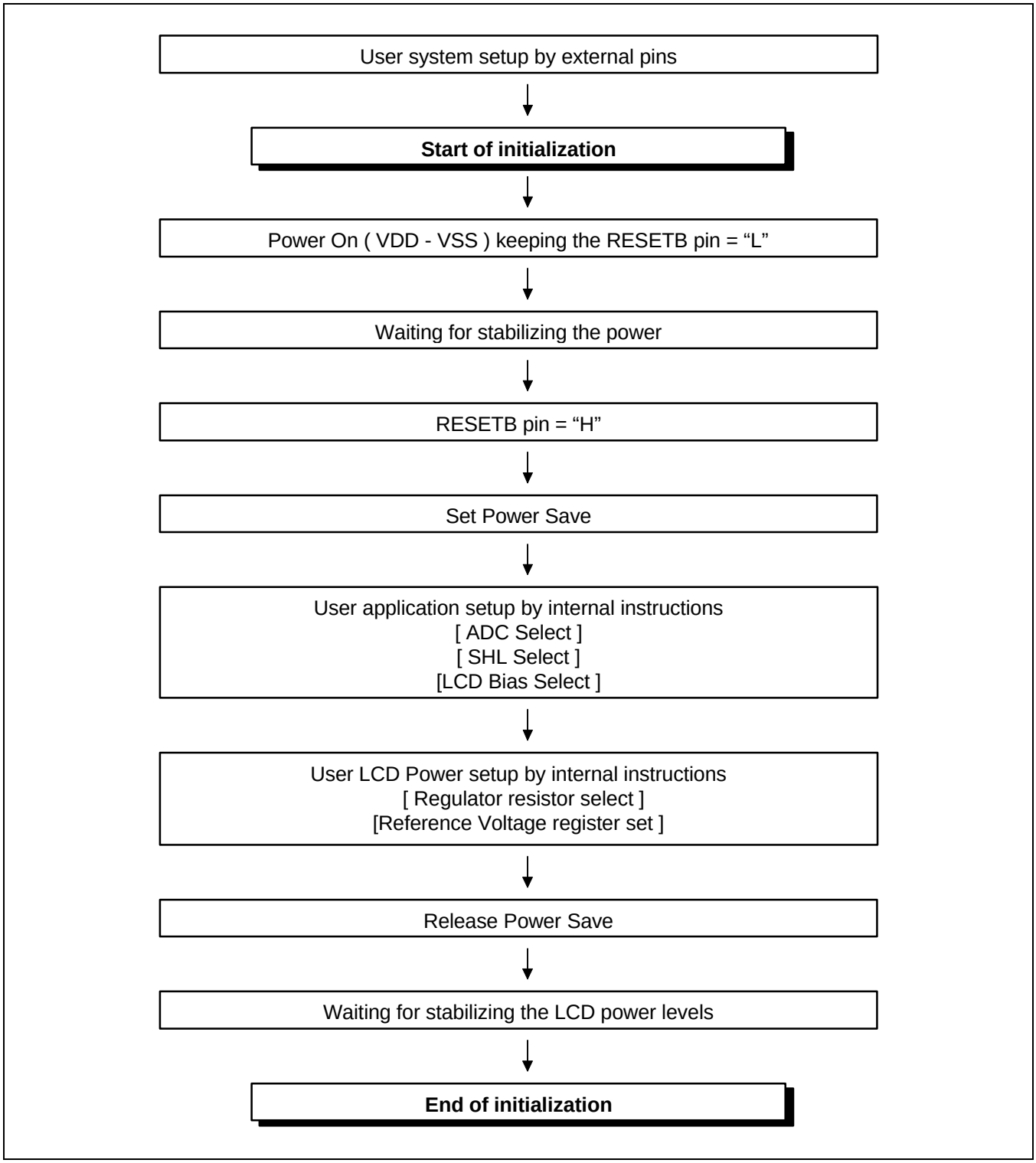


Figure 17. Initializing without the Built-In Power Supply Circuits

— Data displaying

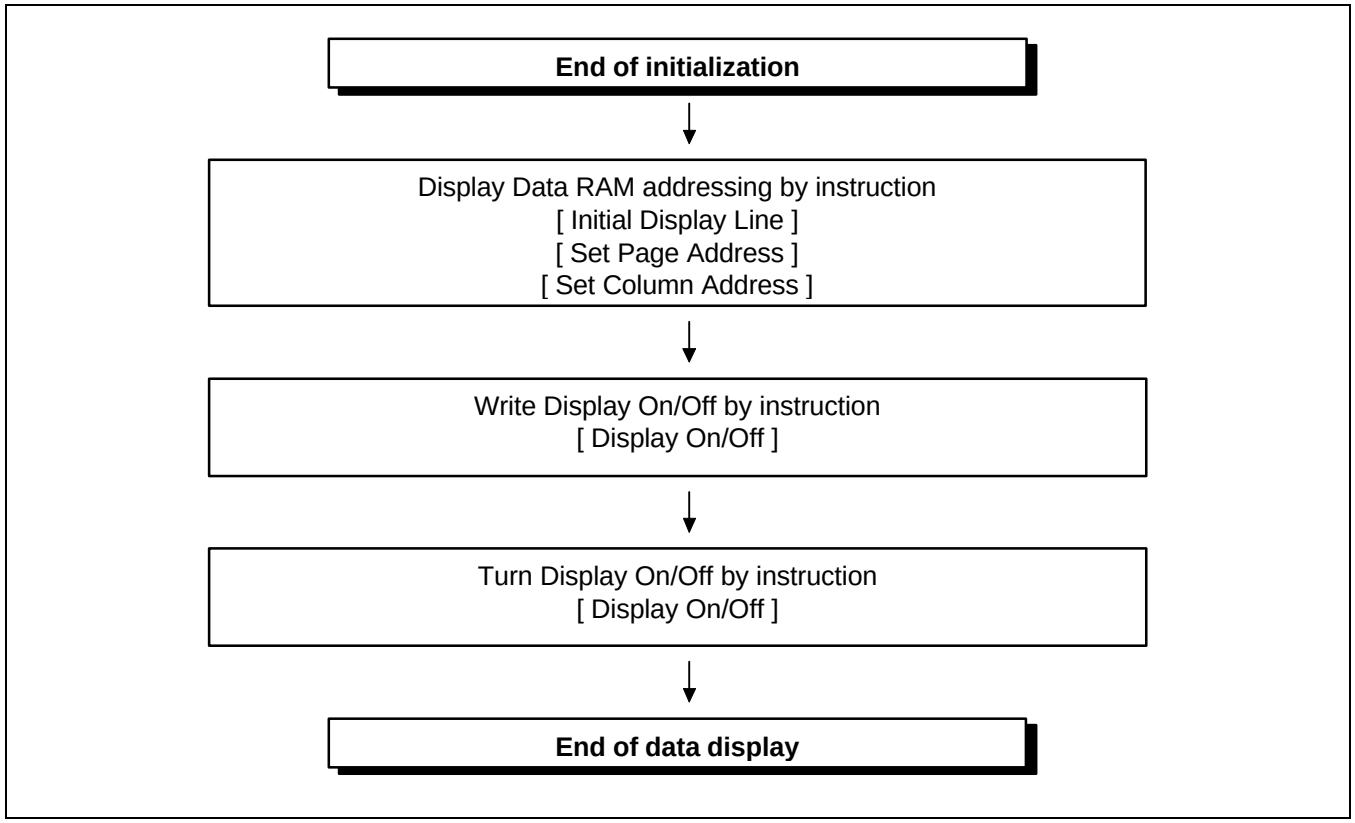


Figure 18. Data Displaying

— Power Off

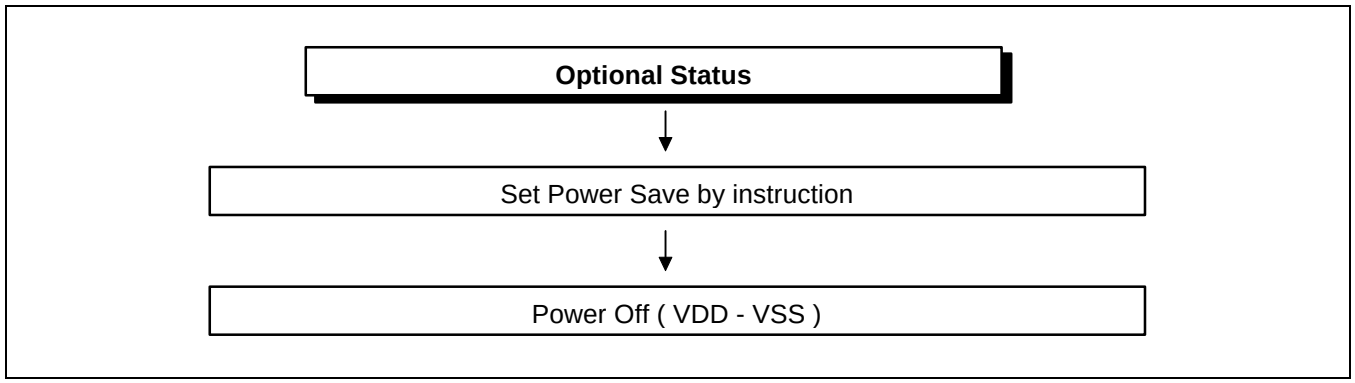


Figure 19. Power Off

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	– 0.3 to + 7.0	V
	V_{LCD}	+ 0.3 to + 17.0	
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	
Operating temperature range	T_{OPR}	– 40 to + 85	°C
Storage temperature range	T_{STR}	– 55 to + 125	

NOTES:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0 V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied (V_{LCD} = V0 – V_{SS}).
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. Use this LSI under specified electrical characteristic conditions during general operation. Otherwise, LSI malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 17. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin Used
Operating voltage (1)		V_{DD}	–		2.4	–	5.5	V	V_{DD} (1)
Operating voltage (2)		V0	–		4.0	–	15.0		V0 (2)
Input voltage	High	V_{IH}	–		0.8 V_{DD}	–	V_{DD}		(3)
	Low	V_{IL}	–		V_{SS}	–	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = – 0.5mA		0.8 V_{DD}	–	V_{DD}		(4)
	Low	V_{OL}	I_{OL} = 0.5mA		V_{SS}	–	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}		– 1.0	–	+ 1.0	µA	(5)
Output Leakage Current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}		– 3.0	–	+ 3.0		(6)
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V		–	2.0	3.0	kΩ	SEGn COMn (7)
Operating frequency		f_{OSC}	Ta = 25°C, REXT = TBD		TBD	TBD	TBD	kHz	OSSCK
Voltage converter input voltage		V_{DD}	× 2		2.4	–	5.5	V	V_{DD}
			× 3		2.4	–	5.0		
			× 4		2.4	–	3.75		
			× 5		2.4	–	3.0		
Voltage converter output voltage		VOUT	× 2/× 3/× 4/× 5 voltage conversion (no-load)		95	99	–	%	VOUT
Voltage regulator operating voltage		VOUT	–		4.0	–	15.0	V	VOUT
Voltage follower operating voltage		V0	–		4.0	–	15.0		V0 (8)
Reference voltage		V_{REF0} to V_{REF3}	Ta = 25°C	TBD	TBD	TBD	TBD	V	(9)
				TBD	TBD	TBD	TBD		
				TBD	TBD	TBD	TBD		
				TBD	TBD	TBD	TBD		
Dynamic Current Consumption (1): When the built-In circuits are OFF (At Operate Mode).									
Dynamic current consumption (1)		I_{DD1}	VDD = 3.0V, V0 – VSS = 8.0V, Built-in power circuit is Off (Operate mode)		–	–	50	µA	(10)
Dynamic Current Consumption (2): When the built-in circuits are ON (At Operate Mode).									
Dynamic current consumption (2)		I_{DD2}	VDD = 3.0V, triple boosting, V0 – VSS = 8.0V, Built-in power circuit is On (Operate mode), Normal mode		–	–	150	µA	(10)

Table 17. DC Characteristics (Continued)

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Dynamic Current Consumption (3): When the built-in power is OFF (At Access Mode).							
Dynamic current consumption (3)	I_{DD3}	VDD = 3.0V, V0 – VSS = 8.0V, f_{cyc} = 1MHz, Built-in power circuit is Off (Operate mode)	–	–	1	mA	
Current Consumption During Power Save Mode							
During sleep	I_{DDS1}	Sleep mode	–	–	2.0	µA	
During standby	I_{DDS2}	Standby mode	–	–	10.0	µA	

NOTES:

1. Though a wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from MPU.
2. When an external power supply is applied.
3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, TEMP0, TEMP1, DCDC5B, CLS, CL, M, DISP pins
4. DB0 – DB7, M, FRS, DISP, CL pins
5. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, TEMP0, TEMP1, DCDC5B, CLS, CL, M, DISP pins
6. Applies when the DB0 to DB7, M, DISP, and CL pins are in high impedance.
7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
   R_{ON} = Δ V / 0.1 [kΩ] (Δ V: voltage change when ± 0.1[mA] is applied in the ON status.)
8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU. The current consumption does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

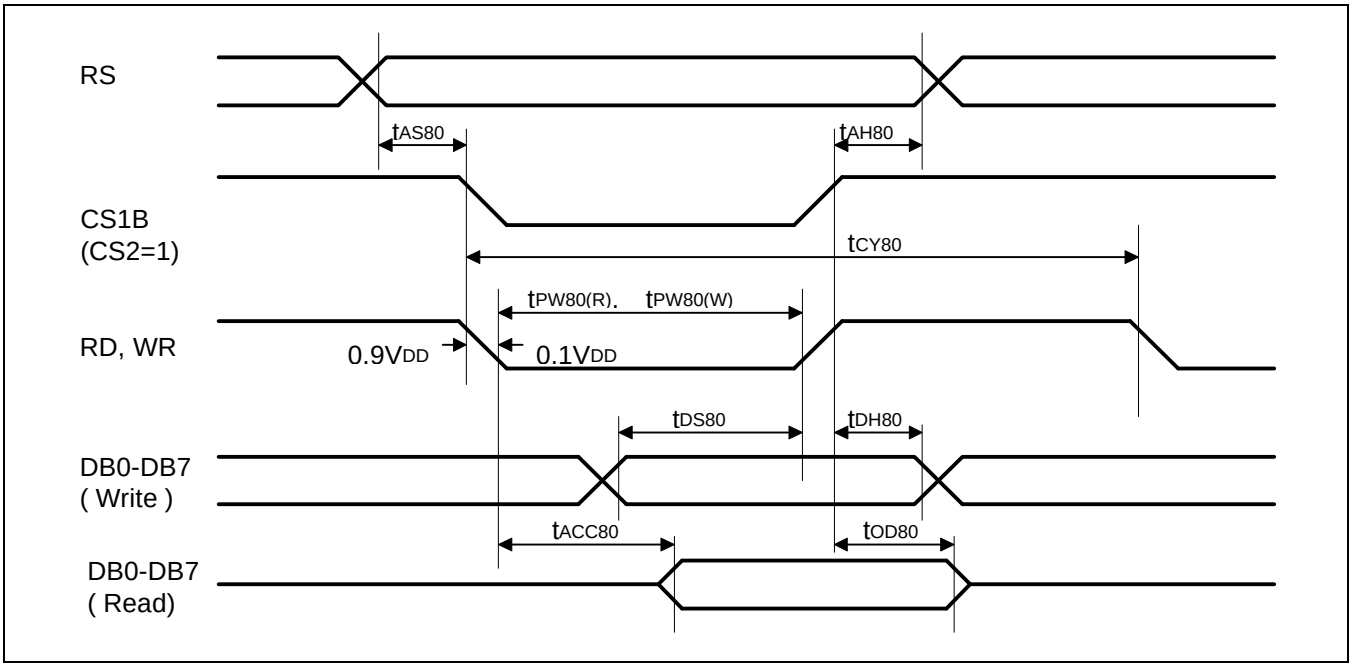


Figure 20. Read / Write Characteristics (8080-Series Microprocessor)

(V_{DD} = 2.4V to 3.3V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	–	–	ns	–
System cycle time	RS	t_{CY80}	400	–	–	ns	–
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	55	–	–	ns	–
Pulse width (RD)	E_RD	$t_{PW80(R)}$	125	–	–	ns	–
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}	35 13	–	–	ns	–
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	125 90	ns ns	C_L = 100pF

(V_{DD} = 4.5V to 5.5V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	10 10	–	–	ns	–
System cycle time	RS	t_{CY80}	150	–	–	ns	–
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	25	–	–	ns	–
Pulse width (RD)	E_RD	$t_{PW80(R)}$	65	–	–	ns	–
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}	18 10	–	–	ns	–
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	65 45	ns ns	C_L = 100pF

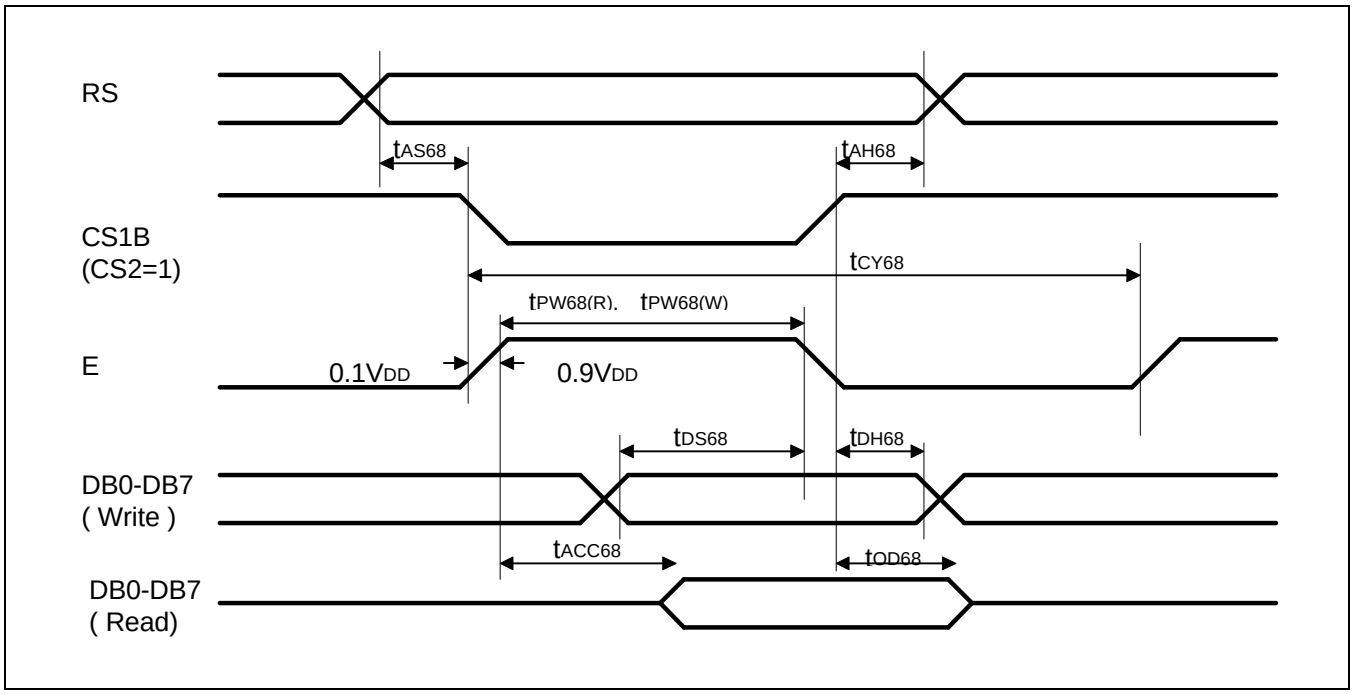


Figure 21. Read/Write Characteristics (6800-Series Microprocessor)

(V_{DD} = 2.4V to 3.3V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	13 17	–	–	ns	–
System cycle time		RS	t_{CY68}	400	–	–	ns	–
Data setup time Data hold time		DB0 to DB7	t_{DS68} t_{DH68}	35 13	–	–	ns	–
Access time Output disable time			t_{ACC68} t_{OD68}	– 10	– –	125 90	ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	–	–	–	–

(V_{DD} = 4.5V to 5.5V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	10 10	–	–	ns	–
System cycle time		RS	t_{CY68}	150	–	–	ns	–
Data setup time Data hold time		DB0 to DB7	t_{DS68} t_{DH68}	18 10	–	–	ns	–
Access time Output disable time			t_{ACC68} t_{OD68}	– 10	– –	65 45	ns ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	65 25	–	–	–	–

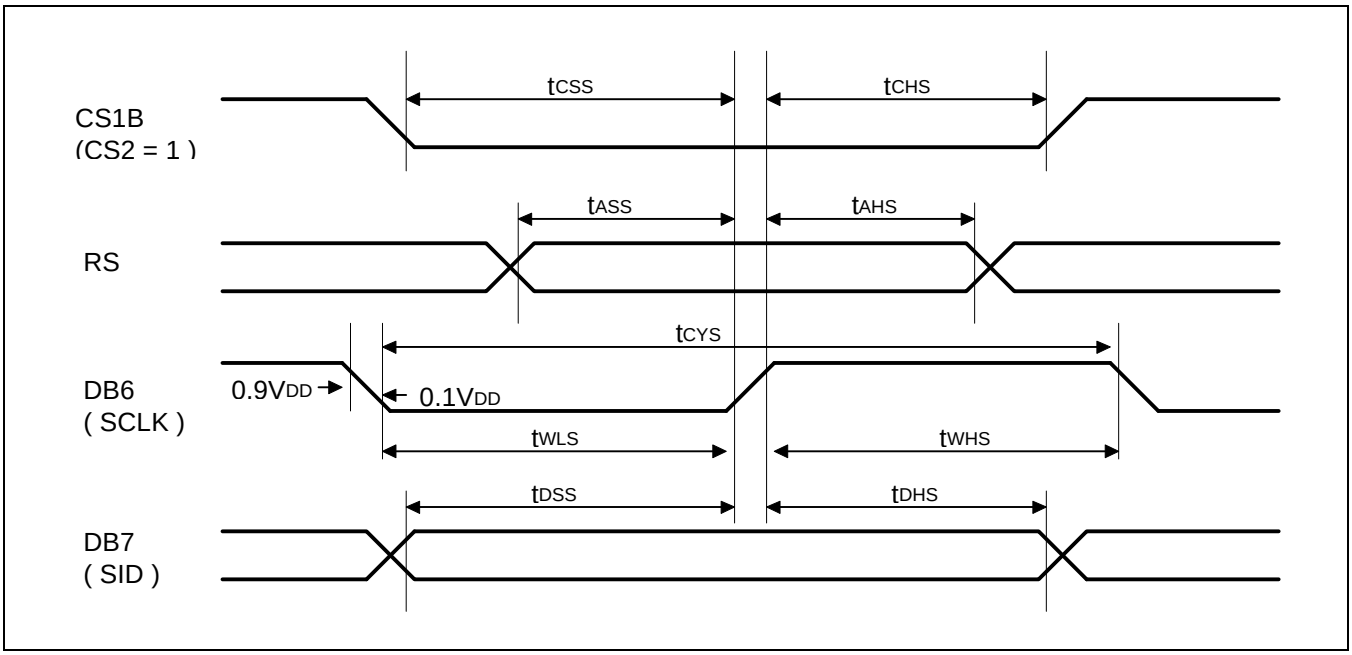


Figure 22. Serial Interface Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	–	–	ns
Data setup time Data hold time	DB7(SID)	t_{DSS} t_{DHS}	90 90	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	55 180	–	–	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	225 90 70	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	45 180	–	–	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	45 45	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	25 90	–	–	ns

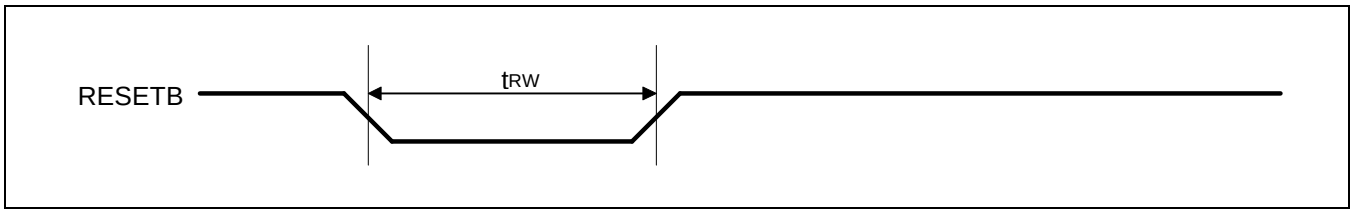


Figure 23. Reset Input Timing

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	900	–	–	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	450	–	–	ns

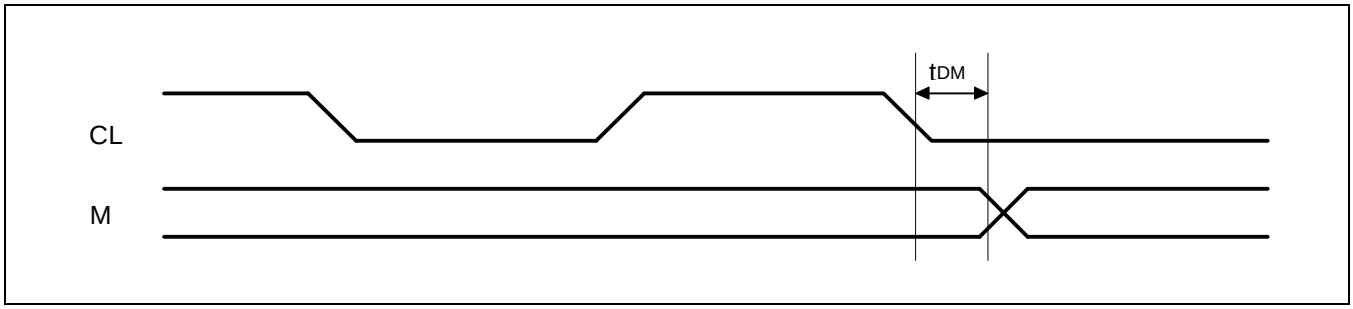


Figure 24. Display Control Output Timing

(V_{DD} = 2.4V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	13	70	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	10	35	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

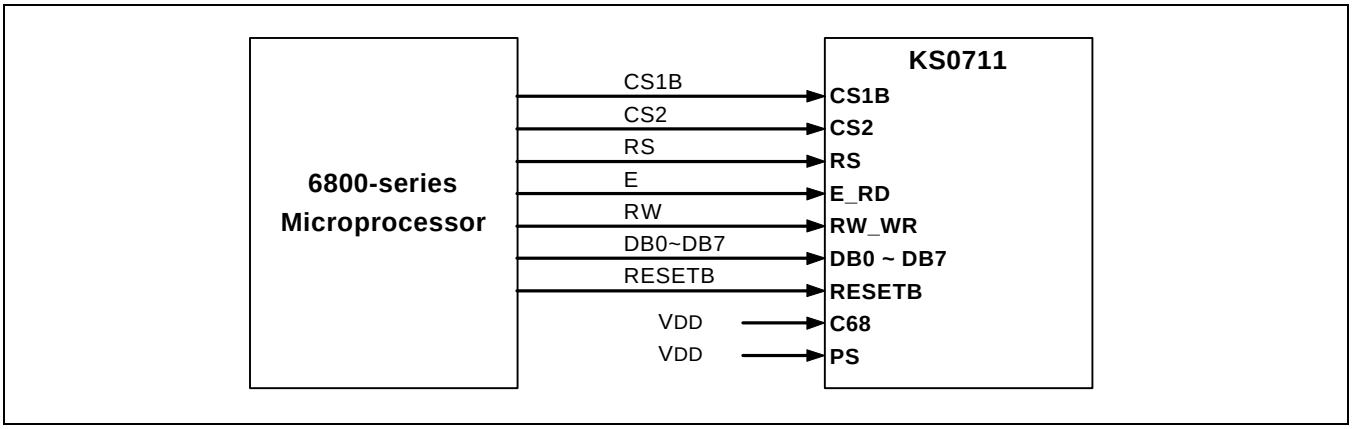


Figure 25. In Case of Interfacing with the 6800_Series (PS = "H", C68 = "H")

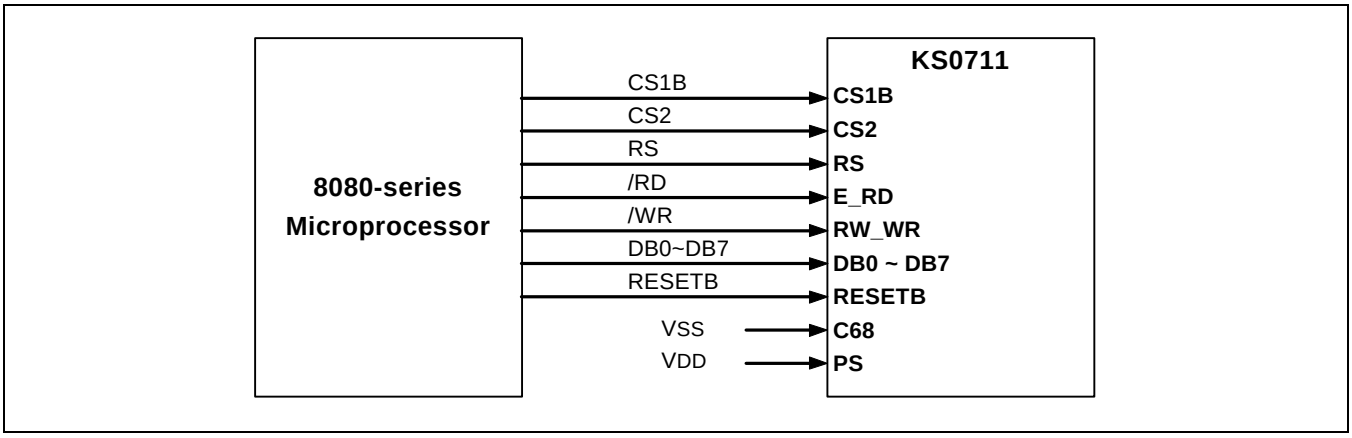


Figure 26. In Case of Interfacing with the 8080-Series (PS = "H", C68 = "L")

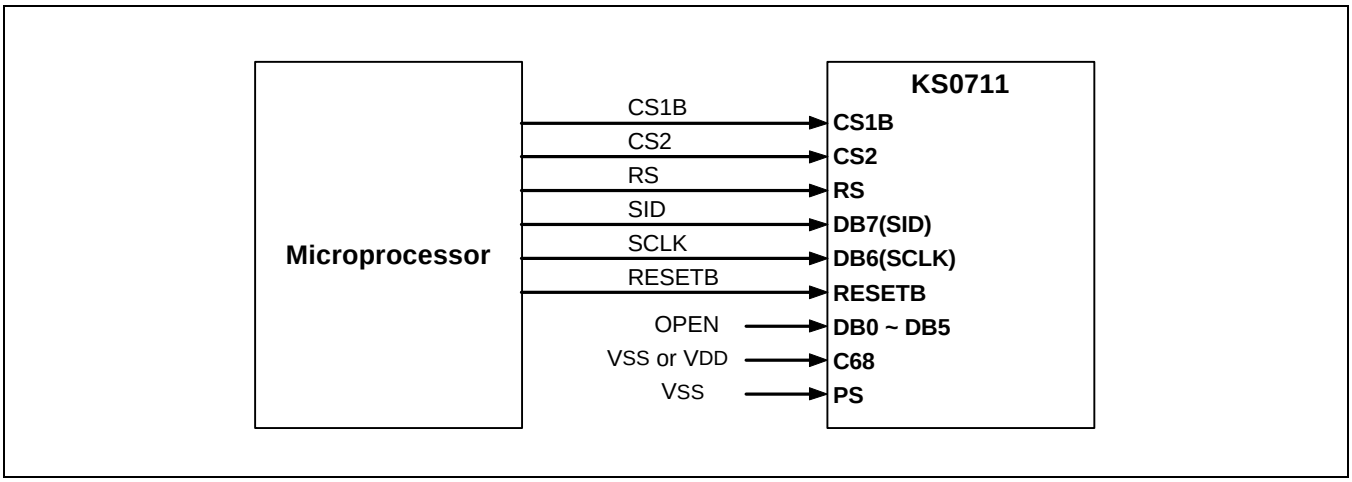
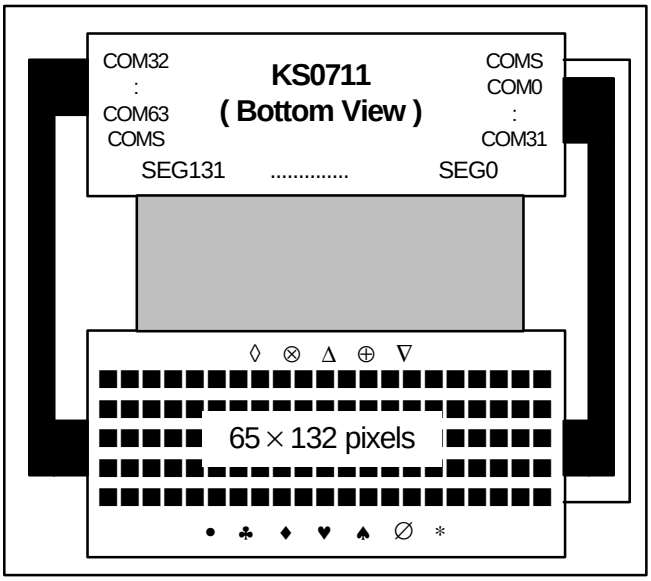


Figure 27. In Case of Serial Interface (PS = "L", C68 = "H/L")

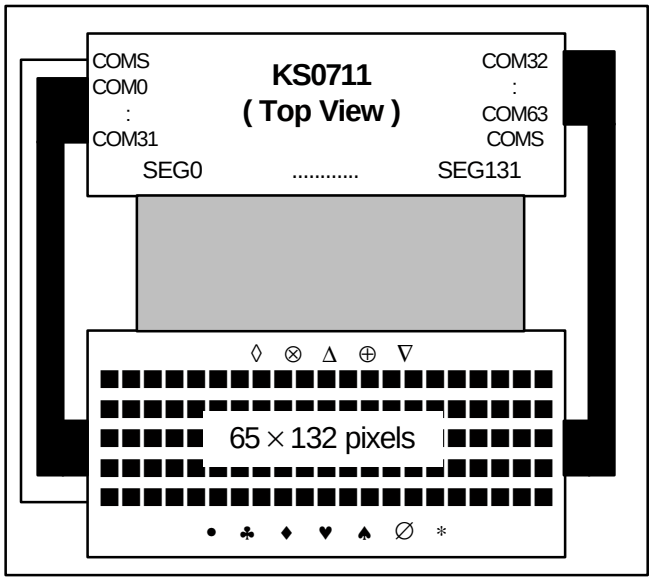
CONNECTIONS BETWEEN KS0717 AND LCD PANEL

Single-Chip Structure (1/55 Duty Configurations)

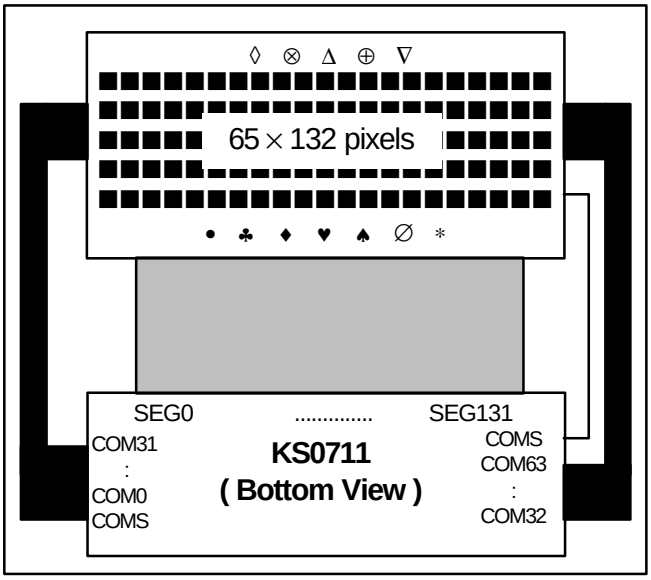
¨ **SHL = 1, ADC = 1**



¨ **SHL = 1, ADC = 0**



¨ **SHL = 0, ADC = 0**



¨ **SHL = 0, ADC = 1**