EG&G RETICON

TC Series
Solid State Line Scanners

General Description

The EG&G Reticon TC series is a family of monolithic self-scanning linear photodiode arrays optimized for application in spectroscopy. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (for example, RL0128TC has 128 elements).

The TC series devices are mounted in ceramic side-brazed dual-inline packages which mate with standard 22-pin integrated circuit sockets. The 128-element array is also available in a ceramic LCC package. Pinout configurations are shown in Figure 1. Package dimensions are shown in the outline drawings of Figure 9. Standard TC devices are sealed with a ground and polished quartz window. However, an optional fiber optic faceplate version is also available for side-brazed packages. The fiber optic faceplate has 6 µm diameter fibers and a numerical aperture of 1.

Key Features

- Simultaneous integration of 128, 256, or 512 photodiode elements with 50 µm center-to-center spacing
- Each sensor element has a 50:1 aspect ratio (50 µm x 2.5 mm)
- Extremely low dark leakage current for longer integration times
- Single-supply operation with HCMOS-compatible inputs
- Static shift register design for simplified clocking requirements
- Differential video output to cancel clock switching transients and Fixed Pattern Noise (FPN)
- Low output capacitance for low noise
- High saturation charge for wide dynamic range
- Antiblooming/Line Reset function
- Wide spectral response
- High UV resistance
- High UV response
- On-chip temperature diodes (2) for temperature monitoring

Sensor Characteristics

The TC series self-scanning photodiode arrays contain 128, 256, or 512 elements (LCC package: 128 elements, only) on 50 µm centers corresponding to a density of 20 diodes/mm and an overall length of 6.4, 12.8, or 25.6 mm. The height of the sensor elements is 2.5 mm giving each element a slit-like geometry with 50:1 aspect ratio suitable for coupling to monochromators or spectrographs. The sensor geometry is shown in Figure 3.

Charge generated by light incident on the p-type surface between two n-regions will divide between the adjacent diodes to produce the response function shown in Figure 3.

Figure 4 shows the typical output charge as a function of exposure at 750 nm wavelength. Exposure in nJ/cm^2 is calculated by multiplying the light intensity in µW/cm^2 by the

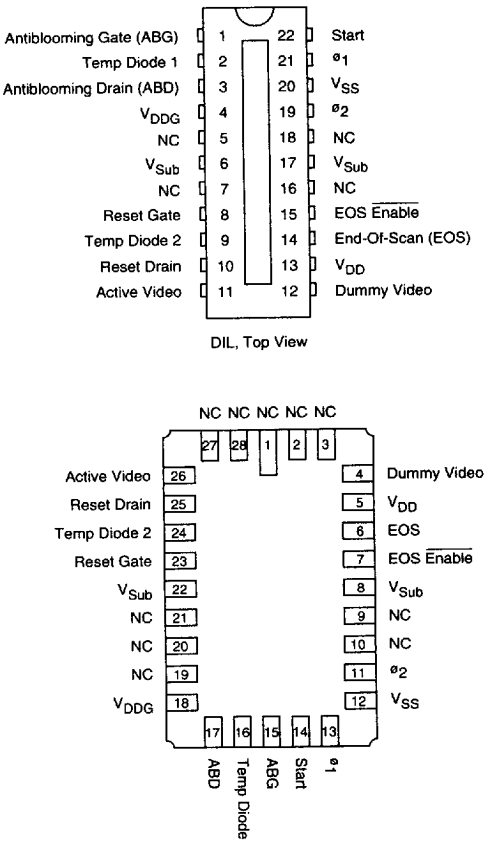


Figure 1. Pinout Configurations

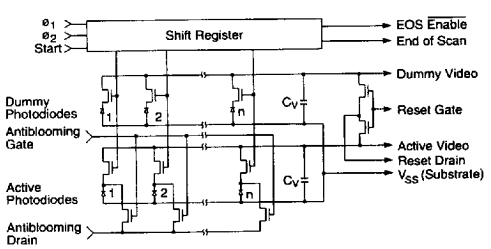


Figure 2. Equivalent Circuit

345 POTRERO AVENUE SUNNYVALE, CALIFORNIA 94086-4197 (408) 738-4266 FAX: (408) 738-6979

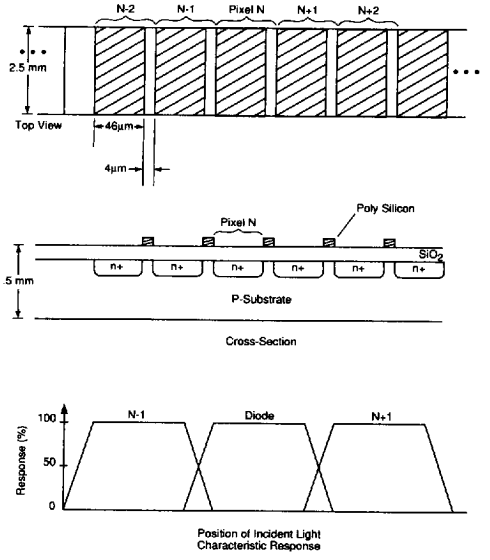


Figure 3. Sensor Geometry and Aperture Response Function

integration time in ms. Note that the response is linear with exposure up to a saturation charge of 20 pC at a saturation exposure of 34 nJ/cm^2. The sensitivity is defined as the ratio of saturation charge to saturation exposure and is 5.4 x 10^{-4} C/J/cm^2 (at 750 nm). Typical relative sensitivity as a function of wavelength is shown in Figure 5. Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (12.5 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm. The dark current of a TC series device is typically .5 pA at 25°C and is a strong function of temperature, approximately doubling for every 7°C increase in temperature. The dark signal charge is given by the dark current multiplied by the integration time. See Table 2 for Electro-optical Characteristics.

Scanning Circuit

The simplified equivalent circuit of a TC series photodiode array is shown in Figure 2. Each cell consists of an active photodiode paired with a dummy photodiode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to active video and dummy video lines. The shift register is driven by complementary square wave clocks with periodic start pulses being introduced to initiate each scan. The pixel sampling rate is determined by the clock frequency. The integration time is the interval between start pulses. The output signal obtained from each scan of an N-element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the active video lines by the multiplex switches. Similar transients are introduced into the dummy video lines and, therefore, can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

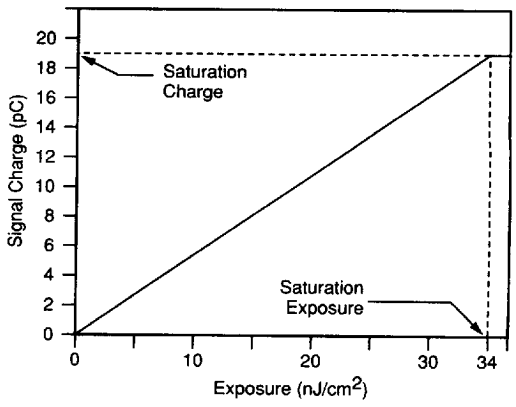


Figure 4. Typical Signal Charge versus Exposure at 750 nm Wavelength

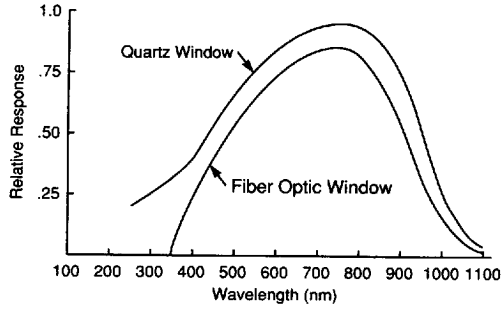


Figure 5. Typical Spectral Response

Clock and Voltage Requirements

Scanning is achieved by means of an integrated shift register. The shift register is driven by complementary square wave clocks, ϕ_1 and ϕ_2. Table 1 gives rise and fall times and crossover points for these clock waveforms. The clock amplitude should be equal to V_{DD} - V_{SS}. With V_{DD} = 5V and V_{SS} = 0V, the clock inputs will be HCMOS-compatible. Since each photodiode is read out on a positive transition of ϕ_2 (see Figure 6), the frequency of the clock signal should be set equal to the desired video data rate.

The start pulse of similar amplitude to the clocks is required to load the shift register and initiate each readout period (each scan of the array). The start pulse is loaded when ϕ_2 is high; the start signal is pulsed high for a minimum of 10 ns during one and only one ϕ_2 clock high cycle. A timing diagram for the start and clock signals is shown in Figure 6. The integration period should be controlled by varying the time between start pulses.

For optimum performance and minimum switching noise, it is important that the clocks are exact complements and that

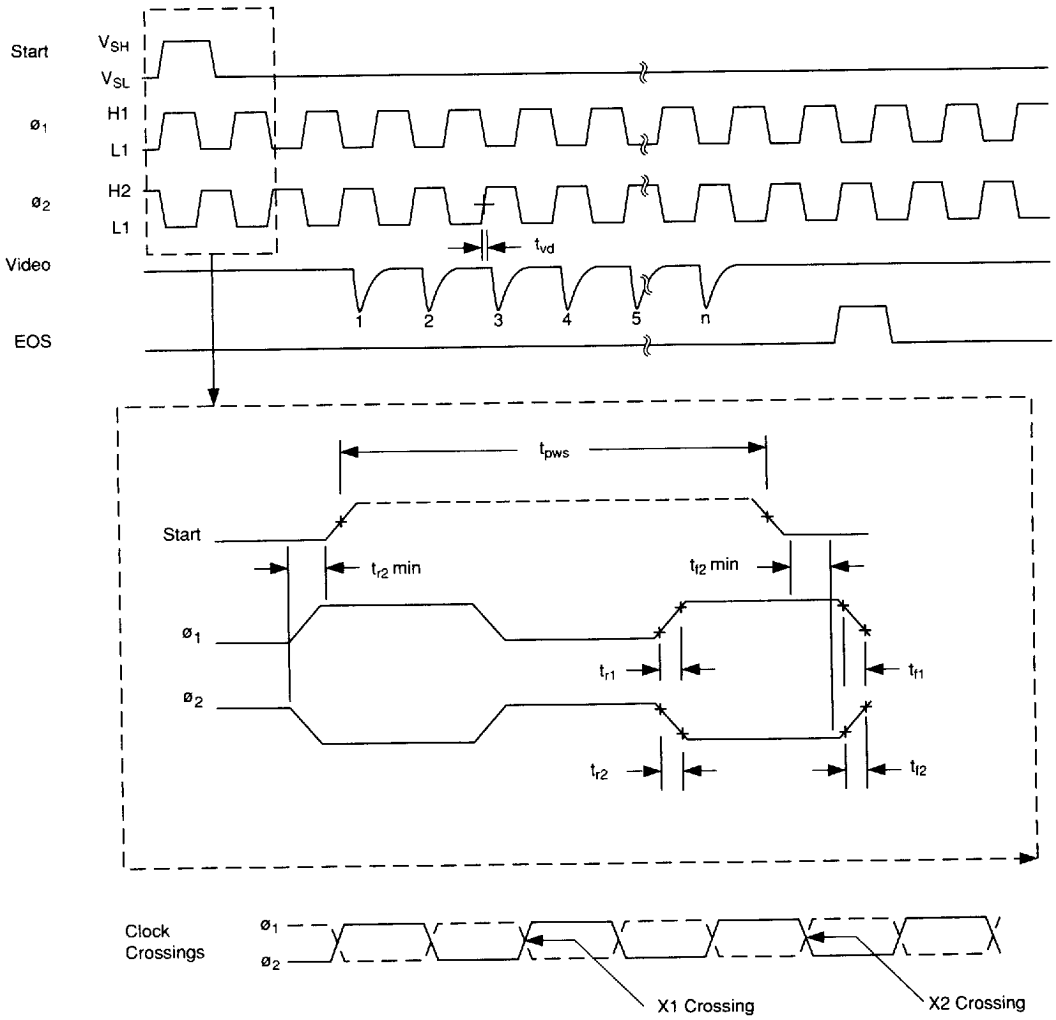


Figure 6. Timing Diagram

their rise and fall times comply with Table 1. A recommended circuit for generating these clocks is shown in Figure 7.

End of Scan (EOS)

An EOS output pulse useful primarily for test purposes is provided two clock cycles after the last photodiode is sampled by the shift register scanning circuit. The timing of the EOS output is shown in Figure 6. The voltage levels on the EOS output will be determined by the V_{DD} and V_{SS} voltage levels supplied to the photodiode array. When V_{DD} is at +5V and V_{SS} is operated at 0V, the EOS output will be compatible with the HCMOS family of logic devices.

Amplifier Requirements

The recommended amplifier for use with the TC devices is a simple current amplifier. A current amplifier holds the video line at a virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses, which each contain a charge of up to 20 pC at saturation, are converted to a train of voltage pulses corresponding to the light intensity on the various diodes. In this mode of operation, the current amplifier must provide a positive bias voltage to the video line since the photodiode anode (the p-substrate) is biased to 0V (V_{SS}). Figure 8

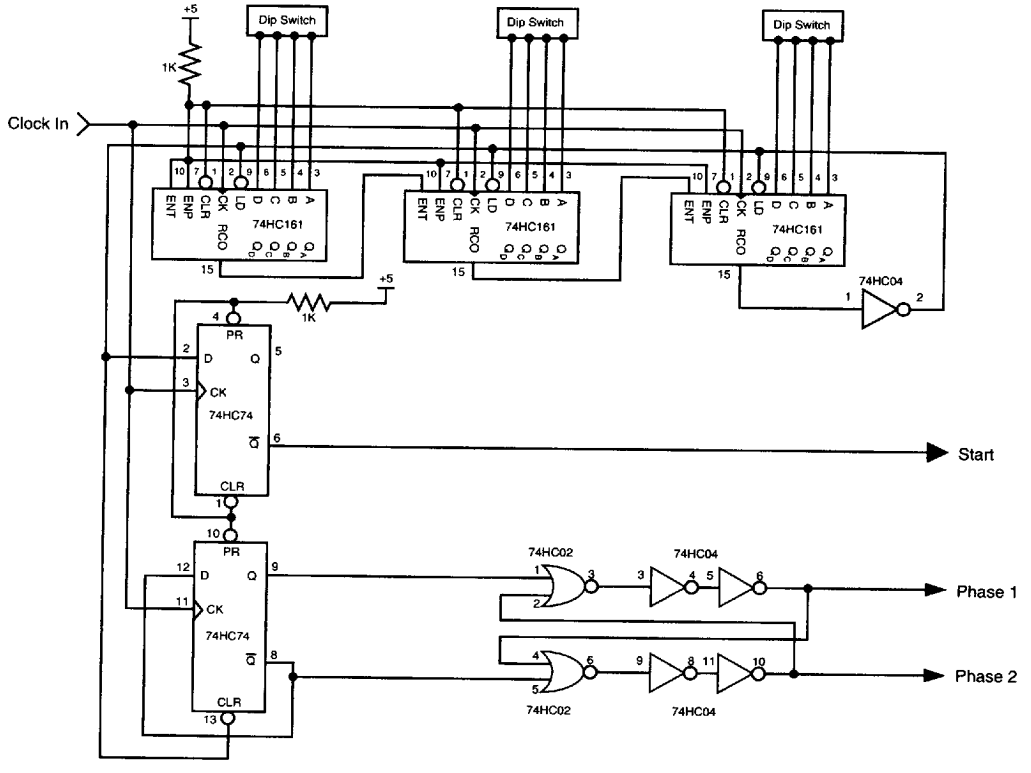


Figure 7. Two-Phase Drive Circuit

shows a differential recharge amplifier suitable for use with TC series devices.

Line Reset/Antiblooming Control

Under certain operating conditions, it may be desirable to control integration time independent of the line scan time (time between start pulses). This can be accomplished by the use of the Antiblooming Gate control input. When the Antiblooming Gate is held at V_{DD}, all photodiodes are simultaneously reset to the bias voltage on the antiblooming drain (the same voltage as the video line bias, typically $V_{DD}/2$). Conversely, when the antiblooming gate is held at V_{SS}, the antiblooming transistor is off and the photodiodes can then integrate photocurrent. Thus, when an active high pulse is applied to V_{ABG}, the integration time for diode 'N' then becomes the time between the negative-going transition of the antiblooming gate input to the time in which diode 'N' is read out through the diode multiplex switch.

Under normal operating conditions, TC series devices do not require any blooming control due to their excellent antiblooming characteristics. However, under extremely high contrast conditions, blooming control can be implemented to further enhance this performance. In this mode of operation, a bias voltage (the same voltage as the video line bias, typically $V_{DD}/2$) is required on the antiblooming drain. The antiblooming gate is then biased to 1-3V. By adjusting the bias level on the antiblooming gate, excess charge present on the video line is shunted to the antiblooming drain.

Dark Signal and Noise

There are two components of the dark signal from the TC series. These are due to: (1) spatial variations in the switching transients coupled into the video line through the clocks and internal multiplex switches, and (2) the integrated dark current. A portion of the switching transient effect will be spatially random and a portion will have the periodicity of the clocks. The latter portion can be minimized by matching the clock amplitudes and rise and fall times and by good circuit layout to minimize capacitance between clocks and video lines. The peak-to-peak fixed pattern due to all switching transient effects should be less than 1% of the saturated signal. The dark signal due to dark current is the dark current multiplied by the integration time. It can be reduced by lowering the temperature or by reducing the integration time.

There are three identifiable sources of readout noise: (1) reset noise, (2) shot noise, and (3) amplifier noise. Reset noise is associated with resetting the diode capacitance to a fixed voltage. Its rms value is given by $(kTC)^{1/2}/q$ where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge and C is the total capacitance of the photo-

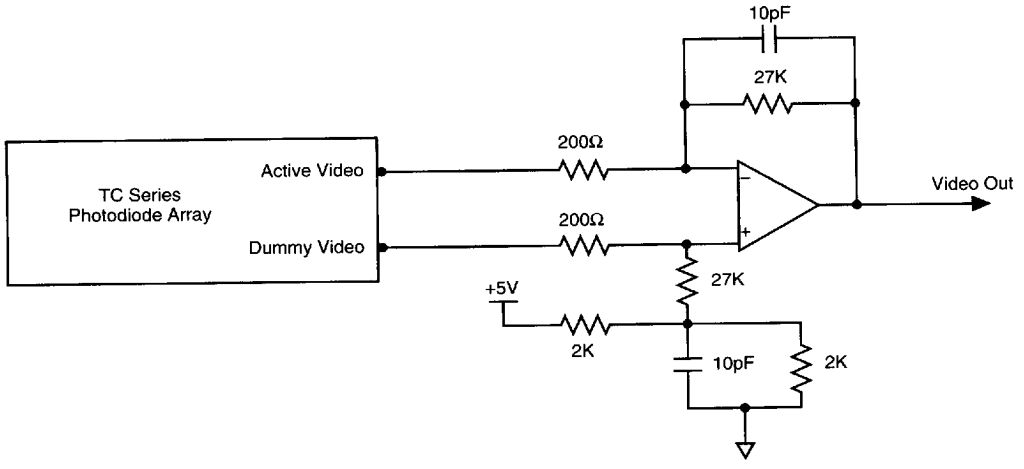


Figure 8. Differential Recharge Mode Video Amplifier

diode (approximately 7 pF), the video line it connects to, and the capacitance of the external circuitry. At room temperature, kTC noise is approximately 1700 electrons rms. It can be reduced somewhat by cooling. The rms value of the dark shot noise is the square root of the number of electrons in the dark signal charge. For example, with a room temperature dark current of .75 pA and 10 ms integration time, the rms dark current shot noise is approximately 210 electrons. Because of the exponential temperature dependence of dark current, shot noise can be reduced dramatically with a moderate amount of cooling. Amplifier noise depends on the amplifier circuit used. In general, the low video output capacitance of the TC series makes it easy to achieve low amplifier noise and values below 2200 electrons are possible.

Temperature Diodes

The TC Series arrays each have 2 on-chip diodes for sensing array temperature. The standard method of use is to force a fixed forward current (normally 10 μA) through the diodes and measure the forward diode voltage drop. For details, please refer to Application Note 130, *How to Use Reticon Temperature Diodes.*

Evaluation Circuit

A complete evaluation circuit for the TC series is available from Reticon (side-brazed packages, only). The RC1032 board provides the user with an easy means of evaluating operation. The RC1032 uses an alternative circuit to that shown in Figure 7.

The RC1032 has a sample-and-held video output with a typical dynamic range of 8,000:1. Provision for cooling the array using a thermal-electric cooler is provided by means of an access hole located directly beneath the array.

The board requires +5 and ±15V supplies and can be adjusted for pixel rates up to 50 kHz.

Table 1. Electrical Characteristics (25°C)
(All voltages measured with respect to V_{Sub})

Signal	Sym		Min	Typ	Max	Units
V_{DD}	V_{DD}		4.5	5	9	V
V_{DD} guard	V_{DDG}			V_{DD}		V
V_{SS}	V_{SS}			0		V
Antiblooming drain	V_{ABD}			V_{SS}		V
Start[1]	V_{Sh}	High	V_{DD} - .1		V_{DD}	V
	V_{Sl}	Low	V_{SS}		V_{SS} + .4	V
Clock $ø_1$, $ø_2$	V_{1h} V_{2h}	High	V_{DD} - .1		V_{DD}	V
	V_{1l}, V_{2l}	Low	V_{SS}		V_{SS} + .4	V
Reset gate	V_{RGh}	High	V_{DD} - .1		V_{DD}	V
	V_{RGl}	Low	V_{SS}		V_{SS} + .4	V
Antiblooming gate	V_{ABGh}	High	V_{DD} - .1		V_{DD}	V
	V_{ABGl}	Low	V_{SS}		V_{SS} + .4	V
Video bias	V_V		2	$V_{DD}/2$	V_{DD} - 2	V
Reset drain	V_{RD}		2	$V_{DD}/2$	V_{DD} - 2	V
Clock rate			.001		10	MHz
Start rise time	t_{rs}			10	50	ns
Start fall time	t_{fs}			10	50	ns
Start pulse width	t_{pws}		10			ns
$ø_1$ rise time [2]	t_{r1}			10	20	ns
$ø_1$ fall time [2]	t_{f1}			10	20	ns
$ø_2$ rise time [2]	t_{r2}			10	20	ns
$ø_2$ fall time [2]	t_{f2}			10	20	ns
Video delay time	t_{VD}			20		ns
Clock crossings	X_1		0		50	%
	X_2		0		50	%
Capacitance $ø_1$, $ø_2$ at 5V bias [3]	C_c					
RL0128TC				33		pF
RL0256TC				38		pF
RL0512TC				44		pF
Capacitance, each video at 2.5V bias [3]	C_v					
RL0128TC				6		pF
RL0256TC				9		pF
RL0512TC				16		pF

Note:
1 Can be TTL.
2 The clock rise and fall times specified are for complementary clocks. The array also can be driven by non-overlapping clocks. There is no restriction on rise and fall time for non-overlapping clocks.
3 Calculated typicals are not measured.

Table 2. Electro-Optical Characteristics (25°C)

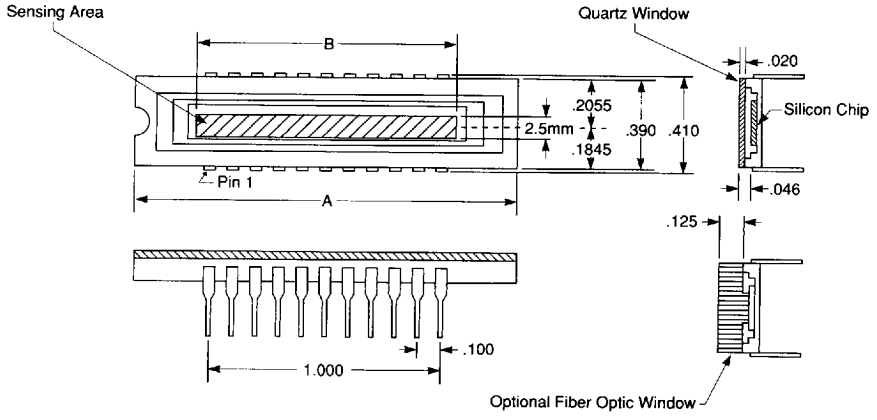
Conditions:
All voltage levels set to typical values shown in Table 1
Light source is 2870°K tungsten filtered with a 750 nm bandpass filter
Video data rate = 250 kHz

Characteristics	Typ	Max	Units
Center-to-center spacing	50		µm
Aperture width	2.5		mm
Sensitivity [1,2,3]	5.4×10^{-4}		$C/J/cm^2$
Photo response nonuniformity			
RL0128TC [2,4,5]	5	10	±%
RL0256TC [2,4,5]	5	10	±%
RL0512TC [2,4,5]	5	10	±%
Saturation exposure (E_{SAT}) [1,2,3]	34		nJ/cm^2
Saturation charge (Q_{SAT})	19		pC
Dynamic range ($Q_{SAT}/Q_{Noise\ (rms)}$)	54,000		
Average dark current [6]	.5	.75	pA
Spectral response peak	750		nm
Spectral response range [5,7]	200-1000		nm

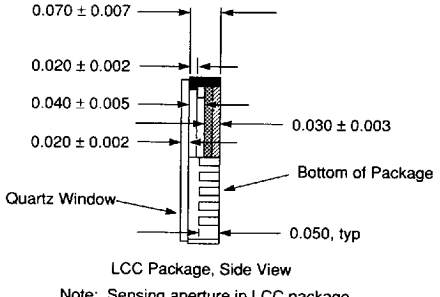
Notes:
1 Measured at 2.5V video line bias
2 Value specified at 750 nm
3 Fiber optic faceplate will modify sensitivity as shown in Figure 5
4 +% PRNU (photo response nonuniformity) is defined as $[(V_{max} - V_{avg})/V_{avg}] \times 100\%$ and -% PRNU is defined as $(V_{avg} - V_{min})/V_{avg}] \times 100\%$, where
V_{max} is the output of the pixel closest to saturation level,
V_{min} is the output of the pixel closest to dark level,
V_{avg} is the numerical average of all the array pixels.
The first and last pixels are not counted in this measurement.
5 Measured at an exposure level of $E_{SAT}/2$
6 Maximum dark current ≤1.5 x average dark current
7 From 250 - 1000 nm, sensitivity is typically at least 20% of its peak value.

Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to common	0	+10	V
Storage of operating temperature			
Quartz window	-78	+85	°C
Fiber optic	-40	+85	°C

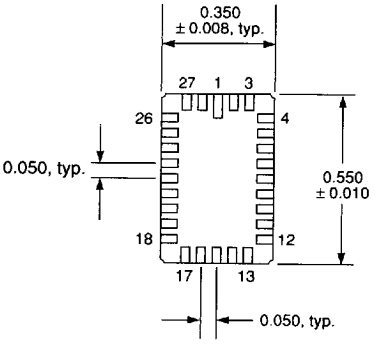


Device	A	B
RL0128TC	1.080	.2520 (6.4 mm)
RL0256TC	1.080	.5039 (12.8 mm)
RL0512TC	1.600	1.008 (25.6 mm)



LCC Package, Side View

Note: Sensing aperture in LCC package is centered with respect to cavity edges.



LCC Package, Bottom View

Figure 9. Package Dimensions (all dimensions are typical and in inches unless otherwise specified)

Ordering Information

Part Number	Evaluation Circuit
Quartz Window	
RL0128TCQ-011	RC1032LNN-020
RL0256TCQ-011	RC1032LNN-020
RL0512TCQ-011	RC1032LNN-020
Fiber Optic Window	
RL0128TCF-011	RC1032LNN-020
RL0256TCF-011	RC1032LNN-020
RL0512TCF-011	RC1032LNN-020
Quartz Window, LCC Package	
RL0128TCQ-111	none

055-0337
May 1994