❑ MN102H74D, MN102H74G

Type	MN102H74D	MN102H74G	MN102HF74G
Internal ROM type	Mask ROM		FLASH
ROM (byte)	64K	128K	
RAM (byte)	4K		
Package (Lead-free)	LQFP100-P-1414		
Minimum Instruction Execution Time	[With main clock operated] 83.3 ns (at 3.0 V to 3.6 V, 12 MHz)		

■ Interrupts

/RST pin, Watchdog, /NMI pin, Timer counter 0 to 9 underflow, Timer counter 10 to 13 under/o Verflow, Timer counter 10 to 13 compare capture A, Timer counter 10 to 13 compare capture B, ATC ch.0 to ch.3 tra nsfer finish, External 0 to 5, Serial ch.0 to ch.3 tra nsmission, Serial ch.0 to ch.3 reception, A/D conversion finish, USB general-purpose, USBSOF, USB end points 1 to 8

■ Timer Counter

Timer counter 0 : 8-bit × 1 (timer output, event count, timer interrupt)
- Clock source..... SYSCLK; XI; prescaler 0; TM0IO pin
- Interrupt source ..... Timer counter 0 underflow

Timer counter 1 : 8-bit × 1 (timer output, event count, timer interrupt)
- Clock source..... SYSCLK; prescaler 0; TM1IO pin
- Interrupt source ..... Timer counter 1 underflow

Connectable Timer counters 0 to 1

Timer counter 2 : 8-bit × 1
(timer output, event count, timer interrupt, A/D conversion start)
- Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 3 underflow; timer counter 4 underflow; TM2IO pin
- Interrupt source ..... Timer counter 2 underflow

Timer counter 3 : 8-bit × 1 (timer output, event count, timer interrupt)
- Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 2 underflow; timer counter 4 underflow; TM3IO pin
- Interrupt source ..... Timer counter 3 underflow

Timer counter 4 : 8-bit × 1 (timer output, event count, timer interrupt)
- Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 2 underflow; timer counter 3 underflow; TM4IO pin
- Interrupt source ..... Timer counter 4 underflow

Timer counter 5 : 8-bit × 1 (timer output, event count, timer interrupt)
- Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 2 underflow; timer counter 3 underflow; timer counter 4 underflow; TM5IO pin
- Interrupt source ..... Timer counter 5 underflow

Connectable Timer counters 2 to 5

Timer counter 6 : 8-bit × 1
(timer output, event count, timer interrupt, serial clock generation)
- Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 7 underflow; timer counter 8 underflow; TM6IO pin
- Interrupt source ..... Timer counter 6 underflow

Timer counter 7 : 8-bit × 1
(timer output, event count, timer interrupt, serial clock generation)
- Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 6 underflow; timer counter 8 underflow; TM7IO pin
- Interrupt source ..... Timer counter 7 underflow

Timer counter 8 : 8-bit × 1
(timer output, event count, timer interrupt, serial clock generation)
Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 6 underflow; timer counter 7 underflow; TM8IO pin
Interrupt source ..... Timer counter 8 underflow

Timer counter 9 : 8-bit × 1 (timer output, event count, timer interrupt)
Clock source..... SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 6 underflow; timer counter 7 underflow; timer counter 8 underflow; TM9IO pin
Interrupt source ..... Timer counter 9 underflow

Connectable Timer counters 6 to 9

Timer counter 10 : 16-bit × 1
(timer output, event count, input capture, PWM output, 2-phase encoder input)
Clock source..... SYSCLK; 1/8 of SYSCLK; timer counter 2 or 3 underflow; 2-phase encoding of TM10IOA/TM10IOB pin (1×, 4×); TM10IOB pin
Interrupt source ..... Timer counter 10 under/overflow; timer counter 10 compare capture A; timer counter 10 compare capture B

Timer counter 11 : 16-bit × 1
(timer output, event count, input capture, PWM output, 2-phase encoder input)
Clock source..... SYSCLK; 1/8 of SYSCLK; timer counter 8 or 9 underflow; 2-phase encoding of TM11IOA/TM11IOB pin (1×, 4×); TM11IOB pin
Interrupt source ..... Timer counter 11 under/overflow; timer counter 11 compare capture A; timer counter 11 compare capture B

Timer counter 12 : 16-bit × 1
(timer output, event count, input capture, PWM output, 2-phase encoder input)
Clock source..... SYSCLK; 1/8 of SYSCLK; timer counter 4 or 5 underflow; 2-phase encoding of TM12IOA/TM12IOB pin (1×, 4×); TM12IOB pin
Interrupt source ..... Timer counter 12 under/overflow; timer counter 12 compare capture A; timer counter 12 compare capture B

Timer counter 13 : 16-bit × 1
(timer output, event count, input capture, PWM output, 2-phase encoder input)
Clock source..... SYSCLK; 1/8 of SYSCLK; timer counter 6 or 7 underflow; 2-phase encoding of TM13IOA/TM13IOB pin (1×, 4×); TM13IOB pin
Interrupt source ..... Timer counter 13 under/overflow; timer counter 13 compare capture A; timer counter 13 compare capture B

■ Serial interface

Serial 0 : 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length)
Clock source..... 1/2 or 1/16 of timer counter 6 underflow; external pin

Serial 1 : 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length)
Clock source..... 1/2 or 1/16 of timer counter 7 underflow; external pin

Serial 2 : 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length)
Clock source..... 1/2 or 1/16 of timer counter 8 underflow; external pin

Serial 3 : 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length)
Clock source..... 1/2 or 1/16 of timer counter 9 underflow; external pin

UART × 4 (common use with serial 0 to 3)

I²C × 2 (common use with serial 0, 1; single master)

■ DMA controller

4-ch.
DMA transfer enabled between memory and memory or memory and peripheral register by set interrupt factor and software activation setting
Transfer unit : bytes/word
Transfer mode : 1 word/burst (max. 128 K bytes)
Transfer addressing : source/destination pointer fix/increment
High-speed transfer enabled between USB-FIFO and internal RAM in single address mode

■ USB Functions

Conforms to USB1.1.
USB transceiver built-in
Full-speed (12 Mbps) supported.
9 end points (FIFO built-in independently)
FIFO size
(EP0, 1, 2, 3, 4, 5, 6, 7, 8) : 64, 128, 128, 128, 128, 128, 128, 128, 128 bytes
・EP0
Control transfer
IN/OUT (two ways)
・EP1 to EP8
Interrupt/Bulk/Isochronous transfer supported.
Settable to IN or OUT.
Double Buffering function supported.
When the MAXP size is set to a half or less of the MAXFIFO size for each EP, the Double Buffering function is made valid automatically.

■ I/O Pins

I/O	77	Common use : 77 (pull-up resistance specifiable)

■ A/D converter

10-bit × 8-ch. (with S/H)

■ Special Ports

USB ports (D+, D-)

■ Notes

4 multiply PLL built-in, generation of internal 48 MHz at external oscillation 12 MHz

■ Electrical Charactreistics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 12 MHz , VDD = 3.3 V			65+10α*	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level f = 12 MHz , VDD = 3.3 V, output open			70	μA
Supply current at HALT0	IDDH				30+10α*	mA

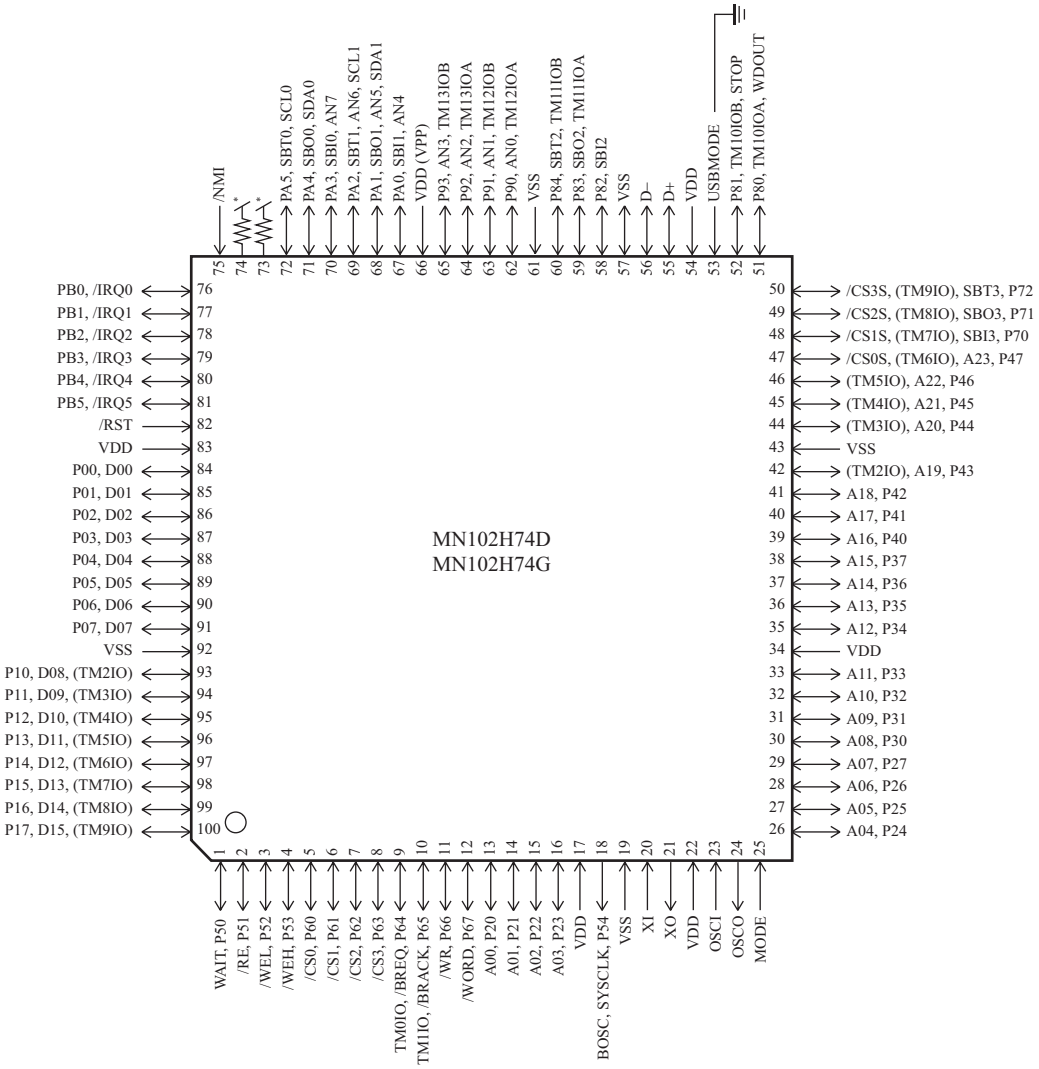
(Ta = –20°C to +70°C , VDD = 3.3 V, VSS = 0 V)

Note) * "α" depends on products.
MN102H74D, MN102H74G α= 0
MN102HF74G α = 1

■ Development tools

In-circuit Emulator
PX-ICE102H74-LQFP100-P-1414

■ Pin Assignment



LQFP100-P-1414

Note ∗: Use 4.7 kΩ to 10 kΩ

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