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S4521

AMERICAN MICROSYSTEMS, INC.

32 Bit Driver

August 1996

Features

- Drives Up to 32 Devices
- Cascadable
- On Chip Oscillator
- Requires Only 3 Control Lines
- CMOS Construction For:
  Wide Supply Range
  High Noise Immunity
  Wide Temperature Range

Applications:

- Liquid Crystal Displays
- LED and Incandescent Displays
- Solenoids
- Print Head Drives
- DC and Stepping Motors
- Relays

General Description

The S4521 is an MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the drivers. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to driving liquid crystal displays, with a backplane A.C. signal option that is provided. The A.C. frequency of the backplane output that can be user supplied or generated by attaching a capacitor to the LCD_f input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

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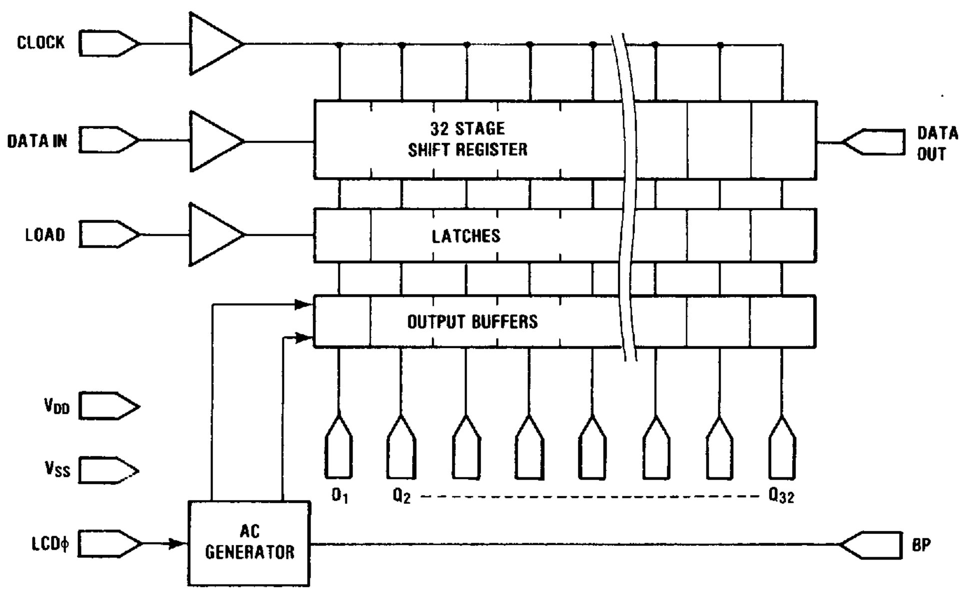
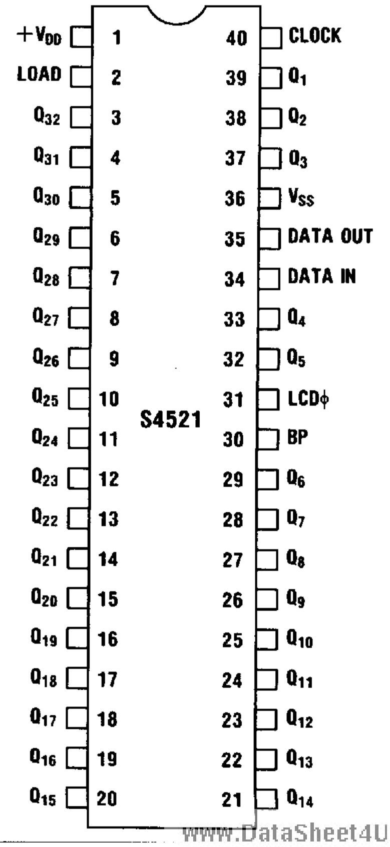
Functional Block Diagram



Pin Configuration



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Absolute Maximum Ratings

V_{DD}	−0.3 to +17V
Inputs (CLK, DATA IN, LOAD, LCDϕ)	$V_{SS}-0.3$ to $V_{DD}+0.3V$
Power Dissipation	250mW
Storage Temperature	−65°C to +125°C
Operating Temperature	−40°C to +85°C

Electrical Characteristics: $3V \leq V_{DD} \leq 13V$, unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	3	13	V	
	Supply Current				
I_{DD1}	Operating		200	μA	f_{BP} = 120Hz, No Load, $V_{DD}=5V$
I_{DD2}	Quiescent		200	μA	LCDϕ High or Low, $f_{BP}=0$ Load @ Logic 0, $V_{DD}=5V$
	Inputs (CLK, DATA IN, LOAD)				
V_{IH}	High Level	0.6 V_{DD}	V_{DD}	V	$3V \leq V_{DD} < 5V$
		0.5 V_{DD}	V_{DD}	V	$5V \leq V_{DD} \leq 13V$
V_{IL}	Low Level	V_{SS}	0.2 V_{DD}	V	
I_L	Input Current		5	μA	
C_I	Input Capacitance		5	pF	
f_{CLK}	CLK Rate	DC	2	MHz	50% Duty Cycle
t_{DS}	Data Set-Up Time	100		ns	Data Change to CLK Falling Edge
t_{DH}	Data Hold Time	10		ns	Falling CLK Edge to Data Change
t_{PW}	Load Pulse Width	200		ns	
t_{PD}	Data Out Prop. Delay		220	ns	$C_L=30pF$, From Rising CLK Edge
t_{LC}	Load Pulse Set-Up	300		ns	Falling CLK Edge to Rising Load Pulse
t_{LCD}	Load Pulse Delay	0		ns	Falling Load Pulse to Falling CLK Edge
V_{OAVG}	DC Bias (Average) Any Q Output to Backplane		±25	mV	f_{BP} = 120Hz
V_{IH}	LCDϕ Input High Level	.9 V_{DD}	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{SS}	.1 V_{DD}	V	Externally Driven
	Capacitance Loads				
C_{LQ}	Q Output		50,000	pF	f_{BP} = 120Hz
C_{LBP}	Backplane		1.5	μF	f_{BP} = 120Hz, See Note 8
R_{ON}	Q Output Impedance		3.0	KΩ	I_L = 10μA, $V_{DD}=5V$
R_{ON}	Backplane Output Impedance		100	Ω	I_L = 10μA, $V_{DD}=5V$
R_{ON}	Data Out Output Impedance		3.0	KΩ	I_L = 10μA, $V_{DD}=5V$

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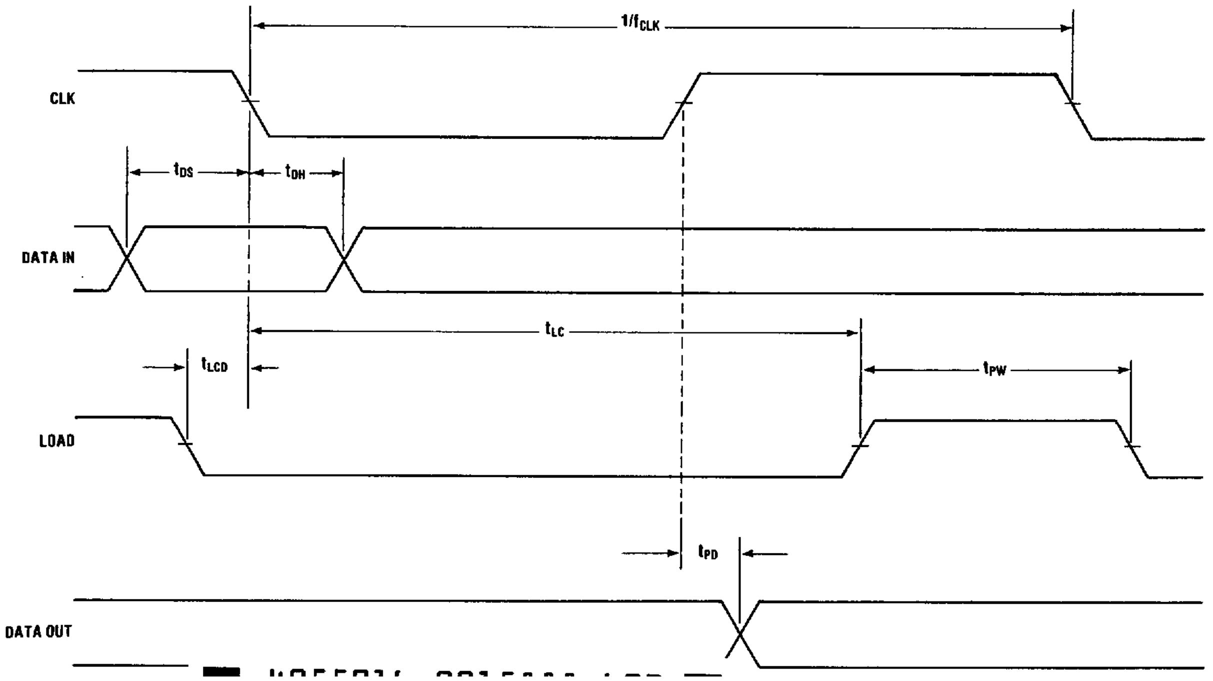
Operating Notes

1. The shift register shifts on the falling edge of CLK. It outputs on the rising edge of the CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q10 was input 10 clock pulses earlier).
3. A logic 1 on Data In causes a Q output to be out of phase with the Backplane.
4. A logic 1 on Load causes a parallel load of the data in the shift register, into the latches that control the Q output drivers.
5. To cascade units, (a) connect the Data Out of one chip to Data In of next chip, and (b) either connect Backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) or connect LCDϕ of all chips to a common driving signal. If the former is chosen, the Backplane that is tied to the LCDϕ inputs of the other chips should **not** also be connected to the Backplanes of those chips.
6. If LCDϕ is driven, it is in phase with the Backplane output.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 32 of the LCDϕ frequency, in the self-oscillating mode.
8. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 0.2 \div C(\text{in } \mu F)$ at $V_{DD} = 5V$.
9. If the total display capacitance is greater than 100,000 pF, a decoupling capacitor of 1μF is required across the power supply (pins 1 and 36).

Pin Description

Pin #	Name	Description
1	V_{DD}	Logic and Q Output Supply Voltage
2	LOAD	Signal to Latch Data from Registers
30	BP	Backplane Drive Output
31	LCDϕ	Backplane Drive Input
34	DATA IN	Data Input to Shift Register
35	DATA OUT	Data Output from Shift Register-primarily used in cascading
36	V_{SS}	Ground Connection
40	CLOCK	System Clock Input
3-29, 32-33, 37-39	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams



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