CMOS CROSSPOINT SWITCH WITH CONTROL MEMORY
MMC 355 — SERIAL SWITCH ADDRESSING
MMC 356 — PARALLEL SWITCH ADDRESSING

GENERAL DESCRIPTION

The MMC 355 and MMC 356 are CMOS integrated circuits containing a 8x8 array of digitally controlled analog switches together with control memory, address decoders and level translators. The array is organized as 8 multiplexers with common inputs. The multiplexers can be individually inhibited. Any of the 8 multiplexers can be addressed by selecting the appropriate 7 bits (address and inhibit) of the programming word.
For the MMC 355 the address and inhibit bits are loaded serially into an internal shift register on the leading edge of clock signal. For the MMC 356 the programming word is loaded parallely. This operation is performed when the select inputs ($\overline{S}_1$, $\overline{S}_2$, S_3 for the MMC 355; S_1, S_2 for the MMC 356) are properly set.
The presence of multiple select inputs facilitates the array connection of such circuits. When the required operating power is applied, the states of the 64 switches must be turned off by inhibiting all the multiplexers in succession.
The MMC 355 and MMC 356 are housed in a 24-pin and a 28-pin dual-in-line package, respectively.

FEATURES

- Low "on" resistance: 125 Ω (typ.) over 15 Vp.p. signal-input range for $V_{DD}-V_{EE}=15V$
- High "off" resistance: channel leakage: ±500 nA (max) for $V_{DD}-V_{EE}=15V$
- Internal memory
- Large analog signal capability
- High cross-talk off-state insolation
- Pull-up or pull-down resistors on all digital inputs
- Low power, high noise immunity CMOS technology
- Serial switch addressing, 3 select inputs (MMC 355)
- Parallel switch addressing, 2 select inputs (MMC 356)

TYPICAL APPLICATIONS

- Telephone switching systems
- Analog or digital multiplexers
- Data acquisition systems
- Test equipments

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	−0.5	to	20	V
		E and F types	−0.5	to	18	V
V_I	Input voltage		−0.5	to	V_{DD}+0.5	V
I_I	DC input current (anyone input)				±10	mA
Ptot	Total power dissipation (per package)					
	MMC 355				400	mW
	MMC 356				400	
	Dissipation per output transistor for T_{op} = full package-temperature range				100	mW
T_A	Operating temperature:	G and H types	−55	to	125	°C
		E and F types	−40	to	85	°C
T_{stg}	Storage temperature		−65	to	150	°C

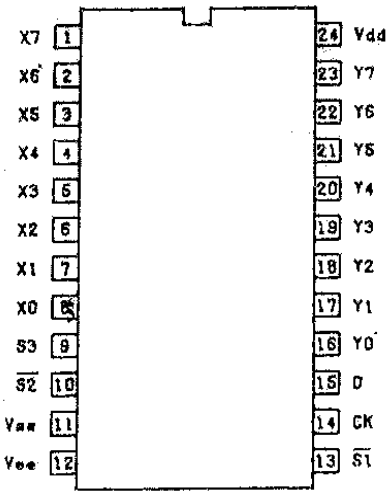
* All voltages are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

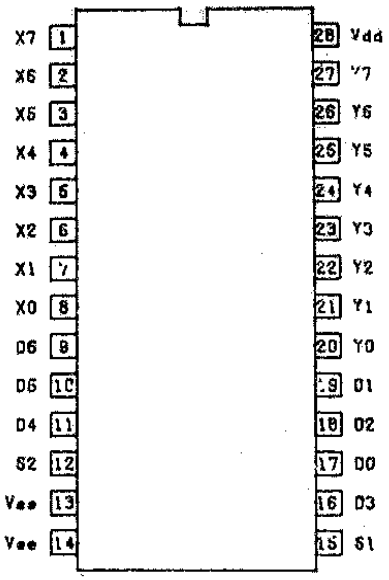
V_{DD}*	Supply voltage:	G and H types	3	to	18	V
		E and F types	3	to	15	V
V_I	Input voltage		0	to	V_{DD}	V
T_A	Operating temperature:	G and H types	−55	to	125	°C
		E and F types	−40	to	85	°C

CONNECTION DIAGRAMS

MMC 355

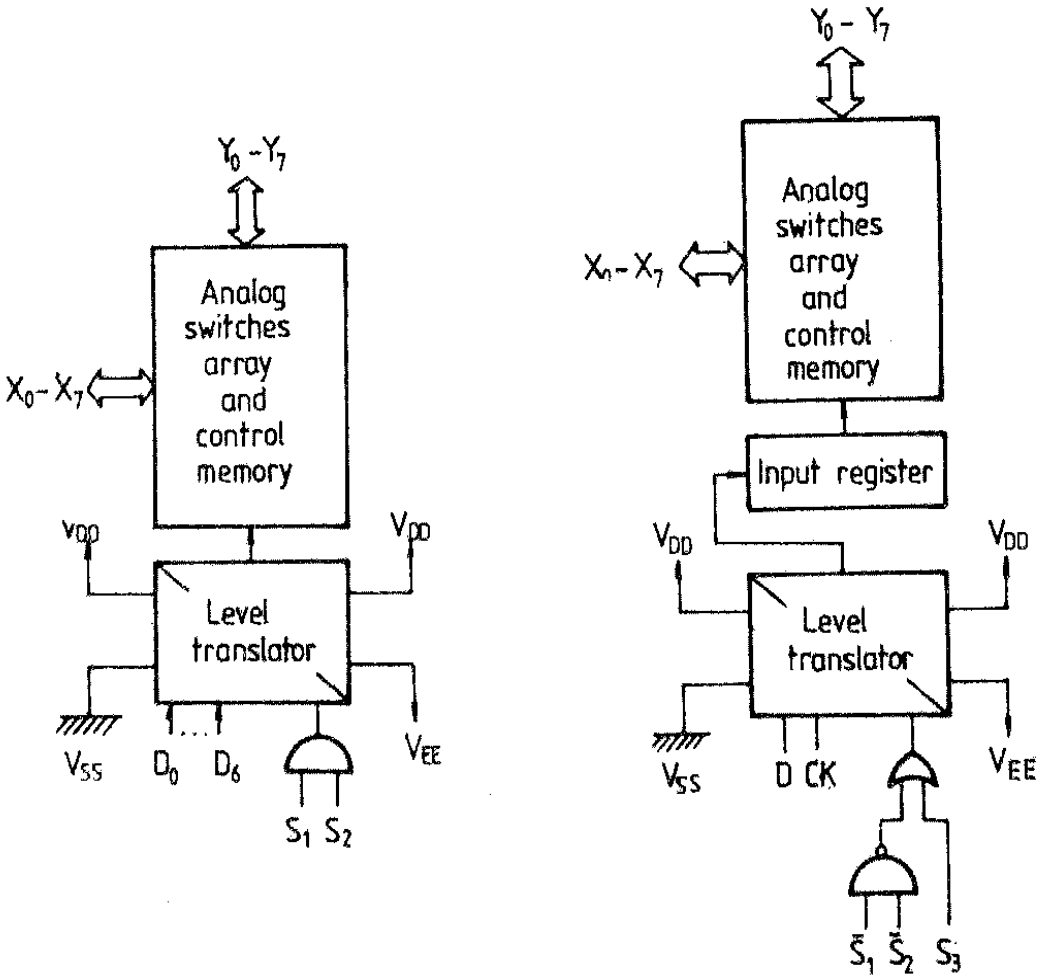


MMC 356

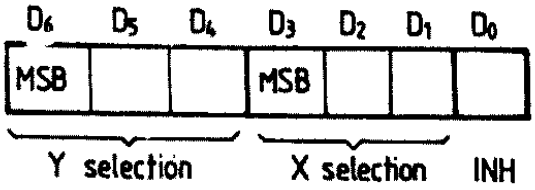


BLOCK DIAGRAMS

MMC 356



PROGRAMMING WORD



TRUTH TABLE

ADDRESS							CONNECTION
DY_2	DY_1	DY_0	DX_2	DX_1	DX_0	INH	
0	0	0	X	X	X	0	MUX 0 inhibited
0	0	1	X	X	X	0	MUX 1 inhibited
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	X	X	X	0	MUX 7 inhibited
0	0	0	0	0	0	1	X0—Y0
0	0	0	0	0	1	1	X1—Y0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
0	0	0	1	1	1	1	X7—Y0
0	0	1	0	0	0	1	X0—Y1
0	0	1	0	0	1	1	X1—Y1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
0	0	1	1	1	1	1	X7—Y1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	0	0	0	1	X0—Y7
1	1	1	0	0	1	1	X1—Y7
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	X7—Y7

X — Don't care

STATIC ELECTRICAL CHARACTERISTICS
(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES			UNIT
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	Min.	Typ.	Max.	
I_{DD}	Quiescent device current		0 0 0	0 0 0	5 10 15			60 150 2500	µA
SWITCH									
R_{ON}	ON resistance	$0 \leq V_I \leq V_{DD}$	0	0	5 10 15		470 180 125	1050 400 280	Ω
ΔR_{ON}	(between any 2 channels)		0	0	5 10 15		15 15 10		Ω
OFF channel leakage current(•)	All switch OFF		0	0	15			500	nA
C capacitance	Input output feedthrough		−5	−5	5		35		pF
CONTROL									
V_{IL}	Input low voltage	=V_{DD} through 1 kΩ	V_{EE}=V_{SS} R_L=1 kΩ to V_{SS}		5 10 15			1,5 3 4	V
V_{IH}	Input high voltage		$I_{IS} < 2$ µA on all OFF channels		5 10 15	3,5 7 11			V
I_I(••)	Input current (Any control input)		V_I=0/15 V		15			60	µA
C_I	Input capacitance (Any data or select input)						5	7,5	pF

(•) Determined by minimum feasible leakage measurement for automatic testing

(••)

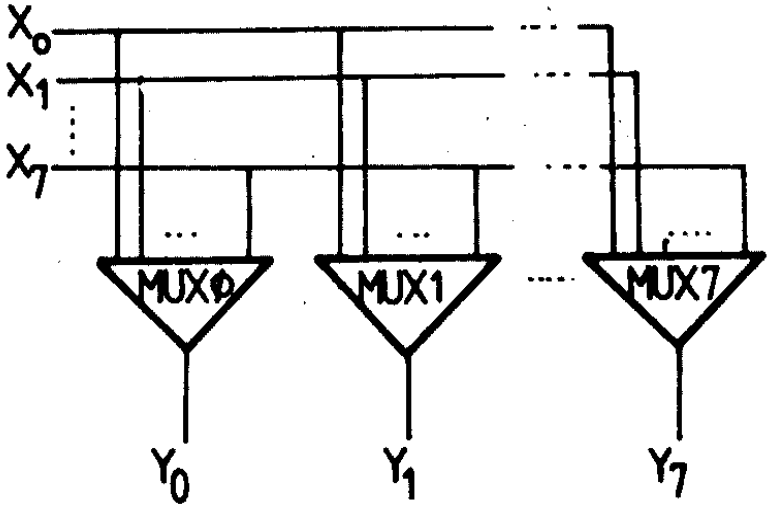
MMC 355: The D, $\overline{S}_1$, $\overline{S}_2$ inputs are tied to V_{DD} through a pull-up resistor.
The CK and S_3 inputs are tied to V_{SS} through a pull-down resistor.

MMC 356: The D_0—D_8, S_1, S_2 inputs are tied to V_{DD} through a pull-up resistors.

CIRCUITS DESCRIPTION

The MMC 355 and MMC 356 are CMOS integrated circuits containing 64 digitally controlled analog switches, control memory, decoders, level translators and addressing logic.

The switches array and the input logic are powered between V_{DD} and V_{EE} and between V_{DD} and V_{SS} respectively.
The analog switches array is organized as eight 8,1 common inputs (X_0, X_1...X_7) multiplexers the outputs being Y_0, Y_1...Y_7



Crospoint array

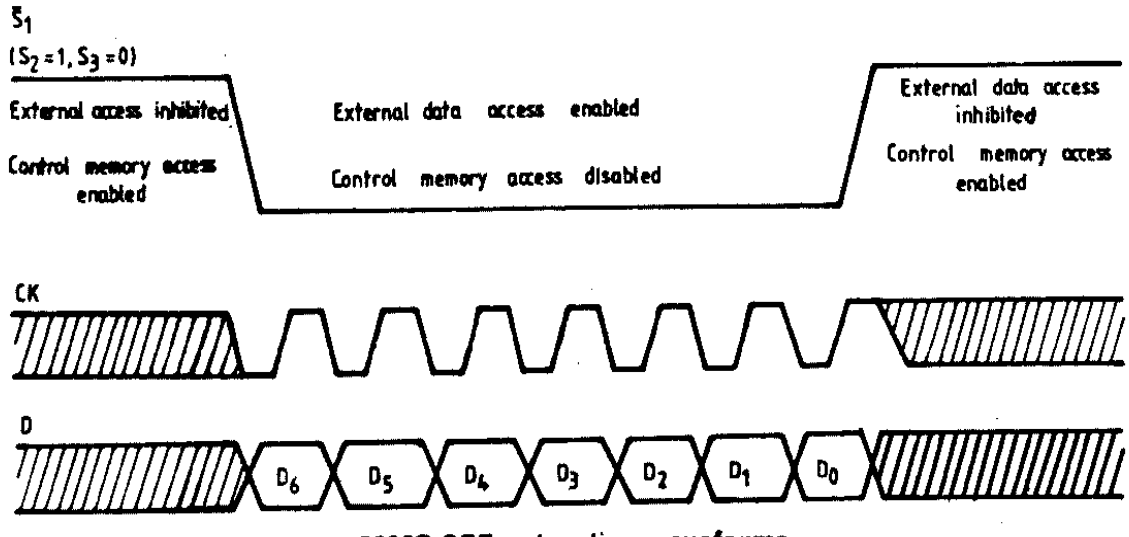
Each multiplexer can be inhibited (all its switches are off).
Each multiplexer must be separately programmed. The programming word is 7 bits long (D_6, D_5,...,D_0). The bit allocation follows:

D_6	D_5	D_4	D_3	D_2	D_1	D_0
DY2	DY1	DY0	DX2	DX1	DX0	INH

$Y_{selection}$ (MUX selection) — $X_{selection}$ (Switch selection) — Inhibit

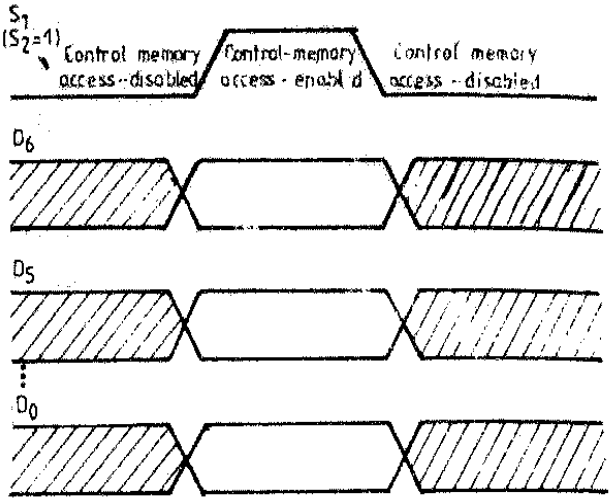
At a time, no more than one channel can be ON in every multiplexer. Thus, in the whole array, a maximum of 8 switches are ON simultaneously.

The D_6, D_5, D_4 bits select the multiplexer the D_3, D_2 D_1 bits select the channel. If $D_0 = 0$, the multiplexer is inhibited (all channels OFF).
If $D_0 = 1$, the channel selected by the D_3, D_2, D_1 will be ON.
The control memory retains the state of every switch.
When the operating power supply is applied, the states of the analog switches are indeterminate. Therefore, all the multiplexer must be turned off, or properly programmed (8 steps).
The programming word can be serially (MMC 355) or parallely (MMC 356) loaded.
The MMC 355 contains a serial input (D) shift register. The loading is performed on the leading edge of the CK signal, and begins with the D_6 bit.
The operation is accomplished only if the select inputs combination ($\bar{S}_1 \cdot \bar{S}_2 \cdot S_3$) is at logic 1. (See fig below)

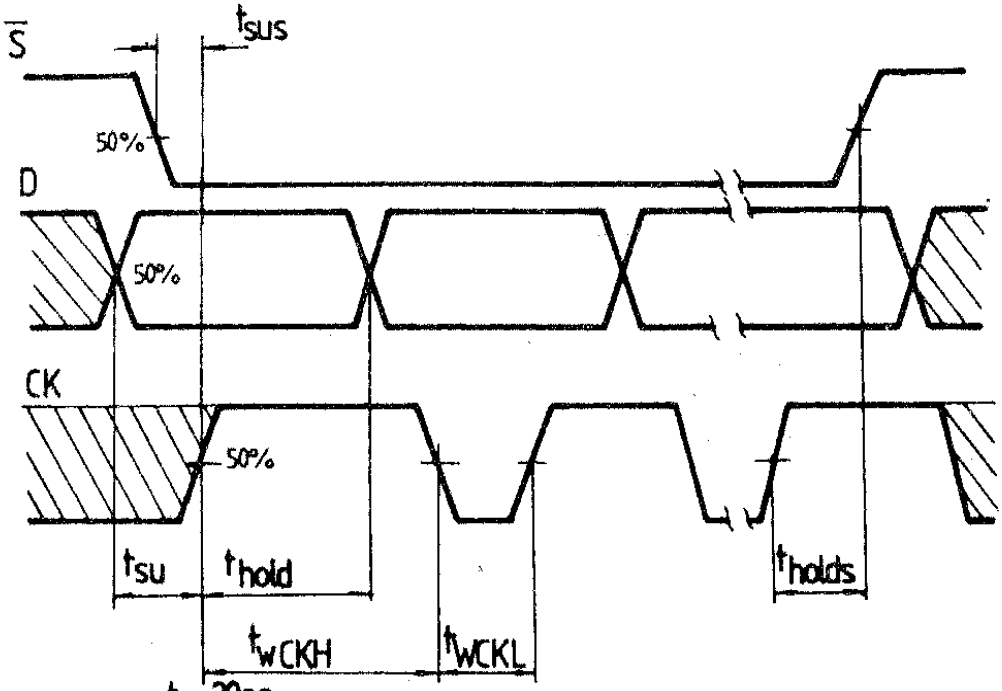


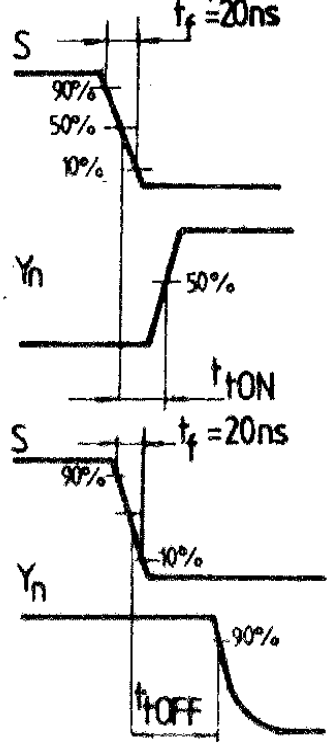
MMC 355 — Loading waveforms

As long as the selection signals are active, the data are shifted through the register without affecting the memory status. When the selection signals are disabled, the information passes from the shift register into the control memory.
For the MMC 356 version, the programming word is loaded directly in the control memory, as long as the select signal is active ($S_1 \cdot S_2$ is at logic 1).



MMC 356 — Loading waveforms



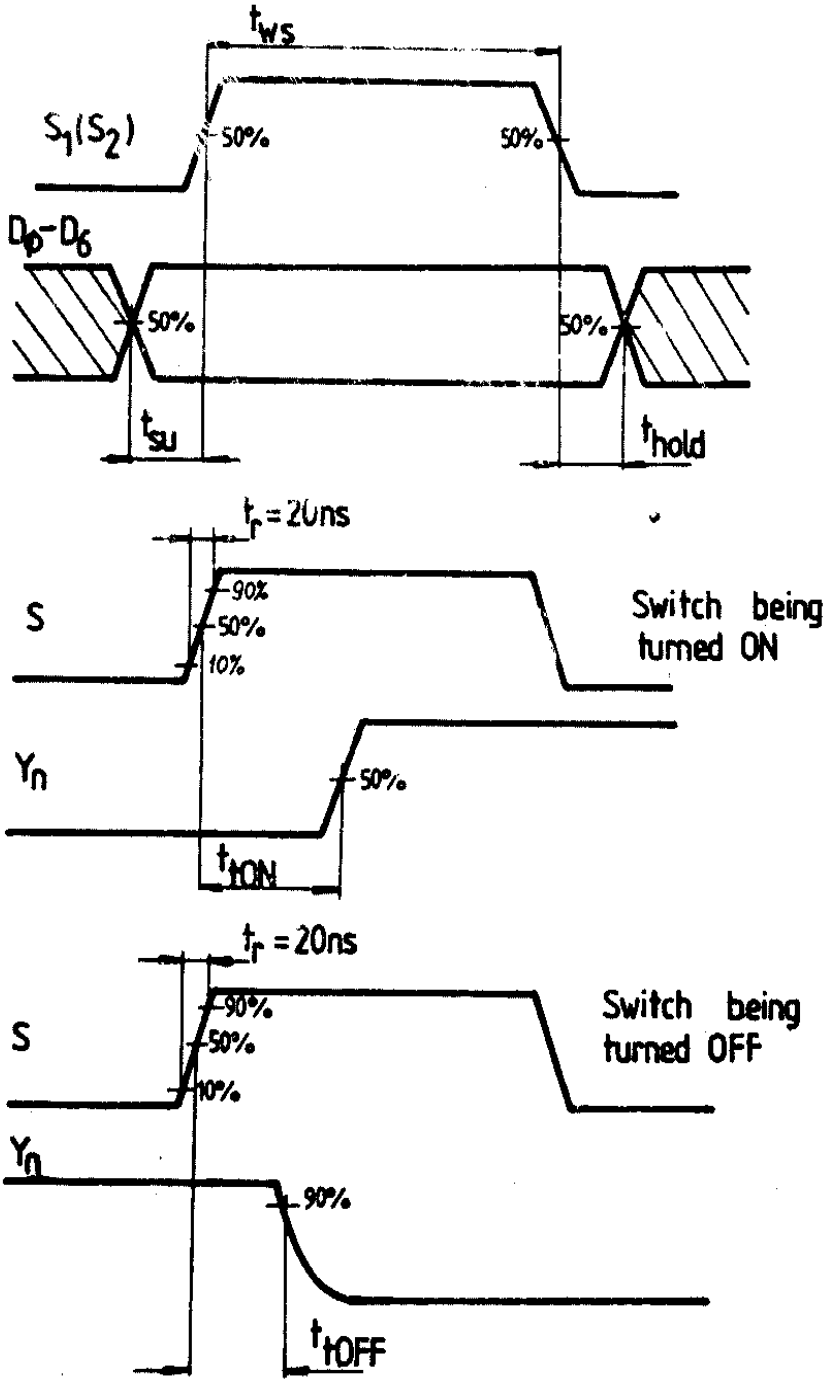


Switch being turned ON
$R_L = 10K$
$C_L = 50pF$

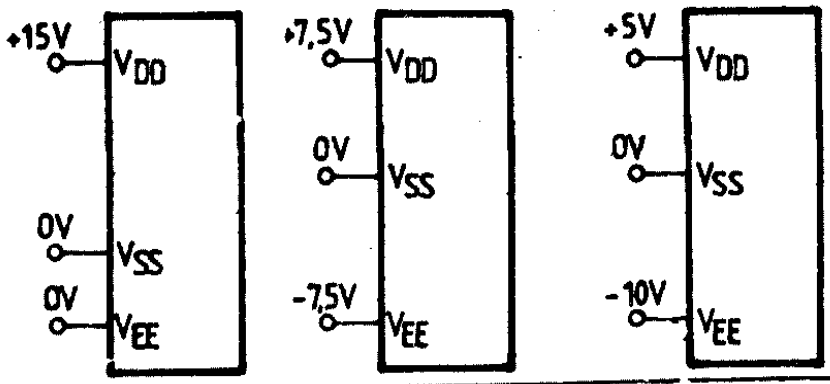
Switch being turned OFF
$R_L = 10K$
$C_L = 50pF$

MMC 355 WAVEFORMS

MMC 356 WAVEFORMS



TYPICAL BIAS VOLTAGES



PROGRAMMING EXAMPLE

Programming words for a certain configuration (MUX5 inhibited!)

D_6	0	0	0	0	1	1	1	1
D_5	0	0	1	1	0	0	1	1
D_4	0	1	0	1	0	1	0	1
D_3	0	0	1	0	1	X	0	0
D_2	0	0	0	1	0	X	1	0
D_1	1	0	0	0	1	X	1	0
D_0	1	1	1	1	1	0	1	1