



SERIAL 10-G ETHERNET/FIBRE CHANNEL TRANSCEIVER WITH XAUI INTERFACE

FEATURES

- IEEE 802.3ae compliant
- Support for XENPAK and XPAK Standards
 - Xenpak support optimized for Xenpak/XPAK layout and thermal
- Fully integrated CMU, CDR, and SerDes
- Integrated limiting amplifier and EyeOpener™ for interfacing to XFP modules
- PMD interface with serial 10.3125/10.5188 Gbps CML
- PSC 64B/66B scrambler/descrambler
- XGXS 8B/10B error detection ENDEC
- XAUI link synchronization/deskew
- Four-lane XAUI interface (3.125/3.5188 Gbps)
- Loss-of-signal detection
- Digital Optical Monitoring (DOM) support
- Loopback modes
- 802.3 clause 45 management interface extended indirect address access
- Built-In Self-Test (BIST)
 - Built-in jitter tests for XAUI and PMD
 - Built-in BERT test support
- EEPROM interface support

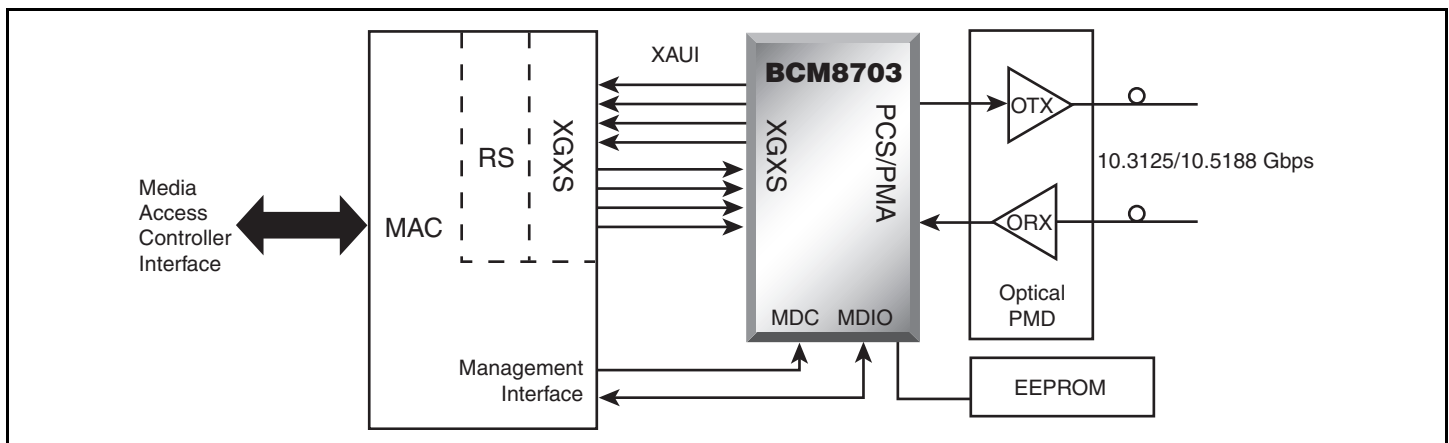
SUMMARY OF BENEFITS

- Automatic device configuration at power-up.
- Core power supply: 1.2V
- Low-power CMOS solution: 1.5W typical
- Low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.
- Reduces design cycle and time to market.
- Uses the most effective silicon economy of scale for CMOS-based devices.

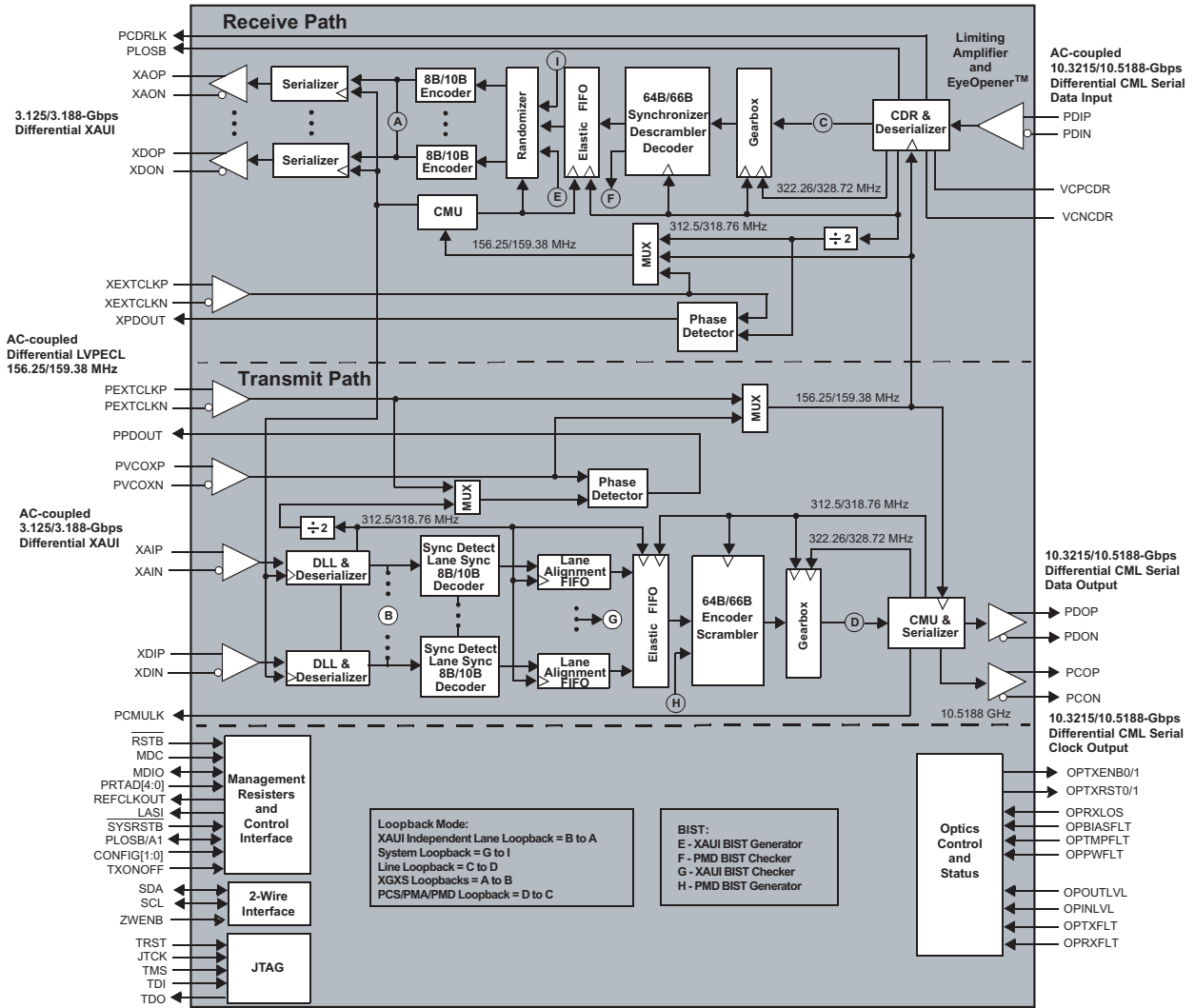
APPLICATIONS

- XENPAK/XPAK fiber-optic modules
- LAN/WAN switches
- Switch/router backbones
- Hubs and repeaters
- Network Interface Cards (NICs)
- Test equipment

BCM8703 Application Block Diagram



OVERVIEW



The **BCM8703** Ethernet/Fibre Channel PHY is a fully integrated serialization/deserialization (10.3125/10.5188-Gbps) interface device performing the extension functions for a 10 Gigabit Serial Ethernet Reconciliation Sublayer (RS) interface. The XGMII Extender Sublayer (XGXS), Physical Codings Sublayer (PCS), and Physical Medium Attachment (PMA) functions include 8B/10B coding, 64B/66B coding, SerDes, Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR).

On-chip clock synthesis is performed by the high-frequency, low-jitter, phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing the on-chip VCOs directly to their respective incoming data streams. Elastic buffers allow the XAUI and PMD interfaces to operate in either a synchronous or asynchronous configuration. An external

156.25-MHz VCXO is required for synchronous mode operation or for asynchronous mode with clock cleanup.

The **BCM8703** is packaged in a 13 x 13 mm BGA package with a 0.8-mm ball pitch.

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8703-PB04-R 04/30/04

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