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MC92610
Quad 3.125 Gbaud SERDES User's Manual

Device Supported:
MC92610VF

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About This Book

The primary objective of this user's manual is to describe the functionality of the MC92610 for software and hardware developers.

Information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure they are using the most recent version of the documentation.

Audience

It is assumed that the reader has the appropriate general knowledge regarding the design and layout requirements for high speed (Gbps) digital signaling and understanding of the basic principles of Ethernet and Fibre Channel communications protocols to use the information in this manual.

Organization

Following is a summary and a brief description of the major sections of this manual:

- Chapter 1, "Introduction," is useful for software and hardware engineers who need to have a general understanding of how the part works.
- Chapter 2, "Transmitter," describes the MC92610 transmitter, its interfaces and operation.
- Chapter 3, "Receiver," gives a description of the receiver.
- Chapter 4, "System Design Considerations," describes the system considerations for the MC92610, including clock configuration, device startup and initialization, and proper use repeater mode.
- Chapter 5, "Test Features," covers the JTAG implementation and the system accessible test modes.
- Chapter 6, "Electrical Specifications and Characteristics," describe the DC and AC electrical characteristics.
- Chapter 7, "Package Description," provides the package parameters and mechanical dimensions of the MC92610 device.

- Appendix A, “Ordering Information,” provides the Motorola part numbering nomenclature for the MC92610 transceiver
- Appendix B, “8B/10B Coding Scheme,” provides fibre channel-specific 8B/10B encoding and decoding based on the ANSI FC-1 fibre channel standard.
- “Glossary of Terms and Abbreviations” contains an alphabetical list of terms, phrases, and abbreviations used in this book.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

General Information

The following documentation, published by Morgan-Kaufmann Publishers, 340 Pine Street, Sixth Floor, San Francisco, CA, provides useful information about the PowerPC architecture and computer architecture in general:

- *The PowerPC Architecture: A Specification for a New Family of RISC Processors*, Second Edition, by International Business Machines, Inc.

  For updates to the specification, see http://www.austin.ibm.com/tech/ppc-chg.html.
- *Computer Architecture: A Quantitative Approach*, Second Edition, by John L. Hennessy and David A. Patterson
- *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, David A. Patterson and John L. Hennessy

Related Documentation

Motorola documentation is available from the sources listed on the back cover of this manual; the document order numbers are included in parentheses for ease in ordering:

- User’s manuals and reference manuals—These books provide details about individual device implementations. The *MC92610DVB SERDES Design Verification Board Reference Manual* (MC92610DVBRM/D) describes how to use the design verification board and should be read in conjunction with this manual, the *MC92610 Quad 3.125 Gbaud SERDES User’s Manual* (MC92610UM/D).
- Addenda/errata to user’s manuals—Because some devices have follow-on parts an addendum is provided that describes the additional features and functionality changes. These addenda are intended for use with the corresponding user’s manuals.
- Hardware specifications—Hardware specifications provide specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations. This manual contains all of the hardware specifications for the MC92610.

- Application notes—These short documents address specific design issues useful to programmers and engineers working with Motorola processors.
- White Paper-These documents provide detail on a specific design platform and are useful to programmers and engineers working on a specific product. *MC92610 3.125 Gbaud Reference Design Platform* (BR1570/D) describes the technical design process used in developing a high speed backplane.
- Additional literature is published as new processors become available. For a current list of documentation, refer to http://www.motorola.com/semiconductors.

Conventions

This document uses the following notational conventions:

	Book titles in text are set in italics
	Internal signals are set in italics, for example, $\overline{qual\ BG}$
0x	Prefix to denote hexadecimal number
0b	Prefix to denote binary number
x	In some contexts, such as signal encodings, an un-italicized x indicates a don't care.
x	An italicized *x* indicates an alphanumeric variable.
n	An italicized *n* indicates an numeric variable.

Signals

A bar over a signal name indicate that the signal is active low—for example, $\overline{\text{XMIT\_A\_IDLE}}$ and $\overline{\text{XMIT\_B\_IDLE}}$. Active low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as XMIT_EQ_EN and DROP_SYNC are referred to as asserted when they are high and negated when they are low.

Chapter 1
Introduction

This user's manual explains the functionality of the MC92610 Quad 3.125 Gbaud SERDES transceiver and enable its use by software and hardware developers. The audience for this publication, therefore, consists of developers and application programmers who are building data path switches and applications.

1.1 Overview

The MC92610, is a high-speed, full-duplex, serial/deserializer (SERDES) data interface device that transmits data between chips across a board, through a backplane, or through cabling. The MC92610 has four transceivers that transmit and receive coded data at a maximum rate of 2.5 gigabits per second (Gbps) through each 3.125 gigabaud link. Each transceiver has redundant transmit and receive I/Os that are independently selectable.

The MC92610 features HSTL class 1 DDR source synchronous parallel interfaces that allow efficient integration with system logic. The MC92610 is designed to minimize the number of data line interconnects in point-to-point communications with low power requirements. The MC92610 SERDES offers high performance with excellent signal integrity and low bit-error-rate (BER). Other features include clock generation and recovery, on-chip termination resistors and coupling capacitors, low transmit jitter, and multiple modes of operation - within a compact 324-pin MAPBGA package. The MC92610 features make it advantageous for use in many different data transfer designs. This in turn simplifies the architectures of switch backplanes while enabling small footprint designs.

The MC92610 SERDES is the latest generation of Motorola's products. Like its predecessors, it features a very low power 0.25µ CMOS implementation, using 1.8 Watts. with all links operating at full-speed. With a high-density packaging solution and a rich feature set the MC92610 is easily adaptable to many applications.

1.2 Features

The following are the features of the MC92610:

- 4 full-duplex differential data links.
- Selectable speed range: 3.125 Gbaud or 1.5625 Gbaud.

- Low power, nominally 1.8W, while operating all transceivers at full speed.
- Internal 8B/10B encoder / decoder that can be bypassed for applications where external coding is used.
- Double data rate (DDR), source synchronous, 8-bit and 10-bit HSTL class-1 parallel data interfaces.
- Received data may be clocked at the recovered clock or the reference clock frequency.
- Link-to-link synchronization supports aligned, 32-bit, word transfers. The synchronization mechanism can tolerates up to 40 bit-times of link-to-link media delay skew.
- Multi-chip link synchronization supports aligned, multi-word transfers. Up to four MC92610 devices may be used to provide 128-bit, four-word, synchronized transfers.
- Selectable Idle character alignment mode enables aligned transfers with automatic realignment or unaligned data transfers.
- Transceiver links operate over 50Ω media (100Ω differential) for lengths of up to one meter of FR-4 board/backplane or six meters of coax.
- Selectable transmit and receive link equalization.
- Link inputs have on-chip receiver termination, AC coupling and are “hot swap” compatible.
- Redundant transmitter outputs and receiver inputs are provided. Redundant links are selectable per transceiver. Broadcast mode enables all transmit link outputs.
- Differential reference clock input with single-ended reference clock input option.
- Link Multiplexer mode enables operation of two links with single data rate (SDR), source synchronous, 16-bit and 20-bit parallel data interfaces.
- Transceiver channels may be individually disabled.
- Repeater mode configures the MC92610 into a four-link receive-transmit repeater.
- At speed built-in self test (BIST) for in-system diagnostics.
- IEEE 1149.1 JTAG boundary scan test support.

1.3 Block Diagram

The MC92610 is a highly integrated device containing all of the logic needed to facilitate the application and test of a high-speed serial interface. A block diagram of the MC92610 device is shown in Figure 1-1.

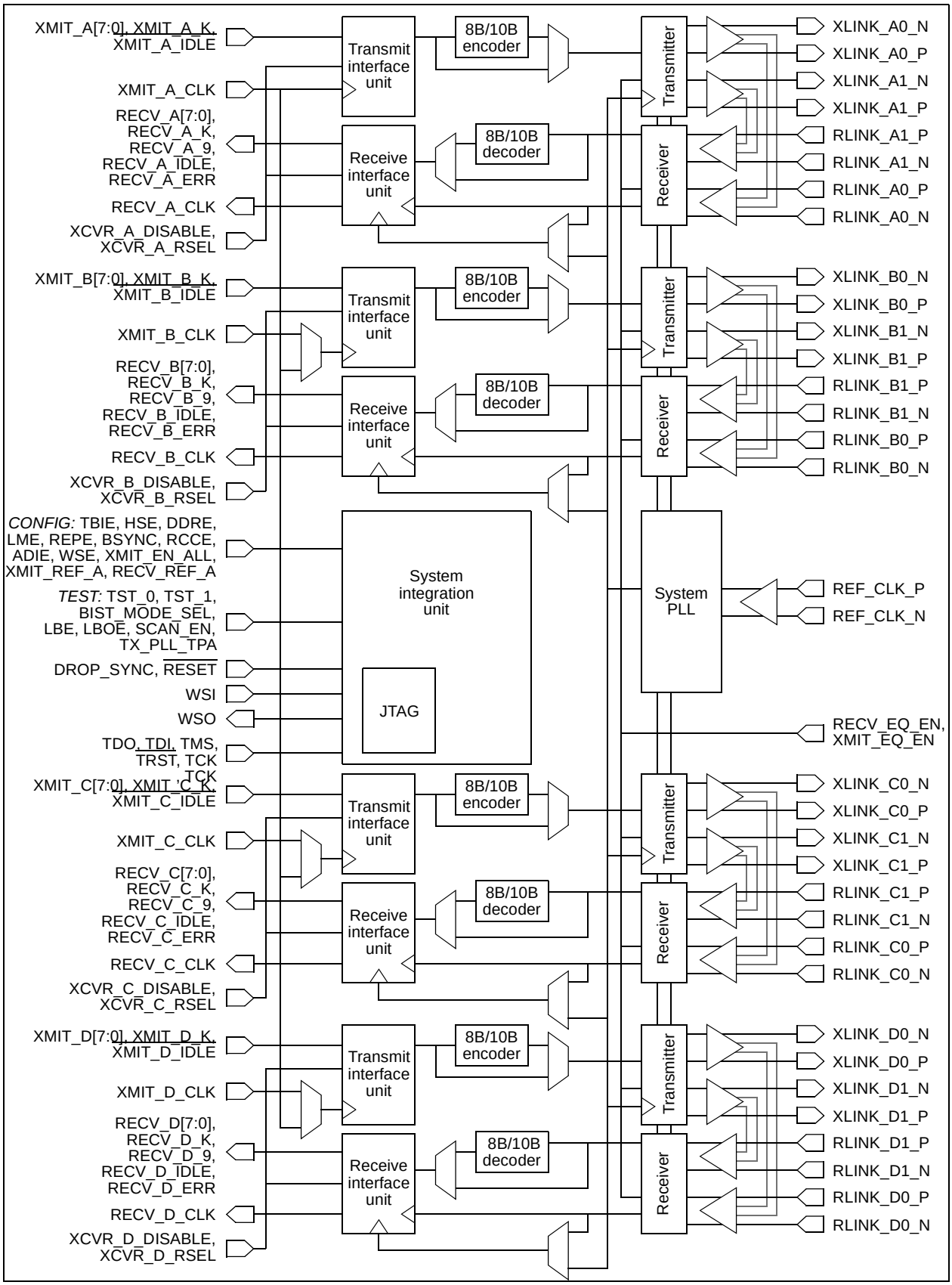


Figure 1-1. MC92610 Block Diagram

1.4 References

This section contains the indexed references in the document.

[1] *Fibre Channel, Gigabit Communications and I/O for Computer Networks*, Brenner, 1996.

[2] *Byte Oriented DC Balanced 8B/10B Partitioned Block Transmission Code*, U.S. Patent #4,486,739, Dec. 4, 1984.

[3] *High Speed Transceiver Logic (HSTL), A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits*, EIA/JEDIC Standard EIA/JESD8-6, Aug. 1995.

[4] *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std. 1149.1-1990 (Includes IEEE Std. 1149.1a-1993), Oct. 1993.

1.5 Revision History

Table 1-1 contains a brief description of the technical updates made to this document.

Table 1-1. MC92610 SERDES User's Manual Revision History

Revision Level	Change
0	First revision of the MC92610 SERDES User's manual.
1	Second revision of the MC92610 SERDES User's manual. Minor edits were made to the entire document. Added note in Section 5.1, "IEEE Std. 1149.1 Implementation," and Section 5.2.2, "BIST Sequence System Test Mode." Changed supply currents, power dissipation, min/max latencies in Chapter 6, "Electrical Specifications and Characteristics."

Chapter 2
Transmitter

This chapter describes the MC92610 transmitter, its interfaces and operation. The chapter consists of the following sections:

- Section 2.1, “Block Diagram”
- Section 2.2, “Transmitter Interface Signals”
- Section 2.3, “Functional Description.”

The transmitter takes the data byte presented at its data input, creates a transmission character using its 8B/10B encoder (if not in 10-bit interface mode), and serially transmits the character out of the differential link output pads. A detailed explanation of the 8B/10B coding scheme is offered in Appendix B, “8B/10B Coding Scheme.”

2.1 Block Diagram

Figure 2-1 shows a block diagram of the MC92610 transmitter.

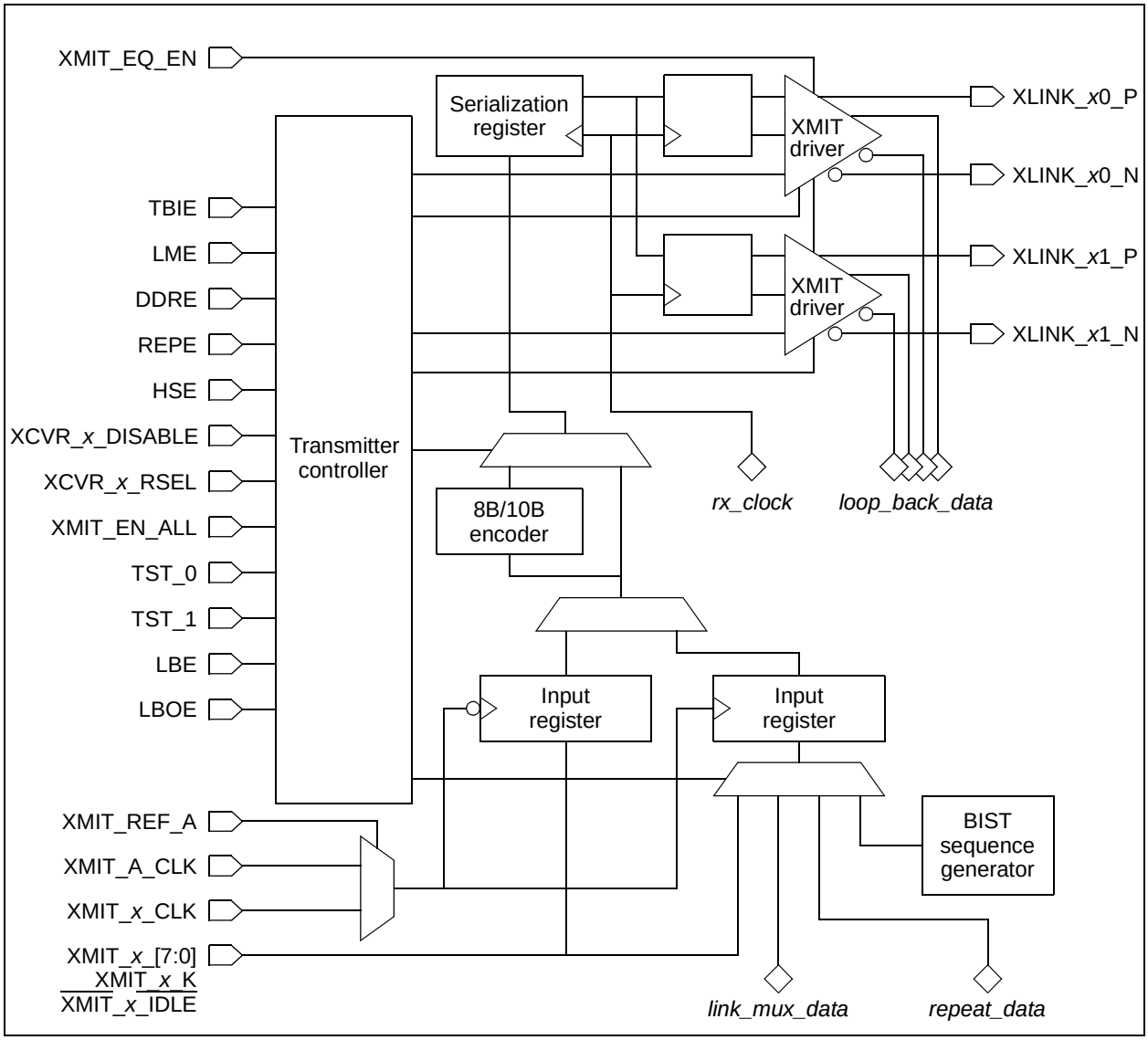


Figure 2-1. MC92610 Transmitter Block Diagram

2.2 Transmitter Interface Signals

This section describes the interface signals of the MC92610 transmitters. Each signal is described, including its name, function, direction, and active state in Table 2-1. The table's signal names use the letter "*x*" as a place holder for the Link identifier letter "A" through "D". Internal signals are not available at the I/O of the device, but are presented to illustrate device operation.

Table 2-1. MC92610 Transmitter Interface Signals

Signal Name	Description	Function	Direction	Active State
XMIT_*x*_7 through XMIT_*x*_0	Transmit Byte	Uncoded data/control byte to transmit. The least significant 8 bits of the pre-coded data transmits in TBI (ten bit interface) mode.	Input	-
XMIT_*x*_K	Special Data Indicator	Indicates that Transmit byte is a special control byte. Must be decoded with $\overline{\text{XMIT}}$_*x*_$\overline{\text{IDLE}}$ to determine action, see Table 2-2. Pre-coded transmit data bit 8 in TBI mode.	Input	High
$\overline{\text{XMIT}}$_*x*_$\overline{\text{IDLE}}$	Transmit Idle Character Bar	Transmit an Idle character. Must be decoded with XMIT_*x*_K to determine action, see Table 2-2. Pre-coded transmit data bit 9 in TBI mode.	Input	Low
XMIT_*x*_CLK	Transmit Interface Clock	Clock to which transmit interface signals are timed. Frequency requirement is dependent on whether HSE and DDRE are asserted. See Section 4.1 and Table 4-1 for configuration options.	Input	-
XMIT_REF_A	Transmit Interface Clock Select	Indicates that the transmit interface signals are timed to XMIT_A_CLK instead of their transmit clock.	Input	High
XCVR_*x*_DISABLE	Transceiver Disable	Indicates that the transmitter and receiver for this transceiver are disabled. The link outputs are not driven.	Input	High
XCVR_*x*_RSEL	Transceiver Link Select	Indicates that the redundant link outputs are active and that the primary link outputs are disabled. The primary link outputs are active and the redundant link outputs are disabled when this signal is low. Both sets of outputs may be simultaneously enabled using the XMIT_EN_ALL signal.	Input	High
XMIT_EN_ALL	Transmitter Link Broadcast Enable	Indicates that both the primary and redundant link outputs are enabled independent of the assertion of the XCVR_*x*_RSEL signal. Broadcast mode does not override XCVR_*x*_DISABLE, which must be set low for transmitter operation.	Input	High
XMIT_EQ_EN	Transmit Equalization Enable	Indicates that transmitter equalization is enabled and that high frequency gain is applied to the transmitted signal.	Input	High

Table 2-1. MC92610 Transmitter Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
TBIE	Ten-Bit Interface Enable	Indicates that pre-coded 10-bit data is at inputs and to bypass internal 8B/10B coding.	Input	High
REPE	Repeater Mode Enable	When enabled, the transmitter obtains transmit data from the receiver.	Input	High
LME	Link Multiplexer Mode Enable	Indicates that the data on transmitter A and B are aggregated and transmit out of link A. Likewise, the data on transmitter C and D are aggregated and transmit out of link C.	Input	High
DDRE	Double Data Rate Enable	When in Link Multiplexer mode (LME signal is high) this signal indicates that the data interfaces are running at double data rate. When not in Link Multiplexer mode, this signal does not affect device operation.	Input	High
HSE	Half Speed Enable	When enabled, link is operated at half-speed. Both data and link interfaces run at half speed.	Input	High
LBE	Loop Back Enable	Activate digital loopback path, such that data transmitted is looped back to its receiver.	Input	High
LBOE	Loop Back Output Enable	Indicates that selected link outputs remain active when loop back is enabled. The link outputs are disabled when LBOE is low and loop back is enabled.	Input	High
TST_1, TST_0	Test Mode Select	Selects a test mode.	Input	-
XLINK_*x*0_N/ XLINK_*x*0_P	Link Serial Transmit Data, Primary Links	Differential serial transmit data output pads for the primary links.	Output	-
XLINK_*x*1_N/ XLINK_*x*1_P	Link Serial Transmit Data, Redundant Links	Differential serial transmit data output pads for the redundant links.	Output	-
Internal Signals				
rx_clock	High Speed Transceiver Clock	Internal, differential high speed clock used to transmit and receive link data.	Input	-
repeat_data	Received Repeat Data	Repeater mode, received data to retransmit.	Input	-
link_mux_data	Link Multiplexer Mode Data	Data from adjacent transmitter to transmit on this transmitter when in Link Multiplexer mode (LME is asserted.)	Input	-
loop_back_data	Loop Back Data	Differential loop back transmit data.	Output	-

2.3 Functional Description

The transmitter takes the data byte presented at its data input, creates a transmission character using its 8B/10B encoder and serially transmits the character out of the differential link output pads. The following sections provide a detailed description of the transmitter and its modes of operation.

2.3.1 Transmit Data Input Register Operation

The transmit data input register accepts data to be transmitted and synchronizes it to the internal clock domain. Transmit data is normally uncoded 8-bit data, however, transmission of pre-coded 10-bit data is supported in Ten-Bit Interface (TBI) mode. TBI mode is enabled by asserting TBIE high.

The transmit data interface is a Double Data Rate (DDR) interface; the data is sampled and stored on the rising and falling edges of the transmit interface clock XMIT_*x*_CLK. There are several clocking options on the transmit data interface that are described in Section 2.3.1.5.

2.3.1.1 Transmitting Uncoded Data

Uncoded data is presented in 8-bit bytes to the input register through the XMIT_*x*_7–XMIT_*x*_0 signals. The uncoded data is coded into 10-bit transmission characters using an on-chip 8B/10B encoder. 8B/10B coding ensures DC balance across the link and sufficient transition density to facilitate reliable data recovery. The XMIT_*x*_7–XMIT_*x*_0 signals are interpreted as data when the XMIT_*x*_K signal is low.

The 8B/10B code includes special control codes. Special control codes may be transmitted by asserting XMIT_*x*_K high, and XMIT_*x*_IDLE high as indicated in Table 2-2. The transmit byte is assumed to be a control code in this state.

The transmitter generates an Idle character (K28.5) when XMIT_*x*_K is high and $\overline{\text{XMIT\_}x\text{\_IDLE}}$ is low as indicated in Table 2-2. An Idle character of proper running disparity is generated when this state is asserted; the state on the XMIT_*x*_7–XMIT_*x*_0 signals are ignored. This eases generation of Idle characters needed for byte and word synchronization and allows the link to maintain alignment when transmission of data is not needed.

Table 2-2. Transmitter Control States

$\overline{\text{XMIT\_}x\text{\_IDLE}}$	XMIT_*x*_K	Description
—	Low	Transmit data present on XMIT_*x*_7–XMIT_*x*_0 inputs.
Low	High	Transmit Idle (K28.5), ignore XMIT_*x*_7–XMIT_*x*_0 inputs.
High	High	Transmit control present on XMIT_*x*_7–XMIT_*x*_0 inputs.

2.3.1.2 Transmitting Pre-Coded Data

Ten-bit pre-coded data may be transmitted, bypassing the internal 8B/10B encoder. Ten-Bit Interface (TBI) mode is enabled by asserting TBIE high. In this mode, the ten bits to transmit are presented on the XMIT_*x*_7–XMIT_*x*_0 inputs, and bits 8 and 9 on the XMIT_*x*_K and $\overline{\text{XMIT\_}x\text{\_IDLE}}$ inputs, respectively.

Precautions must be taken when using TBI mode. The 10-bit pre-coded data must exhibit the same properties as 8B/10B coded data. DC balance must be maintained and there must be sufficient transition density to ensure reliable data recovery at the receiver.

The receiver requires that the K28.5 Idle character be periodically transmitted to enable byte and word synchronization. This 10-bit pattern, ‘0011111010’ or ‘1100000101’ (ordered from bit 0 through 9) is used for alignment and link-to-link synchronization when operating in any of the byte or word synchronization modes. The pattern of Idles and data required to achieve byte or word synchronization depends on the configuration of the receiver, see Section 3.3.4.3. The appropriate sequence must be applied through the Ten-Bit Interface.

The MC92610 transmitter is comprised of several components whose operations are described in the following sections.

2.3.1.3 Link Multiplexer Mode

Link multiplexer mode configures the MC92610 quad device into a dual transceiver. The transmit data interfaces for transmitters A and B are combined to form a 16-bit/20-bit, Single Data Rate (SDR) interface. The data is sampled and stored on the rising edge of the transmit interface clock XMIT_A_CLK. The transmit data is aggregated and transmit out of link A. The outputs of link B are disabled. The transmit interface may also be operated in DDR mode by asserting DDRE high.

Likewise, transmit data interfaces C and D are combined and transmit out of link C. Transmit interface clock XMIT_C_CLK is used for transmitters C and D. The outputs of link D are disabled.

Data on the transmitter A interface is sent first, followed by transmitter B. Data on the transmitter C is sent first, followed by transmitter D.

Link Multiplexer mode is enabled by asserting LME high.

2.3.1.4 Repeater Mode

Repeater mode configures the MC92610 into a 4-link receive-transmit repeater. In this mode, the data to transmit is obtained from its receiver (transmitter A gets receiver A's data, transmitter B gets receiver B's data, and so on). The transmit input signals, XMIT_*x*_7 - XMIT_*x*_0, XMIT_*x*_K and $\overline{\text{XMIT\_}x\text{\_IDLE}}$ are ignored. Repeater mode is enabled by asserting REPE high. See Section 3.3.9 for more information on Repeater mode.

2.3.1.5 Transmit Interface Clock Configuration

The transmitter data interface operates at high frequency (up to 156.25MHz). In order to ease development of devices that interact with the MC92610, all of its data interfaces are source-synchronous. The data for each transmitter has its own dedicated clock input. This allows the clock at the source of the data to be routed with the data ensuring matched delay and timing. However, if per-transmitter clock sources are not available or deemed unnecessary, all transmitters may be clocked by a common clock source. This is enabled by asserting XMIT_REF_A high. When XMIT_REF_A is high, the XMIT_A_CLK becomes the interface clock for all active transmitters.

The transmit interface clock inputs, XMIT_*x*_CLK, and the PLL reference clock, REF_CLK_P/REF_CLK_N, inputs must be operated at exactly the same frequency. However, there may be an arbitrary initial phase relationship between the PLL reference clock and the transmit interface clocks. The phase relationship between the transmit interface clock and the PLL reference clock is established after the internal PLL locks. Once locked, the transmit data interface tolerates $\pm 180^{o}$ of transmit interface clock phase drift relative to the PLL reference clock.

Additionally, all of the MC92610's data interfaces are DDR, except in Link Multiplexer mode. DDR interfaces, in which the data is sampled and stored on the rising and falling edges of the clock, reduces the clock frequency by 50 percent while maintaining throughput.

The configuration assertings of the MC92610 affect the legal range of clock frequencies at which it may be operated. Section 4.1, Table 4-1 shows legal transmit interface clock frequencies for all modes of operation.

2.3.1.6 8B/10B Encoder Operation

The 8B/10B Encoder encodes 8-bit data/control from the input register into 10-bit *transmission characters*. The ANSI standard for Fibre Channel 8B/10B coding standard is followed [1,2]. Running disparity is maintained and the appropriate transmission characters

are produced, maintaining DC balance and sufficient transition density to allow reliable data recovery at the receiver.

The inputs to the 8B/10B Encoder are the data byte (XMIT_*x*_7-XMIT_*x*_0), special code signal (XMIT_*x*_K) and transmit Idle signal ($\overline{\text{XMIT}}$_*x*_$\overline{\text{IDLE}}$).

Data and legal control bytes are coded according to the 8B/10B method. Illegal control bytes produce unpredictable transmission characters, leading to disparity and coding errors, ultimately reducing link reliability.

The 8B/10B encoder produces an Idle character (K28.5) of proper running disparity when $\overline{\text{XMIT}}$_*x*_$\overline{\text{IDLE}}$ is low and XMIT_*x*_K is high, as indicated in Table 2-2.

The 8B/10B Encoder is bypassed in TBI mode.

2.3.1.7 Transmit Driver Operation

The Transmit Driver drives transmission characters serially across the link. There are two transmit drivers per transmitter, the primary driver for outputs XLINK_*x*0_P / XLINK_*x*0_N, and the redundant driver for outputs XLINK_*x*1_P / XLINK_*x*1_N.

Each bit of coded data is transmitted differentially out of the enabled driver. The primary driver outputs, XLINK_*x*0_P / XLINK_*x*0_N, are enabled by asserting XCVR_*x*_RSEL low. The redundant driver outputs, XLINK_*x*1_P / XLINK_*x*1_N, are enabled by asserting XCVR_*x*_RSEL high.

Broadcast mode is enabled by asserting XMIT_EN_ALL high. In broadcast mode, all primary and redundant link outputs of all four transmitters are enabled, independent of the asserting the XCVR_*x*_RSEL signals. When XMIT_EN_ALL is low, only the selected link driver is active as described previously.

Both the primary and redundant link outputs are disabled when the transceiver is disabled by asserting XCVR_*x*_DISABLE high.

2.3.1.8 Transmit Equalization

The Transmit Driver is a 50Ω controlled impedance driver. The media over which the signals are transmit, has high-frequency loss that contributes significantly to a distortion known as Inter-Symbol Interference (ISI). In order to offset, or equalize, the loss at high frequency, the MC92610's Transmit Drivers provide additional gain at high frequencies. This is termed *Transmit Equalization*. Transmit equalization has the greatest benefit when driving longer lengths of coax or when traversing across a large backplane. Transmit equalization is of less benefit for short links. Transmit equalization is enabled by asserting XMIT_EQ_EN high.

2.3.1.9 Loop-Back Test Mode

A special loop-back mode is supported for test. asserting LBE high enables loop-back mode causing the data being driven on the link outputs to be looped back to the input amplifier of the link's receiver.

Loop-back data can be routed through either of the two output drivers. The path taken is controlled by the XCVR_*x*_RSEL signal. When XCVR_*x*_RSEL is low, data loops back through the primary driver (XLINK_*x*0_P / XLINK_*x*0_N), and when XCVR_*x*_RSEL is high, data loops back through the redundant driver (XLINK_*x*1_P / XLINK_*x*1_N).

Loop-back data is processed the same as normally received data. Loop-back enables at-speed self-test to be implemented for production test and for in-system self-test. The loop-back signals are electrically isolated from the link output signals. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally.

When in loop-back mode, the LBOE signal controls the action of the link output signals. When LBOE is low, the link outputs are undriven and are high-impedance. When LBOE is high, the link output signals operate normally.

LBOE has no affect on the operation of the device when LBE is low.

See Section 5.2 for more information on system accessible test modes.

Chapter 3
Receiver

This chapter describes the MC92610 receiver, its interfaces and operation. This chapter has the following sections:

- Section 3.1, “Receiver Block Diagram”
- Section 3.2, “Receiver Interface Signals”
- Section 3.3, “Receiver Functional Description”

The receiver takes a high speed differential serial data stream input, over samples it and recovers the data and clock, decodes it and presents it on a source synchronous parallel output data port.

3.1 Receiver Block Diagram

Figure 3-1 shows a block diagram of the MC92610 receiver.

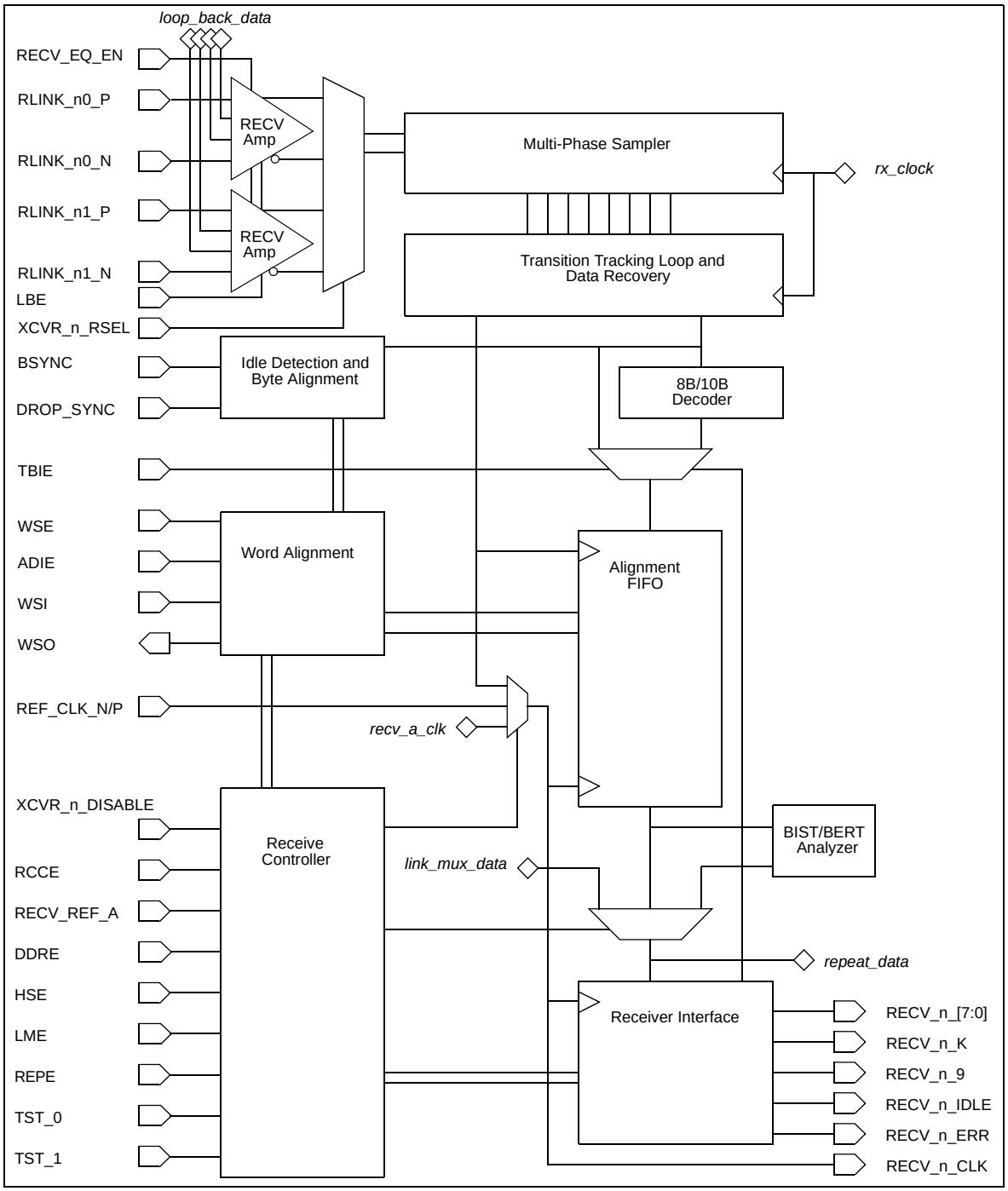


Figure 3-1. MC92610 Receiver Block Diagram

3.2 Receiver Interface Signals

This sections describes the interface signals of the MC92610 receiver. Each signal is described, including its name, function, direction and active state in Table 3-1. The table's signal names use the letter "x" as a place holder for the Link identifier letter "A" through

"D." Internal signals are not available at the I/O of the device, but are presented to illustrate device operation.

Table 3-1. Receiver Interface Signals

Signal Name	Description	Function	Direction	Active State
RECV_*x*_7 through RECV_*x*_0	Received Byte	Received and decoded data/control byte. The least significant 8 bits of received data in TBI mode.	Output	-
RECV_*x*_K	Special Data Indicator/ Received Bit 8	Indicates that received byte is a special control byte. Received bit 8 in TBI mode. Errors are coded using this signal. See Section 3.3.6.3 for error codes.	Output	-
RECV_*x*_9	Received Bit 9	Received bit 9 in TBI mode. Unused in 8-bit mode.	Output	-
RECV_*x*_IDLE	Receiver Idle Detect	Indicates that the receiver detected an Idle character (operates in Byte and TBI modes). Errors are coded using this signal. See Section 3.3.6.3 for error codes.	Output	-
RECV_*x*_ERR	Receiver Error	Indicates that the receiver detected an error. RECV_*x*_IDLE and RECV_*x*_K must be decoded to determine error condition. See Section 3.3.6.3 for error codes.	Output	-
RECV_*x*_CLK	Receiver Interface Clock	Clock used for clocking receiver interface. Source and frequency of this clock depend on operating mode. See Section 4.1 for more information.	Output	-
DROP_SYNC	Drop Synchronization	Indicates that the current byte and word alignment should be invalidated and new alignment acquired. DROP_SYNC is level sensitive and not synchronized to a clock, it must be asserted for at least two clock periods.	Input	High
XCVR_*x*_DISABLE	Transceiver Disable	Indicates that the transmitter and receiver for this transceiver are disabled.	Input	High
XCVR_*x*_RSEL	Transceiver Link Select	Indicates that the redundant link inputs are observed and that primary link inputs are ignored.	Input	High
RECV_EQ_EN	Receive Equalization Enable	Indicates that receiver equalization is enabled and that high frequency gain is applied to the received signal.	Input	High
TBIE	Ten-Bit Interface Enable	Indicates that the receiver interface is in ten-bit mode and that the 8B/10B decoder is bypassed.	Input	High

Table 3-1. Receiver Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
HSE	Half Speed Enable	Indicates to operate link at half-speed. Both data and link interfaces run at half speed.	Input	High
LBE	Loop Back Enable	Activates digital loopback path, such that the loop-back data from the transmitter is accepted by the receiver.	Input	High
WSE	Word Synchronization Enable	Indicates that all four receivers are being used in unison to receive synchronized data.	Input	High
WSI	Word Synchronization Bus Input	Coded word synchronization bus input that is used to synchronize word timing between multiple MC92610 devices. See Section 3.3.4.3 for multi-chip word synchronization operation. This signal should be tied high if multi-chip word synchronization is not being used.	Input	-
WSO	Word Synchronization Bus Output	Coded word synchronization bus output that is used to synchronize word timing between multiple MC92610 devices. See Section 3.3.4.3 for multi-chip word synchronization operation.	Output	-
LME	Link Multiplexer Mode Enable	Indicates that the data received on receiver A is presented 16/20 bits wide on parallel interfaces A and B. Likewise, the data received on receiver C is presented 16/20 bits wide on parallel interfaces C and D.	Input	High
DDRE	Double Data Rate Enable	When in Link Multiplexer Mode (LME is high) this signal indicates that the data interfaces are running at double data rate.	Input	High
BSYNC	Byte Alignment Mode	Indicates that byte alignment is employed in the receiver.	Input	High
RCCE	Recovered Clock Enable	Indicates that the clock frequency recovered by the receiver is used for the receiver interface clock (RECV_*x*_CLK). Otherwise, the reference clock frequency is used. This signal is used with the RECV_REF_A signal to fully determine clock source.	Input	High
RECV_REF_A	Receiver Interface Clock Select	Indicates that the clock frequency recovered by receiver A is used as the receiver interface clock for all four receivers. This signal is used with the RCCE signal to fully determine clock source.	Input	High

Table 3-1. Receiver Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
REF_CLK_P/N	PLL Reference Clock	PLL input reference clock. Provides reference frequency for the receiver interface when Recovered Clock mode is disabled (RCCE is low).	Input	-
ADIE	Add/Delete Idle Enable	Indicates that the receiver is free to add/delete Idle characters to/from the output data stream to maintain alignment.	Input	High
REPE	Repeater Mode Enable	When enabled, the transmitter obtains transmit data from the receiver.	Input	High
TST_0/ TST_1	Test Mode	Indicates operating/test mode of the chip.	Input	-
RLINK_*x*0_N/ RLINK_*x*0_P	Link Serial Receive Data, Primary Links	Differential serial receive data input pads for the primary links.	Input	-
RLINK_*x*1_N/ RLINK_*x*1_P	Link Serial Receive Data, Redundant Links	Differential serial receive data input pads for the redundant links.	Input	-
Internal Signals				
rx_clock	High Speed Transceiver Clock	Internal, differential high speed clock used to transmit and receive link data.	Input	-
recv_a_clk	Receiver A Interface Clock	Internal copy of receiver A's interface clock.	Input	-
loop_back_data	Loop Back Data	Differential loop back receive data.	Input	-
link_mux_data	Link Multiplexer Mode Data	Received data from adjacent receiver to direct to receiver interface when in Link Multiplexer mode (LME is high.)	Input	-
repeat_data	Received Repeat Data	Repeater mode, received data to re-transmit.	Output	-

3.3 Receiver Functional Description

The MC92610 receiver is based upon an oversampled transition tracking loop data recovery method. The receiver receives differential data in one of two operating ranges. It may be operated in full rate range with a maximum data rate of 2.5 Gbps (3.125 gigabaud) or at half-rate at 1.25 Gbps (1.5625 gigabaud). The operating range is determined by the state of the HSE input.

The received serial data is accumulated into ten-bit characters. The ten-bit characters are forwarded to the 8B/10B decoder where the original data is obtained. Alternately, the decoder can be bypassed and the ten-bit character is forwarded to the receiver interface in ten-bit interface (TBI) mode.

The receiver provides for byte (character) alignment. Alignment assures that the byte as presented at the input of the transmitter is preserved when the byte is presented by the receiver. Optionally, alignment may be disabled.

The receiver also provides for word synchronization. In this mode, all of the receivers are being used cooperatively to receive 32-bit (40 bit in TBI mode) words. Word synchronization assures that the receivers present the four bytes of a word simultaneously. The MC92610 also supports multi-chip word synchronization in which up to four MC92610 devices may be used to send and receive synchronized multi-words.

The receiver has primary and redundant link inputs to support applications where redundancy is required. MC92610's transition tracking loop has superior receive signal acquisition performance relative to PLL-based clock and data recovery methods. This enables faster transition between the primary and redundant data streams.

The receiver interface, where the received bytes and status codes are obtained, has several modes of operation and timing to allow it to be used in a variety of applications. The following sections provide a detailed description of the receiver and its modes of operation.

3.3.1 Input Amplifier

The input amplifiers connect directly to the link input pads RLINK_*x*0_P/N and RLINK_*x*1_P/N. There are separate input amplifiers for the primary and redundant link inputs. The input amplifiers are differential with integrated analog multiplexer for loop-back testing. Differential 100Ω link termination and in-line AC coupling capacitors are integrated with the amplifiers.

NOTE

The integrated, in-line, AC coupling capacitors offer an extended common-mode input voltage range, however, compliance to the range as specified in Section 6.2 is required for proper link operation. If a broader common-mode input voltage range is required then additional, off-chip, AC coupling capacitors must be used.

The input amplifier facilitates a loop-back path for production and in-system testing. When the MC92610 is in loop-back mode (LBE set high), the input amplifier selects the loop-back differential input signals and ignores the state on the RLINK_*x*0_P / RLINK_*x*1_P and RLINK_*x*0_N / RLINK_*x*1_N signals. Loop back data can be routed through either the primary or redundant input amplifier. The path taken is controlled by the XCVR_*x*_RSEL signal. When XCVR_*x*_RSEL is low, data loops back through the primary input amplifier, and when XCVR_*x*_RSEL is high, data loops back through the redundant input amplifier.

Loop-back data is processed the same as normally received data. Loop-back enables at-speed self-test to be implemented for production test and for in-system self-test. The loop-back signals are electrically isolated from the link input signals. Therefore, if the inputs are shorted, open, or otherwise disturbed, the loop-back signals still operate normally.

See Section 5.2 for more information on system accessible test modes.

3.3.1.1 Receiver Equalization

The media through which the signals are received, has high-frequency loss that contributes significantly to a distortion known as Inter-Symbol Interference (ISI). In order to offset, or equalize, the loss at high frequency, MC92610's input amplifiers provide additional gain at high frequencies. This is termed *Receive Equalization*. Receive equalization has the greatest benefit when receiving signals through longer lengths of coax or when traversing across a large backplane. Receive equalization is of less-benefit for short links. Receive equalization is enabled by asserting RECV_EQ_EN high.

The input amplifier facilitates a loop-back path for production and in-system testing. When the MC92610 is in loop-back mode (LBE set high), the input amplifier selects the loop-back differential input signals and ignores the state on the RLINK_*x*0_P / RLINK_*x*1_P and RLINK_*x*0_N / RLINK_*x*1_N signals. Loop back data can be routed through either the primary or redundant input amplifier. The path taken is controlled by the XCVR_*x*_RSEL signal. When XCVR_*x*_RSEL is low, data loops back through the primary input amplifier, and when XCVR_*x*_RSEL is high, data loops back through the redundant input amplifier.

Loop-back data is processed the same as normally received data. Loop-back enables at-speed self-test to be implemented for production test and for in-system self-test. The loop-back signals are electrically isolated from the link input signals. Therefore, if the inputs are shorted, open, or otherwise disturbed, the loop-back signals still operate normally.

See Section 5.2 for more information on system accessible test modes.

3.3.1.2 Loop-Back Test Mode

The input amplifier facilitates a loop-back path for production and in-system testing. When the MC92610 is in loop-back mode (LBE set high), the input amplifier selects the loop-back differential input signals and ignores the state on the RLINK_*x*0_P / RLINK_*x*1_P and RLINK_*x*0_N / RLINK_*x*1_N signals. Loop back data can be routed through either the primary or redundant input amplifier. The path taken is controlled by the XCVR_*x*_RSEL signal. When XCVR_*x*_RSEL is low, data loops back through the primary input amplifier, and when XCVR_*x*_RSEL is high, data loops back through the redundant input amplifier.

Loop-back data is processed the same as normally received data. Loop-back enables at-speed self-test to be implemented for production test and for in-system self-test. The loop-back signals are electrically isolated from the link input signals. Therefore, if the inputs are shorted, open, or otherwise disturbed, the loop-back signals still operate normally.

See Section 5.2 for more information on system accessible test modes.

3.3.2 Transition Tracking Loop and Data Recovery

The received differential data from the input amplifier is sent to the transition tracking loop for data recovery. The MC92610 uses an oversampled transition tracking loop method for data recovery. The differentially received data is sampled and processed digitally providing for low bit error rate (better than 10^{-12}) data recovery of a distorted bit stream.

The transition tracking loop is tolerant of frequency offset between the transmitter and receiver. The MC92610 reliably operates with $\pm$100 ppm of frequency offset. The transition tracking loop synthesizes a recovered clock that matches the frequency of the received data.

Recovered data is accumulated into 10-bit characters. Characters are aligned to their original 10-bit boundaries if a Byte Alignment mode is enabled.

3.3.3 Byte Alignment

The receiver supports the alignment of accumulated bits to their original transmitted character boundaries through Idle character recognition. Byte alignment is supported in Byte and TBI interface modes. Byte alignment is enabled by asserting BSYNC high.

3.3.3.1 Byte Alignment and Realignment Method

At power-up, the receiver starts an alignment procedure, searching for the 10-bit pattern defined by the 8B/10B Idle code. Alignment logic checks for the distinct Idle pattern, ‘0011111010’ and ‘1100000101’ (ordered bit 0 to bit 9), characteristic of the K28.5 Idle pattern. The search is done on the 10-bit data in the receiver, and is therefore independent being in Byte or TBI mode. Alignment requires a minimum of four, error-free, received Idle characters to ensure proper alignment and lock. Non-Idle characters may be interspersed with the Idle characters. The disparity of the Idle characters is not important to alignment and can be positive, negative or any combination.

The receiver begins data flow of received characters once alignment is established and locked. However, if word synchronization is enabled, received characters do not flow to the receiver interface until word synchronization is established. Alignment remains locked until any one of three events occur that indicate loss of alignment:

- Alignment is lost when a misaligned Idle sequence is detected. A misaligned Idle sequence is defined as four Idle characters with an alignment different than the

current alignment. Non-Idle characters may be dispersed between the four misaligned Idles, however, a properly aligned Idle character breaks the sequence. Alignment is automatically changed to the newly detected alignment without halting data flow.

- Alignment is lost when the number of received characters with 8B/10B coding errors outnumbers the non-errored characters by four. Credit for non-errored characters in excess of errored characters is limited to four, such that alignment is lost after four consecutive errored characters. Misalignment detection of this type is not available in TBI mode. The receiver restarts its alignment procedure and halts data flow until a new alignment is established.
- Alignment is lost when the DROP_SYNC input is set high for at least two clock periods. Current alignment is invalidated, the receiver restarts its alignment procedure and halts data flow until a new alignment is established. DROP_SYNC is level-sensitive and asynchronous.

When establishing byte alignment, or when data flow is interrupted due to misalignment, the receiver's RECV_*x*_ERR signal is high and the "Not Byte Sync" error is reported as described in Section 3.3.6.3.

NOTE

During the power up sequence the receiver interface may have indeterminate data present and the RECV_*x*_CLK is disabled. When PLL lock is established the RECV_*x*_CLK becomes active and the receiver interface output data is forced to a negative running K28.5 character (0x17C on bits 9, k, data[7:0]) until a Byte-Sync is established.

3.3.3.2 Non-Aligned Method

No attempt is made to align the incoming data stream when BSYNC is low. The bits are simply accumulated into 10-bit characters and forwarded. This mode should be used only with TBI mode, TBIE set high, and with Word Synchronization disabled, WSE set low.

At system reset and until the MC92610's system PLL is locked to its reference, the receiver's RECV_*x*_ERR signal is high and the "Not Byte Sync" error is reported, as described in Section 3.3.6.3. This may seem confusing because no byte synchronization is performed; but in this mode the status simply indicates that the system PLL has not achieved lock.

3.3.4 Word Synchronization

The four receivers in the MC92610 can be used cooperatively to receive 32-bit wide aligned word transfers. Word synchronization is enabled by asserting WSE high. Multiple

MC92610 devices may be used to receive multi-word aligned transfers, through the use of the word synchronization bus interface.

Word synchronization is possible in Byte or TBI mode. However, word synchronization is dependent on the detection of simultaneously transmitted word synchronization events that contain Idle characters. Therefore, if operating in TBI mode, the Idle character must be a supported member of the code set.

3.3.4.1 Word Synchronization Method

Word synchronization aligns characters in the receiver's alignment FIFO. Synchronization is accomplished by lining up *word synchronization events* detected by each of the receivers, such that all are coincident at the same stage of their FIFO.

A word synchronization event is defined as four consecutive non-errored Idle (K28.5) characters followed by at least one non-Idle character.

Word synchronization events must be generated at all concerned transmitters simultaneously in order for synchronization to be achieved. Word synchronization events must be received at all receivers within 40 bit-times of each other. Word synchronization is not attempted until all receivers are byte align locked.

Word synchronization events are used to establish a relationship between the received bytes in each of the receivers. The bytes of a word are matched and presented simultaneously at the receiver interface. Once synchronization is achieved the receiver tolerates $\pm$6 bit-times of drift between receivers. If drift exceeds $\pm$6 bit-times the receiver will continue to operate. However, the received bytes will no longer be synchronized properly because the receiver remains locked on the initially established synchronization. Word synchronization remains locked until any one of the following three events occur that indicate loss of synchronization:

Word synchronization lock is lost when one or more of the receivers lose or change byte alignment. Byte alignment loss is described in Section 3.3.3.1.

Word synchronization lock is lost when overrun/underrun is detected on one or more of the receivers, see Section 3.3.6.3 for more about overrun/underrun.

Word synchronization lock is lost when explicitly invalidated by asserting DROP_SYNC high for at least two clocks. When lock is lost, word synchronization must be re-established before data flow through the receiver resumes.

The receiver interface is disabled during word synchronization. No data is produced at its outputs until word synchronization is achieved and the first non-Idle character is received. When establishing word synchronization, or when word synchronization is lost, the receiver's RECV_*x*_ERR signal is high and the "Not Word Sync" error is reported as described in Section 3.3.6.3.

For further details on how the receiver interface is disabled during initial word synchronization see the note at the end of Section 3.3.3.1, “Byte Alignment and Realignment Method,” on page 3-8.

3.3.4.2 Word Synchronization Bus

Word synchronization information and timing are communicated across the word synchronization bus. The WSO output drives the bus that is connected to the WSI inputs of other MC92610 devices with which word synchronization is desired. One of the MC92610 devices is connected as the Leader and the others as the Followers. The Leader’s WSO output is used to drive its own WSI input and the WSI inputs of all of the Followers. The WSO output of the Follower devices is not used and is not connected.

NOTE

In order for word synchronization to operate properly in applications where only one MC92610 is used, the WSI input must be tied high.

3.3.4.3 Multi-Chip Word Synchronization

Up to four MC92610 devices may be connected to perform multi-word synchronized data transfer. Configurations of one, two, three and four devices are possible supporting 32-bit, 64-bit, 96-bit and 128-bit wide data transfers. One of the MC92610 devices is connected as the Leader and the others as the Followers as described in Section 3.3.4.2.

Multi-chip word synchronization uses the same mechanisms for word synchronization as single-chip word synchronization as described in Section 3.3.4.1. Word synchronization events must be generated at all concerned transmitters simultaneously in order for synchronization to be achieved. Word synchronization events must be received at all receivers within 40 bit-times of each other.

When the Leader device detects a word synchronization event at its receivers, it communicates the timing of the event to the Follower devices through the Word Synchronization Bus. The Follower devices use this timing to establish their own word synchronization relative to the Leader.

Once synchronization is achieved, $\pm$6 bit-times of drift between all of the devices’ receivers is tolerated. If drift exceeds $\pm$6 bit-times the devices will continue to operate. However, the devices will no longer be synchronized properly because they remain locked on the initially established synchronization.

If any of the devices lose word synchronization, as described in Section 3.3.4.1, all of the receiving devices must be forced to lose synchronization to ensure proper resynchronization. Therefore, system logic should detect loss of word synchronization on all of the devices by decoding the “Not Word Sync” error. Then the DROP_SYNC should

be set high for at least two clock cycles and then released to force all devices to re-establish word synchronization.

3.3.4.4 Recommended Mode States for Word Synchronization

Word synchronization can only be used with certain operating modes and has limited application in others. Table 3-2 describes the relationship between modes and word synchronization.

Table 3-2. Word Synchronization States

Mode	Signals	Recommended State	Description
Word Synchronization	WSE	High	Enables word synchronization.
Byte Synchronization	BSYNC	High	Word synchronization depends upon Idle character detection. Byte alignment is required for Idle detection.
Add/Delete Idle	ADIE	High	When enabled, allows the receiver to add/delete Idle patterns in order to maintain word alignment. This is the recommended operating mode when the Reference Clock is being used to time the receiver interface (RCCE set low) and there is a frequency offset between the transmitter and receiver. Idles are added or dropped to maintain word alignment.
Recovered Clock	RCCE	Low	The receiver interface must be timed with the Reference Clock when utilizing multi-chip word synchronization. Timing errors will occur on the word synchronization bus if RCCE is high. If utilizing single chip word synchronization, then either the Recovered Clock or the Reference Clock may be used to time the receiver interface. RCCE may be set as it best suites the application.
Receiver Interface Clock Select	RECV_REF_A	High	If utilizing single chip word synchronization and using the Recovered Clock (RCCE set high) then receiver A's recovered clock must be used for all receivers. The data at the receiver interfaces will be skewed if the individual receiver recovered clocks (RECV_REF_A set low) are used to time the receiver interfaces.
Transceiver Disable	XCVR_*x*_DISABLE	Low	All four transceivers must be enabled for word synchronization.
Repeater Mode	REPE	Low	Word synchronization is not recommended in Repeater mode.
Ten-Bit Interface	TBIE	n/a	When enabled, the Idle character must be part of the TBI code set. When disabled, the Idle is naturally supported by the 8B/10B codes.
Link Multiplexer Mode	LME	n/a	Word synchronization operates normally in Link Multiplexer mode.

Table 3-2. Word Synchronization States (continued)

Mode	Signals	Recommended State	Description
Half-Speed Enable	HSE	n/a	Does not affect word synchronization.
Double Data Rate	DDRE	n/a	Does not affect word synchronization.

3.3.5 8B/10B Decoder

The 8B/10B decoder takes the 10-bit character from the Transition Tracking Loop and decodes it according to the 8B/10B coding standard [1,2]. The decoder does two types of error checking. First it checks that all characters are a legal member of the 8B/10B coding space. The decoder also checks for running disparity errors. If the running disparity exceeds the limits set in the 8B/10B coding standard then a disparity error is generated.

NOTE

8B/10B coding is meant only to improve data transmission characteristics and is not a good error detection code. Many 8B/10B characters alias to other valid 8B/10B characters in the presence of bit errors. Error detection and correction techniques must be applied outside of MC92610 if better than 10^{-12} bit error rate is required.

An illegal character or disparity error sets the RECV_*x*_ERR signal high, coincident with the received data for one byte output period. The “Code Error” or “Disparity Error” is reported as described in Section 3.3.6.3. It is difficult to determine the exact byte that causes a disparity error, so the error should not be associated with a particular received byte. It is rather a general indicator of the improper operation of the link. Its intended use is for the system to monitor link reliability.

The 8B/10B decoder is bypassed when operating in TBI mode (TBIE set high.)

3.3.6 Receiver Interface

The receiver interface facilitates transfer of received data to the system. It also provides information on the status of the link. Table 3-1 describes each of the signals involved in receiver operation.

The receiver interface, through which received data is obtained, may be operated in Byte mode or in TBI mode. There are several timing mode options for the receiver interface. Each of the operating modes are described below.

3.3.6.1 Byte Interface

Byte interface mode is enabled by setting TBIE low. Received data is a byte (8 bits) of uncoded data when in Byte mode. The internal 8B/10B decoder is used to decode data from the 10-bit character received. The received byte is on the RECV_*x*_7–RECV_*x*_0 signals.

The RECV_*x*_K is high when the byte represents a special 8B/10B code, otherwise it is low, indicating that the byte is normal data.

The RECV_*x*_IDLE is high when the byte is the special 8B/10B Idle (K28.5) code. This can be used by system logic for synchronization or data parsing. RECV_*x*_IDLE is low when the byte is normal data or a non-Idle special code. RECV_*x*_IDLE is high and RECV_*x*_K is low to indicate that an underrun/overrun error occurred. See Section 3.3.6.3 for more information on error conditions.

The RECV_*x*_ERR is low when the receiver is operating normally, and is high when received data contains an error or the receiver is in an error state. The state of the RECV_*x*_IDLE and RECV_*x*_K signals are decoded to determine the error condition. Table 3-3 describes the error codes and their meaning.

3.3.6.2 Ten-Bit Interface

Ten-Bit Interface mode is enabled by setting TBIE high. Received data is ten-bits of pre-coded data when in TBI mode. The internal 8B/10B decoder is not used and it is assumed that decoding is done externally. Ten-bit data is the collection of signals: RECV_*x*_9, RECV_*x*_K, and RECV_*x*_7–RECV_*x*_0 making up bits 9 through 0, respectively.

The RECV_*x*_IDLE is high when the 10-bit character is the special 8B/10B Idle (K28.5) code. This can be used by system logic for synchronization or data parsing. RECV_*x*_IDLE is low when the data is normal data or a non-Idle special code.

The RECV_*x*_ERR is low when the receiver is operating normally, and is high when the receiver is in an error state. The state of the RECV_*x*_IDLE signal is decoded to determine the error condition. Table 3-4 describes the error codes and their meaning.

3.3.6.3 Receiver Interface Error Codes

The receiver's status and data error conditions are coded on the RECV_*x*_ERR, RECV_*x*_IDLE and RECV_*x*_K signals. When RECV_*x*_ERR is low, the receiver is operating normally and no error conditions exist (with exception of Underrun/overrun error in Byte mode.) When RECV_*x*_ERR is high, the data on the receiver's output is questionable due to an error condition or lack of synchronization. Initially, RECV_*x*_ERR is high indicating that the receiver is in one of its start-up phases. Table 3-3 describes the error conditions and their signal coding for Byte mode. Table 3-4 describes the error conditions and their signal coding for TBI mode. The Priority column in the tables show

the error reported if multiple errors occur at the same time. The lower the Priority numbered errors are reported first.

Table 3-3. Receiver Interface Error Codes (Byte Interface)

RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_IDLE	Priority	Description
Low	Low	Low	8	Normal operation, valid data character received.
Low	Low	High	3	Overrun / Underrun: The receiver interface synchronization logic detected an overrun/underrun condition. Data may be dropped or repeated.
Low	High	Low	7	Normal operation, valid control character received.
Low	High	High	6	Normal operation, valid Idle (K28.5) character received.
High	Low	Low	4	Code Error: The 8B/10B decoder detected an illegal character.
High	Low	High	5	Disparity Error: The 8B/10B decoder detected a disparity error.
High	High	Low	1	Not Byte Sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.
High	High	High	2	Not Word Sync: The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.

Table 3-4. Receiver Interface Error Codes (Ten-Bit Interface)

RECV_*x*_ERR	RECV_*x*_IDLE	Priority	Description
Low	Low	4	Normal operation, non-Idle character received.
Low	High	3	Normal operation, Idle (K28.5) character received.
High	Low	1	Not Byte/Word Sync: The receiver is in start-up or has lost byte or word alignment and is searching for alignment.
High	High	2	Overrun/Underrun: The receiver interface synchronization logic detected and overrun/underrun condition. Data may be dropped or repeated.

3.3.7 Receiver Interface Clock Timing Modes

The receiver interface is double data rate, source synchronous. Each of the receiver's eleven output signals (eleven for byte interface and twelve for ten-bit interface) are timed relative to the rising and falling edges of the receiver interface clock output, RECV_*x*_CLK. The receiver interface clock frequency may be selected between its own recovered clock frequency, receiver A's recovered clock frequency, or the frequency of the reference clock input(s) REF_CLK_P / REF_CLK_N.

The recovered clock enable signal, RCCE, determines if the receiver interface is timed to the recovered clock or to the local reference clock. Asserting RCCE enables timing relative to the recovered clock, and set low enables timing relative to the reference clock. When

RCCE is asserted high, then the signal RECV_REF_A is used to select the recovered clock to be used. If RECV_REF_A is asserted then Channel A's recovered clock is used for all four channels. If it is low then each channel uses its own recovered clock.

The receiver interface clock signals, RECV_*x*_CLK, will always be present when the PLL is in lock. This is true even if there is no signal present on the serial inputs or if the receiver has not achieved alignment or byte sync. The frequency of the receiver clock will be the local reference clock. The clock signals however, are not present during power up or when the MC92610 is in reset mode and the PLL is not locked.

3.3.7.1Recovered Clock Timing Mode

With RCCE asserted, the recovered clock signal, RECV_*x*_CLK, is generated by the receiver and, on average, runs at the reference clock frequency of the transmitter at the other end of the link. The recovered clock is not generated by a clock recovery PLL, but is generated by the receiver bit-accumulation and byte-alignment logic.

In order to track a transmitter frequency that is offset from the receiver's reference clock frequency, the duty cycle and period of the recovered clock is modulated. The MC92610 is designed to tolerate up to a 200 ppm of frequency offset. The recovered clock duty cycle may be reduced or increased (by 200 ps, if the nominal frequency is 156.25 Mhz) in order to match the transmitter frequency.

For example: If the transmitter is sending data at a rate faster than the receiver, then a shortened cycle is generated as needed to track the incoming data rate. Alternately, if the transmitter is running slower than the receiver, then a long cycle is generated.

All receiver channel outputs are source synchronous with their respective RECV_*x*_CLK outputs. If the receivers are being operated in word synchronization mode (WSE = high), the data for all four receivers are timed relative to link A's recovered clock RECV_A_CLK. In word synchronization all four clocks are derived from channel A and may be used if necessary.

3.3.7.2 Reference Clock Timing Mode

Data is timed relative to the local reference clock frequency when RCCE is low. Synchronization between the recovered clock and the reference clock is handled by the receiver interface. Frequency offset between the transmitter's reference clock and the receiver's reference clock causes overrun/underrun situations. Overrun occurs when the transmitter is running faster than the receiver. Underrun occurs when the transmitter is running slower than the receiver.

In an overrun situation, a byte of data needs to be dropped in order to maintain synchronization between the clock domains. The receiver interface searches for an Idle byte to drop when overrun is imminent. However, the Idle is dropped only if Add/Delete Idle (ADI) mode is enabled by asserting ADIE. When enabled, Idle patterns are dropped to

maintain synchronization. If sufficient Idle patterns are not available to drop, receiver overrun may occur. When overrun occurs, the “overrun/underrun” error is reported as described in Section 3.3.6.3, “Receiver Interface Error Codes,” for one byte clock period. An overrun error is also reported if ADI mode is disabled and overrun occurs, even if Idles are available to drop. A sufficient number of Idles must be transmitted to guard against overrun. The frequency of Idles can be computed based upon the maximum frequency offset between transmitter and receiver in the system. The number of bytes (characters) that can be transmitted between Idles is:

$(10^6 / N) - 1$ bytes

where: N is the frequency offset in ppm.

In an underrun situation, a byte of data needs to be added in order to maintain synchronization between the clock domains. The receiver interface adds an Idle byte when underrun is imminent. However, the Idle is added only if Add/Delete Idle (ADI) mode is enabled by asserting ADIE. If ADI mode is disabled and underrun occurs, the “overrun/underrun” error is reported as described in Section 3.3.6.3, “Receiver Interface Error Codes,” for a one byte clock period.

3.3.8 Half-Speed Mode

Half speed (HS) mode, enabled when HSE is high, operates the receiver in its lower speed range. In HS mode, the link speed is 1.25 Gbps (1.5625 gigabaud.) The receiver interface operates at half speed as well, in pace with received data.

3.3.9 Repeater Mode

Repeater mode configures the MC92610 quad device into a 4-link receive-transmit repeater. In this mode, received data is forwarded to the transmitter for re-transmission. Link A’s receiver forwards to Link A’s transmitter, Link B’s receiver to Link B’s transmitter and so on. The receiver’s data outputs and status signals reflect the received data and the current status of the receiver. See Section 2.3.1.4 for more information on repeater mode.

3.3.10 Link Multiplexer Mode

Link multiplexer mode configures the MC92610 quad device into a dual transceiver. The Link multiplexer mode is enabled by asserting LME high. Receivers A and C are active and are used to receive data. The input circuitry to receivers B and D are disabled and inactive.

The advantage of this mode is that data from a single receiver is demultiplexed onto two receiver interfaces. Their single data rate (SDR) operation allows full speed link operation while lowering the parallel interface speeds by one-half.

Data from receiver A is presented on receiver interfaces A and B. Once byte synchronization is achieved, the first non-Idle character received is output on receiver

interface A, the second on receiver interface B. It is recommended that Idles be transmitted simultaneously as A and B pairs. If Idles are transmitted on only one input byte, they must be on B to maintain the proper byte order in the 16 bit output. The link status codes on receiver interface A and B represent the status of the current character. Both sets of status signals are active and must be observed.

The received data is timed relative to the rising edge of the receiver interface clock, RECV_*x*_CLK. The receive interface may also be operated in DDR mode by asserting DDRE high.

Link Multiplexer mode is enabled by asserting LME high.

Chapter 4
System Design Considerations

This chapter describes the system design considerations for the MC92610, including clock configuration, device startup and initialization, and proper use of repeater mode.

4.1 Reference Clock Configuration

The clock inputs REF_CLK_P and REF_CLK_N are the differential reference clock inputs for the MC92610. The frequency of the clock signal applied to these inputs along with the settings on the configuration inputs determine the speed at which the serial links operate. Also, the legal ranges of reference clock frequencies vary depending on the configuration selected. Table 4-1 shows the ranges allowed for each configuration.

Table 4-1. Legal Reference Clock Frequency Ranges

HSE	LME	DDRE	Reference Frequency Min (MHz)	Reference Frequency Max (MHz)	Link Transfer Rate (Gigabaud)
Low	Low	Low	reserved	reserved	reserved
Low	Low	High	95.00	156.25	1.900 - 3.125
Low	High	Low	95.00	156.25	1.900 - 3.125
Low	High	High	47.50	78.125	1.900 - 3.125
High	Low	Low	reserved	reserved	reserved
High	Low	High	47.50	78.125	0.950 - 1.5625
High	High	Low	47.50	78.125	0.950 - 1.5625
High	High	High	23.75	39.0625	0.950 - 1.5625

NOTE

The device must be reset by setting $\overline{\text{RESET}}$ low, if the reference clock configuration is changed after power-up.

The clock inputs REF_CLK_P and REF_CLK_N are normally driven with a differential clock source. However, the reference clock may also be driven with a single-ended source. In this situation, the REF_CLK_P signal is driven by the single-ended clock source and the REF_CLK_N signal is held at the HSTL reference voltage as defined in Section 6.2. The

REF_CLK_N signal may be connected to its own reference voltage circuit or may share the reference voltage circuit used for the HSTL_VREF signal, if board layout allows.

4.2 Startup

The MC92610 begins a startup sequence upon application of the reference clock (REF_CLK_N/P input) to the device. This is considered a *cold* startup. The cold startup sequence is as follows:

1. PLL Startup
2. Receiver Initialization and Byte Alignment
3. Word Alignment (if enabled)
4. Run

The expected duration of each step in the startup sequence is shown in Table 4-2. A cold startup can be initiated at any time by setting $\overline{\text{RESET}}$ low. It is recommended that $\overline{\text{RESET}}$ be low at initial startup, however, it is not strictly required.

Table 4-2. Startup Sequence Step Duration

Startup Step	Typical Duration (in bit times)	Note
PLL Startup	20,480 + 25 µs	
Receiver Initialization	300	**WSE** = low
	460	**WSE** = high
Word Alignment	160	

4.3 Repeater Mode

The MC92610 may be configured into a four-link receive-transmit repeater by setting REPE high. In repeater mode data received on link A's receiver is forwarded to link A's transmitter, link B's receiver to link B's transmitter and so on. The configuration inputs may be used to control how the repeater handles the data as it passes through the repeater. Certain configurations are more effective than others for various applications. The transmitter at the source, the receiver at the destination and the repeater must have compatible configurations to ensure proper operation. The following sections describe how each configuration control affects repeater operation.

4.3.1 Ten-Bit Interface Mode

When the device is in TBI mode (TBIE set high) the internal 8B/10B encoder and decoder are bypassed and the ten-bit data received is forwarded directly to the transmitter. Running disparity is assumed correct and is not checked. This is important when using disparity based word synchronization where incorrect running disparity is used as a word

synchronization event marker. Ten-bit mode must be enabled for disparity based word alignment to operate properly because it allows the improper disparity to pass through the repeater. When Byte interface mode is enabled (TBIE set low) received data is passed through the 8B/10B decoder where it is converted into its eight-bit data or control byte. Running disparity and code validity are checked and reported with the received byte at the receiver interface as described in Section 3.3. The decoded byte is re-coded by the transmitter's 8B/10B encoder for transmission.

NOTE

Byte Interface mode must not be used with *Non-Aligned* mode.

4.3.2 Byte Alignment Mode

The Byte Alignment may be used in repeater mode as long as Ten-Bit Interface mode is not also being used.

When establishing byte alignment for the link through the repeater, the byte alignment sequence must be repeated twice, once for the repeater and once for the destination's receiver. For example, at least eight Idle characters must be transmit, four for repeater alignment and four for the destination's receiver alignment.

4.3.3 Word Synchronization Mode

Word synchronization may be used in Repeater mode. This allows the incoming bytes to be synchronized into their corresponding words, removing cable skew from the transmission source and re-establishing synchronization.

Similar to Byte Alignment, the Word Synchronization sequence must be repeated twice, once for the repeater and once for destination's receiver. For example, a 4 Idle/1 non-Idle word synchronization event must be transmit followed by a second 4 Idle/1 non-Idle word synchronization event to enable the entire link to establish word synchronization. Of course, byte alignment must be established, as described in Section 4.3.2, prior to word synchronization.

4.3.4 Recovered Clock Timing Mode

The MC92610's four transmitters are timed exclusively to the Reference Clock domain. Recovered Clock mode cannot be used in Repeater mode. The setting on the Recovered Clock Enable input, RCCE, is ignored when in Repeater mode and all data is timed to the Reference Clock.

4.3.5 Reference Clock Timing Mode

Repeater mode is timed exclusively to the reference clock domain as stated above. A frequency offset between the source transmitter and the repeater will cause the repeater's receiver to eventually overrun/underrun. To ensure that overrun/underrun does not cause data to be lost, add/drop idle mode must be used. Add/drop idle mode is enabled by setting ADIE high. The repeater adds or drops Idles from the data stream to maintain alignment to the reference clock. The guidelines for Idle density are discussed in Section 4.3.2.

4.3.6 Half-Speed Mode, Double Data Rate Mode

Half-speed mode and double data rate mode simply affect the frequency of the reference clock that must be provided and the timing of the receiver interface. All combinations of these modes are supported in repeater mode. See Section 3.3.8 for more information on half-speed mode and Section 3.3.6 for more information on double data rate mode.

4.4 Configuration and Control Signals

MC92610 has many configuration and control signals that are asynchronous to all inputs clocks. Most of the signals affect internal configuration state and must be set at power-up. If their state is changed after power-up, some require that the chip be reset by setting RESET_B low and then releasing high. While other configuration signals are meant to be changed during normal operation and do not require chip reset. However, these signals may still affect device operation. Table 4-3 lists all of the MC92610's asynchronous configuration and control signals and describes the effect of changing their state after power up.

Table 4-3. Asynchronous Configuration and Control Signals

Signal Name	Description	Effect of Changed State
XCVR_*x*_RSEL	Transceiver Redundant Link Select	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
XCVR_*x*_DISABLE	Transceiver Disable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
DROP_SYNC	Drop Synchronization	Receiver must re-establish byte and word synchronization.
XMIT_REF_A	Transmitter Reference Clock A Select	Device must be reset.
RECV_REF_A	Receiver Reference Clock A Select	Device must be reset.
XMIT_EQ_EN	Transmitter Equalization Enable	May cause short burst of bit errors.
RECV_EQ_EN	Receiver Equalization Enable	May cause short burst of bit errors.
XMIT_EN_ALL	Transmitter Enable, All Outputs	No action required.

Table 4-3. Asynchronous Configuration and Control Signals (continued)

Signal Name	Description	Effect of Changed State
TBIE	Ten-Bit Interface Enable	Device must be reset.
HSE	Half-Speed Enable	Device must be reset.
DDRE	Double Data Rate Enable	Device must be reset.
BSYNC	Byte Synchronization Mode	Device must be reset.
ADIE	Add/Drop Idle Enable	Device must be reset.
REPE	Repeater Mode Enable	Device must be reset.
LME	Link Multiplexer Mode	Device must be reset.
RCCE	Recovered Clock Enable	Device must be reset.
WSE	Word Synchronization Enable	Device must be reset.
LBE	Loop Back Enable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
LBOE	Loop Back Output Enable	No action required.
$\overline{\text{RESET}}$	System Reset Bar	Device is reset.

4.5 Power Supply Requirements

The recommended board for the MC92610 has a minimum of two solid planes of one ounce copper. One plane is to be used as a ground plane and the second plane is to be used for the 1.8V supply. It is recommended that the board has its own 1.8V and 1.5V regulators with less than 50mV ripple.

4.6 Phase Locked Loop (PLL) Power Supply Filtering

An analog power supply is required. The TX_PLLVDD signal provides power for the analog portions of the PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 4-1. For maximum effectiveness, the filter circuit is placed as close as possible to the TX_PLLVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the TX_PLLVDD ball. The 0.003mF capacitor is closest to the ball, followed by the 1 mF capacitor, and finally the 1 W resistor to Vdd on the 1.8V power plane. The capacitors are connected from TX_PLLVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

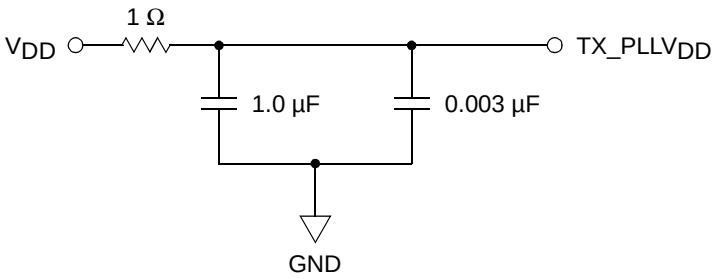


Figure 4-1. PLL Power Supply Filter Circuits

4.7 Power Supply Decoupling Recommendations

The MC92610 requires a clean, tightly regulated source of power to ensure low jitter on transmit, and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used, to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

First, the board should have about 10 x 10nF SMT ceramic chip capacitors as close as possible to the 1.8v (Vdd and XVdd) balls of the device. The board should also have about 10 x 10nF SMT ceramic chip capacitors as close as possible to the 1.5v (V_{DDQ}) balls of the device. Where the board has blind vias, these capacitors should be placed directly below the MC92610 supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the MC92610, as close to the supply and ground connections as possible.

Second, there should be a 1uF ceramic chip capacitor on each side of the MC92610 device. This should be done for both the 1.8v supply and the 1.5v supply.

Third, between the MC92610 device and the voltage regulator, there should be a 10uF, low equivalent series resistance (ESR) SMT tantalum chip capacitor, and a 100uF, low ESR SMT tantalum chip capacitor. This should be done for both the 1.8v supply and the 1.5v supply.

4.8 HSTL Reference Voltage Recommendation

The MC92610 uses HSTL Class-I inputs and outputs for all of its high-frequency parallel interface signals. The HSTL Class-I interfaces are compatible with the EIA/JEDEC standard EIA/JESD8-6 [3].

HSTL Class-I inputs define their switching thresholds about a reference voltage supplied at an input of the device. The reference voltage is applied to the HSTL_VREF input of the MC92610. The reference voltage, referred to as V_{REF} in Table 6-3, must fall within the

minimum and maximum voltages as specified and must have no more than 2 percent peak-to-peak AC noise. In practice, V_{REF} for the HSTL inputs should track the variations in the DC value of V_{DDQ} of the sending device for best noise margin. The value of V_{REF} is to be selected by the user to provide optimum noise margin. Figure 4-2 shows a recommended circuit topology to generate V_{REF} with recommended ceramic chip filter capacitor.

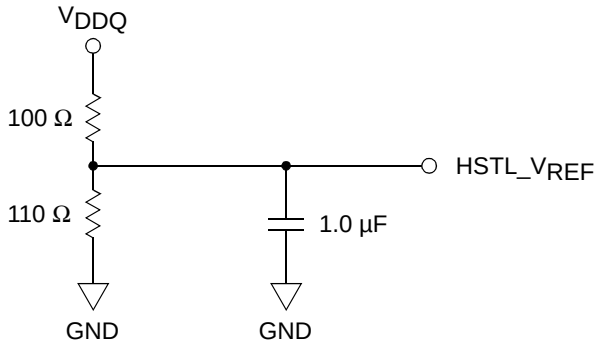


Figure 4-2. HSTL Class-I V_{REF} Circuit

4.8.1 Voltage Reference for Single-Ended Reference Clock Use

The differential reference clock inputs, REF_CLK_P/N, may also be driven by a single-ended source as described in Section 4.1. The REF_CLK_N input must be set at VREF for single-ended operation of REF_CLK_P. The REF_CLK_N signal may be connected to its own reference voltage circuit or may share the reference voltage circuit used for the HSTL_VREF signal, if board layout allows.

4.9 Impedance Control Reference Recommendation

The MC92610 has an integrated active impedance calibration circuit to ensure the best possible impedance control of the receiver's link termination resistors. The calibration circuit uses an externally established impedance against which internal impedance is calibrated. The user connects a 250 Ω, 1percent tolerance, resistor between the MC92610 Z_CALIB input and ground. The Z_CALIB input may be tied to GND to disable impedance calibration, or may be tied to VDD which will set the input impedance to its maximum value. Figure 4-3 shows an example impedance reference circuit topology.

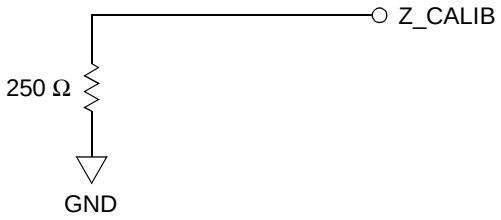


Figure 4-3. Impedance Reference Circuit

Chapter 5
Test Features

The MC92610 supports several test modes for in-system BIST and production testing. The MC92610 also has an IEEE Std. 1149.1 [4] compliant Test Access Port and Boundary Scan Architecture implementations. This chapter covers the JTAG implementation and the system accessible test modes.

5.1 IEEE Std. 1149.1 Implementation

This section describes the IEEE Std. 1149.1 compliant Test Access Port and Boundary Scan Architecture implementation in the MC92610.

NOTE

There are no internal pull-ups/pull-downs on any JTAG input. This is an exception to the IEEE Std. 1149.1 standard. The inputs should be properly terminated externally.

5.1.1 Test Access Port (TAP) Interface Signals

Table 5-1 lists the interface signals for the TAP.

Table 5-1. TAP Interface Signals

Signal Name	Description	Function	Direction	Active State
TCK	Test Clock	Test logic clock.	Input	-
TMS	Test Mode Select	TAP mode control input.	Input	-
TDI	Test Data In	Serial test instruction/data input.	Input	-
$\overline{\text{TRST}}$	Test Reset Bar	Asynchronous test controller reset.	Input	Low
TDO	Test Data Out	Serial test instruction/data output.	Output	-

NOTE

If $\overline{\text{TRST}}$ is not held low during power-up or does not receive an active low reset after power-up, the test logic may assume an indeterminate state disabling some of the normal transceiver functions. It is recommended that $\overline{\text{TRST}}$ be terminated in one of the following manners.

1. $\overline{\text{TRST}}$ be driven by a TAP controller that provides a reset after power-up.

2. Connect $\overline{\text{TRST}}$ to $\overline{\text{RESET}}$.

3. Terminate $\overline{\text{TRST}}$ with a 1K Ohm resistor (or hard wire) to ground.

5.1.2 Instruction Register

Bit Position	4	3	2	1	0
Field	IR				
Capture-IR Value	0	0	0	0	1

Figure 5-1. Instruction Register

5.1.3 Instructions

Table 5-2 lists the Public instructions provided in the implementation and their instruction codes.

Table 5-2. Tap Controller Public Instructions

Instruction	Code	Enabled Serial Test Data Path
BYPASS	11111	Bypass Register
CLAMP	01100	Bypass Register
EXTEST	00000	Boundary Scan Register
HIGHZ	01001	Bypass Register
IDCODE	00001	ID Register
SAMPLE	00010	Boundary Scan Register

Table 5-3 lists the Private instruction codes that if executed could be hazardous to device operation. The user should not execute these instructions.

Table 5-3. Tap Controller Private Instruction Codes

Instruction Code	Instruction Code
10000	10001
10010	10011
10100	10101
10110	10111
11000	11001
11010	11011
11100	11101
11110	-

5.1.4 Boundary-Scan Register

A full description of the boundary scan register may be found in the BSDL file provided by Motorola upon request.

5.1.5 Device Identification Register (0x0280E01D)

	31			28	27														12	11									0
Field	VERSION				PART NUMBER															MANUFACTURER ID									
Value	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0	1

Figure 5-2. Device Identification Register

5.1.6 Performance

The performance and electrical properties of the tap controller, boundary scan, and JTAG inputs and outputs are described in Chapter 6, “Electrical Specifications and Characteristics.

5.2 System Accessible Test Modes

System accessible test modes are selected through the TST_0, TST_1 and LBE signals. Table 5-4 shows test mode state selection.

Table 5-4. Test Mode State Selection

TST_1	TST_0	LBE	Description
Low	Low	Low	Normal operation. No test mode enabled.
Low	Low	High	Loop back system test mode.
Low	High	Low	BIST sequence system test mode.

Table 5-4. Test Mode State Selection

TST_1	TST_0	LBE	Description
Low	High	High	Loop back BIST sequence system test mode.
High	Don't care	Don't care	Reserved.

5.2.1 Loop Back System Test

The MC92610 can be configured in loop back mode where the transmitted data is looped back to its receiver independent of the receiver's link inputs. This is enabled by setting LBE high. The characters transmitted are controlled by the normal transmitter controls. If the transceiver is working properly, the data/control characters transmitted are received by the receiver. This allows system logic to use various data sequences to test the operation of the transceiver.

The data is looped back though the primary link path if XCVR_*x*_RSEL is low and through the redundant path if XCVR_*x*_RSEL is high.

The loop-back signals are electrically isolated from the XLINK0/1_*x*_P or XLINK0/1_*x*_N output signals. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally. When in loop-back mode, the LBOE signal controls the action of the selected link output signals. When LBOE is low, the XLINK0_*x*_P / XLINK1_*x*_P or XLINK0_*x*_N / XLINK1_*x*_Noutput signals are undriven and are high-impedance. When LBOE is high, the link output signals enabled by XCVR_*x*_RSEL continue to operate normally.

The receiver's link input signals, RLINK0_*x*_P / RLINK1_*x*_P and RLINK0_*x*_N / RLINK1_*x*_N, are electrically isolated during loop back mode, such that their state does not affect the loop back path.

5.2.2 BIST Sequence System Test Mode

The MC92610's transmitter has an integrated, 23rd order, Pseudo-Noise (PN) pattern generator. Stimulus from this generator may be used for system testing. The receiver, has a 23rd order signature analyzer that is synchronized to the incoming PN stream and may be used to count character mismatch errors relative to the internal PN reference pattern.

This implementation of the 23-bit PN generator and analyzer uses one of the two the polynomials depending on the state of BIST_MODE_SEL:

PN Equation 1: $f = 1 + x^5 + x^{23}$ (BIST_MODE_SEL asserted low)

PN Equation 2: $f = 1 + x^{18} + x^{23}$ (BIST_MODE_SEL asserted high)

When inter-operating with Motorola's 1.25 Gbaud SERDES devices (MC92600 or MC92602) use PN equation 1. PN equation 2 is meant for use with external test equipment

that supports this PN equation. Either may be used when inter-operating with another MC92610 device as long as both devices use the same PN equation.

In addition to using PN equation 2, setting BIST_MODE_SEL high causes the transmitter to insert 2 Idle characters for every 2048 PN characters transmit. This makes Idles available to be removed to account for frequency offset between devices. The receiver will properly handle the inserted Idles when analyzing the PN character stream.

NOTE

For the two Idle characters to be inserted, the ADIE signal must be asserted. If the ADIE signal is low, the PN Equation 2 is generated with no inserted Idles.

The total mismatch error count is reset to zero when BIST mode is entered. The count is updated continuously while in BIST mode. The value of the count is presented on the receiver interface signals: RECV_*x*_7 through RECV_*x*_0, making up the eight-bit error count, ordered bits 7 through 0, respectively. The value of the count is *sticky* in that the count will not wrap to zero upon overflow, but rather, stays at the maximum count value (11111111).

The RECV_*x*_ERR, RECV_*x*_K and RECV_*x*_IDLE, have special meaning during this test mode. They report the status of the receiver and PN analysis logic. Table 5-5 describes the BIST error codes and their meaning.

The BIST sequence makes use of the 8B/10B encoder/decoder. Therefore, this test mode overrides the setting on TBIE signal and forces Byte Interface mode. The BIST sequence requires that a normal byte alignment mode be used. The setting of BSYNC is overridden, forcing the device into the Byte Aligned mode. Also, BIST exercises all transceivers and their transmission paths, ignoring the setting of LME. Finally, the BIST logic operates at the reference clock frequency, all received BIST data is synchronized to the reference clock frequency, overriding the setting of RCCE.

BIST is run at the speed indicated by the frequency of the reference clock and by the speed range selected by half-speed mode (HSE). The settings of WSE is not altered and BIST will follow its setting order to properly use this test mode, the system must provide the proper stimulus in a special sequence. The sequence is as follows:

Table 5-5. BIST Error Codes

RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_IDLE	Description
Low	Low	Low	BIST running, no PN mismatch this character.
High	Low	Low	BIST running, PN mismatch error this character.
High	Low	High	Receiver byte/word synchronized, PN analyzer is not locked.

Table 5-5. BIST Error Codes

High	High	Low	Not Byte Sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.
High	High	High	Not Word Sync: The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.

Step 1: Enter test mode by setting the test mode inputs as described in Table 5-4.

Step 2: Set $\overline{\text{RESET}}$ low and release high; wait PLL lock period (~32 µs at 3.125 gigabaud).

Step 3: Transmit to the receiver 32 or more Idle (K28.5) characters.

Step 4: Transmit to the receiver an 8B/10B encoded PN sequence as described above.

The transmitter will automatically go through step 3, transmitting 4,096 Idles, and step 4 upon entering this test mode. When testing is complete, the transceiver will need to be resynchronized before normal operation can resume.

NOTE

The receiver signature analyzers assume all four channels are being exercised. If BIST testing is being performed between devices, or by means of external loop back on selected channels, the unused channel receivers must be disabled or the analyzers will not go into the PN Sync state. That is, receivers not having an PN stimulus must have XCVR_*x*_DISABLE asserted. In link multiplexer mode (LME asserted), the secondary receiver interface (channels B and D), must be disabled.

5.3 Loop-Back BIST Sequence System Test Mode

The test mode is the combination of the Loop-Back and BIST Sequence System Test Modes. The device operates as described in Section 5.2.1 and Section 5.2.2. However, the need to go through the startup sequence is eliminated because the transmitter automatically goes through the proper sequence.

Chapter 6
Electrical Specifications and Characteristics

This chapter explains the electrical specifications and characteristics for the MC92610 device. This chapter consists of the following sections:

- Section 6.1, “General Characteristics,”
- Section 6.2, “DC Electrical Specifications,” and
- Section 6.3, “AC Electrical Characteristics.”

6.1 General Characteristics

This section presents the general technical parameters, the maximum and recommended operating conditions and for the MC92610.

6.1.1 General Parameters

The following provides a summary of the general parameters of the MC92610:

- Technology—0.25µ lithography, HiP4 CMOS, 5 layer metal
- Package—324 MAPBGA, 19x19mm Body Size, 1mm Ball Pitch
- Core Power Supply—1.8V $\pm$ 0.15V dc
- HSTL I/O Power Supply—1.5V $\pm$ 0.1 V dc *or* 1.8V $\pm$ 0.15V dc
- Link I/O Power Supply—1.8V $\pm$ 0.15V dc

6.1.2 Absolute Maximum Ratings

The following Table 6-1, describes the DC electrical characteristics for the MC92610.

Table 6-1. Absolute Maximum Ratings

Characteristics [1]	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	-0.3	2.2	V
PLL Supply Voltage	AV_{DD}	-0.3	2.2	V

Table 6-1. Absolute Maximum Ratings (continued)

Characteristics [1]	Symbol	Min	Max	Unit
HSTL I/O Supply Voltage	V_{DDQ}	-0.3	2.2	V
Link I/O Supply Voltage	XV_{DD}	-0.3	2.2	V
HSTL Input Voltage	V_{in}	-0.3	V_{DDQ}+0.3	V
CMOS Input Voltage	V_{in}	-0.3	V_{DD}+0.3	V
Link Input Voltage	V_{in}	-0.3	XV_{DD}+0.3	V
Storage Temperature Range	T_{stg}	-55	150	^oC
ESD Tolerance	HBM	2,000	-	V
	MM	200	-	V

1 Functional and tested operating conditions are given in Table 6-2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums are not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

6.1.3 Recommended Operating Conditions

Table 6-2 in this section describes the recommended operating conditions for the MC92610.

Table 6-2. Recommended Operating Conditions

Characteristic [1, 2]	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	1.65	1.95	V
PLL Supply Voltage	AV_{DD}	1.65	1.95	V
HSTL I/O Supply Voltage (1.5V Operation)	V_{DDQ}	1.40	1.60	V
HSTL I/O Supply Voltage (1.8V Operation)	V_{DDQ}	1.65	1.95	V
Link I/O Supply Voltage	XV_{DD}	1.65	1.95	V
HSTL Input Voltage	V_{in}	0	V_{DDQ}	V
CMOS Input Voltage	V_{in}	0	V_{DD}	V
Link Input Voltage	V_{in}	0	XV_{DD}	V
Junction Temperature	T_j	-40	105	^oC
Ambient Temperature [3]	T_a	–	–	^oC

1 These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

2 Recommended supply power-up order is V_{DD}, AV_{DD}, V_{DDQ}, XV_{DD}, however, any order is acceptable as long as Maximum Ratings are not exceeded.

3 Operating Ambient Temperature is dependent on proper thermal management to meet operating Junction Temperature

6.2 DC Electrical Specifications

Table 6-3 in this section describes the MC92610's electrical characteristics.

Table 6-3. DC Electrical Specifications

Characteristic [1]	Symbol	Min	Max	Unit
Core Supply Current [2]	I_{DD}	—	1040	mA
PLL Supply Current[2]	AI_{DD}	—	10	mA
HSTL I/O Supply Current[2]	I_{DDQ}	—	240	mA
Link I/O Supply Current[2]	XI_{DD}	—	70	mA
Total Power Dissipation (typical) [3]	P_D	—	—	mW
HSTL Reference Voltage	V_{REF}	0.68	0.9	V
HSTL Input High Voltage (DC)	V_{IH} DC	V_{REF} + 0.1	—	V
HSTL Input Low Voltage (DC)	V_{IL} DC	-	V_{REF} - 0.1	V
HSTL Input High Voltage (AC)	V_{IH} AC	V_{REF} + 0.2	-	V
HSTL Input Low Voltage (AC)	V_{IL} AC	-	V_{REF} - 0.2	V
HSTL Input Leakage Current, $V_{in} = V_{DDQ}$	I_{IH}	-	80	µA
HSTL Input Leakage Current, V_{in} = GND	I_{IL}	-	275	µA
HSTL Output High Voltage	V_{OH}	V_{DDQ}-0.4	-	V
HSTL Output Low Voltage	V_{OL}	-	0.4	V
HSTL Input Capacitance	C_{in}	-	8	pF
HSTL Output Impedance, Vout = V_{DDQ}/2	R_{out}	35	55	Ω
CMOS Input High Voltage	V_{IH}	1.0	-	V
CMOS Input Low Voltage	V_{IL}	-	0.5	V
CMOS Input Leakage Current, V_{in} = $_{VDDQ}$	I_{IH}	-	10	µA
CMOS Input Leakage Current, V_{in} = GND	I_{IL}	-	10	µA
CMOS Input Capacitance	C_{in}	-	10	pF
Link Common Mode Input Impedance	R_{cm}	2	4	kΩ
Link Differential Input Impedance (calibration active)	R_{diff}	90	115	Ω
Link Differential Input Impedance (calibration disabled)	R_{diff}	75	130	Ω
Link Common Mode Input Level [4]	V_{cm}	0.1	XV_{DD}-0.1	V

Table 6-3. DC Electrical Specifications (continued)

Characteristic [1]	Symbol	Min	Max	Unit
Link Differential Input Amplitude	ΔV_{in}	0.2	2.2	V_{p-p}
Link Input Capacitance	C_{in}	-	3	pF
Link Common Mode Output Level	V_{cm}	0.725	1.075	V
Link Differential Output Amplitude, 100Ω diff load (xmit equalization disabled)	ΔV_{out}	900	1350	mV_{p-p}
Link Differential Output Impedance	R_{out}	80	130	Ω

1 $V_{DD} = AV_{DD} = XV_{DD} = 1.8 \pm 0.15$ V dc, $V_{DDQ} = 1.5 \pm 0.1$ V dc, GND = 0 V dc, $-40 \leq T_j \leq 105°C$.

2 Currents maximums at $V_{DD} = AV_{DD} = XV_{DD} = V_{DDQ}$ =1.95 V dc, all links terminated, operating at full-speed.

3 P_D (typical) mWatts = 208 + 51n + 1.25nf + 3.96f; where n = number of active channels and f = Reference frequency in MHz.

4 Subject to absolute voltage on link input pin remaining in recommended range per Table 6-2.

6.3 AC Electrical Characteristics

The figures and tables in this section describe the AC electrical characteristics of MC92610. All specifications stated for T_j= -40°C to 105°C, $V_{DD} = AV_{DD} = XV_{DD}$ = 1.65V to 1.95V, V_{DDQ} = 1.4V to 1.6V.

6.3.1 Parallel Port Interface Timing

The following Figure 6-1 and Table 6-4 describe the transmitter DDR interface timing.

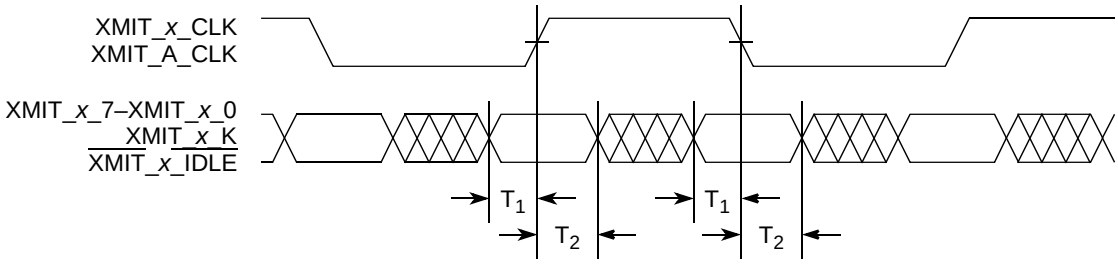


Figure 6-1. Transmitter DDR Interface Timing

Table 6-4. Transmitter DDR Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_1 [1]	Setup time to rising/falling edge of XMIT_x_CLK	0.480	-	ns
T_2 [1]	Hold time to rising/falling edge of XMIT_x_CLK	0.480	-	ns
Φ_{drift}	Phase drift between XMIT_x_CLK and REF_CLK_P	-180	180	degrees

1 156.25MHz operation

The following Figure 6-2 and Table 6-5 describe the transmitter SDR interface timing.

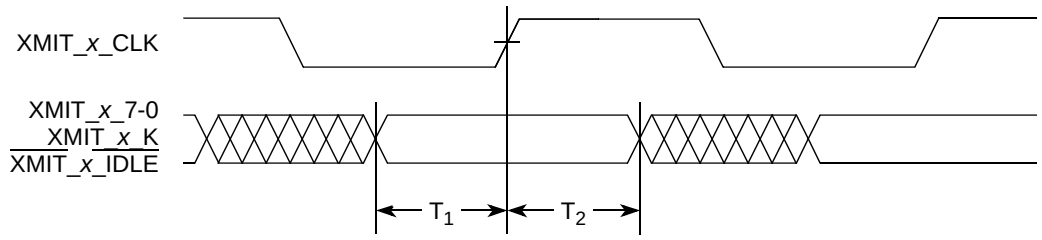


Figure 6-2. Transmitter Interface SDR Timing Diagram (LME = High, DDRE = Low)

Table 6-5. Transmitter SDR Timing Specification (LME = High, DDRE = Low)

Symbol	Characteristic	Min	Max	Unit
T_1 [1]	Setup time to rising edge of XMIT_x_CLK	0.480	-	ns
T_2 [1]	Hold time to rising edge of XMIT_x_CLK	0.480	-	ns

[1] 156.25MHz operation

The following Figure 6-3 and Table 6-6 describe the receiver DDR interface timing.

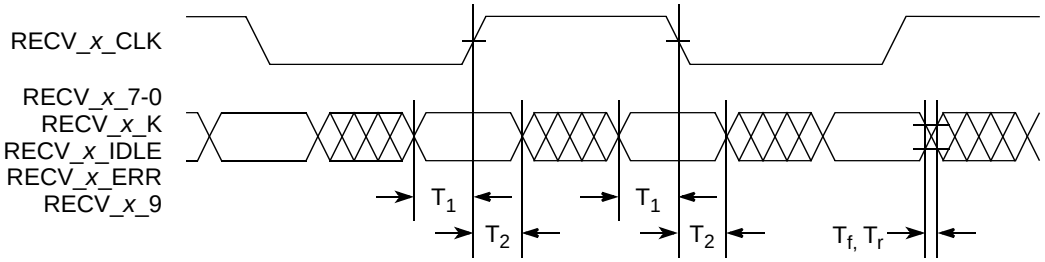


Figure 6-3. Receiver Interface DDR Timing Diagram

Table 6-6. Receiver DDR Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising/falling edge of RECV_x_CLK	0.96 [1]	-	ns
		4.0 [2]	-	ns
T_2	Output valid time after rising/falling edge of RECV_x_CLK	0.96 [1]	-	ns
		0.96 [2]	-	ns

Table 6-6. Receiver DDR Timing Specification (continued)

Symbol	Characteristic	Min	Max	Unit
T_f [3]	Output fall time	-	1.0	ns
T_r [3]	Output rise time	-	1.0	ns

1 Full speed, 156.25MHz operation (HSE = low).
2 Half-speed, 78.125MHz operation (HSE = high).
3 10pF output load.

The following Figure 6-4 and Table 6-7 describe the receiver SDR interface timing.

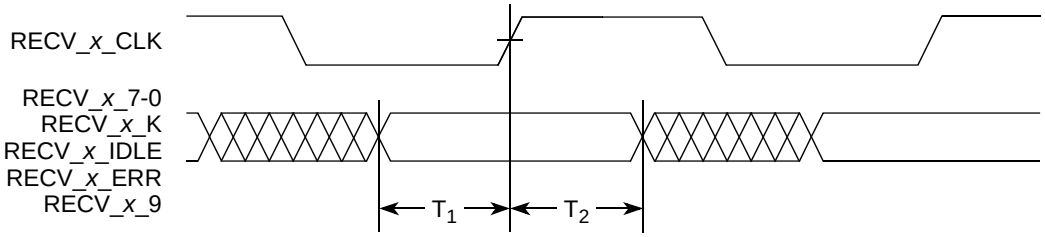


Figure 6-4. Receiver Interface SDR Timing Diagram (LME = High, DDRE = Low)

Table 6-7. Receiver SDR Timing Specification (LME = High, DDRE = Low)

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising edge of RECV_x_CLK	4.16 [1]	-	ns
		7.36 [2]	-	ns
T_2	Output valid time after rising edge of RECV_x_CLK	0.96 [1]	-	ns
		0.96 [2]	-	ns

1 Full speed, 156.25MHz operation (HSE = low).
2 Half-speed, 78.125MHz operation (HSE = high).

6.3.2 Word Synchronization Bus Timing

The following Figure 6-5 and Table 6-8 describe the word synchronization bus timing.

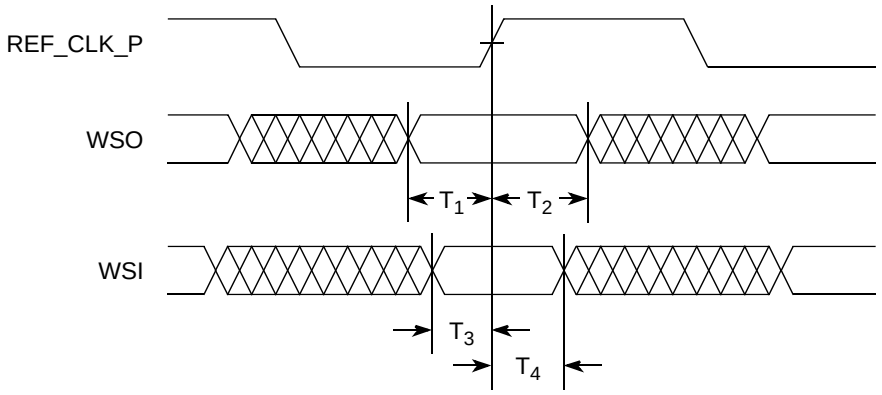


Figure 6-5. Word Synchronization Bus Timing Diagram

Table 6-8. Word Synchronization Bus Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising edge of REF_CLK_P	1.25 [1, 2]	-	ns
		4.45 [2, 3]	-	ns
T_2	Output valid time after rising edge of REF_CLK_P	1.66 [1, 2]	-	ns
		1.66 [2, 3]	-	ns
T_3	Setup time to rising edge of REF_CLK_P	-0.25	-	ns
T_4	Hold time to rising edge of REF_CLK_P	1.45	-	ns

1 Full speed, 156.25MHz operation (HSE = low).

2 10 pF output load.

3 Half-speed, 78.125MHz operation (HSE = high).

6.3.3 Reference Clock Timing

The following Figure 6-6 and Table 6-9 describe the reference clock timing.

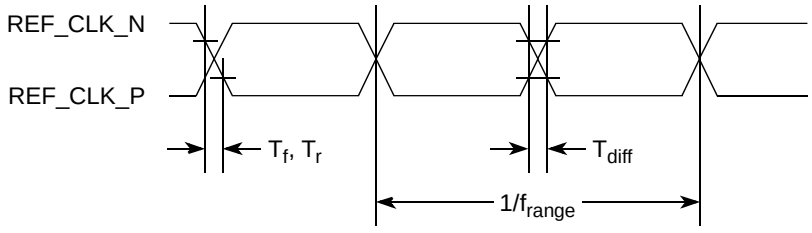


Figure 6-6. Reference Clock Timing Diagram

Table 6-9. Reference Clock Specification

Symbol	Characteristic	Min	Max	Unit
T_r [1]	**REF_CLK_P/N** rise time	-	2.0	ns
T_f [1]	**REF_CLK_P/N** fall time	-	2.0	ns
f_{range}	**REF_CLK_P/N** frequency range	95 [2]	156.25	MHz
		47.5 [3]	78.125	MHz
		23.75 [4]	39.0625	MHz
T_D	**REF_CLK_P/N** duty cycle	40	60	Percent
T_{diff}	**REF_CLK_P** to **REF_CLK_N** differential skew	-	1.0	ns
f_{tol}	**REF_CLK_P/N** frequency tolerance	-100	100	ppm
T_j [5]	**REF_CLK_P/N** input jitter	-	80	ps
T_{lock} [6]	PLL lock time	-	20,480 + 25 µs	bit-times

1 Measured between 10-90 percent points.

2 Full speed operation (HSE = low).

3 Half speed operation, not link multiplexer mode (HSE = high, LME = low) or half speed operation, link multiplexer mode SDR (LME = high, DDRE = low).

4 Half speed operation (HSE = high), link multiplexer mode DDR (LME = high, DDRE = high).

5 Total peak-to-peak jitter.

6 Lock time after compliant REF_CLK_P/N signal applied.

6.3.4 Receiver Recovered Clock Timing

The following Figure 6-7 and Table 6-10 describe the recovered clock timing.

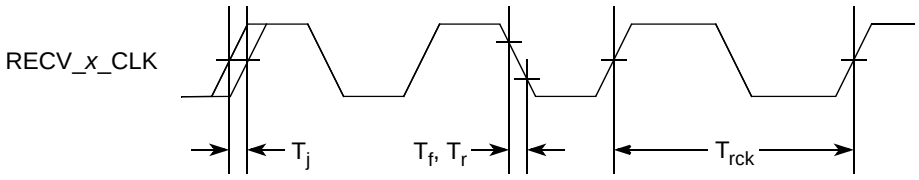


Figure 6-7. Recovered Clock Timing Diagram

Table 6-10. Recovered Clock Specification

Symbol	Characteristic	Min	Max	Unit
T_{rck}	RECV_*x*_CLK	6.20 [1, 2]	-	ns
		12.44 [3]	-	ns
T_r [4]	RECV_*x*_RCLK rise time	-	1.0	ns
T_f [4]	RECV_*x*_CLK fall time	-	1.0	ns

Table 6-10. Recovered Clock Specification (continued)

Symbol	Characteristic	Min	Max	Unit
T_j	RECV_*x*_CLK jitter	-	400 [1, 5]	ps
		-	720 [3, 5]	ps

1 Measured between 50-50 percent points, 156.25MHz REF_CLK, full speed DDR (HSE = low).
2 Includes jitter component.
3 Measured between 50-50 percent points, 78.125MHz REF_CLK, half speed DDR (HSE = high).
4 Measured between 10-90 percent points.
5 Total peak-to-peak jitter.

6.3.5 Serial Data Link Timing

The following Figure 6-8 and Table 6-11 describe the link differential output timing.

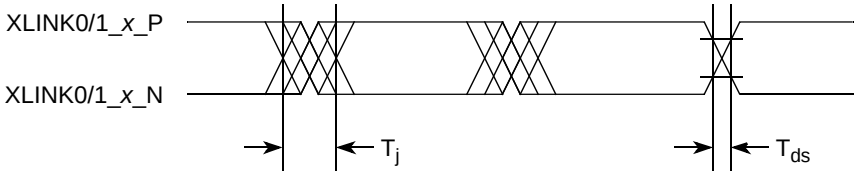


Figure 6-8. Link Differential Output Timing Diagram

Table 6-11. Link Differential Output Specification

Symbol	Characteristic	Min	Max	Unit
T_j [1]	Total jitter	-	0.35	UI
T_{dj} [1]	Deterministic jitter	-	0.17	UI
T_{ds} [1]	Differential skew	-	15	ps
X_{la} [2] $_t$	Transmit latency	150	190	bit-times

1 Measured between 50-50 percent points.
2 Rising edge REF_CLK_P to bit 0 transmit.

The following Figure 6-9 and Table 6-12 describe the link differential output timing.

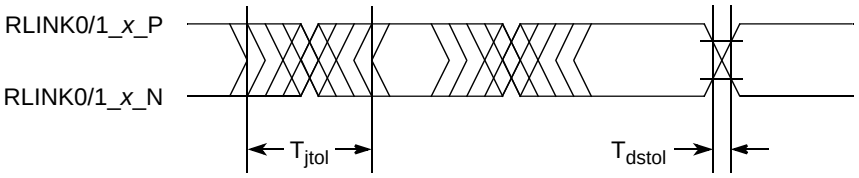


Figure 6-9. Link Differential Input Timing Diagram

Table 6-12. Link Differential Input Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_{jtol} [1, 2]	Total jitter tolerance	0.70	-	UI
T_{djtol} [1]	Deterministic jitter tolerance	0.36	-	UI
T_{dstol} [1]	Differential skew tolerance	75	-	ps
R_{lat}	Receive latency	270	340 [3]	bit-times
		-	400 [4]	bit-times
		-	440 [5]	bit-times
T_{acq}	Receiver phase acquisition time	-	300 [6]	bit-times

1 Measured between 50-50 percent points.

2 Includes 0.1 UI of band-limited sinusoidal noise, 1.875Mhz < f_{noise} < 20MHz.

3 Bit 0 at receiver input to parallel data out, no word synchronization.

4 Bit 0 at receiver input to parallel data out, single-chip word synchronization.

5 Bit 0 at receiver input to parallel data out, multi-chip word synchronization.

6 Measured with worst-case eye opening, Idle pattern, and reference PLL locked.

6.3.6 JTAG Test Port Timing

The following Figure 6-10 and Table 6-13 describe the JTAG test port timing.

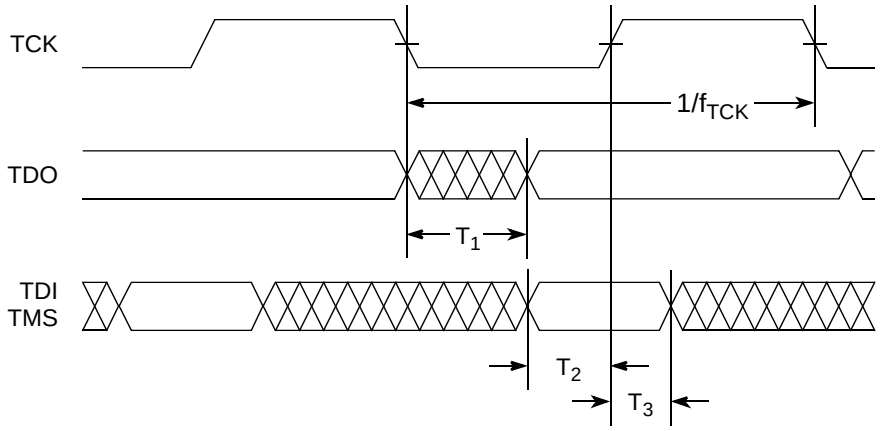


Figure 6-10. JTAG I/O Timing Diagram

Table 6-13. JTAG I/O Timing Specification

Symbol	Characteristic	Min	Max	Unit	Note
T_1 [1]	Output propagation time after falling edge of TCK	1.0	8.0	ns	1
T_2	Setup time to rising edge of TCK	1.0	-	ns	
T_3	Hold time to rising edge of TCK	0.5	-	ns	
f_{TCK}	TCK frequency	-	20	MHz	
T_D	TCK duty cycle	35	65	Percent	

[1] 10 pF output load

Chapter 7
Package Description

The following section provides the package parameters and mechanical dimensions of the MC92610 device. The MC92610 is offered in a 324 MAPBGA package. The 324 MAPBGA utilizes an aggressive 1 mm ball pitch and 19 mm body size for applications where board space is limited.

7.1 324 MAPBGA Package Parameter Summary

- Package Type—MAP Ball Grid Array
- Package Outline—19 mm x 19 mm
- Package Height—1.76 mm (typ.)
- Number of Balls—324
- Ball Pitch—1 mm
- Ball Diameter—0.63 mm (typ.)

7.2 Nomenclature and Dimensions of the 324 MAPBGA Package

Figure 7-1 provides the bottom surface nomenclature and package outline drawing of the 324 MAPBGA package. Figure 7-2 provides the package dimensions. Figure 7-3 provides a graphic of the package pin to signal mappings.

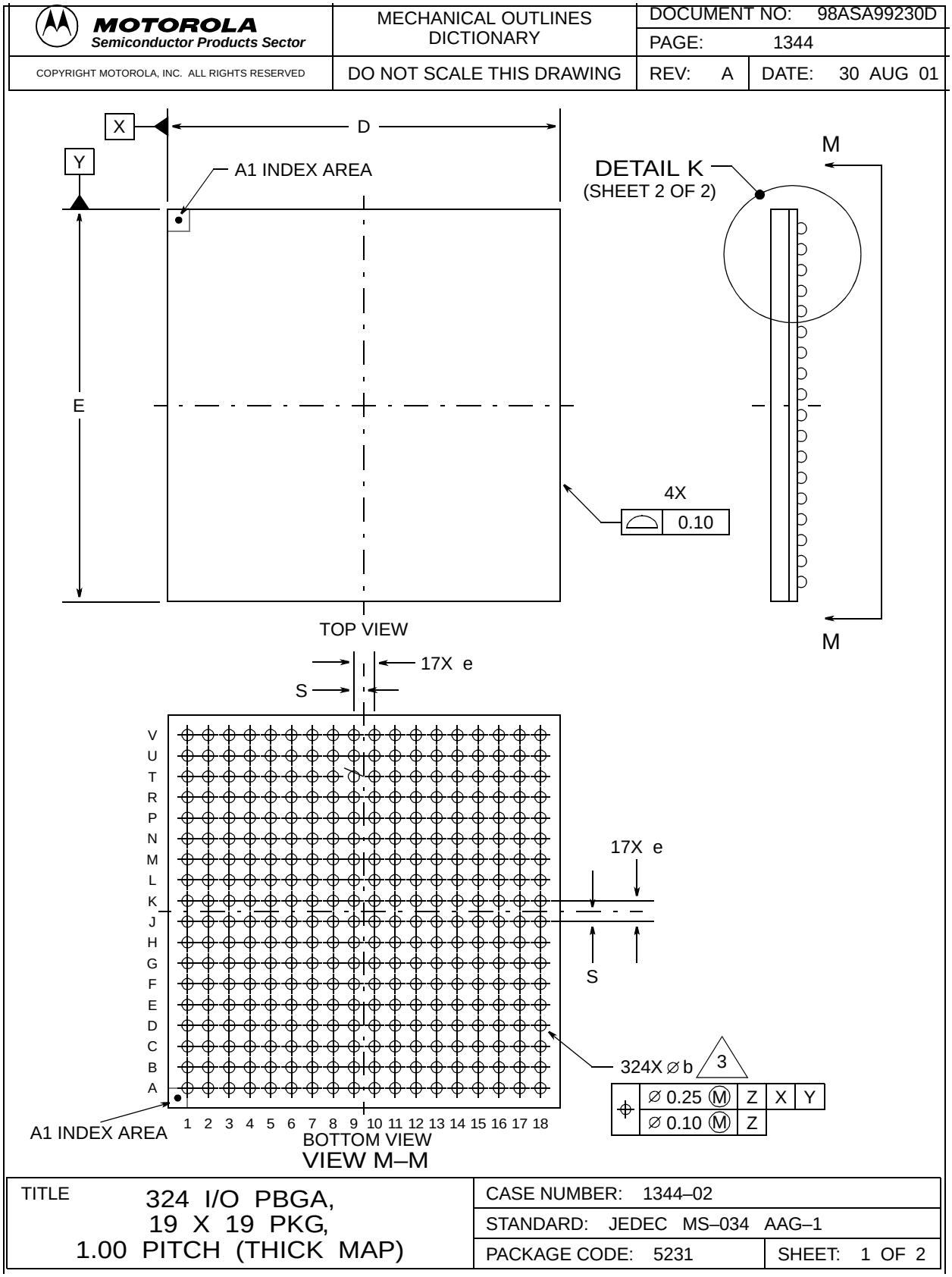
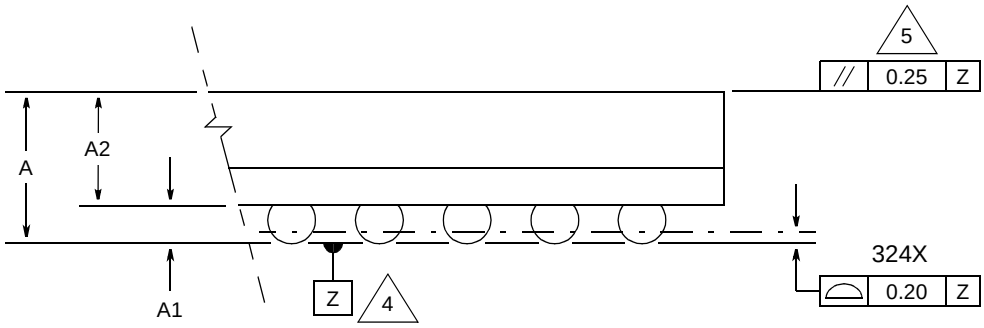


Figure 7-1. 324 MAPBGA Nomenclature

MOTOROLA Semiconductor Products Sector	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA99230D	
		PAGE: 1344	
	DO NOT SCALE THIS DRAWING	REV: A	DATE: 30 AUG 01



DETAIL K
VIEW ROTATED 90° CLOCKWISE

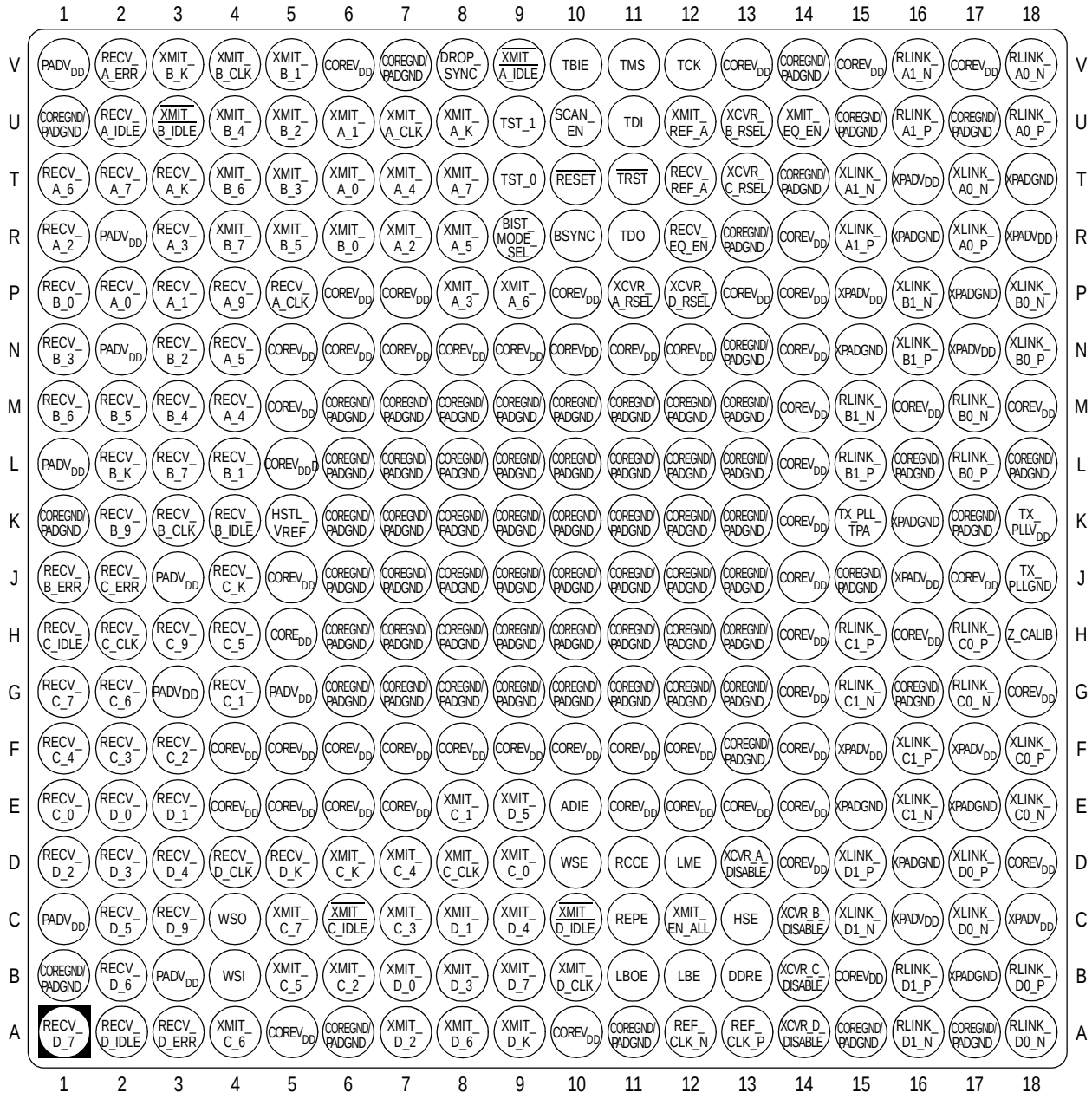
DIM	MIN	MAX
A	1.66	1.86
A1	0.45	0.55
A2	1.26 REF	
b	0.50	0.70
D	19.00 BSC	
E	19.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE	CASE NUMBER: 1344–02	
324 I/O PBGA, 19 X 19 PKG, 1.00 PITCH (THICK MAP)	STANDARD: JEDEC MS–034 AAG–1	
	PACKAGE CODE: 5231	SHEET: 2 OF 2

Figure 7-2. MAPBGA Dimensions



VIEW M–M (BOTTOM VIEW)

Figure 7-3. 324 MAPBGA Package

7.3 Package Thermal Characteristics

Thermal values for the 324 pin MAPBGA are listed below in Table 7-1. The values listed below assume the customer will be mounting these packages on a thermally enhanced mother board. This is defined as a minimum 4-layer board with one ground plane. The values listed below were simulated in accordance with established JEDEC (Joint Electron Device Engineering Council) standards.

Table 7-1. Package Thermal Resistance Values

Symbol	Description	Value	Units
$\theta_{ja\text{-}0}$	Thermal resistance from junction to ambient, still air	23	$^{o}C/W$
$\theta_{ja\text{-}2}$	Thermal resistance from junction to ambient, 200 LFM [1]	20	$^{o}C/W$
$\theta_{ja\text{-}4}$	Thermal resistance from junction to ambient, 400 LFM [1]	19	$^{o}C/W$

[1] Linear feet per minute

7.4 MC92610 Chip Pinout Listing

The MC92610 is offered in a 324 MAPBGA package. Table 7-2 lists the MC92610 signal to ball location mappings for the package. Also shown are signaling direction (input or output), and the type of logic interfaces.

Table 7-2. 324 MAPBGA Signal to Ball Mapping

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
XMIT_A_0	Transmitter A, Data bit 0	T6	Input	HSTL
XMIT_A_1	Transmitter A, Data bit 1	U6	Input	HSTL
XMIT_A_2	Transmitter A, Data bit 2	R7	Input	HSTL
XMIT_A_3	Transmitter A, Data bit 3	P8	Input	HSTL
XMIT_A_4	Transmitter A, Data bit 4	T7	Input	HSTL
XMIT_A_5	Transmitter A, Data bit 5	R8	Input	HSTL
XMIT_A_6	Transmitter A, Data bit 6	P9	Input	HSTL
XMIT_A_7	Transmitter A, Data bit 7	T8	Input	HSTL
XMIT_A_K	Transmitter A, Special Character (Data bit 8 for TBI mode)	U8	Input	HSTL
$\overline{\text{XMIT\_A\_IDLE}}$	Transmitter A, Idle Enable Bar, (Data bit 9 for TBI mode)	V9	Input	HSTL

Table 7-2. 324 MAPBGA Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
XMIT_A_CLK	Transmitter A, Transmit Interface Clock	U7	Input	HSTL
RECV_A_0	Receiver A, Data bit 0	P2	Output	HSTL
RECV_A_1	Receiver A, Data bit 1	P3	Output	HSTL
RECV_A_2	Receiver A, Data bit 2	R1	Output	HSTL
RECV_A_3	Receiver A, Data bit 3	R3	Output	HSTL
RECV_A_4	Receiver A, Data bit 4	M4	Output	HSTL
RECV_A_5	Receiver A, Data bit 5	N4	Output	HSTL
RECV_A_6	Receiver A, Data bit 6	T1	Output	HSTL
RECV_A_7	Receiver A, Data bit 7	T2	Output	HSTL
RECV_A_K	Receiver A, Special Character (Data bit 8 for TBI mode)	T3	Output	HSTL
RECV_A_9	Receiver A, Data bit 9 for TBI mode	P4	Output	HSTL
RECV_A_IDLE	Receiver A, Idle Detect	U2	Output	HSTL
RECV_A_ERR	Receiver A, Error Detect	V2	Output	HSTL
RECV_A_CLK	Receiver A, Receive Data Clock	P5	Output	HSTL
XCVR_A_RSEL	Transceiver A, Redundant Link Select	P11	Input	CMOS
XCVR_A_DISABLE	Transceiver A, Disable	D13	Input	CMOS
RLINK_A0_P	Receiver A, Primary Positive Link Input	U18	Input	Link
RLINK_A0_N	Receiver A, Primary Negative Link Input	V18	Input	Link
RLINK_A1_P	Receiver A, Redundant Positive Link Input	U16	Input	Link
RLINK_A1_N	Receiver A, Redundant Negative Link Input	V16	Input	Link
XLINK_A0_P	Transmitter A, Primary Positive Link Out	R17	Output	Link
XLINK_A0_N	Transmitter A, Primary Negative Link Out	T17	Output	Link
XLINK_A1_P	Transmitter A, Redundant Positive Link Out	R15	Output	Link
XLINK_A1_N	Transmitter A, Redundant Negative Link Out	T15	Output	Link
XMIT_B_0	Transmitter B, Data bit 0	R6	Input	HSTL
XMIT_B_1	Transmitter B, Data bit 1	V5	Input	HSTL
XMIT_B_2	Transmitter B, Data bit 2	U5	Input	HSTL
XMIT_B_3	Transmitter B, Data bit 3	T5	Input	HSTL
XMIT_B_4	Transmitter B, Data bit 4	U4	Input	HSTL
XMIT_B_5	Transmitter B, Data bit 5	R5	Input	HSTL
XMIT_B_6	Transmitter B, Data bit 6	T4	Input	HSTL
XMIT_B_7	Transmitter B, Data bit 7	R4	Input	HSTL

Table 7-2. 324 MAPBGA Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
XMIT_B_K	Transmitter B, Special Character (Data bit 8 for TBI mode)	V3	Input	HSTL
$\overline{\text{XMIT\_B\_IDLE}}$	Transmitter B, Idle Enable Bar, (Data bit 9 for TBI mode)	U3	Input	HSTL
XMIT_B_CLK	Transmitter B, Transmit Interface Clock	V4	Input	HSTL
RECV_B_0	Receiver B, Data bit 0	P1	Output	HSTL
RECV_B_1	Receiver B, Data bit 1	L4	Output	HSTL
RECV_B_2	Receiver B, Data bit 2	N3	Output	HSTL
RECV_B_3	Receiver B, Data bit 3	N1	Output	HSTL
RECV_B_4	Receiver B, Data bit 4	M3	Output	HSTL
RECV_B_5	Receiver B, Data bit 5	M2	Output	HSTL
RECV_B_6	Receiver B, Data bit 6	M1	Output	HSTL
RECV_B_7	Receiver B, Data bit 7	L3	Output	HSTL
RECV_B_K	Receiver B, Special Character (Data bit 8 for TBI mode)	L2	Output	HSTL
RECV_B_9	Receiver B, Data bit 9 for TBI mode	K2	Output	HSTL
RECV_B_IDLE	Receiver B, Idle Detect	K4	Output	HSTL
RECV_B_ERR	Receiver B, Error Detect	J1	Output	HSTL
RECV_B_CLK	Receiver B, Receive Data Clock	K3	Output	HSTL
XCVR_B_RSEL	Transceiver B, Redundant Link Select	U13	Input	CMOS
XCVR_B_DISABLE	Transceiver B, Disable	C14	Input	CMOS
RLINK_B0_P	Receiver B, Primary Positive Link Input	L17	Input	Link
RLINK_B0_N	Receiver B, Primary Negative Link Input	M17	Input	Link
RLINK_B1_P	Receiver B, Redundant Positive Link Input	L15	Input	Link
RLINK_B1_N	Receiver B, Redundant Negative Link Input	M15	Input	Link
XLINK_B0_P	Transmitter B, Primary Positive Link Out	N18	Output	Link
XLINK_B0_N	Transmitter B, Primary Negative Link Out	P18	Output	Link
XLINK_B1_P	Transmitter B, Redundant Positive Link Out	N16	Output	Link
XLINK_B1_N	Transmitter B, Redundant Negative Link Out	P16	Output	Link
XMIT_C_0	Transmitter C, Data bit 0	D9	Input	HSTL
XMIT_C_1	Transmitter C, Data bit 1	E8	Input	HSTL
XMIT_C_2	Transmitter C, Data bit 2	B6	Input	HSTL
XMIT_C_3	Transmitter C, Data bit 3	C7	Input	HSTL
XMIT_C_4	Transmitter C, Data bit 4	D7	Input	HSTL

Table 7-2. 324 MAPBGA Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
XMIT_C_5	Transmitter C, Data bit 5	B5	Input	HSTL
XMIT_C_6	Transmitter C, Data bit 6	A4	Input	HSTL
XMIT_C_7	Transmitter C, Data bit 7	C5	Input	HSTL
XMIT_C_K	Transmitter C, Special Character (Data bit 8 for TBI mode)	D6	Input	HSTL
$\overline{\text{XMIT\_C\_IDLE}}$	Transmitter C, Idle Enable Bar, (Data bit 9 for TBI mode)	C6	Input	HSTL
XMIT_C_CLK	Transmitter C, Transmit Interface Clock	D8	Input	HSTL
RECV_C_0	Receiver C, Data bit 0	E1	Output	HSTL
RECV_C_1	Receiver C, Data bit 1	G4	Output	HSTL
RECV_C_2	Receiver C, Data bit 2	F3	Output	HSTL
RECV_C_3	Receiver C, Data bit 3	F2	Output	HSTL
RECV_C_4	Receiver C, Data bit 4	F1	Output	HSTL
RECV_C_5	Receiver C, Data bit 5	H4	Output	HSTL
RECV_C_6	Receiver C, Data bit 6	G2	Output	HSTL
RECV_C_7	Receiver C, Data bit 7	G1	Output	HSTL
RECV_C_K	Receiver C, Special Character (Data bit 8 for TBI mode)	J4	Output	HSTL
RECV_C_9	Receiver C, Data bit 9 for TBI mode	H3	Output	HSTL
RECV_C_IDLE	Receiver C, Idle Detect	H1	Output	HSTL
RECV_C_ERR	Receiver C, Error Detect	J2	Output	HSTL
RECV_C_CLK	Receiver C, Receive Data Clock	H2	Output	HSTL
XCVR_C_RSEL	Transceiver C, Redundant Link Select	T13	Input	CMOS
XCVR_C_DISABLE	Transceiver C, Disable	B14	Input	CMOS
RLINK_C0_P	Receiver C, Primary Positive Link Input	H17	Input	Link
RLINK_C0_N	Receiver C, Primary Negative Link Input	G17	Input	Link
RLINK_C1_P	Receiver C, Redundant Positive Link Input	H15	Input	Link
RLINK_C1_N	Receiver C, Redundant Negative Link Input	G15	Input	Link
XLINK_C0_P	Transmitter C, Primary Positive Link Out	F18	Output	Link
XLINK_C0_N	Transmitter C, Primary Negative Link Out	E18	Output	Link
XLINK_C1_P	Transmitter C, Redundant Positive Link Out	F16	Output	Link
XLINK_C1_N	Transmitter C, Redundant Negative Link Out	E16	Output	Link
XMIT_D_0	Transmitter D, Data bit 0	B7	Input	HSTL
XMIT_D_1	Transmitter D, Data bit 1	C8	Input	HSTL

Table 7-2. 324 MAPBGA Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
XMIT_D_2	Transmitter D, Data bit 2	A7	Input	HSTL
XMIT_D_3	Transmitter D, Data bit 3	B8	Input	HSTL
XMIT_D_4	Transmitter D, Data bit 4	C9	Input	HSTL
XMIT_D_5	Transmitter D, Data bit 5	E9	Input	HSTL
XMIT_D_6	Transmitter D, Data bit 6	A8	Input	HSTL
XMIT_D_7	Transmitter D, Data bit 7	B9	Input	HSTL
XMIT_D_K	Transmitter D, Special Character (Data bit 8 for TBI mode)	A9	Input	HSTL
$\overline{\text{XMIT\_D\_IDLE}}$	Transmitter D, Idle Enable Bar, (Data bit 9 for TBI mode)	C10	Input	HSTL
XMIT_D_CLK	Transmitter D, Transmit Interface Clock	B10	Input	HSTL
RECV_D_0	Receiver D, Data bit 0	E2	Output	HSTL
RECV_D_1	Receiver D, Data bit 1	E3	Output	HSTL
RECV_D_2	Receiver D, Data bit 2	D1	Output	HSTL
RECV_D_3	Receiver D, Data bit 3	D2	Output	HSTL
RECV_D_4	Receiver D, Data bit 4	D3	Output	HSTL
RECV_D_5	Receiver D, Data bit 5	C2	Output	HSTL
RECV_D_6	Receiver D, Data bit 6	B2	Output	HSTL
RECV_D_7	Receiver D, Data bit 7	A1	Output	HSTL
RECV_D_K	Receiver D, Special Character (Data bit 8 for TBI mode)	D5	Output	HSTL
RECV_D_9	Receiver D, Data bit 9 for TBI mode	C3	Output	HSTL
RECV_D_IDLE	Receiver D, Idle Detect	A2	Output	HSTL
RECV_D_ERR	Receiver D, Error Detect	A3	Output	HSTL
RECV_D_CLK	Receiver D, Receive Data Clock	D4	Output	HSTL
XCVR_D_RSEL	Transceiver D, Redundant Link Select	P12	Input	CMOS
XCVR_D_DISABLE	Transceiver D, Disable	A14	Input	CMOS
RLINK_D0_P	Receiver D, Primary Positive Link Input	B18	Input	Link
RLINK_D0_N	Receiver D, Primary Negative Link Input	A18	Input	Link
RLINK_D1_P	Receiver D, Redundant Positive Link Input	B16	Input	Link
RLINK_D1_N	Receiver D, Redundant Negative Link Input	A16	Input	Link
XLINK_D0_P	Transmitter D, Primary Positive Link Out	D17	Output	Link
XLINK_D0_N	Transmitter D, Primary Negative Link Out	C17	Output	Link
XLINK_D1_P	Transmitter D, Redundant Positive Link Out	D15	Output	Link

Table 7-2. 324 MAPBGA Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
XLINK_D1_N	Transmitter D, Redundant Negative Link Out	C15	Output	Link
DROP_SYNC	Drop Synchronization	V8	Input	HSTL
XMIT_REF_A	Transmitter Reference Clock A Select	U12	Input	CMOS
RECV_REF_A	Receiver Reference Clock A Select	T12	Input	CMOS
XMIT_EQ_EN	Transmitter Equalization Enable	U14	Input	CMOS
RECV_EQ_EN	Receiver Equalization Enable	R12	Input	CMOS
XMIT_EN_ALL	Transmitter Enable, All Outputs	C12	Input	CMOS
TBIE	Ten-Bit Interface Enable	V10	Input	CMOS
HSE	Half Speed Enable	C13	Input	CMOS
DDRE	Double Data Rate Enable	B13	Input	CMOS
BSYNC	Byte Synchronization Mode	R10	Input	CMOS
ADIE	Add/Drop Idle Enable	E10	Input	CMOS
REPE	Repeater Mode Enable	C11	Input	CMOS
LME	Link Multiplexer Mode Enable	D12	Input	CMOS
RCCE	Recovered Clock Enable	D11	Input	CMOS
REF_CLK_P	Reference Clock Positive	A13	Input	HSTL
REF_CLK_N	Reference Clock Negative	A12	Input	HSTL
$\overline{\text{RESET}}$	System Reset Bar	T10	Input	CMOS
WSE	Word Synchronization Enable	D10	Input	CMOS
WSO	Word Synchronization Bus Output	C4	Output	HSTL
WSI	Word Synchronization Bus Input	B4	Input	HSTL
TX_PLL_TPA	PLL Analog Test Point	K15	Output	Analog
TST_0	Test Mode Select 0	T9	Input	CMOS
TST_1	Test Mode Select 1	U9	Input	CMOS
SCAN_EN	Test Mode, Scan Shift Enable	U10	Input	CMOS
LBE	Loop Back Enable	B12	Input	CMOS
LBOE	Loop Back Output Enable	B11	Input	CMOS
BIST_MODE_SEL	BIST Mode Equation Select	R9	Input	CMOS
TDO	JTAG Test Data Out	R11	Output	HSTL
TMS	JTAG Test Mode Select	V11	Input	CMOS
TDI	JTAG Test Data In	U11	Input	CMOS
$\overline{\text{TRST}}$	JTAG Test Reset Bar	T11	Input	CMOS
TCK	JTAG Test Clock	V12	Input	CMOS

Table 7-2. 324 MAPBGA Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (324 MAPBGA)	Direction	I/O Type
Z_CALIB	Impedance Calibration Reference	H18	Z_{REF}	Analog
HSTL_VREF	HSTL Voltage Reference	K5	V_{REF}	Analog
$COREV_{DD}$	Core logic supply	A5, A10, B15, D14, D18, E4, E5, E6, E7, E11, E12, E13, E14, F4, F5, F6, F7, F8, F9, F10, F11, F12, F14, G14, G18, H5, H14, H16, J5, J14, J17, K14, L5, L14, M5, M14, M16, M18, N5, N6, N7, N8, N9, N10, N11, N12, N14, P6, P7, P10, P13, P14, R14, V6, V13, V15, V17	V_{DD}	Supply
COREGND/PADGND	Core logic ground / HSTL I/O ground	A6, A11, A15, A17, B1, F13, G6, G7, G8, G9, G10, G11, G12, G13, G16, H6, H7, H8, H9, H10, H11, H12, H13, J6, J7, J8, J9, J10, J11, J12, J13, J15, K1, K6, K7, K8, K9, K10, K11, K12, K13, K17, L6, L7, L8, L9, L10, L11, L12, L13, L16, L18, M6, M7, M8, M9, M10, M11, M12, M13, N13, R13, T14, U1, U15, U17, V7, V14	GND	Ground
TX_PLLV_{DD}	PLL analog supply	K18	AV_{DD}	Supply
TX_PLLGND	PLL analog ground	J18	GND	Ground
$PADV_{DD}$	HSTL I/O supply	B3, C1, G3, G5, J3, L1, N2, R2, V1	$V_{DD}Q$	Supply
$XPADV_{DD}$	Link I/O supply	C16, C18, F15, F17, J16, N17, P15, R18, T16	XV_{DD}	Supply
XPADGND	Link I/O ground	B17, D16, E15, E17, K16, P17, N15, R16, T18	GND	Ground

Appendix A
Ordering Information

Figure A-1 provides the Motorola part numbering nomenclature for the MC92610. For product availability, contact your local Motorola Semiconductor sales representative.

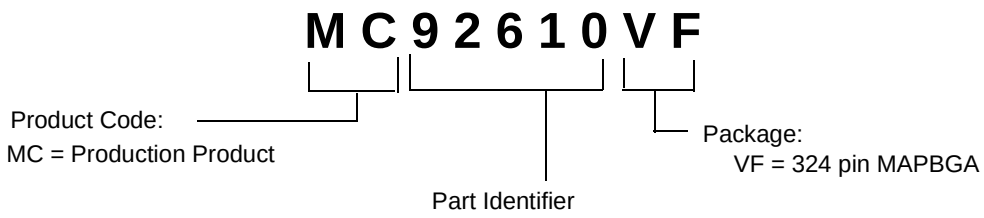


Figure A-1. Motorola Part Number Key

Appendix B
8B/10B Coding Scheme

The MC92610 provides fibre channel-specific 8B/10B encoding and decoding based on the FC-1 fibre channel standard. Given 8 bits entering a channel, the 8B/10B encoding converts them to 10 bits thereby increasing the transition density of the serially transmitted signal.

B.1 Overview

The FC-1 standard applies an algorithm that ensures that no more than five 1's or 0's are transmitted consecutively, giving a transition density equal to 2.5 for each 10 bit data block. Such a density ensures proper DC balance across the link and is sufficient for good clock recovery.

In the 8B/10B notation scheme, bytes are referred to as transmission characters, and each bit is represented by letters. Unencoded bits, the 8 bits that have not passed through a 8B/10B encoder, are represented by letters "A" through "H," which are bits 0 through7.

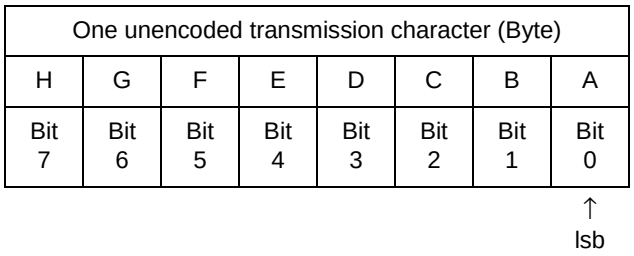


Figure B-1. Unencoded Transmission Character Bit Ordering

Encoded bits, those that have passed through an encoder, are represented with the letters "a" through "j," representing bits 0–9 respectively. Character (bit) ordering in the fibre channel nomenclature is little-endian, with "a" being the least significant bit in a byte.

One coded transmission character (Byte)									
j	h	g	f	i	e	d	c	b	a
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

↑
lsb

Figure B-2. Encoded Transmission Character Bit Ordering

B.1.1 Naming Transmission Characters

Transmission characters are given names based on the type of data in the byte and the bit values of the character. Two types of transmission characters are specified: data and special. Data characters are labeled “D” characters and special characters are labeled “K” characters. Each transmission character has a bit value and a corresponding decimal value. These elements are combined to provide each character with a name, see Table B-1.

Table B-1. Components of a Character Name

H G F	E D C B A	8B/10B notation
0 0 1	1 1 1 0 0	Data bit value
1	28	Decimal value of the bit value
D or K		Kind of transmission character
K28.1 = Data name assigned to this special character		

B.1.2 Encoding

Following is a simplified sequence of steps in 8B/10B coding:

1. An 8-bit block of unencoded data (a transmission character) is picked up by a transmitter.
2. The transmission character is broken into sub-blocks of three bits and five bits. The letters H G and F comprise the 3-bit block, and the letters E D C B and A comprise the 5-bit block.
3. The 3-bit and 5-bit sub-blocks pass through a 3B/4B encoder and a 5B/6B encoder, respectively. A bit is added to each sub-block, such that the transmission character is encoded and expanded to a total of 10-bits.
4. At the time the character is expanded into 10 bits, it is also encoded into the proper running disparity, either positive (RD+) or negative (RD-) depending on certain calculations (see Section B.1.3, “Calculating Running Disparity”). At start-up, the transmitter assumes negative running disparity.

5. The positive or negative disparity transmission character (see Figure B-3) is passed to the transmit driver, available for differentialization (See Section 2.3.1.7, “Transmit Driver Operation”).

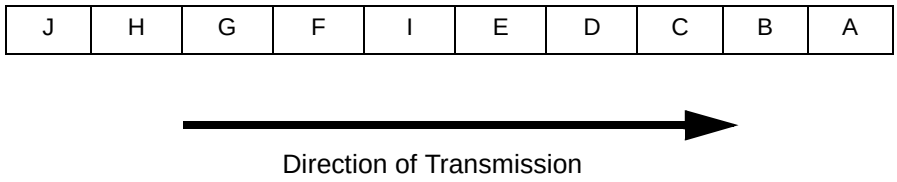


Figure B-3. Character Transmission

B.1.3 Calculating Running Disparity

Running disparity improves error detection and recovery. The rules for calculating the running disparity for sub-blocks are as follows (reference *Fibre Channel, Gigabit Communications and I/O for Computer Networks*):

- Running disparity at the end of any sub-block is positive if (1) the encoded sub-block contains more 1s than 0s, (2) if the 6-bit sub-block is 6’b00 0111, or (3) if the 4-bit sub-block is 4’b0011.
- Running disparity at the end of any sub-block is negative if (1) the encoded sub-block contains more 0 than 1 bits, (2) if the 6-bit sub-block is 6’b11 1000, or (3) if the 4-bit sub-block is 4’b1100.
- Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

B.2 Data Tables

Table B-2 displays the full valid data character 8B/10B codes. The values in the “Data Value HGFEDCBA” column are the possible bit values of the unencoded transmission characters. The current RD values are the possible positive and negative running disparity values.

Table B-2. Valid Data Characters

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	010101 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table B-3 displays the full valid special character 8B/10B codes.

Table B-3. Valid Special Characters

Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdie fghj
K28.0	000 11100	001111 0100	110000 1011	K28.6	110 11100	001111 0110	110000 1001
K28.1	001 11100	001111 1001	110000 0110	K28.7	111 11100	001111 1000	110000 0111
K28.2	010 11100	001111 0101	110000 1010	K23.7	111 10111	111010 1000	000101 0111
K28.3	011 11100	001111 0011	110000 1100	K27.7	111 11011	110110 1000	001001 0111
K28.4	100 11100	001111 0010	110000 1101	K29.7	111 11101	101110 1000	010001 0111
K28.5	101 11100	001111 1010	110000 0101	K30.7	111 11110	011110 1000	100001 0111

Glossary of Terms and Abbreviations

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this book. Some of the terms and definitions included in the glossary are reprinted from IEEE Std 754-1985, *IEEE Standard for Binary Floating-Point Arithmetic*, copyright ©1985 by the Institute of Electrical and Electronics Engineers, Inc., with the permission of the IEEE.

A

Asserted. Indicates active state of signal has been set. Refers to either inputs or outputs.

B

BERC. Bit Error Rate Checking.

BERT. Bit Error Rate Testing.

BIST. Built-In Self-Test.

Bit alignment. Refers to the transition tracking loop recovering data bits from the serial input stream.

Byte. Eight bits of uncoded data.

Byte alignment. Receiver identification of character boundaries through use of Idle character recognition.

C

Character. An 8B/10B encoded byte of data.

G

Gigabit. A unit of speed of data transfer. One gigabit indicates a data throughput of 1 billion bits per second requiring a transfer rate of 1.25 billion symbols per second of 8B/10B encoded data.

Gigabaud. A unit of speed of symbol transfer. One gigabaud indicates a data throughput of 800 million bits per second requiring a transfer rate of 1.0 billion symbols per second of 8B/10B encoded data.

I

ISI. Inter Symbol Interference, a distortion caused by the high-frequency loss characteristics of the transmission media.

N

Negated. Indicates inactive state of signal has been set. Refers to either inputs or outputs.

P

PLL. Phase Locked Loop.

PPM. parts per million.

R

Running disparity. The amount of DC imbalance over a history of symbols transmitted over a link. Equal to the difference between the number of one and zero symbols transmitted.

S

Symbol. One piece of information sent across the link; different from a bit in that bit implies data where symbol is encoded data.

W

Word synchronization. Alignment of four or more receivers' data by adjusting for differences in media and systemic delay between them such that data is presented by the receivers in the same grouping as they were transmit.

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W