AN1436
APPLICATION NOTE

Changing from the ST95010/ST95020 to the M95010/M95020 In Your Application Using a Simple Recognition Method

Customers who upgrade from the ST95010, or ST95020, to the M95010, or M95020, in their production could be interested in the algorithm described in this document. It is a simple way for the application automatically to identify the memory parts mounted on board.

INSTRUCTION CODE FORMAT

There are only two differences between the ST95010 and the M95010, and between the ST95020 and the M95020:

- Performance (the M95 offers a significant performance improvement over the ST95 family)
- Instruction format

ST95010 and ST95020 instructions have the following format (where I2, I1, and I0 are instruction bits, as documented in the data sheet):

```
0 0 0 0 0 I2 I1 I0
```

while M95010 and M95020 instructions have the following format (where I2, I1, and I0 are instruction bits, as documented in the data sheet, and X represents a Don't Care bit):

```
0 0 0 0 X I2 I1 I0
```

SOFTWARE RECOGNITION ALGORITHM

This difference can be used by the application software to differentiate between the two types of memory device (between the ST95010 and the M95010, and between the ST95020 and the M95020). Table 1 compares the instruction formats of these devices.

Table 1. Differences between the Instruction Formats

Instruction	Description	Instruction Format	
		ST95010 ST95020	**M95010 M95020**
WREN	Set Write Enable Latch	0000 0110	0000 X110
WRDI	Reset Write Enable Latch	0000 0100	0000 X100
RDSR	Read Status Register	0000 0101	0000 X101
WRSR	Write Status Register	0000 0001	0000 X001
READ	Read Data from Memory Area	0000 0011	0000 X011
WRITE	Write Data to Memory Array	0000 0010	0000 X010

As shown in Table 1, "0000 1101" is a valid Write Enable (WREN) instruction for the M95010 and M95020, but not for the ST95010 or ST95020.

The Write Enable Latch (WEL) bit, in the status register of the memory device, must be set to 1 before a Write Data Bytes (WRITE) is accepted by the memory. The Write Enable (WREN) instruction is used to set this bit.

The following algorithm is short and easy to insert in the MCU code. It is also safe to use, inasmuch that it does not attempt to write to any non-volatile bits. This algorithm only activates the internal logic of the memory device, and is therefore fast to execute, and does not have any significant impact on the performance of the application.

After Power-up, the following algorithm is executed:

– The Bus Master sends a Write Enable (WREN) instruction (0000 1110) to the memory
– The Bus Master sends a Read Status Register (RDSR) instruction (0000 0101) to the memory, and stores the value of the Write Enable Latch (WEL) bit in a variable called *WEL1*
– The Bus Master sends a modified Write Disable (WRDI) instruction (0000 1100) to the memory
– The Bus Master sends a Read Status Register (RDSR) instruction (0000 0101) to the memory, and stores the value of the Write Enable Latch (WEL) bit in a variable called *WEL2*.
– If *(WEL1,WEL2*)=(1,0) Then the device is an M95010/20, Else the device is an ST95010/20
– The Bus Master sends a Write Disable (WRDI) instruction (0000 0100) to protect the application from data corruption

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

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Please remember to include your name, company, location, telephone number and fax number.