AN1536
APPLICATION NOTE

Designing Applications that Work with any M25Pxx Device Taking Advantage of their Hardware and Software Compatibility

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One of the great advantages of the M25Pxx Serial Flash memory devices from STMicroelectronics is that all members of the family have the same footprint – all the way from the lowest end of the family (512 Kbit memory) to the highest (16 Mbit memory).

As a result, the application designer can allow for any member of the family to be substituted on the circuit board. Thus one design can serve for a whole range of applications, from the lowest end of the range to the highest.

There are some functional differences, though, between the individual members of the family – most of them connected to the differences in memory capacity. This application note highlights these differences.

The Electronic Signature feature of the M25Pxx family (Table 1) allows the application software to identify which memory is connected on the board, and to adapt itself accordingly.

Table 1. Electronic Signature

Device	Electronic Signature
M25P05-A	05h
M25P10-A	10h
M25P20	11h
M25P40	12h
M25P80	13h
M25P16	14h

The number of bits in a sector can be 256K, for the M25P05-A and M25P10-A, or 512K, for the M25P20/40/80/16. The number of sectors varies according to the total memory capacity of the device (Table 2).

Table 2. Number of Sectors

Device	Number of Sectors	Bits per Sector
M25P05-A	2	256K
M25P10-A	4	256K
M25P20	4	512K
M25P40	8	512K
M25P80	16	512K
M25P16	32	512K

The number of Block Protect (BP) bits in the Status Register needs to vary, to allow for the different number of sectors in the various members of the family (Table 3 and Table 4).

Table 3. Protected Area Sizes (M25P05-A, M25P10-A, M25P20)

Status Register Content		Protected Area		
BP1 Bit	BP0 Bit	M25P05-A	M25P10-A	M25P20
0	0	none[1]	none[1]	none[1]
0	1	none (protected against Bulk Erase only)[1]	Upper quarter (256 Kbits)	Upper quarter (512 Kbits)
1	0		Upper half (512 Kbits)	Upper half (1 Mbits)
1	1	All	All	All

Note: 1. The device is ready to accept a Bulk Erase instruction if, and only if, both Block Protect (BP1, BP0) bits are 0.

Table 4. Protected Area Sizes (M25P40, M25P80, M25P16)

Status Register Content			Protected Area		
BP2 Bit	BP1 Bit	BP0 Bit	M25P40	M25P80	M25P16
0	0	0	none[1]	none[1]	none[1]
0	0	1	Upper eighth (512 Kbits)	Upper sixteenth (512 Kbits)	Upper 32nd (512 Kbits)
0	1	0	Upper quarter (1 Mbits)	Upper eighth (1 Mbits)	Upper sixteenth (1 Mbits)
0	1	1	Upper half (2 Mbits)	Upper quarter (2 Mbits)	Upper eighth (2 Mbits)
1	0	0	All	Upper half (4 Mbits)	Upper quarter (4 Mbits)
1	0	1	All	All	Upper half (8 Mbits)
1	1	0	All	All	All
1	1	1	All	All	All

Note: 1. The device is ready to accept a Bulk Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

Consistent with its use on standard SPI EEPROM, the protection is started from the end of the memory. This means that, even if a given combination of Block Protect (BP) bits protects the same block size at the end of the memory, the address of the protected area is not the same across the different memory capacities of the devices.

For example, (BP0, BP1, BP2) = (001) protects the upper 512 Kbits of the memory for the M25P40, M25P80 and M25P16, but not at the same address.

Each device contains all the hardware necessary to conduct the complex Erase and Program algorithms internally, without further reference to the Bus Master. The duration of these algorithms is dependent on the amount of memory being addressed, which, in the case of a bulk erase algorithm, means that it depends on the memory capacity of the device, as summarized in Table 5.

Table 5. Bulk Erase: Time to Erase the Whole Memory Area

Device	Bulk Erase	Duration of Erase Cycle
M25P05-A	512 Kbits	6 s (max)
M25P10-A	1 Mbits	6 s (max)
M25P20	2 Mbits	6 s (max)
M25P40	4 Mbits	10 s (max)
M25P80	8 Mbits	20 s (max)
M25P16	16 Mbits	40 s (max)

SPECIAL POINTS ABOUT THE M25P05-A

Two final points should be noted, concerning the behavior of the M25P05-A that is distinctive:

1. The unused address bits (A23 to A16) are *not* Don't Care. They must each be set to 0
2. There is no roll-over at the end of the M25P05-A memory during a Read operation

CONCLUSION

When designing an application to use an M25Pxx Serial Flash memory device, the application designer can allow for any member of the family to be substituted on the circuit board, because their footprints and pin-outs are the same. Thus one design can serve for a whole range of applications, from the lowest end of the range to the highest, provided that the few functional differences, noted in this document, are considered, and allowed for. To make this possible, the application software merely needs to act on the information contained in the Electronic Signature of the M25Pxx device.

For current information on ST Flash Memory products, please consult our pages on the world wide web:
www.st.com/serialflash

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.serial-flash@st.com (for application support)
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Please remember to include your name, company, location, telephone number and fax number.