PIP212-12M

DC-to-DC converter powertrain

Rev. 02 — 2 March 2005 Preliminary data sheet

1. General description

The PIP212M-12M is a fully optimized powertrain for high current high frequency synchronous buck DC-to-DC applications. The PIP212M-12M replaces two power MOSFETs, a Schottky diode and a driver IC, resulting in a significant increase in power density. The integrated solution allows for optimization of individual components and greatly reduces the parasitics associated with conventional discrete solutions, resulting in higher system efficiencies at higher frequency operation.

2. Features

- Input conversion range from 3.3 V to 16 V
- Output voltages from 0.8 V to 6 V
- Capable of up to 30 A maximum output current
- Operating frequency up to 1 MHz
- Peak system efficiency > 90 % at 500 kHz
- Automatic Dead-time Reduction (ADR) for maximum efficiency
- Internal thermal shutdown
- Auxiliary 5 V output
- Power ready output flag
- Power sequencing functions
- Fault flag for lost phase detection
- Internal 6.5 V regulator for efficient gate drive
- Compatible with single and multi-phase PWM controllers
- Internal boost switch for high efficiency and low noise
- Low-profile, surface-mounted package (8 mm × 8 mm × 0.85 mm)

3. Applications

- High-current DC-to-DC point-of-load converters
- Small form-factor voltage regulator modules
- Microprocessor and memory voltage regulators
- Intel® compatible VRM (VRM9 and VRM10)
- Intel® Driver MOS (DrMOS) compatible

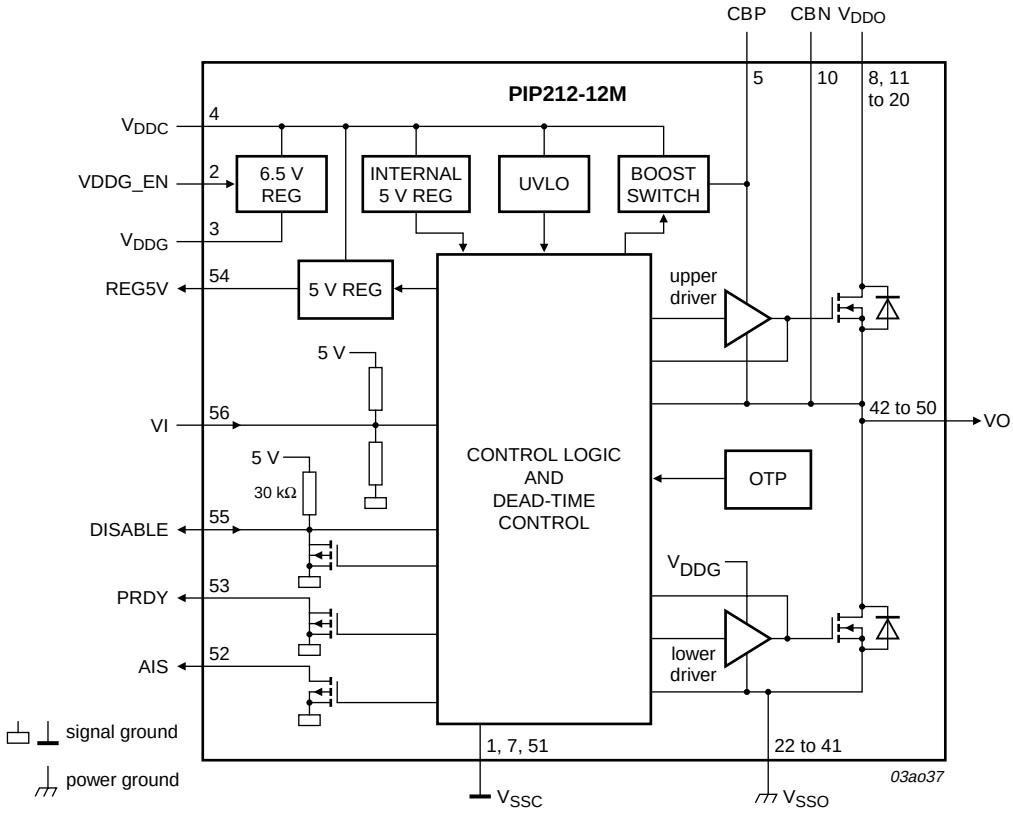
PHILIPS

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PIP212-12M	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-4

5. Block diagram



A bootstrap switch is integrated into the design of the PIP212-12M between V_{DDC} and CBN

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

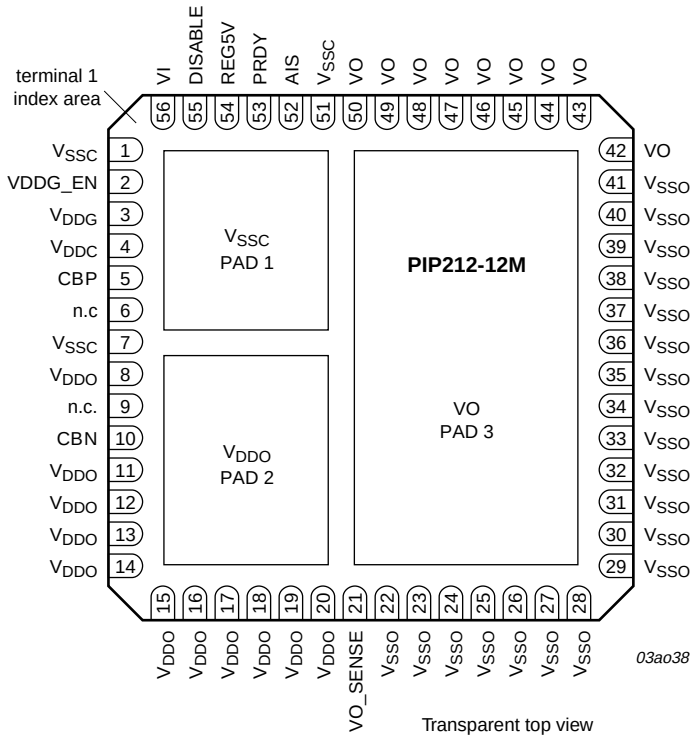


Fig 2. Pin configuration

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
V_{DDC}	4	-	control circuit supply voltage
V_{DDO}	8, 11 to 20, pad 2	I	output stage supply voltage
V_{SSC}	1, 7, 51, pad 1	-	control circuit ground
V_{SSO}	22 to 41	-	output stage (supply) ground
VI	56	I	pulse width modulated input
VO	42 to 50, pad 3	O	output voltage
VO_SENSE	21	O	sense connection to VO often required by PWM for current sensing
CBP	5	-	connection for bootstrap capacitor
CBN	10	-	connection for bootstrap capacitor
VDDG_EN	2	I	enables internal 6.5 V regulator for V_{DDG}
V_{DDG}	3	-	gate drive supply voltage
AIS	52	O	indicates the switching status of VO (open drain)
PRDY	53	O	indicates that V_{DDC} is above the UVLO level (open drain)

Table 2: Pin description *...continued*

Symbol	Pin	Type	Description
REG5V	54	O	5 V regulated supply output
DISABLE	55	I/O	disable driver function (active LOW)
n.c.	6, 9	-	not connected

7. Functional description

7.1 Basic operation

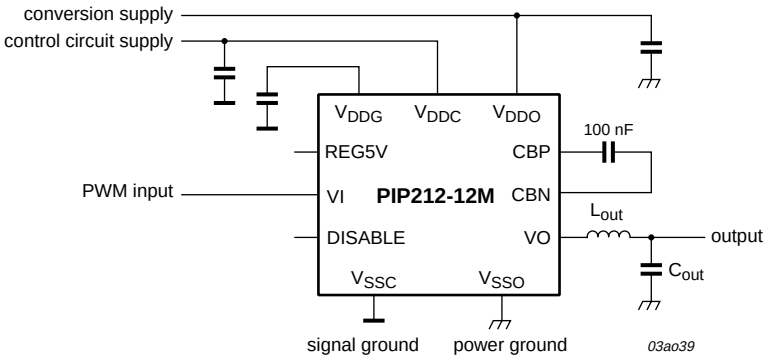


Fig 3. Simplified functional block diagram of a synchronous DC-to-DC converter output stage

The PIP212-12M combines two MOSFET transistors and a MOSFET driver in a thermally enhanced low inductance package for use in high frequency and high efficiency synchronous buck DC-to-DC converters; see Figure 3. The two MOSFETs are connected in a half bridge configuration between V_{DDO} and V_{SSO}. The mid point of the two transistors is VO which is connected to the output of a DC-to-DC converter via an inductor. A logic HIGH signal on the VI pin causes the lower MOSFET to be switched off and the upper MOSFET to be switched on. Current will then flow from the supply (V_{DDO}), through the upper MOSFET and the inductor (L_{out}) to the output.

A logic LOW signal on the VI pin causes the upper MOSFET to be turned off and the lower MOSFET to be switched on. Current then flows from the power ground (V_{SSO}), through the lower MOSFET and the inductor (L_{out}), to the output. The output voltage is determined by the ratio of time that the upper and lower MOSFETs conduct.

7.2 Undervoltage Lockout (UVLO)

The UVLO function ensures the correct operation of the control circuit during a power-up and power-down sequence. Power to the control circuit is provided by the V_{DDC} pin. This voltage is internally monitored to ensure that if V_{DDC} is below the UVLO threshold, the DISABLE pin is internally pulled LOW and both MOSFETs are off. This is indicated by the power ready (PRDY) flag, an open drain output that is pulled LOW whenever V_{DDC} is below the UVLO threshold.

7.3 Boost switch

The gate drive to the upper MOSFET is provided by a bootstrap capacitor (typically 100 nF) that is placed between the CBP and CBN pins. This capacitor is charged via an internal boost switch to a voltage within a few millivolts of V_{DDC} up to a maximum of 12 V (this is to prevent excessive gate charge losses when V_{DDC} > 12 V). The upper MOSFET will be switched according to PWM input once the boost capacitor voltage is above 4.3 V. When ever the voltage is below 2.7 V, the upper MOSFET will remain off.

7.4 V_{DDG} regulator

The gate drive to the lower MOSFET is provided by the V_{DDG} pin. A 1 µF capacitor should be connected between this pin and V_{SSC}. For minimum power loss within the PIP212-12M, an external power supply of between 5 V and 12 V should be connected to this pin. The optimum value for this voltage is dependent on the application but in the majority of cases a 5 V supply is recommended; see Figure 11. In cases where the V_{DDG} maximum voltage will not be exceeded, the V_{DDG} capacitor can be omitted by connecting the V_{DDG} and V_{DDC} pins; see Figure 13.

When V_{DDC} is connected to a supply greater than 9 V, an internal 6.5 V regulator connected to V_{DDG} can be used to provide the gate drive for the lower MOSFET; see Figure 12. The V_{DDG} regulator is enabled by leaving the VDDG_EN pin open resulting in this pin being pulled internally to 5 V. If an external supply is to be connected to V_{DDG} then the VDDG_EN pin must be connected to V_{SSC} to disable the internal V_{DDG} regulator.

Table 3: V_{DDG} biasing

VDDG_EN	V_{DDG}
Open circuit	internal 6.5 V regulator used (V_{DDC} > 9 V)
V_{SSC}	connection to external supply required

7.5 3-state function

If the input to VI from the PWM controller becomes high impedance, then the VI input is driven to 2.5 V by an internal voltage divider. A voltage on the VI pin that is in-between the V_{IH} and V_{IL} levels and present for longer than $t_{d(3\text{-state})}$, causes both MOSFETs to be turned off. Normal operation commences once the VI input is outside this window for longer than $t_{d(3\text{-state})}$.

7.6 Automatic Dead-time Reduction (ADR)

Protection against cross-conduction (shoot-through) is achieved via the insertion of a delay (or dead-time) between the switching off of one MOSFET and the switching on of the other MOSFET. The automatic dead-time reduction feature continuously monitors the body diode of the lower MOSFET adjusting the dead-time to minimize body diode conduction. This reduces power loss in both the upper and lower MOSFETs due to the reduction in body diode conduction and reverse recovery charge. The lower power dissipation leads to higher system efficiency and enables higher frequency operation.

7.7 Over Temperature Protection (OTP)

Protection against over temperature is provided by an internal thermal shutdown incorporated into the control circuit. When the control circuit die temperature exceeds the upper thermal trip level, both MOSFETs are switched off and the internal V_{DDG} regulator disabled. This state continues until the die temperature falls below the lower trip temperature. This function is only operational when V_{DDC} is above the UVLO level.

7.8 Am I Switching (AIS)

The AIS flag is designed for use with lost phase detection circuitry. During normal operation (i.e. when PRDY and DISABLE are HIGH and VI is either HIGH or LOW), the AIS pin is pulled LOW if no voltage transients have been detected on the V_O pin for a period of approximately 40 µs. If DISABLE is LOW or the driver is in 3-state mode, the AIS pin will become floating (open drain) irrespective of any previous state. False signals during start-up are prevented by activating this function approximately 200 µs after either the DISABLE pin becoming HIGH or the driver leaving the 3-state mode.

7.9 Disable

This is the disable or enable function of the driver. Pulling the DISABLE pin LOW switches off both MOSFETs, disables the REG5V output, and makes the AIS flag open drain. This pin is internally pulled LOW whilst V_{DDC} remains below the UVLO threshold. Once V_{DDC} exceeds the UVLO threshold, this pin is pulled HIGH by an internal resistor. In this way the driver will enable itself unless there is an external pull down. In multiphase applications, connecting the DISABLE pins of multiple PIP212-12M devices together will ensure that all devices will only become enabled when the voltage on the V_{DDC} pins of all of the devices has exceeded the UVLO threshold; see Figure 10.

7.10 Reg5V

This function provides a low current regulated 5 V output voltage suitable for providing power to a PWM controller. It is operational when both PRDY and DISABLE are HIGH. Operation as a 5 V power supply is only guaranteed when V_{DDC} is > 7 V. This pin can also be used as part of an enable function for a PWM controller; this ensures that the PWM is enabled only when the PIP212-12M is fully operational (i.e. both PRDY and DISABLE are HIGH).

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDC}	control circuit supply voltage			–0.5	+15	V
V_{DDO}	output stage supply voltage			–0.5	+24	V
V_I	input voltage			–0.5	+12.6	V
V_{DDG}	gate drive supply voltage			–0.5	+12.6	V
V_O	output voltage			–0.5	V_{DDO} + 0.5	V
V_{CB}	bootstrap capacitor voltage			–0.5	V_O + 15	V
$I_{O(AV)}$	average output current	V_{DDC} = 12 V; $T_{pcb} \leq 90$ °C; f_i = 1 MHz		-	30	A
I_{ORM}	repetitive peak output current	V_{DDC} = 12 V; $t_p \leq 10$ µs	[1]	-	60	A
V_{PRDY}	power ready voltage at pin PRDY			–0.5	+12.6	V
$V_{DISABLE}$	driver enable voltage at pin DISABLE			–0.5	+12.6	V
V_{REG5V}	5 V regulated supply output voltage at pin REG5V			–0.5	+12.6	V
V_{AIS}	output voltage at pin AIS			–0.5	+12.6	V
P_{tot}	total power dissipation	T_{pcb} = 25 °C	[2]	-	25	W
		T_{pcb} = 90 °C	[2]	-	12	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C

[1] Pulse width and repetition rate limited by maximum value of T_j.

[2] Assumes a thermal resistance from junction to printed-circuit board of 5 K/W.

9. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	device tested with upper and lower MOSFETs in series	-	3	5	K/W

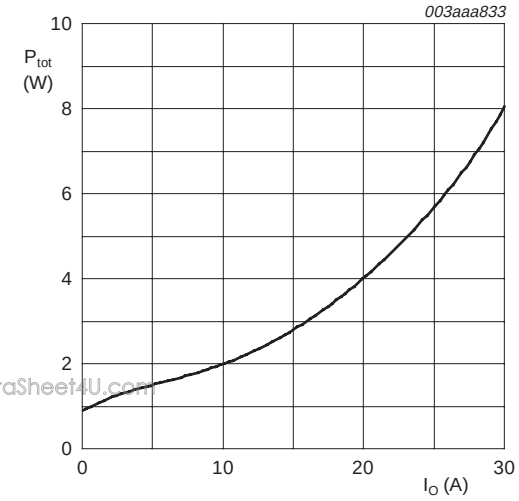
10. Characteristics

Table 6: Characteristics

V_{DDC} = 12 V; T_j = 25 °C unless otherwise specified.

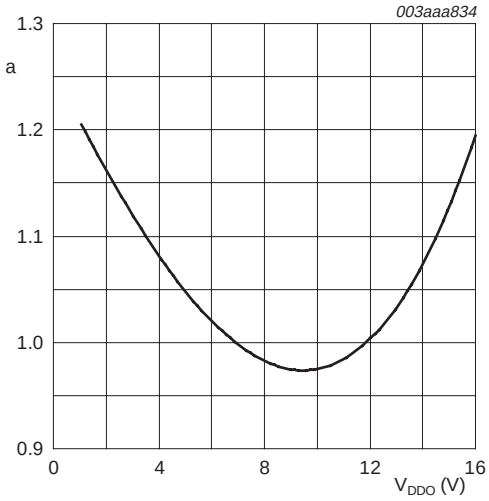
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V_{DDC}	control circuit supply voltage	25 °C ≤ T_j ≤ 150 °C		6	12	14	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage	turn on		4.1	4.2	4.4	V
		turn off		3.75	3.9	4.0	V
V_{IH}	HIGH-level input voltage		[1]	3.3	3.5	3.7	V
V_{IL}	LOW-level input voltage		[1]	1.4	1.5	1.6	V
I_{LI}	input leakage current	0 V ≤ V_I ≤ 5 V		-	170		µA
I_{DDC}	control circuit supply current	f_i = 0 Hz, V_I = 0 V		-	8.2	-	mA
		f_i = 500 kHz, VDDG_EN = open		-	50	-	mA
		f_i = 500 kHz, VDDG_EN = ground		-	12	-	mA
V_{DDG}	gate driver supply voltage	I_L = 65 mA		6	6.5	7	V
V_{REG5V}	5 V regulated supply output voltage at pin REG5V	I_L = 10 mA		4.5	5.0	5.5	V
I_{REG5V}	5 V regulated supply output current from pin REG5V	V_{REG5V} = 4.5 V		-	24.0	-	mA
$V_{th(en)}$	enable threshold voltage at pin DISABLE	V_{DDC} > 4.5 V		-	3.1	-	V
$V_{th(dis)}$	disable threshold voltage at pin DISABLE	V_{DDC} > 4.5 V		-	1.6	-	V
T_{otp}	over temperature trip point			165	-	180	°C
$T_{otp(hys)}$	over temperature trip hysteresis			-	15	-	°C
P_{tot}	total power dissipation	V_{DDO} = 12 V; $I_{O(AV)}$ = 25 A; V_O = 1.3 V; T_{pcb} = 90 °C;					
		f_i = 500 kHz		-	4.5	-	W
		f_i = 1 MHz		-	5.8	-	W
Dynamic characteristics							
$t_{d(on)(IH-OH)}$	turn-on delay time input HIGH to output HIGH	V_{DDO} = 12 V; $I_{O(AV)}$ = 12.5 A		-	-	85	ns
$t_{d(off)(IL-OL)}$	turn-off delay time input LOW to output LOW			-	-	45	ns
$t_{d(3-state)}$	3-state delay time			-	100	-	ns

[1] If the input voltage remains between V_{IH} and V_{IL} (2.5 V typ) for longer than $t_{d(3-state)}$, then both MOSFETs are turned off.



V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.3 V; f_i = 1 MHz

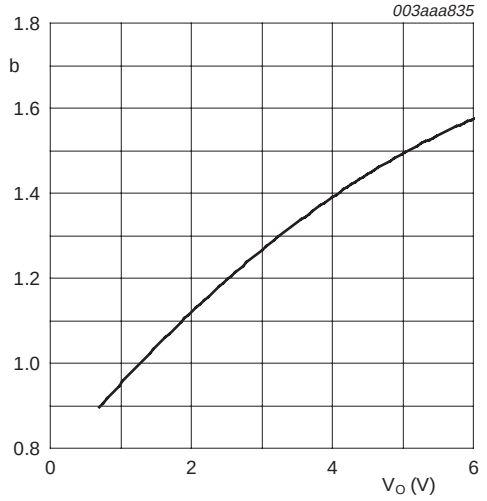
Fig 4. Total power dissipation as a function of average output current; typical values



V_{DDC} = 12 V; V_O = 1.3 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

$$a = \frac{P_{tot}}{P_{tot(V_{DDO} = 12\ V)}}$$

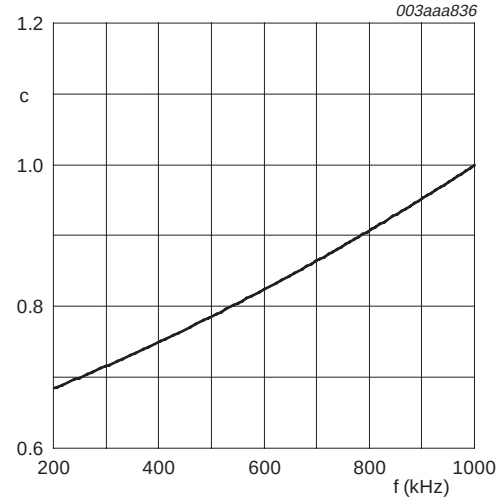
Fig 5. Normalized power dissipation as a function of output stage supply voltage; typical values



V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

$$b = \frac{P_{tot}}{P_{tot(V_O = 1.3\ V)}}$$

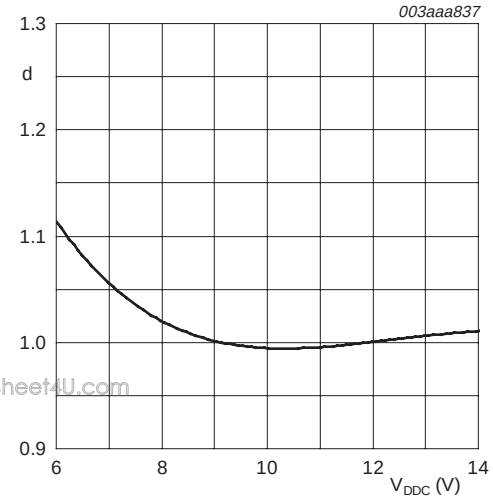
Fig 6. Normalized power dissipation as a function of output voltage; typical values



V_{DDC} = 12 V; V_{DDO} = 1.3 V; V_O = 1.3 V; $I_{O(AV)}$ = 25 A

$$c = \frac{P_{tot}}{P_{tot(f_i = 1\ MHz)}}$$

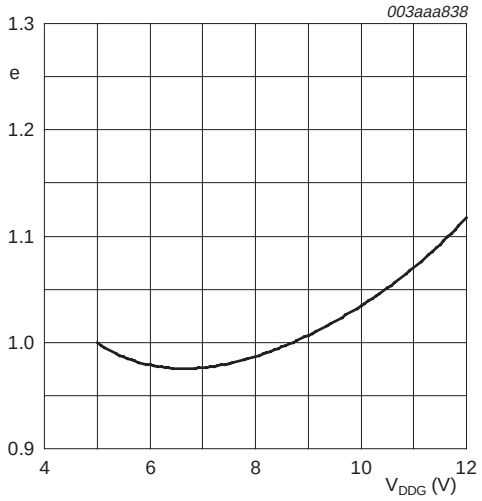
Fig 7. Normalized power dissipation as a function of input frequency; typical values



V_{DDO} = 12 V; V_O = 1.3 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

$$d = \frac{P_{tot}}{P_{tot(V_{DDC} = 12\,V)}}$$

Fig 8. Normalized power dissipation as a function of control circuit supply voltage; typical values



V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

$$e = \frac{P_{tot}}{P_{tot(V_{DDG} = 5\,V)}}$$

Fig 9. Normalized power dissipation as a function of gate drive supply voltage; typical values

11. Application information

11.1 Typical application

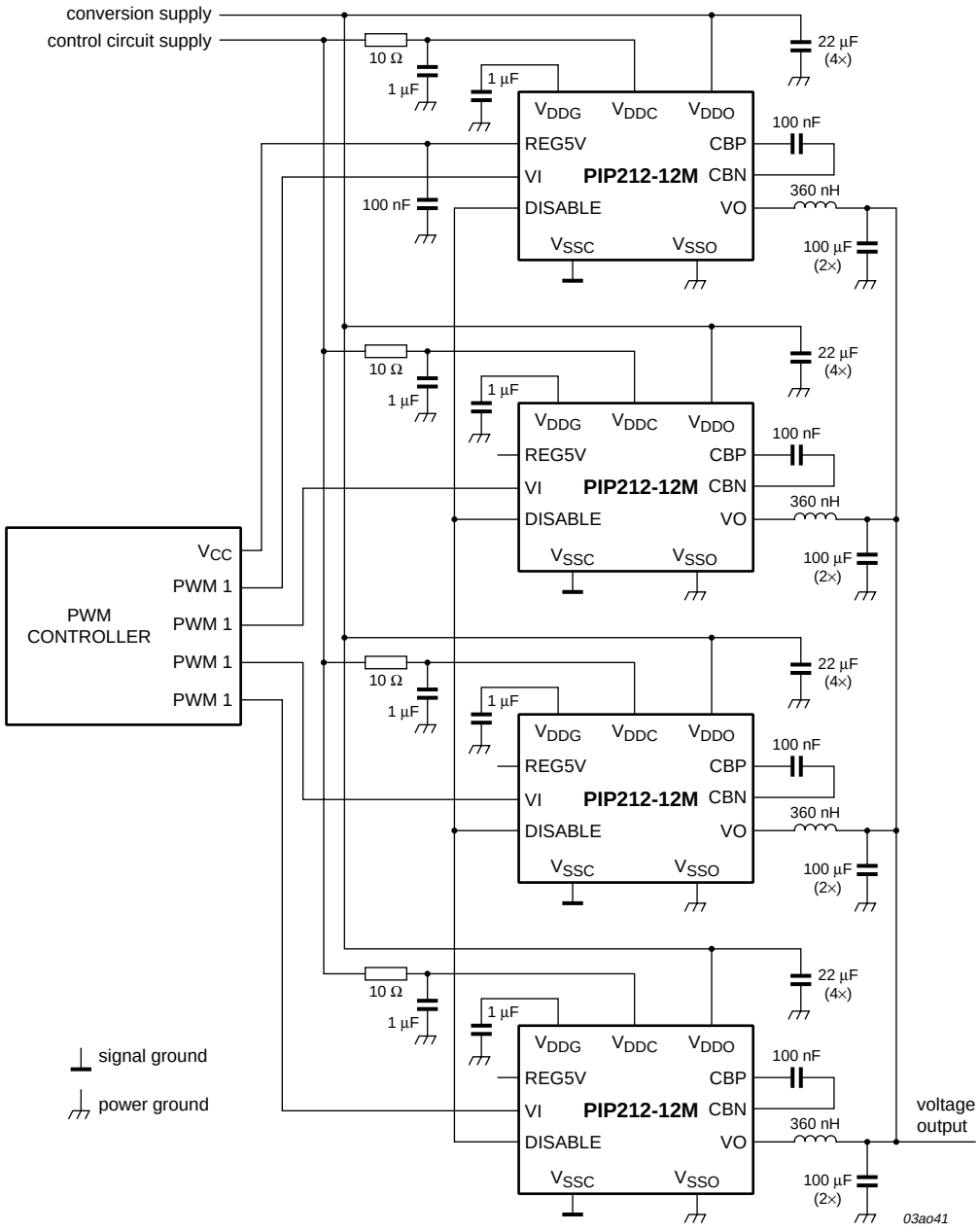


Fig 10. Typical application circuit using the PIP212-12M in a four-phase converter

A typical four-phase buck converter is shown in Figure 10. This system uses four PIP212-12M devices to deliver a continuous output current of 120 A at an operating frequency of 500 kHz.

11.2 V_{DDG} supply options

The following options can be used for the lower MOSFET driver supply (V_{DDG}).

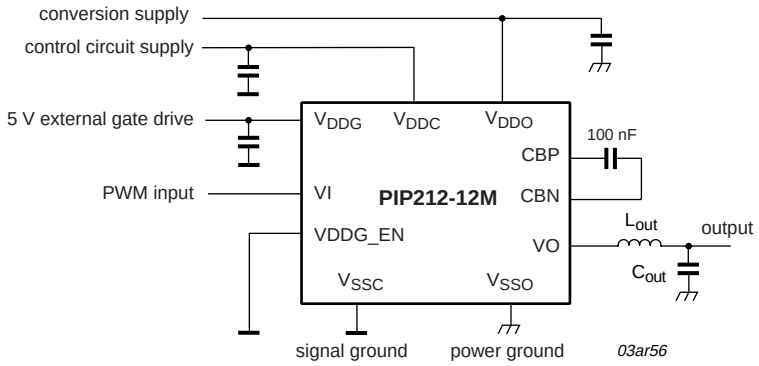


Fig 11. Dual supply operation using 5 V external supply for V_{DDG}

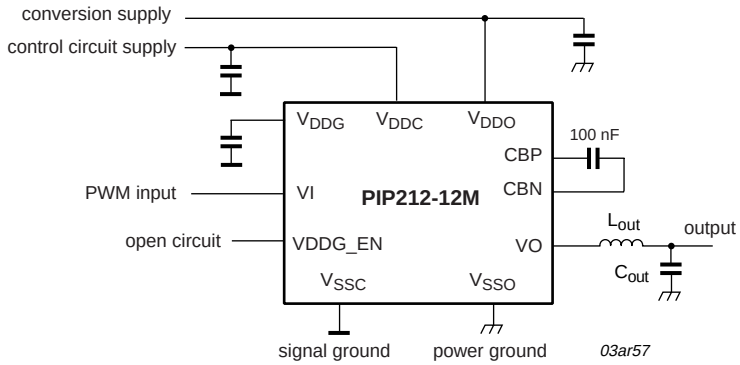


Fig 12. Single supply operation using internal supply for V_{DDG}

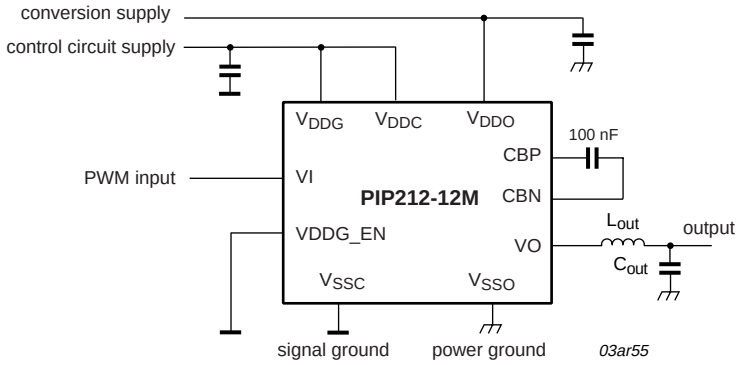
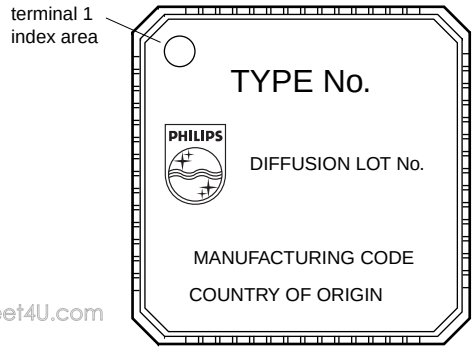


Fig 13. Single supply operation using external supply for V_{DDG}

12. Marking



TYPE No: PIP212-12M-NN (NN is revision number)

DIFFUSION LOT No: 7 characters

MANUFACTURING CODE; see Figure 15

COUNTRY OF ORIGIN: Korea

Fig 14. SOT684-4 marking

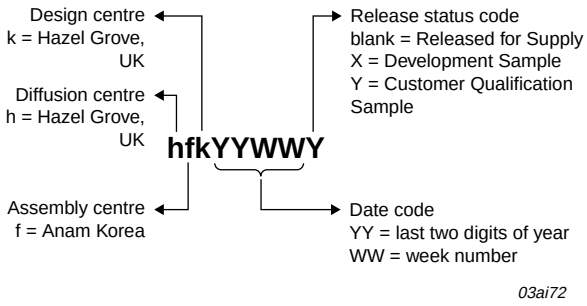
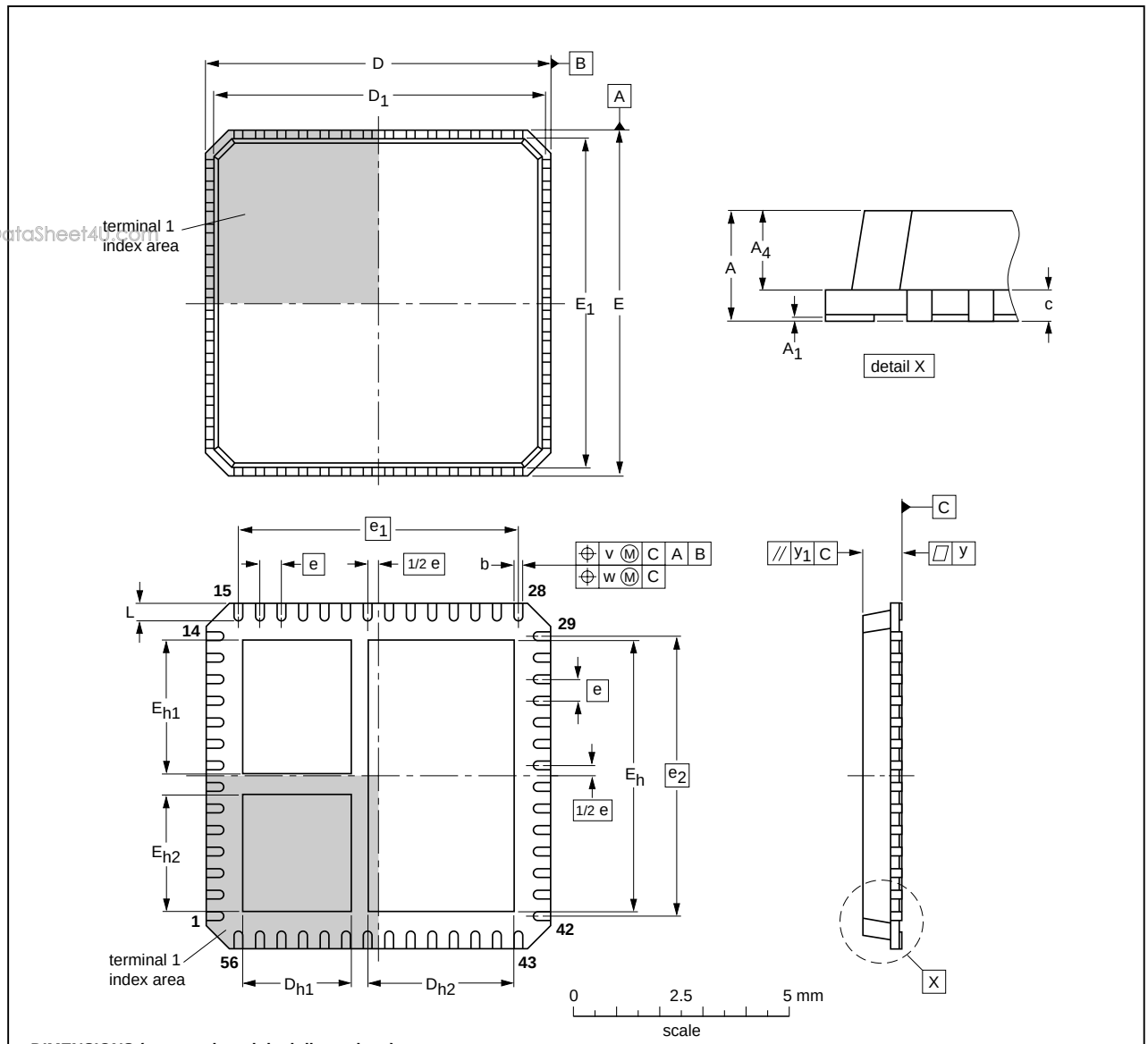


Fig 15. Interpretation of manufacturing code

13. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-4**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_4	b	c	D	D_1	D_{h1}	D_{h2}	E	E_1	E_h	E_{h1}	E_{h2}	e	e_1	e_2	L	v	w	y	y_1
mm	0.9	0.05 0.00	0.70 0.65	0.30 0.18	0.2	8.1 7.9	7.8 7.7	2.65 2.35	3.55 3.25	8.1 7.9	7.8 7.7	6.45 6.15	3.25 2.95	2.85 2.55	0.5	6.5	6.5	0.5 0.3	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT684-4	- - -	MO-220	- - -			~~03-10-23~~ 04-09-14

Fig 16. Package outline SOT684-4 (HVQFN56)

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 7: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Mounting

15.1 PCB design guidelines

The terminals on the underside of the package are rectangular in shape with a rounded edge on the inside. Electrical connection between the package and the printed-circuit board is made by printing solder paste onto the PCB footprint followed by component placement and reflow soldering. The PCB footprint shown in Figure 17 is designed to form reliable solder joints.

The use of solder resist between each solder land is recommended. PCB tracks should not be routed through the corner areas shown in Figure 17. This is because there is a small, exposed remnant of the leadframe in each corner of the package, left over from the cropping process.

Good surface flatness of the PCB lands is desirable to ensure accuracy of placement after soldering. Printed-circuit boards that are finished with a roller tin process tend to leave small lumps of tin in the corners of each land. Levelling with a hot air knife improves flatness. Alternatively, an electro-less silver or silver immersion process produces completely flat PCB lands.

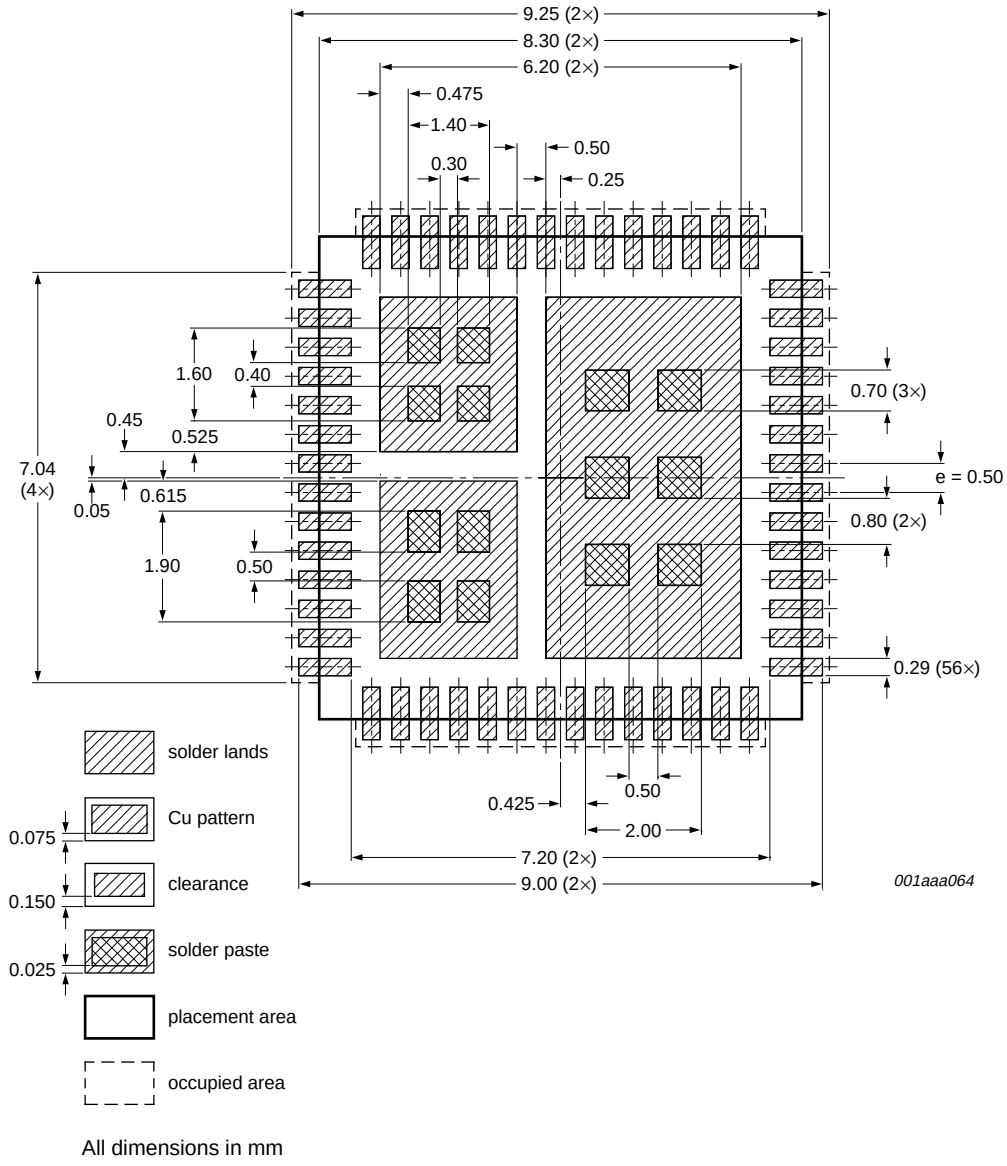


Fig 17. PCB footprint for SOT684-4 package (reflow soldering)

15.2 Solder paste printing

The process of printing the solder paste requires care because of the fine pitch and small size of the solder lands. A stencil thickness of 0.125 mm is recommended. The stencil apertures can be made the same size as the solder lands in Figure 17.

The type of solder paste recommended for MLF packages is “No clean”, Type 3, due to the difficulty of cleaning flux residues from beneath the MLF package.

16. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PIP212-12M_2	20050302	Preliminary data sheet	-	9397 750 14586	PIP212-12M_1
Modifications:	• Data sheet status changed to Preliminary data sheet				
PIP212-12M_1	20041223	Objective data sheet	-	9397 750 14464	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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