FEATURES

- Integrates two full-featured T1 performance monitors in a single device.
- Provides analog circuitry for receiving DSX-1 signals.
- Recovers clock and data using a digital PLL.
- Indicates low level signals and loss of signal.
- Frames to SF, ESF, T1DM and SLC®96 format DS1 signals.
- Provides optional ZBTSI decoding.
- Detects Yellow Carrier Fail Alarms (CFAs).
- Detects and integrates Red and AIS CFAs.
- Detects violation of the ANSI T1.403 12.5% pulse density violation rule.
- Counts up to 333 ESF CRC-6 error events, 31 framing bit errors, 4095 line code violations, and 7 out-of-frame or change of frame alignment events per second.
- Detects ESF bit-oriented codes.
- Provides an HDLC interface for terminating the ESF or ZBTSI data link.
- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Customizable design based on PMC's Telecom System Block megacells.
- Low power CMOS technology.
- 68-pin PLCC package.

APPLICATIONS

- Continuous performance monitors for T1 Network Management Systems.
- Hand-held T1 testers and continuous performance monitors in T1 test equipment.
- CSUs with integrated performance monitors.
- Multiplexers with integrated performance monitors.
- DACS with integrated performance monitors.

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DESCRIPTION

The PM4322 DXPM Dual DSX-1 Performance Monitor provides all the functions necessary to monitor the transmission characteristics of most T1 connections. It also provides analog circuitry for receiving each DSX-1 signal with only the addition of an external transformer and passive components. Direct digital input of a DS1 signal is also supported. The DXPM recovers clock and data with excellent jitter tolerance and can be configured to frame to any of the common DS1 signal formats: SF, ESF, T1DM or SLC®96. Optional ZBTSI decoding is provided.

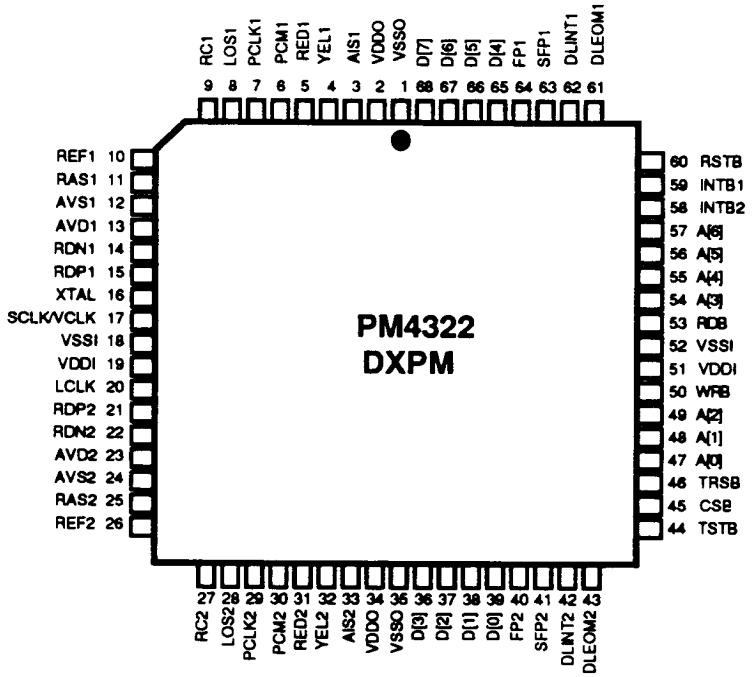
The DXPM supports detection of various alarm conditions such as Loss Of Signal, Pulse Density Violation, Red Alarm, Yellow Alarm, and AIS Alarm. Line and path performance monitoring are also supported through counters that allow accumulation of line code violations, framing bit errors, CRC-6 errors, and out-of-frame or change of frame alignment events. These counters are intended to be polled once per second and are sized so as not to saturate at a 10^{-3} bit error rate. To aid in identifying when equipment is improperly configured, the DXPM also detects a number of conditions such as eight successive zeros, B8ZS signatures, and sixteen successive zeros.

Termination of the ESF data link is supported through an HDLC interface and a bit oriented code detector. These circuits also operate when ZBTSI decoding is enabled. The HDLC interface supports polled, interrupt-driven and DMA servicing.

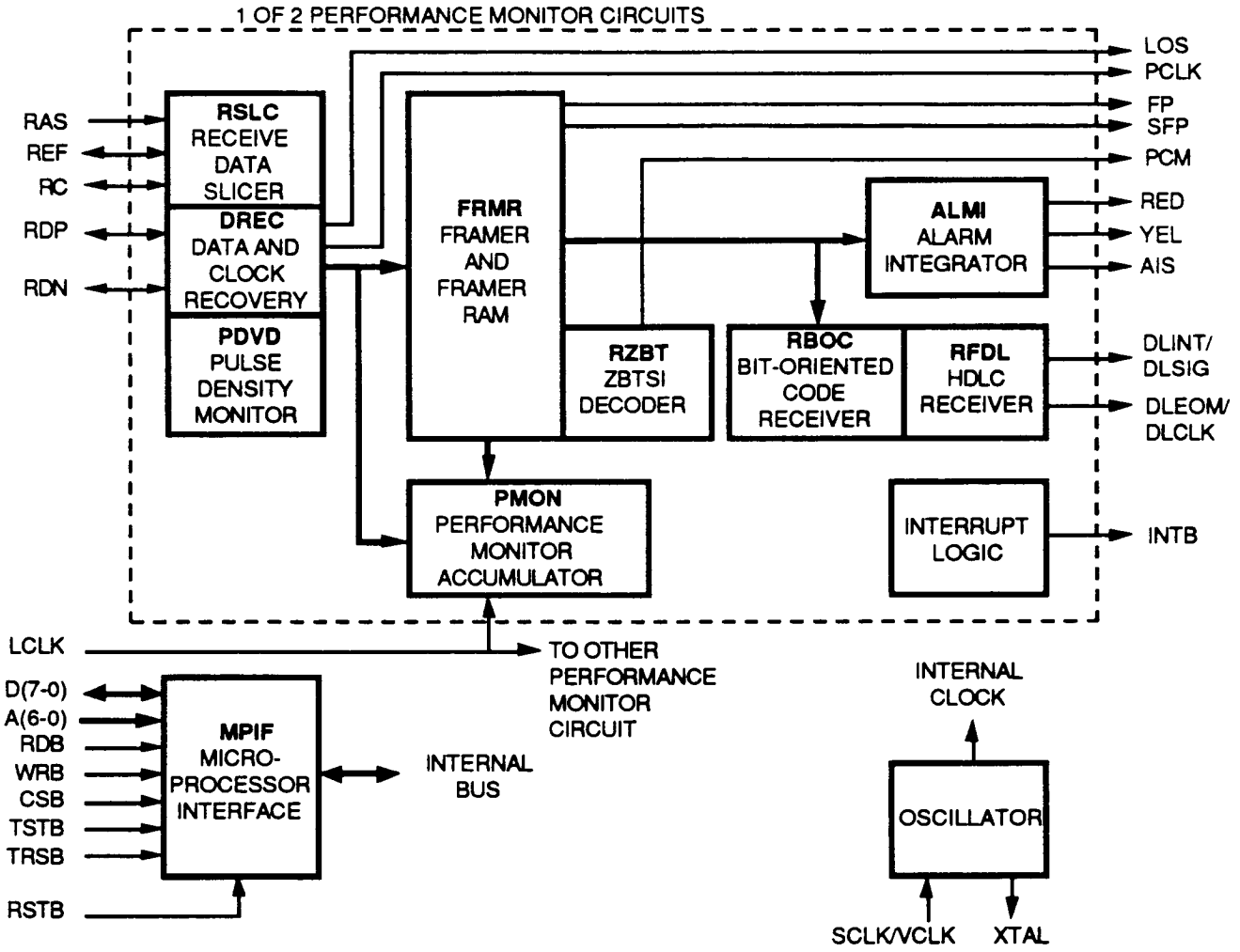
Timing for the DXPM may be provided by an on-chip 12.352 MHz crystal oscillator or an external clock source.

The DXPM is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed.

PIN DIAGRAM



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
SCLK/ VCLK	Input	17	The System Clock (SCLK) provides timing for DXPM operation. SCLK is nominally a 12.352 MHz, 50% duty cycle clock. SCLK may be driven externally or connected to a 12.352 MHz crystal. The Test Vector Clock (VCLK) signal is used during DXPM production test to verify internal functionality.
XTAL	Output	16	The Crystal Output (XTAL) may be connected to a 12.352 MHz crystal in conjunction with SCLK to form a crystal oscillator. When not used, XTAL should be left unconnected.
RDP1	I/O	15	The Receive Digital Positive Pulse 1 (RDP1) signal represents positive pulses. When PM-1 is not using the receive data slicer, RDP1 is the input pin for receiving DS1 positive line pulses. When PM-1 is using the receive data slicer, RDP1 outputs the DS1 positive pulses extracted from the DSX-1 signal.
RDP2	I/O	21	The Receive Digital Positive Pulse 2 (RDP2) signal represents positive pulses. When PM-2 is not using the receive data slicer, RDP2 is the input pin for receiving DS1 positive line pulses. When PM-2 is using the receive data slicer, RDP2 outputs the DS1 positive pulses extracted from the DSX-1 signal.
RDN1	I/O	14	The Receive Digital Negative Pulse 1 (RDN1) signal represents negative pulses. When PM-1 is not using the receive data slicer, RDN1 is the input pin for receiving DS1 negative line pulses. When PM-1 is using the receive data slicer, RDN1 outputs the DS1 negative pulses extracted from the DSX-1 signal.
RDN2	I/O	22	The Receive Digital Negative Pulse 2 (RDN2) signal represents negative pulses. When PM-2 is not using the receive data slicer, RDN2 is the input pin for receiving DS1 negative line pulses. When PM-2 is using the receive data slicer, RDN2 outputs the DS1 negative pulses extracted from the DSX-1 signal.

RAS1	Input	11	The Receive Analog Signal 1 (RAS1) input connects the line coupling transformer to the receive data slicer used by PM-1. This input should be connected to AVS1 when the receive data slicer used by PM-1 is disabled by connecting AVD1 to AVS1.
RAS2	Input	25	The Receive Analog Signal 2 (RAS2) input connects the line coupling transformer to the receive data slicer used by PM-2. This input should be connected to AVS2 when the receive data slicer used by PM-2 is disabled by connecting AVD2 to AVS2.
REF1	I/O	10	The Reference 1 (REF1) signal provides a bias voltage for the line coupling transformer associated with PM-1. This I/O connection should be left unconnected when the receive data slicer used by PM-1 is disabled by connecting AVD1 to AVS1.
REF2	I/O	26	The Reference 2 (REF2) signal provides a bias voltage for the line coupling transformer associated with PM-2. This I/O connection should be left unconnected when the receive data slicer used by PM-2 is disabled by connecting AVD2 to AVS2.
RC1	I/O	9	The External Peak Detector RC Network 1 (RC1) signal connects the peak detector of the receive data slicer used by PM-1 to an external RC network. This I/O connection should be left unconnected when the receive data slicer used by PM-1 is disabled by connecting AVD1 to AVS1.
RC2	I/O	27	The External Peak Detector RC Network 2 (RC2) signal connects the peak detector of the receive data slicer used by PM-2 to an external RC network. This I/O connection should be left unconnected when the receive data slicer used by PM-2 is disabled by connecting AVD2 to AVS2.
LOS1	Output	8	The Loss Of Signal Indication 1 (LOS1) signal is set high upon detection of 176 consecutive zero bit intervals on the PM-1 PCM stream. The LOS1 output is reset (low) upon the next occurrence of a PCM line pulse. The PCM stream is examined prior to B8ZS or ZBTSI decoding.

LOS2	Output	28	The Loss Of Signal Indication 2 (LOS2) signal is set high upon detection of 176 consecutive zero bit intervals on the PM-2 PCM stream. The LOS2 output is reset (low) upon the next occurrence of a PCM line pulse. The PCM stream is examined prior to B8ZS or ZBTSI decoding.
LCLK	Input	20	The Latch Clock (LCLK) triggers sample and hold of the internal performance monitor counters in PM-1 and PM-2 when it is brought high. The recommended accumulation interval is one second and thus LCLK should be driven with a 1 Hz clock signal. Note that an equivalent action may be triggered through register accesses if use of LCLK is not desired.
RED1	Output	5	The Red Alarm Indication 1 (RED1) signal indicates whether PM-1 has declared a RED carrier fail alarm.
RED2	Output	31	The Red Alarm Indication 2 (RED2) signal indicates whether PM-2 has declared a RED carrier fail alarm.
YEL1	Output	4	The Yellow Alarm Indication 1 (YEL1) signal indicates whether PM-1 has declared a YELLOW carrier fail alarm.
YEL2	Output	32	The Yellow Alarm Indication 2 (YEL2) signal indicates whether PM-2 has declared a YELLOW carrier fail alarm.
AIS1	Output	3	The AIS Alarm Indication 1 (AIS1) signal indicates whether PM-1 has declared an AIS carrier fail alarm.
AIS2	Output	33	The AIS Alarm Indication 2 (AIS2) signal indicates whether PM-2 has declared an AIS carrier fail alarm.
PCLK1	Output	7	The Recovered PCM Clock 1 (PCLK1) is derived from the DS1 or DSX-1 signal processed by PM-1 and is nominally a 1.544 MHz, 40-60% duty cycle clock. Note that PCLK1 has jitter due to the clock recovery process and jitter due to the reference DS1 or DSX-1 signal.
PCLK2	Output	29	The Recovered PCM Clock 2 (PCLK2) is derived from the DS1 or DSX-1 signal processed by PM-2 and is nominally a 1.544 MHz, 40-60% duty cycle clock. Note that PCLK2 has jitter due to the clock recovery process and jitter due to the reference DS1 or DSX-1 signal.

PCM1	Output	6	The Decoded PCM 1 (PCM1) signal outputs data recovered from the DS1 or DSX-1 signal processed by PM-1 after B8ZS or ZBTSI decoding has been performed. PCM1 is updated on the falling edge of PCLK1.
PCM2	Output	30	The Decoded PCM 2 (PCM2) signal outputs data recovered from the DS1 or DSX-1 signal processed by PM-2 after B8ZS or ZBTSI decoding has been performed. PCM2 is updated on the falling edge of PCLK2.
FP1	Output	64	The active high Frame Pulse 1 (FP1) signal indicates that the framing bit position (bit 1 of the 193 bit frame) is present on the PCM1 output. This output remains high for one PCLK1 period and is updated on the falling edge of PCLK1.
FP2	Output	40	The active high Frame Pulse 2 (FP2) signal indicates that the framing bit position (bit 1 of the 193 bit frame) is present on the PCM2 output. This output remains high for one PCLK2 period and is updated on the falling edge of PCLK2.
SFP1	Output	63	The active high Superframe Pulse 1 (SFP1) signal indicates that the superframe bit position (bit 1 in the first frame of the 12 or 24 frame superframe) is present on the PCM1 output. This output remains high for one PCLK1 period and is updated on the falling edge of PCLK1.
SFP2	Output	41	The active high Superframe Pulse 2 (SFP2) signal indicates that the superframe bit position (bit 1 in the first frame of the 12 or 24 frame superframe) is present on the PCM2 output. This output remains high for one PCLK2 period and is updated on the falling edge of PCLK2.
DLINT1/ DLSIG1	Output	62	The Data Link Interrupt 1 (DLINT1) signal indicates that the internal HDLC receiver in PM-1 is requesting servicing. DLINT1 is valid when the internal HDLC receiver is enabled in PM-1. When the internal HDLC receiver is disabled in PM-1, this output becomes Data Link Signal 1 (DLSIG1). DLSIG1 carries the data link extracted from the DS1 frame as appropriate for the framing format utilized, T1DM, SLC96, ESF, or ZBTSI. DLSIG1 is updated on the falling edge of DLCLK1.

DLINT2/ DLSIG2	Output	42	The Data Link Interrupt 2 (DLINT2) signal indicates that the internal HDLC receiver in PM-2 is requesting servicing. DLINT2 is valid when the internal HDLC receiver is enabled in PM-2. When the internal HDLC receiver is disabled in PM-2, this output becomes Data Link Signal 2 (DLSIG2). DLSIG2 carries the data link extracted from the DS1 frame as appropriate for the framing format utilized, T1DM, SLC96, ESF, or ZBTSI. DLSIG2 is updated on the falling edge of DLCLK2.
DLEOM1/ DLCLK1	Output	61	The Data Link End of Message 1 (DLEOM1) signal indicates that the internal HDLC receiver in PM-1 has received the final byte in a message and requires servicing. DLEOM1 is useful when interfacing to an external DMA controller and is valid when the internal HDLC receiver is enabled in PM-1. When the internal HDLC receiver is disabled in PM-1, this output becomes Data Link Clock 1 (DLCLK1). DLCLK1 provides timing for the data link extracted from the DS1 frame. DLCLK1 operates at 8 kHz, 4 kHz, 2 kHz or is held inactive, as appropriate for the framing format utilized; T1DM, SLC96, ESF, ZBTSI, or SF.
DLEOM2/ DLCLK2	Output	43	The Data Link End of Message 2 (DLEOM2) signal indicates that the internal HDLC receiver in PM-2 has received the final byte in a message and requires servicing. DLEOM2 is useful when interfacing to an external DMA controller and is valid when the internal HDLC receiver is enabled in PM-2. When the internal HDLC receiver is disabled in PM-2, this output becomes Data Link Clock 2 (DLCLK2). DLCLK2 provides timing for the data link extracted from the DS1 frame. DLCLK2 operates at 8 kHz, 4 kHz, 2 kHz or is held inactive, as appropriate for the framing format utilized; T1DM, SLC96, ESF, ZBTSI, or SF.
INTB1	Output	59	The active low, open-drain Interrupt (INTB1) signal is asserted when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that the internal PM-1 HDLC receiver also has a separate interrupt output (DLINT1).
INTB2	Output	58	The active low, open-drain Interrupt (INTB2) signal is asserted when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that the internal PM-2 HDLC receiver also has a separate interrupt output (DLINT2).

CSB	Input	45	The active low Chip Select (CSB) signal is low during DXPM register accesses.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	68 67 66 65 36 37 38 39	The bidirectional data bus (D[7:0]) is used during DXPM register accesses.
RDB	Input	53	The active low Read Enable (RDB) signal is low during a DXPM read access. The DXPM drives the D[7:0] bus with the addressed register's contents while RDB and CSB are low.
WRB	Input	50	The active low Write Strobe (WRB) signal is low during a DXPM write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
TSTB	Input	44	The active low Test Mode Select (TSTB) signal is low during DXPM production test. TSTB is high during normal operation.
RSTB	Input	60	The active low Reset (RSTB) signal is low to provide an asynchronous DXPM reset. This pin has an internal pullup resistor and is a Schmitt trigger input.
TRSB	Input	46	The Test Register Select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test register accesses, and is high during normal mode register accesses. TRSB is high during normal operation.
A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	57 56 55 54 49 48 47	The Address Bus (A[6:0]) selects specific registers during DXPM register accesses.

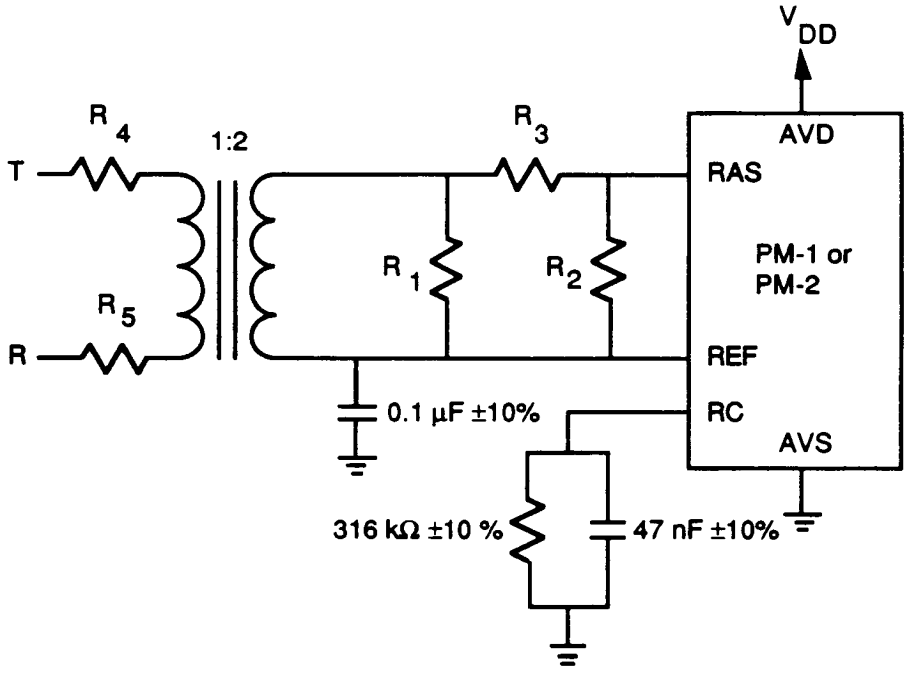
VDDO[1] VDDO[0]	Power	2 34	The Pad Ring Power (VDDO[1:0]) connections provide power for pad ring circuitry. VDDO[1:0] must be connected to a well decoupled +5 V DC supply. Both connections must be utilized. VDDO[1:0] and VDDI[1:0] should be externally connected to the same supply in a manner that minimizes switching noise coupling from VDDO[1:0] to VDDI[1:0].
VDDI[1] VDDI[0]	Power	51 19	The Core Power (VDDI[1:0]) connections provide power for core circuitry. VDDI[1:0] must be connected to a well decoupled +5 V DC supply. Both connections must be utilized.
VSSO[1] VSSO[0]	Ground	1 35	The Pad Ring Ground (VSSO[1:0]) connections provide ground for pad ring circuitry. Both connections must be utilized. VSSO[1:0] and VSSI[1:0] should be externally connected to the same ground in a manner that minimizes switching noise coupling from VSSO[1:0] to VSSI[1:0].
VSSI[1] VSSI[0]	Ground	52 18	The Core Ground (VSSI[1:0]) connections provide ground for core circuitry. Both connections must be utilized.
AVD1	Power	13	The Analog Power 1 (AVD1) connection provides power for the receive data slicer associated with PM-1. AVD1 must be connected to a well decoupled +5 V DC supply. AVD1 should be connected to AVS1 to disable the receive data slicer used by PM-1.
AVD2	Power	23	The Analog Power 2 (AVD2) connection provides power for the receive data slicer associated with PM-2. AVD2 must be connected to a well decoupled +5 V DC supply. AVD2 should be connected to AVS2 to disable the receive data slicer used by PM-2.
AVS1	Ground	12	The Analog Ground 1 (AVS1) connection provides ground for the receive data slicer associated with PM-1.
AVS2	Ground	24	The Analog Ground 2 (AVS2) connection provides ground for the receive data slicer associated with PM-2.

FUNCTIONAL DESCRIPTION

Receive Data Slicer

The Receive Data Slicer (RSLC) block provides the first stage of signal conditioning for a DSX-1 serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ output pulse is generated by the RSLC block, bipolar input signals must rise to 67% of their peak amplitude. This level is referred to as the Slicing Level. The threshold criteria insures accurate pulse or mark recognition in the presence of noise.

Fig. 1 External Analog Interface Circuit



Terminate Mode	Bridging Mode
R_1 = 412 Ω ± 1%	R_1 = 400 Ω ± 1%
R_2 = 1.1 kΩ ± 1%	R_2 = Open Circuit
R_3 = 9.0 kΩ ± 1%	R_3 = Closed Circuit
R_4 = R_5 = Closed Circuit	R_4 = R_5 = 432 Ω ± 5 %

1. All capacitors ceramic
2. R_4 and R_5 are part of a DSX bridge-tap
3. Recommended Transformer: Pulse Engineering 64931
   BH Electronics 500-1775

The RSLC block is configured via an off-chip attenuator pad (as shown in Figure 1) to operate in one of two modes: terminate mode or bridging mode. In terminate mode, the amplitude of a received pulse at the line-coupling transformer's primary can be in the range from 3.6 V to 0.5 V depending on the DXPM's distance from the DSX-1 cross-connect. In bridging mode, the DXPM is bridged across the line and the expected signal levels are 20 dB lower than standard DSX-1 levels. In each mode the sensitivity below minimum DSX-1 levels is -10 dB. The sensitivity of the receiver is defined as the difference between the worst case DSX-1 signal amplitude (2.4 V) and the squelching level.

The RSLC block has two signal level alarms which are operational in both terminate and bridging modes. The first alarm is the low signal level alarm. This alarm occurs when input pulses at the line-coupling transformer's primary are below the low level threshold but above the squelching level threshold. During a low level alarm the RSLC block continues to operate and the LV status bit goes high. The low level signal threshold is 1.5 V for terminate mode, and 150 mV for bridging mode. The RSLC block can be configured to generate an interrupt when the LV status bit goes high.

The second alarm occurs when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. For the terminate mode of operation, the squelching threshold is 0.5 V; for bridging mode, the squelching threshold is 50 mV. The SQ status bit goes high whenever the RSLC block is squelching. The block can be configured to generate an interrupt whenever the SQ status bit goes high.

When the RSLC block is active, the positive and negative line pulses of the DS1 signal extracted from the DSX-1 input are output on the RDP and RDN pins, respectively. The RSLC block can be bypassed by strapping the analog power pin, AVD, to ground. When the RSLC block is disabled, the performance monitor accepts DS1 input pulses on the RDP and RDN pins.

Data and Clock Recovery

The Data and Clock Recovery (DREC) block provides clock and PCM data recovery, B8ZS decoding, line code violation detection, 8 consecutive zeros detection, and loss of signal detection functions. The DREC block recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop. NRZ data is restored and B8ZS substitution is performed when enabled. The use of AMI or B8ZS line code format is user-selectable. Bipolar violations which form part of the B8ZS line code are only reported as line code violations when AMI line code is selected. The detection of B8ZS signatures and 8 consecutive zeros is always reported, regardless of the selected line code. Loss of signal is indicated after 176 consecutive bit periods of the absence of pulses on both the RP and RN inputs and is cleared after the occurrence of a single line pulse. If enabled, a microprocessor interrupt is generated upon the occurrence of line events and/or alarms.

Fig. 2 Typical External Crystal Oscillator Circuit

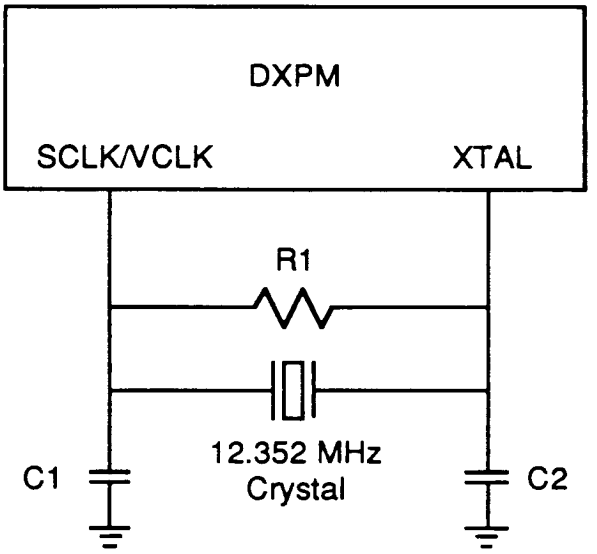


Figure 2 shows a typical circuit using an external crystal for timing generation. Typically, R1 has a value of 1 MΩ or greater. The values of the two capacitors are dependent upon the specified load capacitance of the crystal. An AT cut crystal with a parallel resonant frequency of 12.352 MHz for an 18 pF load is recommended. For the recommended crystal, the capacitors, C1 and C2 each have a value of 30 pF (taking into account the capacitance of the pins). The performance monitors in the DXPM share the same timing source.

Framer and Framer RAM

The Framer (FRMR) block searches for the framing bit position in the incoming recovered PCM stream. SF, ESF, T1DM and SLC®96 framing formats are supported. When searching for frame, the FRMR block examines each of the 193 (SF, T1DM, SLC®96), or each of 4*193 (ESF) framing bit candidates. The Framer RAM (FRAM) block is used to store up to four frames of PCM data while the FRMR block is finding frame.

It is possible for channel data to mimic the framing bit pattern for a period of time in any of the supported framing formats. The FRMR block does not declare the in-frame condition while mimic framing patterns are detected in the SF or T1DM formats. False framing (i.e. declaring the in-frame condition on a mimic framing pattern) is thus avoided. While mimic framing patterns are detected in ESF format, a CRC-6 calculation can be performed for each framing bit candidate to determine the most likely framing bit position and to minimize the probability of false framing while allowing the declaration of the in-frame condition to occur. The CRC-6 calculation criteria can be disabled under software control (using the ESFFA bit in the FRMR configuration register) so that the ESF framing algorithm does not declare an in-

frame condition while mimic framing patterns are detected, and hence avoids false framing. The FRMR block does not provide protection against false framing while the SLC®96 format is enabled.

Once the FRMR block has found frame, the INF status in the register is asserted and the incoming PCM data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or SLC®96, a framing bit error or sync byte bit error in T1DM, or a CRC-6 error in ESF), and severely-errored framing events (more than 1 out of 12 F-bits in error in SF, more than 1 out of 12 sync byte or framing bit errors in T1DM, more than 1 out of 6 F_T bits in error in SLC®96, or more than 1 out of 6 F_E bits in error in ESF). The FRMR block detects out-of-frame, based on a selectable ratio of framing bit errors (2 out of 6, 2 out of 5, or 2 out of 4).

The FRMR block extracts the yellow alarm signal bits from the incoming PCM data stream in SF and SLC®96 framing formats, and extracts the Y-bit from the T1DM sync word in T1DM framing format. The FRMR block also extracts the SLC®96 data link in SLC®96 framing format, extracts the facility data link bits in ESF framing format (with or without ZBTSI), and extracts the R-bit from the T1DM sync byte in T1DM framing format.

ZBTSI Decoder

The ZBTSI Decoder (RZBT) block is a ZBTSI (zero byte time slot interchange) decoder without partial error correction. The RZBT block requires frame and extended superframe synchronization to identify octet boundaries and the Z-bit location. The ZBTSI decoding algorithm requires 2 kbit/s of overhead information carried within the ESF data link. While the DXPM is out-of-frame and searching for the framing bit position in the incoming ESF DS1 stream, ZBTSI decoding is disabled so that framing circuitry can operate correctly. A uniform delay is applied to the PCM data passing through the RZBT block whether the DXPM is in-frame or out-of-frame so that enabling the ZBTSI decoding algorithm after detection of the framing bit does not result in out-of-frame (or failure to reframe). ZBTSI decoding is activated under software control by a register bit in the RZBT block.

Alarm Integrator

The Alarm Integrator (ALMI) block detects the presence of Yellow, Red, and AIS Carrier Fail Alarms (CFAs) in SF, T1DM, SLC®96 and ESF formats. The CFA alarm detection algorithms operate in the presence of a random 10^{-3} bit error rate.

Framing format selection is performed under software control by programming the ALMI Configuration. For the ESF format, software must also control the integration algorithm for Yellow alarm by selecting the data rate of the ESF message link to be 2 kbit/s (ZBTSI compatible) or the standard 4 kbit/s rate.

The ALMI block declares the presence of Yellow alarm when the Yellow pattern has been received for 425 ms (±50 ms); the Yellow alarm indication is negated when

the Yellow alarm pattern has been absent for 425 ms (±50 ms). The Yellow alarm status is frozen while out-of-frame.

For SF, ESF and SLC®96 formats, the presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 s (±40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 s (±500 ms). In order to allow fast deassertion of Red alarm, the ALMI Configuration Register can be programmed to deassert Red alarm within 120 ms of the in-frame condition. In T1DM framing format, two Red alarm detection options are available. With one option, the Red alarm assertion and deassertion times are identical to those for SF, ESF and SLC®96 formats. With the other option, Red alarm is declared in 400 ms (±100 ms) and removed in 100 ms (±50 ms).

The presence of AIS alarm is declared when an AIS condition (out-of-frame condition and all-ones in the PCM data stream) has been present for 1.5 s (±100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 s (±500 ms). In order to allow fast deassertion of AIS alarm, the ALMI Configuration Register can be programmed to remove the AIS alarm after a 60 ms interval containing 127 or more zeros in the incoming DS1 stream is observed.

Alarm indication is provided on the YEL, RED and AIS outputs, as well as through the ALMI Interrupt Status Register. The ALMI block can be programmed to generate an interrupt when any of the alarms changes state.

Pulse Density Violation Detector

The Pulse Density Violation Detector (PDVD) block detects pulse density violations of the requirement that there be 'N' ones in each and every time window of 8(N+1) data bits (where 'N' can equal from 1 to 23). The PDVD block also detects periods of 16 consecutive zeros in the incoming data stream.

Pulse density violation detection is indicated in the PDVD Interrupt Enable/Status Register. The PDVD block can be programmed to generate an interrupt to signal a 16 consecutive zero event and/or a change of state in the pulse density violation indication.

Performance Monitor Accumulator

The Performance Monitor (PMON) block accumulates CRC error events, frame synchronization bit error events, line code violation events, and out-of-frame or change of frame alignment events with saturating counters over consecutive intervals as defined by the period (typically 1 second) of the supplied latch clock signal, LCLK. A single LCLK input serves both performance monitors in the DXPM. An internal latch clock signal, unique to each performance monitor in the DXPM, can be generated by writing to any of the PMON counter data registers. A write to any PMON data register in PM-1 generates an internal latch clock pulse and similarly a

write to any PMON data register in PM-2 generates an internal latch clock pulse. On the rising edge of the latch clock signal, the counter values are transferred into holding registers and the counters are reset. The counters are reset in a manner such that error events occurring during the reset are not missed.

If enabled, an interrupt is generated whenever counter data is transferred into the holding registers. If the holding registers are not read between successive transfer clocks, the overrun (OVR) bit in the PMON Interrupt Enable/Status Register is set.

Bit Oriented Code Detector

The Bit Oriented Code Detector (RBOC) block detects the presence of 63 of the 64 possible bit oriented codes (BOCs) transmitted in the facility data link (FDL) channel in ESF framing format. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored by the RBOC.

Bit oriented codes are received on the FDL channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times in normal ESF mode (4 kbit/s link) or at least 5 times in ESF mode with ZBTSI coding (2 kbit/s). The RBOC block can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Control Register.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") if no valid code has been detected. The RBOC block can be programmed to generate an interrupt when a detected code has been validated.

HDLC Data Link Receiver

The Receive Facility Data Link (RFDL) block is a microprocessor peripheral used to receive LAPD/HDLC frames on the ESF facility data link (FDL). The RFDL block detects the change from flag characters to the first data frame byte, removes stuffed bits from the frame data, and computes the frame check sequence (CRC-CCITT) associated with the frame.

The RFDL places received data into a four-byte FIFO buffer. Interrupts can be enabled to occur after one, two, or three frame bytes have been received (programmable FIFO fill level), or disabled completely. Software selects the interrupt generation interval by assigning values to two bits in the RFDL Enable Register. Each read of the RFDL data register should be followed by a read of the RFDL Status Register. The RFDL Status Register contains a FIFO status bit (FE) that indicates the full/empty status of the four-byte FIFO. If the FE bit is a zero, the FIFO is not empty, so successive reads of the RFDL Data Register must be performed followed by reads of the RFDL Status Register until the FE bit is a one (i.e. until the

FIFO buffer is empty). The RFDL Data Register must not be read if the FE bit is a one.

If the software selects the FIFO fill level to be two bytes before an interrupt is generated (i.e. 4 ms in an ESF 4 kbit/s message link), the corresponding maximum interrupt service time is 6 msec (i.e. 3 frame byte periods). If the maximum interrupt service time is exceeded, the overrun bit (OVR) in the RFDL Status Register is set to one, and an interrupt is immediately generated. An interrupt is also generated upon reception of an abort sequence while the link is active. The FLG bit in the RFDL Status Register is set to zero upon reception of an abort sequence.

Initialization

Upon reset, the RFDL Configuration Register is set to 00H, and the RFDL is disabled. The RFDL Interrupt Status/Control Register must be written to select the FIFO fill level for which an interrupt is generated.

After the RFDL Interrupt Status/Control Register has been written, the RFDL can be enabled at any time by setting the EN bit in the RFDL Configuration Register to one. When the RFDL is enabled, it assumes the link status is idle (all ones) and immediately begins searching for flags. When the first flag is found, an interrupt is generated, regardless of the FIFO fill level. An RFDL Status Register read following an RFDL Data Register read returns EOM=1 and FLG=1. The first interrupt and data byte read after the RFDL is enabled is an indication of the link status and the data byte should be discarded. It is up to the controlling software to keep track of the link state as idle (all ones or bit oriented messages active) or active (flags received).

Servicing

The microprocessor interrupt service routine should process data the following order:

1) Read the RFDL Data Register
2) Read the RFDL Status Register to check for underrun (status register returns 00H), OVR, FLG, EOM and if more data is available (FE), in that order.
3) If underrun (status register returned 00H), then discard last byte and wait for next interrupt.
4) If OVR=1, discard last packet and wait for next interrupt.
5) If FLG=0 (abort) and the link state was active, set the link state to inactive, discard the last packet and wait for the next interrupt.
6) If FLG=1 and the link state was inactive, set the link state to active, discard the last packet and wait for the next interrupt.
7) Otherwise save the last data byte read.

8) If EOM=1, check the CRC bit and process the packet.

9) If FE=0, go to step 1, or else wait for the next interrupt.

The link state is a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

The DLEOM status output is provided for interfacing the RFDL block to a DMA controller.

Microprocessor Interface

The Microprocessor Interface (MPIF) block allows for device level configuration of each performance monitor (PM) in the DXPM package. The low-power modes and the use of the internal or an external HDLC controller are configured via the Configuration Register. The interrupts from each block in each PM are masked and monitored with the Master Interrupt Enable and Master Interrupt Status Registers, respectively. A software reset mode is provided through the Master Reset Register.

The MPIF block also serves as the physical interface between the microprocessor and the internal blocks. Functions such as data bus buffering and address decoding are provided by the MPIF block.

Normal Mode Register Memory Map

PM-1	PM-2	REGISTER DESCRIPTION
00H	40H	MASTER CONFIGURATION
01H	41H	MASTER INTERRUPT ENABLE
02H	42H	MASTER INTERRUPT STATUS
03H	43H	MASTER RESET
04H	44H	RFDL CONFIGURATION
05H	45H	RFDL INTERRUPT ENABLE/STATUS
06H	46H	RFDL STATUS
07H	47H	RFDL RECEIVE DATA
08H	48H	Reserved for PMON test
09H	49H	PMON INTERRUPT ENABLE/STATUS
0AH	4AH	PMON LINE CODE VIOLATION EVENT COUNT LSB
0BH	4BH	PMON LINE CODE VIOLATION EVENT COUNT MSB
0CH	4CH	PMON BIT ERROR EVENT COUNT LSB
0DH	4DH	PMON BIT ERROR EVENT COUNT MSB
0EH	4EH	PMON FRAMING BIT ERROR EVENT COUNT
0FH	4FH	PMON OOF/COFA EVENT COUNT
10H	50H	DREC CONFIGURATION

11H	51H	DREC INTERRUPT ENABLE STATUS
12H	52H	DREC STATUS
13H	53H	Reserved for DREC test
14H	54H	FRMR CONFIGURATION
15H	55H	FRMR INTERRUPT ENABLE
16H	56H	FRMR INTERRUPT STATUS
17H	57H	Reserved for FRMR test
18H	58H	ALMI CONFIGURATION
19H	59H	ALMI INTERRUPT ENABLE
1AH	5AH	ALMI INTERRUPT STATUS
1BH	5BH	Reserved for ALMI test
1CH-1FH	5CH-5FH	Reserved
20H	60H	RBOC CONFIGURATION/INTERRUPT ENABLE
21H	61H	RBOC INTERRUPT STATUS
22H	62H	Reserved for PDVD test
23H	63H	PDVD INTERRUPT ENABLE/STATUS
24H	64H	RZBT CONFIGURATION
25H	65H	Reserved for RZBT test
26H	66H	Reserved for RSLC test
27H	67H	RSLC INTERRUPT ENABLE/STATUS
28H	68H	Reserved for FRAM test
29H	69H	Reserved for FRAM test
2AH-3FH	6AH-7FH	Unused

Note: All register bits are cleared to zero upon activation of DXPM reset unless otherwise noted.

NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the DXPM. Normal mode registers (as opposed to test mode registers) are selected when TRSB is high.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the DXPM to determine the programming state of the chip.

3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect DXPM operation unless otherwise noted.

Internal Registers

Register 00H, 40H: Master Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R/W	CCOFA
Bit 2	R/W	PATHE
Bit 1	R/W	LINEE
Bit 0	R/W	EXHDLC

This register allows software to configure the associated performance monitor (address 00H for PM-1, address 40H for PM-2) in the DXPM package. The state of the EXHDLC (external HDLC) bit determines whether the PM uses the internal HDLC receiver or provides the data and clock signals for an external HDLC receiver. When the EXHDLC bit is a logic 0, the DLINT/DLSIG pin is configured to output the interrupt signal (DLINT) from the internal HDLC receiver and the DLEOM/DLCLK pin is configured to output the end-of-message signal (DLEOM) from the internal HDLC receiver. When the EXHDLC bit is a logic 1, the DLINT/DLSIG pin is configured to output the facility data link data stream (DLSIG) and the DLEOM/DLCLK pin is configured to output the facility data link clock signal (DLCLK) for use by an external HDLC receiver. Upon reset of a PM, the EXHDLC bit is cleared to zero, thus the internal HDLC receiver is selected.

The line enable (LINEE) and path enable (PATHE) bits select whether the PM is enabled to monitor the line or the path, respectively. When the PM is only enabled to monitor the line, the following blocks are deactivated: FRMR, FRAM, RFDL, RBOC and RZBT. When the path is being monitored, all blocks are active. When neither the line nor the path is being monitored, the PM is in low-power mode. In low-power mode, only the DREC and RSLC blocks are active. The mode selection is given in the following table:

PATHE	LINEE	DESCRIPTION
0	0	Low-power mode; only DREC and RSLC are active
0	1	Line monitoring mode; FRMR, FRAM, RBOC, RFDL, RZBT inactive
1	X	Path monitoring mode; all blocks active

Upon reset of the PM, both the PATHE and LINEE bits are cleared to zero which places the PM in low-power mode.

The count change of frame alignment bit, CCOFA, determines whether the PMON block counts COFA or OOF (out-of-frame) events. When the CCOFA bit is logic 1, COFA events are counted by the PMON block; conversely, when the CCOFA bit is a logic 0, OOF events are counted by the PMON block. Upon reset of a PM, the CCOFA bit is cleared to zero, thus the PMON block counts OOF events.

Register 01H, 41H:
Master Interrupt Enable

Bit	Type	Function
Bit 7	R/W	DLINTE
Bit 6	R/W	PDVDE
Bit 5	R/W	RBOCE
Bit 4	R/W	PMONE
Bit 3	R/W	ALMIE
Bit 2	R/W	FRMRE
Bit 1	R/W	DRECE
Bit 0	R/W	RSLCE

This register provides an interrupt enable bit for each of the blocks comprising one performance monitor in the DXPM. Interrupts may still be masked at the source block level. Interrupts enabled at the block level but masked by this register are reported in the Master Interrupt Status Register. Interrupts disabled at the block level are not reported by the Master Interrupt Status Register. The RFDL block also generates a separate, active high, interrupt output (DLINT). Interrupts on the DLINT pin are not maskable with this register.

Register 02H, 42H:
Master Interrupt Status

Bit	Type	Function
Bit 7	R	DLINTI
Bit 6	R	PDVDI
Bit 5	R	RBOCI
Bit 4	R	PMONI
Bit 3	R	ALMII
Bit 2	R	FRMRI
Bit 1	R	DRECI
Bit 0	R	RSLCI

This register identifies the block which is the source of a pending interrupt. After identifying the block which generated the interrupt, it may be necessary to read the interrupt status register of that block to determine the actual event which generated the interrupt. This register is provided as a convenience to the user since the source block of an interrupt can be determined by polling the interrupt status registers of every block in the DXPM. Unlike the interrupt status registers associated with each block, this register only reports interrupt sources capable of generating a hardware interrupt, that is interrupts masked at the block interrupt enable register level are not reported by this register. The RFDL block also generates a separate, active high, interrupt output (DLINT).

Register 03H, 43H:
Master Reset

Bit	Type	Function
Bit 7	R/W	RESET
Bit 6	R	TYPE
Bit 5	R	ID[5]
Bit 4	R	ID[4]
Bit 3	R	ID[3]
Bit 2	R	ID[2]
Bit 1	R	ID[1]
Bit 0	R	ID[0]

This register allows software to asynchronously reset the associated performance monitor (address 03H for PM-1 and address 43H for PM-2) in the DXPM package; the two performance monitors in the DXPM package have independent software resets. The software reset is equivalent to setting the RSTB input pin to low, except that only one performance monitor is affected. Setting the RESET bit to logic 1

causes the associated PM to be reset; clearing the RESET bit to logic 0 disables the reset mode. In reset mode, all bits in all PM registers are reset except for the RESET bit itself. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register. The DXPM RSTB pin resets both performance monitors in the DXPM package and clears the RESET bit in this register to logic 0, disabling the software reset mode.

The device identification bit, TYPE, is set to 0 to identify the DXPM. The version identification bits, ID[5:0], are set to a fixed value representing the version number of the DXPM. The identification bits can be used to determine the DXPM version via software. The identification bits of each PM are identical.

RFDL Registers

Register 04H, 44H: RFDL Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	TR
Bit 0	R/W	EN

The enable bit, EN, controls the overall operation of the RFDL block. When EN is set to logic 1, the RFDL is enabled; when EN is reset to logic 0 the RFDL is disabled. When the RFDL is disabled, the FIFO and interrupts are cleared. The programming of the Enable/Status Register is not affected. When the RFDL is enabled, it immediately begins to look for flag sequences in the data link. An interrupt is generated when the first flag is detected.

Setting the terminate reception, TR, bit forces the RFDL to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration Register resets itself following a rising and a falling edge on the CLK input to the RFDL TSB after the write to this register has completed and the WRB signal becomes inactive. If the Configuration Register is read after this time, the TR bit value will be zero.

Register 05H, 45H: RFDL Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	INTC[1]
Bit 1	R/W	INTC[0]
Bit 0	R	INT

The interrupt control bits, INTC[1] and INTC[0], control interrupt generation as follows:

INTC[1]	INTC[0]	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

The interrupt bit, INT, reflects the status of the external interrupt unless the INTC[1] and INTC[0] bits are set to disable interrupts. If interrupts are disabled, the external interrupt output is forced to 0, but the INT bit of the Enable/Status Register reflects the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a FIFO overrun is cleared by reading the Status Register, by disabling the RFDL, or by setting TR high.

The contents of the Enable/Status Register should only be changed when the RFDL TSB is disabled (EN=0) to prevent any erroneous interrupt generation. When the DXPM is reset, the INTC[1] and INTC[0] bits are reset to 0; therefore, interrupt generation is disabled.

Register 06, 46H: RFDL Status

Bit	Type	Function
Bit 7	R	FE
Bit 6	R	OVR
Bit 5	R	FLG
Bit 4	R	EOM
Bit 3	R	CRC
Bit 2	R	NVB[2]
Bit 1	R	NVB[1]
Bit 0	R	NVB[0]

The NVB[2:0] bit positions indicate the number of valid bits in the Receive Data Register byte. It is possible that not all of the bits in the Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. A NVB[2:0] value of zero ("000") indicates that only the MSB in the register is valid. NVB[2:0] is only valid when the EOM bit is logic 1, the FLG bit is logic 1 and the OVR bit is logic 0.

The CRC bit is set to logic 1 if a CRC error was detected in the last received LAPD frame. The CRC bit is only valid when the EOM bit is logic 1, FLG is logic 1 and OVR is logic 0. On an interrupt generated from the detection of the first flag, reading the Status Register returns invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

The end of message bit (EOM) follows the EOM output. It is set when: the last byte in the LAPD frame (EOM) is being read from the Receive Data Register, an abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO, the first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO, or a FIFO overrun is detected. The EOM bit is passed through the FIFO with the data so that the status corresponds to the data just read from the FIFO.

The flag bit (FLG) is set to logic 1 if the RFDL has detected the presence of the LAPD flag sequence ("01111110") on the data link. FLG is reset to logic 0 only when the LAPD abort sequence ("01111111") is detected in the data or when the RFDL is disabled. This bit is passed through the FIFO with the data so that the status corresponds to the data just read from the FIFO. The reception of bit oriented codes

over the data link will also force an abort due to the eight ones pattern in the bit oriented codes.

The receiver overrun (OVR) bit is set to logic 1 when data overwrites unread data in the FIFO. The OVR bit is not reset until after the Status Register is read. While OVR is high, the RFDL and FIFO are held in the reset state, which causes the FLG and EOM bits in the Status Register to be reset as well.

The FIFO empty (FE) bit is logic 1 when the last FIFO entry is read and changes to logic 0 when the FIFO is loaded with new data.

If the Receive Data Register is read while there is no valid data in the FIFO, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status Register by forcing all bits to logic 0 on the first Status Register read immediately following the Received Data Register read which caused the underrun condition.

Register 07H, 47H:
RFDL Receive Data

Bit	Type	Function
Bit 7	R	RD[7]
Bit 6	R	RD[6]
Bit 5	R	RD[5]
Bit 4	R	RD[4]
Bit 3	R	RD[3]
Bit 2	R	RD[2]
Bit 1	R	RD[1]
Bit 0	R	RD[0]

This register is actually a 4-level FIFO buffer. RD[0] corresponds to the first bit of the serial byte received on the data link. If data is available, the FE bit in the Status Register is logic 0. If INTC[1:0] (in the Enable/Status Register) is set to "01", the Receive Data Register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to "11" the Receive Data Register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status Register is read. When the LAPD abort sequence ("01111111") is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial-to-parallel converter is written into the FIFO.

Reading the Receive Data Register increments the FIFO pointer at the end of the operation. If the Receive Data Register read causes a FIFO underrun, then the pointer is not incremented. The underrun condition is signalled in the next Status Register read by returning all zeros.

PMON Registers
Register 09H, 49H:
PMON Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	INTE
Bit 1	R	INT
Bit 0	R	OVR

This register enables an interrupt to be generated whenever counter data is transferred into the holding registers. This register also contains status information as to whether the holding registers have been overrun.

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt; a logic 0 bit in the INTE position disables the generation of an interrupt. When the DXPM is reset, the INTE bit is reset to 0, disabling the interrupt. The interrupt is cleared (acknowledged) by reading this register.

The INT bit is the current status of the interrupt signal; however, the INTE bit does not mask the INT bit. Regardless of whether interrupts are enabled or disabled, the INT bit retains its event capture function. A logic 1 in this bit position indicates that a transfer has occurred. A logic 0 indicates that no transfer has occurred.

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt was not acknowledged before the next transfer clock was issued and that the contents of the holding registers were overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Latching Performance Data

The Performance Monitor (PMON) data registers (0AH-0FH, 4AH-4FH) are updated by the rising edge of LCLK. The time between successive rising edges of LCLK determines the accumulation interval which is nominally one second. A single LCLK input serves both performance monitors in the DXPM. A microprocessor write to any of the PMON data registers also causes an update of the PMON data registers associated with that performance monitor in the DXPM. The PMON block is loaded with new performance data within 27 SCLK periods of the rising edge of

LCLK. With SCLK at its nominal frequency of 12.352 MHz, the PMON registers should not be read until 2.2 µsec have elapsed since the rising edge of LCLK. The data contained in the holding registers are subsequently read from the PMON registers by the microprocessor. The loading is synchronized to the internal event timing so that no events are missed.

Register 0AH, 4AH:
PMON Line Code Violation Event Count LSB

Bit	Type	Function
Bit 7	R	LCV7
Bit 6	R	LCV6
Bit 5	R	LCV5
Bit 4	R	LCV4
Bit 3	R	LCV3
Bit 2	R	LCV2
Bit 1	R	LCV1
Bit 0	R	LCV0

This register contains the eight least significant bits of the 12-bit line code violation event counter. The line code violation counter accumulates the number of line code violations (LCVs) in the received DS1 signal. When B8ZS line code is selected in the DREC Configuration Register, the bipolar violations occuring within error-free B8ZS signatures are not counted as line code violations.

Register 0BH, 4BH:
PMON Line Code Violation Event Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	LCV11
Bit 2	R	LCV10
Bit 1	R	LCV9
Bit 0	R	LCV8

This register contains the four most significant bits of the 12-bit line code violation event counter.

Register 0CH, 4CH: PMON Bit Error Event Count LSB

Bit	Type	Function
Bit 7	R	BEE7
Bit 6	R	BEE6
Bit 5	R	BEE5
Bit 4	R	BEE4
Bit 3	R	BEE3
Bit 2	R	BEE2
Bit 1	R	BEE1
Bit 0	R	BEE0

This register contains the eight least significant bits of the 9-bit bit error event counter. A bit error event is defined as a CRC-6 error in ESF, an F-bit error in SF, an F_T-bit error in SLC®96, and an F-bit or sync byte bit error (there can be up to 7 bits in error per frame) in T1DM.

Register 0DH, 4DH: PMON Bit Error Event Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R	BEE8

This register contains the most significant bit of the 9-bit bit error event counter.

Register 0EH, 4EH: PMON Framing Bit Error Event Count

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	FER4
Bit 3	R	FER3
Bit 2	R	FER2
Bit 1	R	FER1
Bit 0	R	FER0

This register contains the value of the 5-bit framing bit error event counter. A framing bit error event is defined as an F-bit error for SF and T1DM framing formats, an F_e-bit error for ESF framing format, and an F_T-bit error for SLC®96 framing format.

Register 0FH, 4FH: PMON OOF/COFA

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R	OOF2
Bit 1	R	OOF1
Bit 0	R	OOF0

This register contains the value of the 3-bit OOF/COFA event counter. When the CCOFA bit in the Master Configuration register is low, out-of-frame (OOF) events are accumulated. When the CCOFA bit in the Master Configuration register is high, change-of-frame-alignment (COFA) events are accumulated.

DREC Registers

Register 10H, 50H: DREC Configuration

Bit	Type	Function
Bit 7	R/W	AMI
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0		Unused

The AMI bit selects the line code of the incoming DS1 line. A logic 1 selects AMI (alternate mark inversion) line code; a logic 0 selects B8ZS (bipolar 8 zero substitution) line code.

Register 11H, 51H: DREC Interrupt Enable/Status

Bit	Type	Function
Bit 7	R/W	BPVE
Bit 6	R/W	LOSE
Bit 5	R/W	B8ZSE
Bit 4	R/W	Z8DE
Bit 3	R	BPVI
Bit 2	R	LOSI
Bit 1	R	B8ZSI
Bit 0	R	Z8DI

The bit positions BPVE, LOSE, B8ZSE and Z8DE (bits 7 to 4) of this register select which of the status events (bipolar line code violation, loss of signal, B8ZS signature or 8 zeros, respectively), either singly or in combination, will generate an interrupt when it is detected. A logic 1 bit in a bit position enables the detection of the corresponding signal to generate an interrupt; a logic 0 bit in a bit position disables the corresponding signal from generating an interrupt. Status events, line code violations, B8ZS signature detection and 8 zeros detection all generate an interrupt only on a rising edge of the signal (that is only when the event is detected). The loss of signal event generates an interrupt whenever the LOS output changes state.

When the DXPM is reset, BPVE, LOSE, B8ZSE and Z8DE are all reset to logic 0; therefore, interrupt generation is disabled.

The bit positions BPVI, LOSI, B8ZSI and Z8DI (bits 3 to 0) of this register indicate which of the status events generated an interrupt. A logic 1 in a bit position indicates that the corresponding event was detected and generated an interrupt; a logic 0 in a bit position indicates that no corresponding event was detected. The bit positions BPVI, B8ZSI and Z8DI are set on the rising edge of the corresponding output signal (i.e. upon declaration of the event). LOSI is set on any state transition of the LOS output. Bits BPVI, LOSI, B8ZSI and Z8DI are cleared by reading this register. Regardless of whether interrupts are enabled or disabled, the BPVI, LOSI, B8ZSI and Z8DI bits retain their event capture function.

Register 12H, 52H:
DREC Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R	LOS

The current state of the LOS output is reported in bit 0 of this register.

FRMR Registers

Register 14H, 54H: FRMR Configuration

Bit	Type	Function
Bit 7	R/W	M2O[1]
Bit 6	R/W	M2O[0]
Bit 5	R/W	ESFFA
Bit 4	R/W	ESF
Bit 3	R/W	FMS[1]
Bit 2	R/W	FMS[0]
Bit 1		Unused
Bit 0		Unused

The M2O[1:0] bits select the ratio of errored to total framing bits to declare the out-of-frame condition in SF, SLC®96 and ESF framing formats. In T1DM framing format, the ratio of errored to total framing bits to declare the out-of-frame condition is always 4 of 12 bits in error.

The following table summarizes the out-of-frame declaration modes:

M2O[1]	M2O[0]	Description
0	0	2 of 4 bits in error
0	1	2 of 5 bits in error
1	0	2 of 6 bits in error
1	1	Locked-in-frame mode; ignores framing errors

The "locked-in-frame" mode prevents the declaration of the out-of-frame condition regardless of the number of detected framing errors.

The ESF framing algorithm bit, ESFFA, selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR TSB does not assert INF while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either standard superframe, T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF framing format; a logic 0 bit enables FMS[1] and FMS[0] to select SF, T1DM or SLC®96 framing format.

The framing mode select bits, FMS[1] and FMS[0], select standard superframe, T1DM, or SLC®96 framing formats. Logic "00" in these bit positions enables the SF framing format; logic "01" or "11" in these bit positions enables the T1DM framing format; logic "10" in these bit positions enables the SLC®96 framing format.

When ESF is selected (ESF bit set to logic 1), the FMS[1] and FMS[0] bits select the data rate and the source channel for the facility data link. Logic "00" in these bits enables the FRMR to receive FDL data at the full 4 kbit/s rate from every odd frame. Logic "01" in these bits enables the FRMR to receive FDL data at a 2 kbit/s rate from frames 3, 7, 11, 15, 19 and 23. Logic "10" in these bits enable the FRMR to receive FDL data at a 2 kbit/s rate from frames 1, 5, 9, 13, 17 and 21. Logic value "11" is unassigned and currently configures the FRMR to default to the full 4 kbit/s data rate.

The valid combinations of the ESFFA, ESF, FMS1 and FMS0 bits are summarized in the table below:

ESFFA	ESF	FMS1	FMS0	Mode
X	0	0	0	SF framing format
X	0	0	1	T1DM framing format
X	0	1	0	SLC®96 framing format
X	0	1	1	T1DM framing format
X	1	0	0	ESF framing format & 4 kbit/s FDL data rate
0	1	0	1	ESF framing format & 2 kbit/s FDL data rate using frames 3, 7, 11, 15, 19, 23 (required combination for ZBTSI)
X	1	1	0	ESF framing format & 2 kbit/s FDL data rate using frames 1, 5, 9, 13, 17, 21
X	1	1	1	ESF framing format & 4 kbit/s FDL data rate

Register 15H, 55H:
FRMR Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6	R/W	ACCEL
Bit 5	R/W	COFAE
Bit 4	R/W	FERE
Bit 3	R/W	BEEE
Bit 2	R/W	SEFE
Bit 1	R/W	MFPE
Bit 0	R/W	INFE

This register selects which of the COFA (change of frame alignment), FER (framing bit error), BEE (bit error), SEF (severely errored frame), MFP (mimic framing pattern) or INF (in frame) events generates an interrupt when their state changes or their event condition is detected. A logic 1 in the MFPE or INFE bit positions enables a transition of the corresponding MFP or INF output to generate an interrupt; a logic 0 in the bit positions disables transition generated interrupts. A logic 1 in the COFAE, FERE, BEEE or SEFE enable bit positions enables the detection of the corresponding event to generate an interrupt; a logic 0 in the bit positions disables the detection of the corresponding event from generating an interrupt. When the PM is reset, all bit positions are set to 0; therefore, interrupt generation is disabled.

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

Register 16H, 56H:
FRMR Interrupt Status

Bit	Type	Function
Bit 7	R	COFAI
Bit 6	R	FERI
Bit 5	R	BEEI
Bit 4	R	SEFI
Bit 3	R	MFPI
Bit 2	R	INFI
Bit 1	R	MFP
Bit 0	R	INF

This register indicates which of the COFA, FER, BEE or SEF events generated an interrupt, or indicates which of the MFP or INF signals generated an interrupt when its state changed. A logic 1 in the status bit positions COFAI, FERI, BEEI and SEFI indicate that the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI and SEFI indicate that the corresponding event did not generate an interrupt. A logic 1 in the status bit positions MFPI and INFI indicates that a state change on the corresponding output generated an interrupt; a logic 0 in the status bit positions MFPI and INFI indicates that no change in the state of the corresponding output occurred. The bit positions MFP and INF indicate the current state of the corresponding outputs.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SEFI, MFPI and INFI) are cleared to logic 0 when this register is read. Regardless of whether interrupts are enabled or disabled, the COFAI, FERI, BEEI, SEFI, MFPI and INFI bits retain their event capture function.

ALMI Registers

Register 18H, 58H: ALMI Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	ESF
Bit 3	R/W	FMS[1]
Bit 2	R/W	FMS[0]
Bit 1		Unused
Bit 0		Unused

This register allows selection of the framing format and the data rate of the facility data link in ESF to allow operation of the carrier failure alarm (CFA) detection algorithms.

The ESF bit selects either extended superframe format or enables the frame mode select bits (FMS1 and FMS0) to select either regular superframe, T1DM, "alternate" T1DM or SLC®96 framing format. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, "alternate" T1DM, or SLC®96.

The FMS1 and FMS0 bits select standard superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. Logic "00" in these bits enables the SF framing format; logic "01" in these bit positions enables the T1DM framing format; logic "10" in these bit positions enables the SLC®96 framing format; and logic "11" in these bit positions enables the "alternate" T1DM framing format. The "alternate" T1DM framing format configures the Red alarm block to process the out-of-frame condition as if the SF, SLC®96 or ESF framing format were selected; the Yellow alarm is still processed as T1DM.

When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the Facility Data Link. Logic "00" in these bits enables the ALMI to receive FDL data and validate the Yellow alarm at the full 4 kbit/s rate. Logic "01" or "10" in these bits enables the ALMI to receive FDL data and validate the Yellow alarm at the 2 kbit/s rate.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

ESF	FMS[1]	FMS[0]	Mode
0	0	0	Superframe framing format
0	0	1	T1DM framing format
0	1	0	SLC®96 framing format
0	1	1	"Alternate" T1DM mode
1	0	0	ESF framing format & 4 kbit/s FDL data rate
1	0	1	ESF framing format & 2 kbit/s FDL data rate
1	1	0	ESF framing format & 2 kbit/s FDL data rate
1	1	1	ESF framing format & default to 4 kbit/s FDL data rate

Register 19H, 59H:
ALMI Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	FASTD
Bit 3	R/W	ACCEL
Bit 2	R/W	YELE
Bit 1	R/W	REDE
Bit 0	R/W	AISE

This register selects which of the three CFAs can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

A logic 1 in the enable bit positions (YELE, REDE and AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state change in the corresponding CFA from generating an interrupt. The enable bits are independent; any combination of Yellow, Red and AIS CFAs can be enabled to generate an interrupt. When the DXPM is reset, YELE, REDE and AISE are all set to logic 0; therefore, interrupt generation by these alarms is disabled.

The FASTD bit enables the "fast" deassertion of the RED and AIS alarms. If FASTD is a logic 1, deassertion of RED alarm for SF, SLC®96, alternate T1DM and ESF modes occurs within 120 ms of going in-frame. Fast deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in-frame. If FASTD is a logic 0, deassertion of RED alarm occurs after 2.55 s in SF,

SLC®96, alternate T1DM and ESF modes and after 100 ms in T1DM mode. If FASTD is a logic 0, deassertion of AIS alarm occurs after 16.8 s.

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

Register 1AH, 5AH:
ALMI Interrupt Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R	YELI
Bit 4	R	REDI
Bit 3	R	AISI
Bit 2	R	YEL
Bit 1	R	RED
Bit 0	R	AIS

This register indicates which of the three CFAs generated an interrupt (bits 5 to 3) and indicates the current state of each CFA (bits 2 to 0). A logic 1 in the interrupt status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change occurred. Both the status bit positions (bits 5 through 3) and the interrupt are cleared to logic 0 when this register is read. Regardless of whether interrupts are enabled or disabled, the YELI, REDI and AISI bits retain their event capture function.

RBOC Registers

Register 20H, 60H: RBOC Configuration/Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	AVC
Bit 0	R/W	INTE

This register selects the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt at code validation.

The AVC bit position selects the validation criterion used in determining a valid BOC. A logic 0 selects the 8 out of 10 matching BOC criterion; a logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs.

The INTE bit position enables or disables the generation of an interrupt when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation. When the DXPM is reset, INTE is reset to logic 0; therefore, interrupt generation is disabled.

Register 21H, 61H: RBOC Interrupt Status

Bit	Type	Function
Bit 7		Unused
Bit 6	R	BOCI
Bit 5	R	BOC[5]
Bit 4	R	BOC[4]
Bit 3	R	BOC[3]
Bit 2	R	BOC[2]
Bit 1	R	BOC[1]
Bit 0	R	BOC[0]

This register indicates whether an interrupt was generated by a detection of a valid BOC and indicates the current state value of the BOC[5:0] bits. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0

in the BOCI bit position indicates that no BOC has been detected. Since the bit oriented code "111111" is not recognized by the RBOC, the BOC[5:0] bits are set to all ones ("111111") if no valid code has been detected. The BOCI bit position and the interrupt are cleared to logic 0 when this register is read.

PDVD Register

Register 23H, 63H: PDVD Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	PDV
Bit 3	R	Z16DI
Bit 2	R	PDVI
Bit 1	R/W	Z16DE
Bit 0	R/W	PDVE

This register indicates the current state of the PDV output, selects which events can generate interrupts and identifies the source of the pending interrupt. The PDV bit indicates the current state of the pulse density violation detect (PDV) output.

The PDVE bit is an interrupt enable bit. When the PDVE bit is set to logic 1, an interrupt is generated whenever the state of the PDV output changes. When the PDVE bit is logic 0, interrupt generation by changes in the state of PDV is disabled. When the Z16DE interrupt enable bit is set to logic 1, an interrupt is generated when the Z16D output goes high. When the Z16DE bit is logic 0, interrupt generation by Z16D is disabled.

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 if a change in the state of the PDV output generated an interrupt. Z16DI is a logic 1 whenever the Z16D output goes high. PDVI and Z16DI are cleared to 0 when this register is read. Regardless of whether interrupts are enabled or disabled, the PDVI and Z16DI bits retain their event capture function.

RZBT Register

Register 24H, 64H: RZBT Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R/W	ZBTSI

This register enables and disables ZBTSI decoding. ZBTSI decoding is disabled when the ZBTSI bit is cleared. When the RZBT block is disabled, PCM data is clocked through to the DPCM output unmodified, but the data is delayed by the same amount as the ZBTSI decoding delay. ZBTSI decoding is enabled when the ZBTSI bit is set and the performance monitor is in-frame.

RSLC Register

Register 27H, 67H: RSLC Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R	LV
Bit 4	R	SQ
Bit 3	R	LVI
Bit 2	R	SQI
Bit 1	R/W	LVE
Bit 0	R/W	SQE

This register indicates the current state of the alarm outputs, selects which alarms can generate interrupts and identifies the source of the pending interrupt. The LV and SQ bits reflect the current state of the the low level alarm and the squelch alarm. The LVE bit and the SQE bit are interrupt enables for the low level signal alarm and squelch alarm, respectively. The LVI and SQI bits indicate whether the low level alarm or the squelch alarm generated the interrupt. These bits and the interrupt are cleared when this register is read. Regardless of whether interrupts are enabled or disabled, the LVI and SQI bits retain their event capture function.

TEST FEATURES DESCRIPTION

The DXPM may be placed into a tri-state test mode in which all of the DXPM outputs, including the data bus, are held in a high impedance state. The DXPM tri-state mode is active while RDB and WRB are held low (normally an illegal combination of input states).

Test mode registers are used to apply test vectors during production test of the DXPM. Test mode registers (as opposed to normal mode registers) are selected when TRSB is low.

Test mode 0 provides access to the values on the DXPM's primary inputs and control of the primary outputs. Test mode 0 can be used to facilitate board level testing. Test modes other than those described in this section are reserved for production test to verify the internal circuitry of the device.

For further information on testability features, refer to the PMC "Telecom System Block User's Manual".

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 01H:
Test Mode Select

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	W	DBCTRL
Bit 2	W	IOTST
Bit 1	W	HIZDATA
Bit 0	W	HIZIO

This register is used to select DXPM test features. All bits are reset to zero by a hardware reset of the DXPM; a software reset of either PM in the DXPM does not affect the state of the bits in this register.

The IOTST bit is used to allow normal microprocessor access to the test registers in each block in the DXPM. When IOTST is a logic 1, all blocks are held in test mode (i.e. the TSTB line to each block is asserted internally) and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the chip (refer to the section "Test Mode 0" for details). When IOTST is a logic 0, the timing and signals associated with test mode 0 are not compatible with normal microprocessor bus cycles.

The HIZIO and HIZDATA bits control the tri-state modes of the DXPM. While the HIZIO bit is a logic 1, all output pins in the DXPM are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the

data bus is also held in a high-impedance state which inhibits microprocessor read cycles. These bits may be used to facilitate board level testing.

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the DXPM to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads during production test.

Test Mode 0

In test mode 0, the DXPM allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the TSTB and TRSB inputs must be set low (the IOTST bit in the Test Mode Select Register may be set to logic 1 in lieu of the TSTB line being asserted) and the following addresses must be written with 00H: 05H, 09H, 11H, 15H, 19H, 21H, 23H, 25H, 27H, 45H, 49H, 51H, 55H, 59H, 61H, 63H, 65H, 67H.

Reading the following address locations returns the values for the indicated inputs :

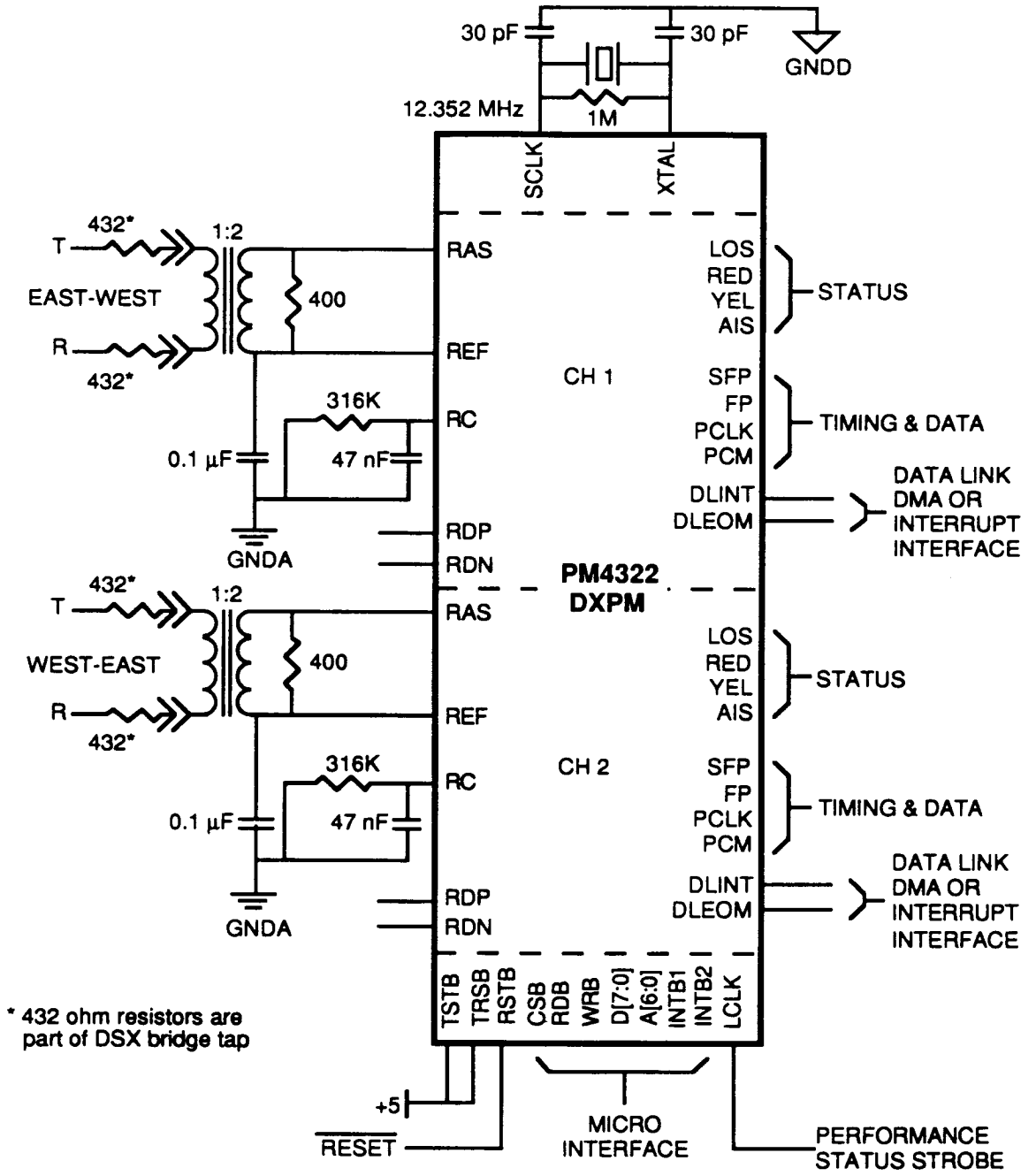
PM-1	PM-2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08H	48H				LCLK				
10H	50H						SCLK	RDN	RDP

Writing the following address locations forces the outputs to the value in the corresponding bit position:

PM-1	PM-2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04H	44H							DLEOM	DLINT
08H	48H								PMONI†
10H	50H		DRECI†			LOS			PCLK
14H	54H	SFP				FP			
16H	56H		FRMRI†	DLSIG	DLCLK				
18H	58H					YEL	RED	AIS	ALMII†
20H	60H		RBOCI†						
22H	62H						PDVDI†		
24H	64H								PCM
26H	66H								RSLCI†

†Note: the active high block interrupt lines (PMONI, DRECI, FRMRI, ALMII, RBOCI, PDVDI and RSLCI) may be masked by the Master Interrupt Enable Register and thus not assert the active low INTB output. Any of the unmasked block interrupt signals can assert the INTB output.

TYPICAL APPLICATION



FUNCTIONAL TIMING

Clock and Data Recovery

Fig. 3 Clock Recovery

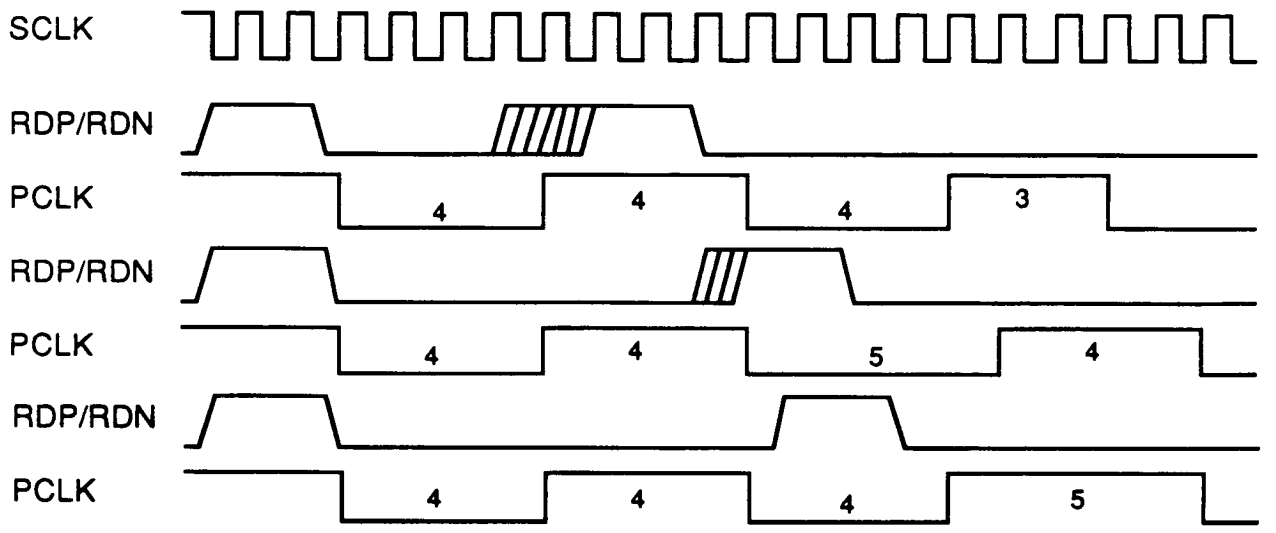


Figure 3 shows the recovery of the PCM clock, PCLK, by the DREC block. The nominal period of PCLK is 8 SCLK cycles but the period may be from 7 to 9 SCLK cycles. The early arrival of an RDP/RDN pulse causes the instantaneous frequency of PCLK to increase as shown in the first PCLK trace (note that PCLK may be high for three SCLK cycles but it may not be low for three SCLK cycles). The late arrival of an RDP/RDN pulse causes the instantaneous frequency of PCLK to decrease as shown in the second and third PCLK traces (note that PCLK may be either high or low for five SCLK cycles).

Frame Alignment

Fig. 4 Frame Alignment

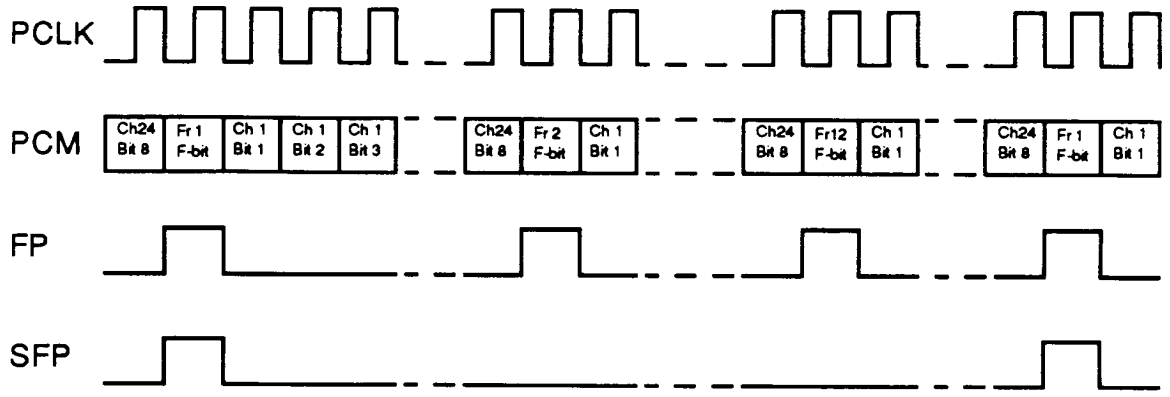


Figure 4 shows the relationship between the PCM clock (PCLK), the PCM data (PCM) and the framing pulses (FP and SFP) for the case where there are twelve frames per superframe (SF, SLC®96 and T1DM framing format). For the case where there are twenty-four frames per superframe (ESF framing format), the SFP pulse occurs every twenty-four frames (during the first bit of frame one) instead of every twelve frames.

Yellow Alarm

Fig. 5 Yellow Alarm Assertion

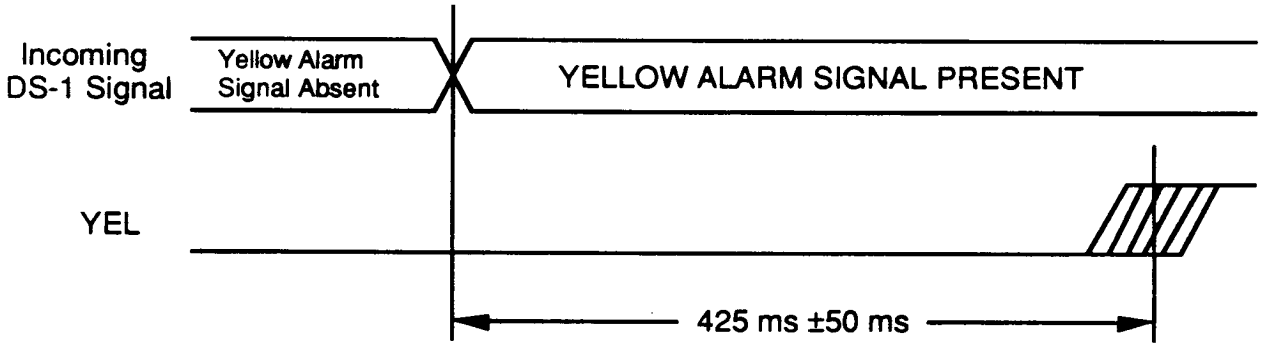


Figure 5 illustrates the assertion of the YEL output following the detection of an incoming Yellow Alarm signal. In SF and SLC®96 framing formats, the Yellow Alarm signal is transmitted by forcing bit 2 of every channel to zero. In T1DM framing format, the Yellow Alarm state is indicated by the Y-bit in the T1DM sync byte located in channel 24 of every frame. Yellow alarm is transmitted by setting the Y-bit to zero. In ESF framing format, Yellow Alarm is transmitted in the facility data

link (DL bits). An alternating pattern of eight ones followed by eight zeros is transmitted to indicate the Yellow Alarm condition.

Fig. 6 Yellow Alarm Deassertion

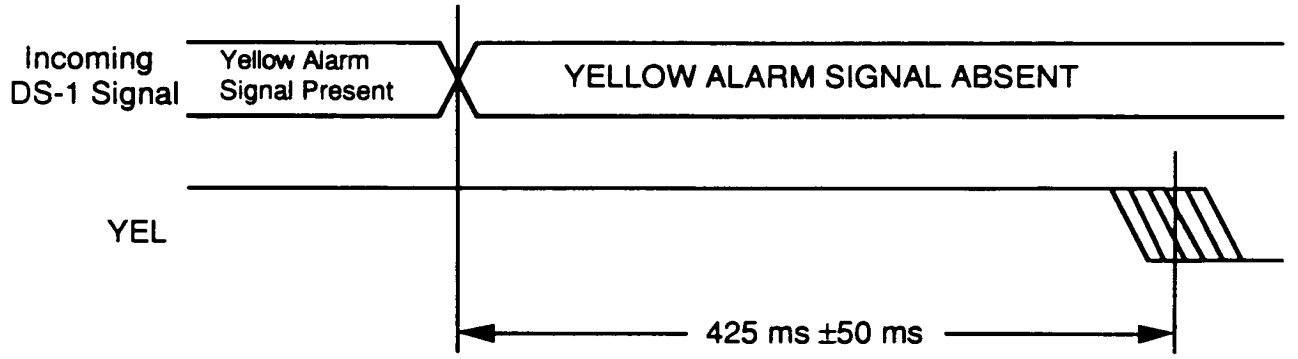


Figure 6 illustrates the deassertion of the YEL output following the detection of the lack of the Yellow Alarm signal in the input data data stream.

Red Alarm

Fig. 7 Red Alarm Assertion

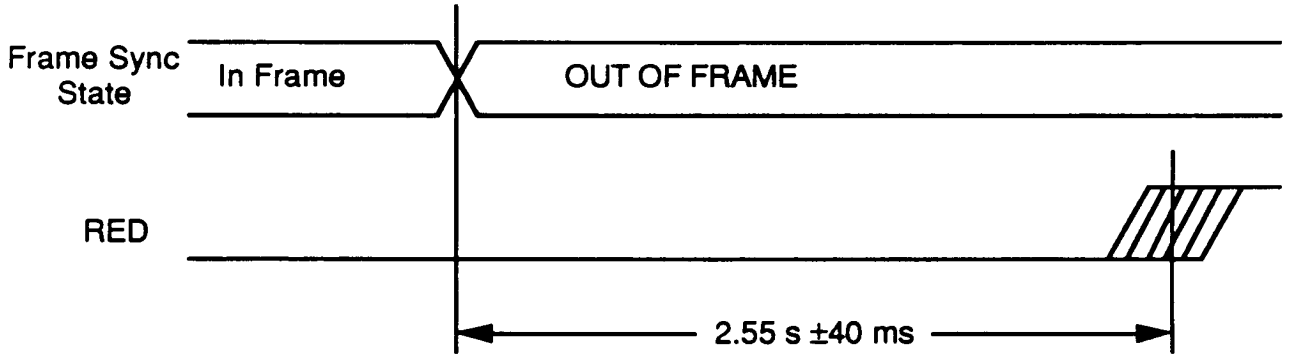


Figure 7 shows the assertion of the RED output following the out-of-frame.

Fig. 8 Red Alarm Deassertion

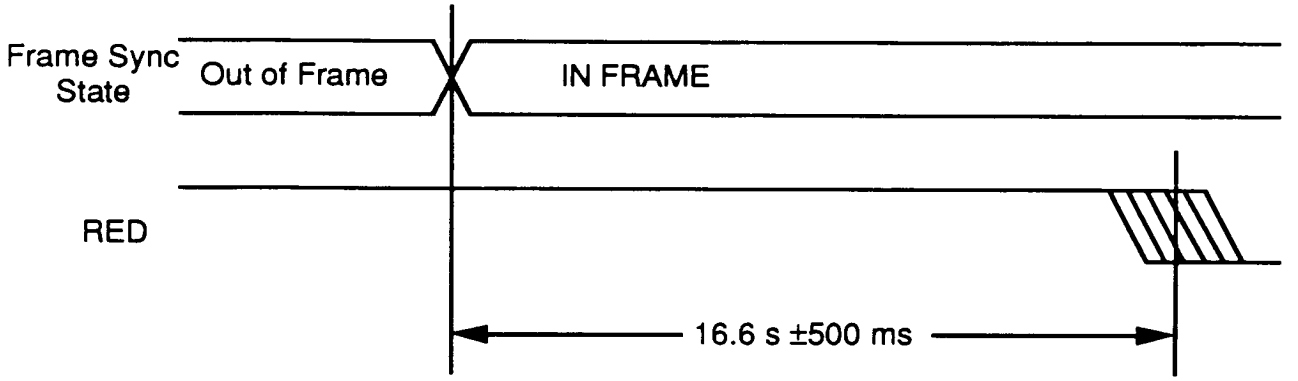


Figure 8 shows the deassertion of the RED output following frame synchronization.

Fig. 9 Red Alarm "Fast" Deassertion

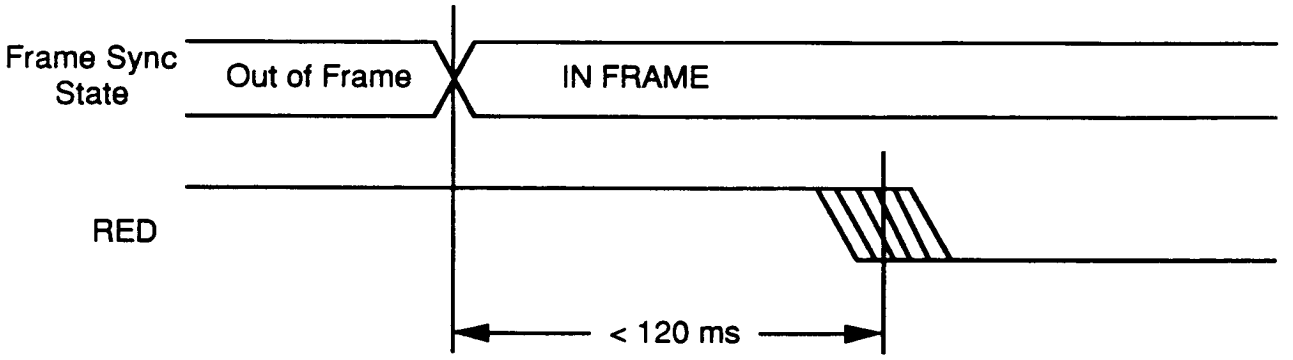


Figure 9 shows the "fast" deassertion of the RED output following frame synchronization. Fast deassertion mode is enabled by setting the FASTD bit of the ALMI Interrupt Enable Register to logic 1.

Alarm Indication Signal

Fig. 10 AIS Assertion

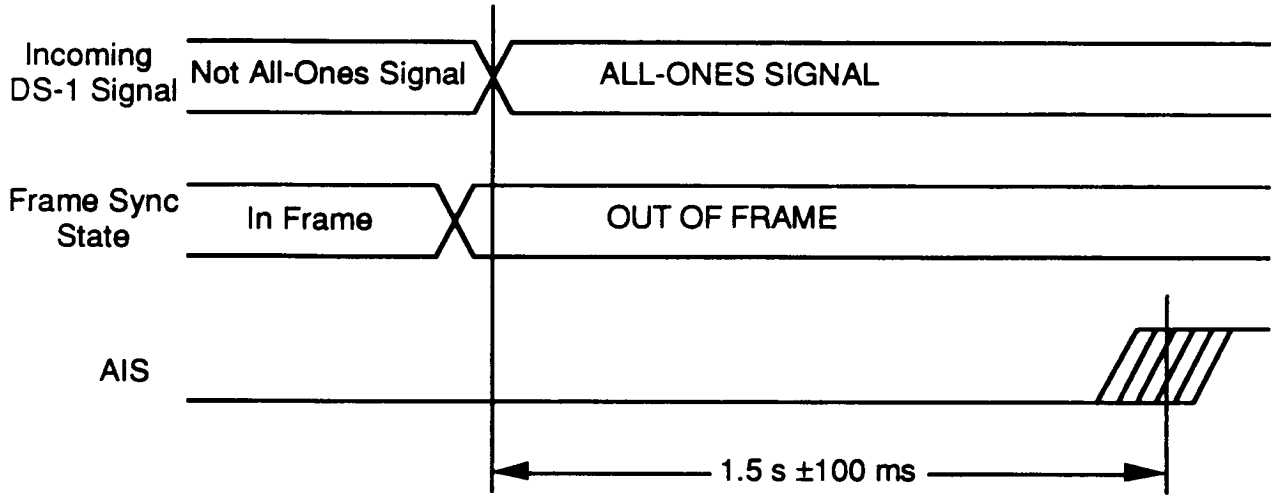


Figure 10 shows the assertion of the AIS output following the out-of-frame synchronization and the detection of the all-ones signal on the input.

Fig. 11 AIS Deassertion (Frame Synchronization)

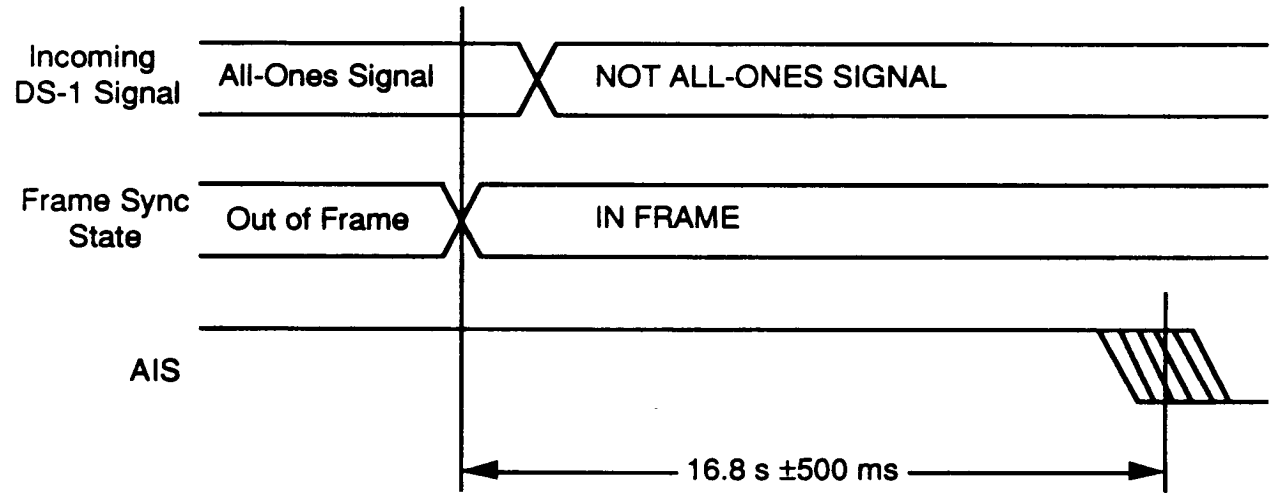


Figure 11 shows the deassertion of the AIS output following frame synchronization.

Fig. 12 AIS "Fast" Deassertion (Frame Synchronization)

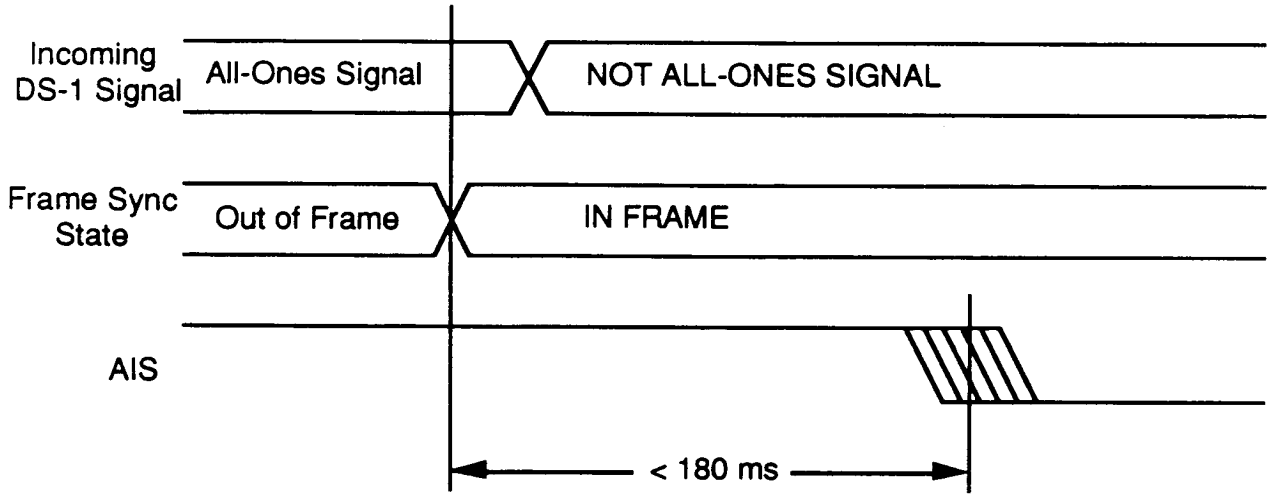


Figure 12 shows the "fast" deassertion of the AIS output following frame synchronization. Fast deassertion mode is enabled by setting the FASTD bit of the ALMI Interrupt Enable Register to logic 1.

Fig. 13 AIS Deassertion (All-Ones Signal)

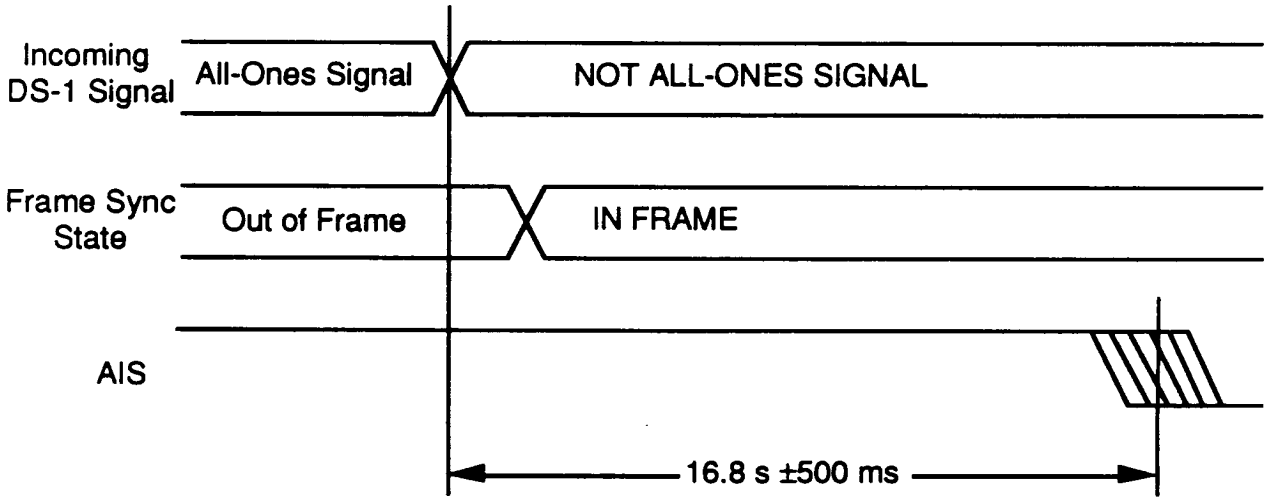


Figure 13 shows the deassertion of the AIS output after the all-ones signal has not existed on the input data.

Fig. 14 AIS "Fast" Deassertion (All-Ones Signal)

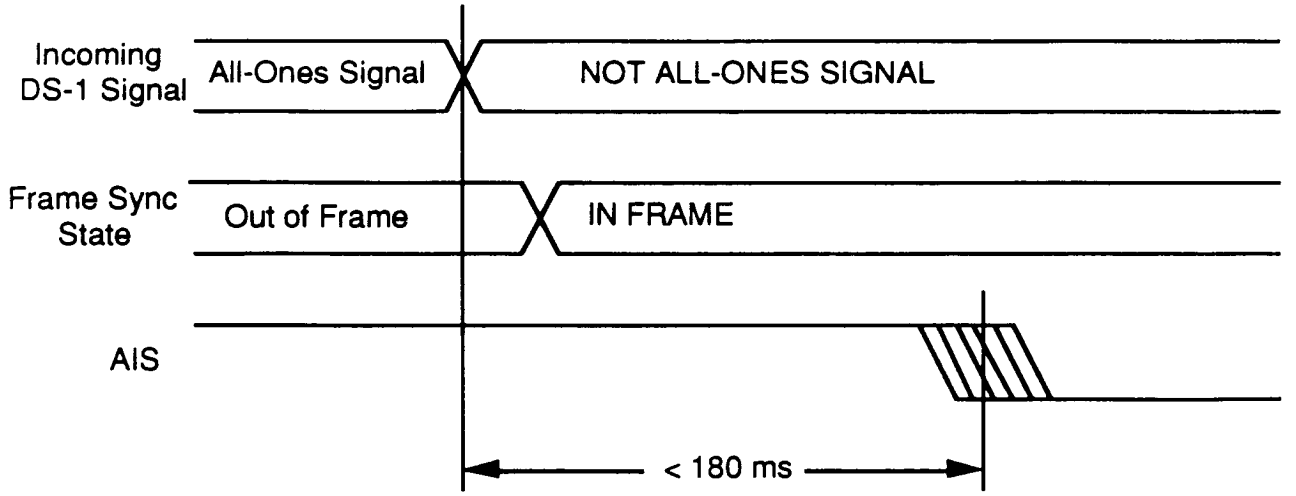
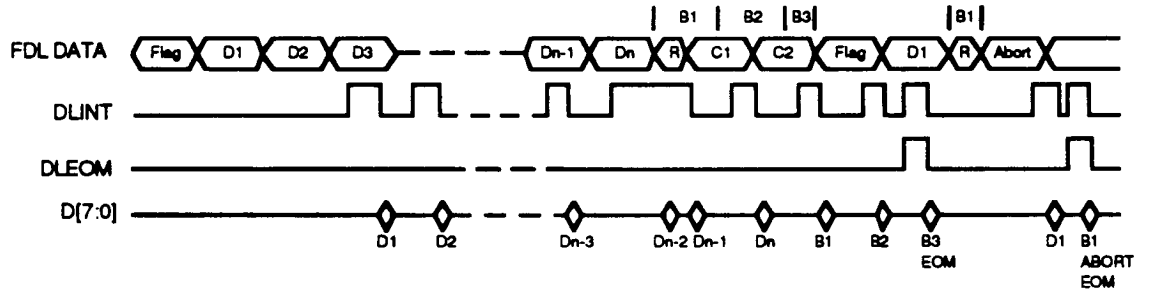


Figure 14 shows the deassertion of the AIS output after the all-ones signal has not existed on the input data. Fast deassertion mode is enabled by setting the FASTD bit of the ALMI Interrupt Enable Register to logic 1.

HDLC Interface

Fig. 15 Normal Data and Abort Sequence



The Normal Data and Abort Sequence timing diagram (Fig. 15) shows the relationship between the facility data link and the DLINT and DLEOM outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO. The RFDL block is assumed to be operating in the interrupt driven mode. Each read shown is composed of two reads, first a read of the RFDL Receive Data Register followed by a read of the RFDL Status Register. The data register reads clear the DLINT output if no more data exists in the FIFO. The state of the FE bit returned from the status register indicates the FIFO fill status as well. The data register read Dn-2 is shown to occur after two bytes have been written into the FIFO. The DLINT output is not cleared after the first data read because a data byte still

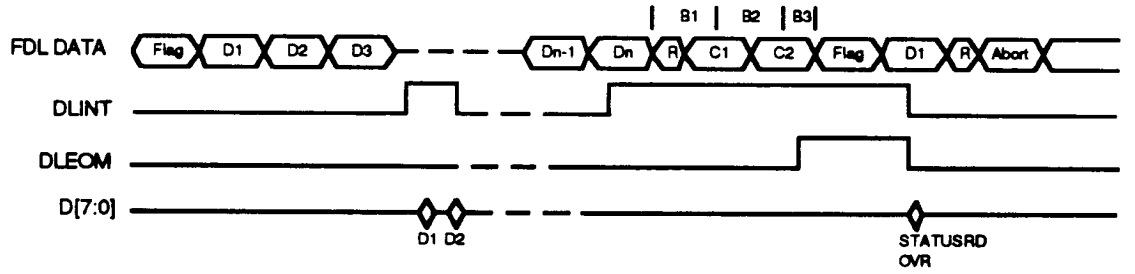
remains to be read. The DLINT output is cleared after data register read Dn-1. The FE bit will be 0 in status register read Dn-2 and 1 in status register read Dn-1.

The DLEOM signal is asserted as soon as the last byte in the frame is read from the RFDL Receive Data Register. The DLINT output is cleared if the FIFO is empty. The following status register read returns EOM = 1, FLG = 1 and causes the DLEOM output to return to zero.

In the next frame, the first data byte is received and after a delay of 10 bit periods, it is written to the FIFO. After the interrupt the byte is read by the processor. When the ABORT sequence is detected, the data received up to the abort is written to the FIFO and an interrupt generated. The processor then reads the partial byte from the received data register and the DLEOM output is asserted. The processor then reads the status register which returns EOM = 1, FLG = 0 and clears the DLEOM output. The FIFO is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

After an abort, the RFDL state machine is in the receiving all ones state and the data link is in the inactive state. When the first flag is detected, a new interrupt is generated with a dummy data byte loaded into the FIFO to indicate that the data link is active.

Fig. 16 FIFO Overrun



The FIFO Overrun timing diagram (Fig. 16) shows the relationship between the facility data link and the DLINT and DLEOM outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO. Each read is composed of two reads as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets DLEOM high and resets both the RFDL and FIFO. The RFDL is held disabled until the RFDL Status Register is read. The start flag sequence is not detected since the RFDL is still disabled when it occurs. Consequently, the RFDL ignores the entire frame including the abort sequence (since it did not occur in a valid frame nor during flag reception according to the RFDL).

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +85°C
Storage Temperature	-40°C to +125°C
Voltage on V_{DD} with Respect to GND	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to +6.0V
Static Discharge Voltage	2000 V
Latch-Up Current (T_A = 0°C to +85°C)	400 mA

DC CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0	V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{RAS}	Analog Input Voltage	A_{VS} - 0.6	A_{VD} + 0.6	Volts	
V_{REF}	Analog Reference Voltage	1.5	1.9	Volts	REF Unloaded
V_{OL}	Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, Note 3
V_T	Reset Input High Voltage	2.3	2.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage	0.5	1.2	Volts	
I_{ILPU}	Input Low Current	-26	-110	µA	$V_{IL} \leq 1.65$ V, Notes 1, 3
I_{IHPU}	Input High Current	-48	-110	µA	$V_{IH} \geq 3.85$ V, Notes 1, 3
I_{IL}	Input Low Current	-10	0	µA	$V_{IL} \leq 1.65$ V, Notes 2, 3
I_{IH}	Input High Current	-10	10	µA	$V_{IH} \geq 3.85$ V, Notes 2, 3

Symbol	Parameter	Min	Max	Unit	Conditions
I_{DDOP1}	Active Current		46	mA	V_{DD}=5.5V, Outputs Unloaded, Path Monitoring Enabled, Line Monitoring Enabled, at TSB Nominal Operating Frequencies, Note 4
I_{DDOP2}	Active Current		16	mA	V_{DD}=5.5V, Outputs Unloaded, Path Monitoring Disabled, Line Monitoring Enabled, at TSB Nominal Operating Frequencies, Note 4
I_{DDOP3}	Active Current		8	mA	V_{DD}=5.5V, Outputs Unloaded, Path and Line Monitoring Disabled, at TSB Nominal Operating Frequencies, Note 4
I_{DDSB}	Idle Current		100	µA	V_{DD}=5.5 V, A_{VD}=0 V, Outputs Unloaded, Device Unclocked
I_{ADOP}	Active Current		30	mA	A_{VD}=5.5 V, V_{DD}=5.5V, Outputs Unloaded, All Ones Signal
I_{ADSB}	Idle Current		30	mA	A_{VD}=5.5 V, V_{DD}=5.5 V, Outputs Unloaded, Device Unclocked

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. I_{DDOP} can increase by 1 mA maximum with external crystal.

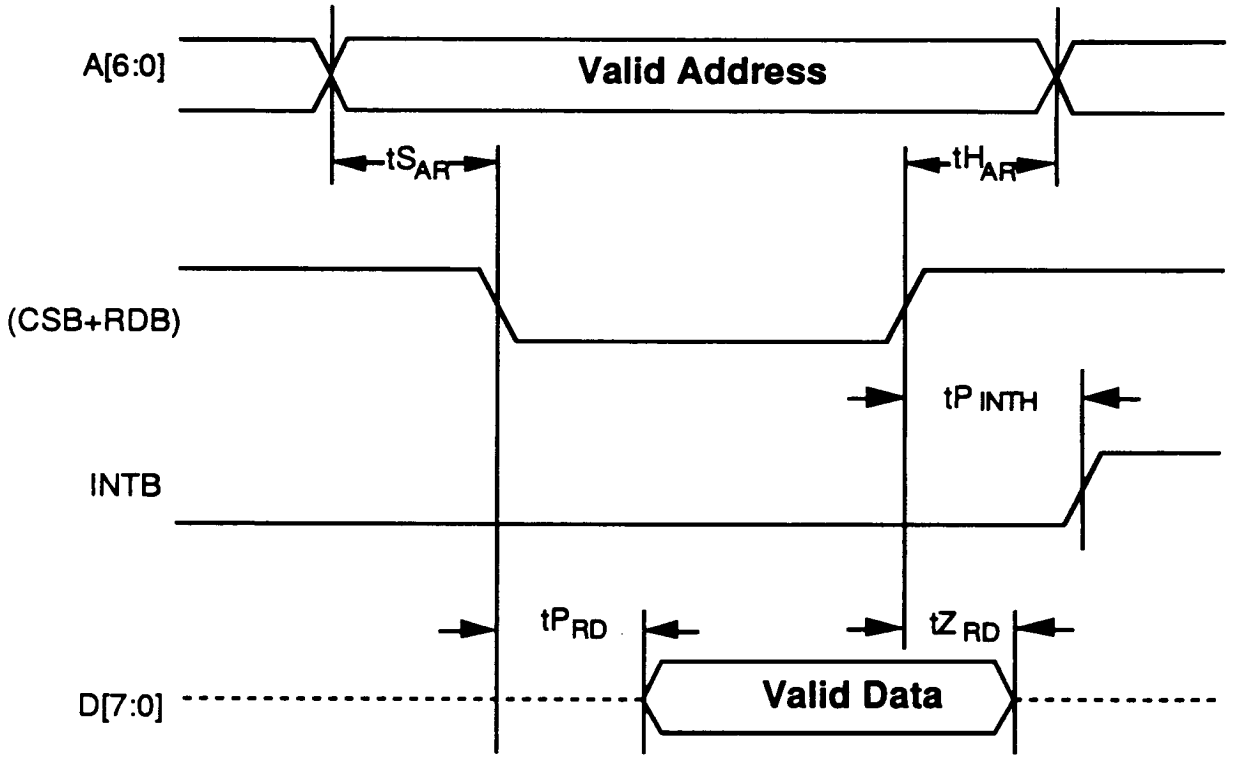
MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

Microprocessor Read Access (Fig. 17)

Symbol	Parameter Min	Max	Units	
tS_{AR}	Address to Valid Read Set-up Time	20		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		100	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		40	ns
tP_{INTH}	Valid Read Deasserted to Interrupt Deasserted		100	ns

Fig. 17 Microprocessor Read Access Timing



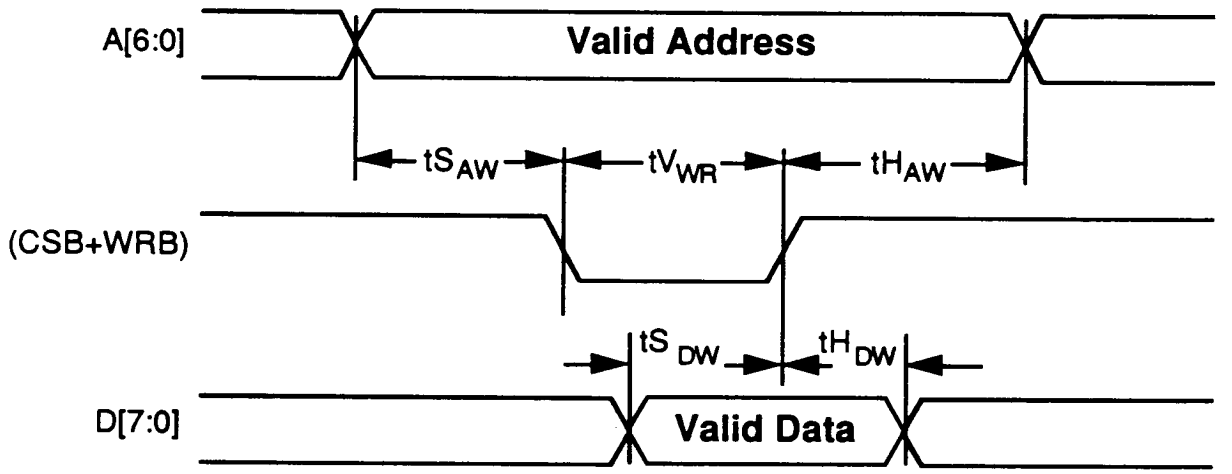
Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the microprocessor data bus, (D[7:0]).
3. A valid read cycle is defined as the logical OR of the CSB and the RDB signals.
4. Microprocessor timing applies to normal mode register accesses only.

Microprocessor Write Access (Fig. 18)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	20		ns
tS_{DW}	Data to Valid Write Set-up Time	40		ns
tH_{DW}	Data to Valid Write Hold Time	40		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 18 Microprocessor Write Access Timing



Notes on Microprocessor Write Timing:

1. A valid write cycle is defined as the logical OR of the CSB and the WRB signals.
2. Microprocessor timing applies to normal mode register accesses only.

DXPM TIMING CHARACTERISTICS

(T_A = 0° to +85°C, V_{DD} = 5 V ±10%)

Input Timing (Fig. 19 & 20)

Symbol	Description	Min	Max	Units
	SCLK Frequency (typically 12.352 MHz)	12.350	12.354	MHz
	SCLK duty cycle	30	70	%
tP_{AIN}	RAS analog input pulse width	300	405	ns
tP_{DIN}	RDP/RDN digital input pulse width	100		ns

Fig. 19 Analog Input Timing

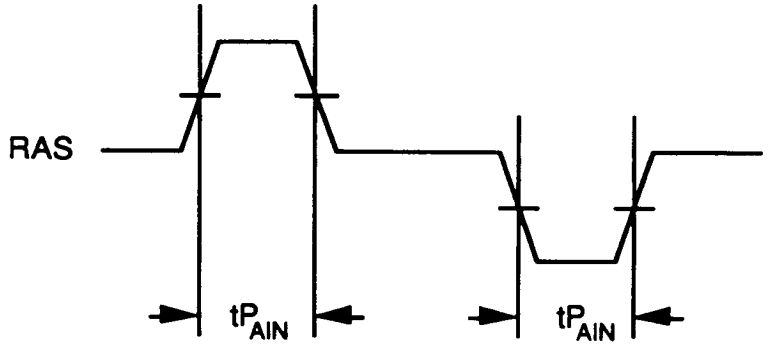
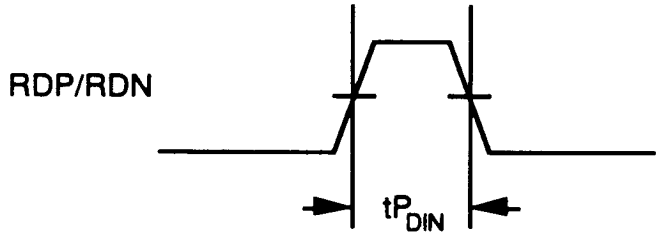


Fig. 20 Digital Input Timing



Output Timing (Fig. 21, 22, 23, 24 & 25)

Symbol	Description	Min	Max	Units
tP_{PCLK}	PCLK propagation delay		60	ns
tP_{PCM}	PCM propagation delay		25	ns
tP_{FP}	FP propagation delay		60	ns
tP_{SFP}	SFP propagation delay		60	ns
tP_{RED}	RED propagation delay		70	ns
tP_{YEL}	YEL propagation delay		70	ns
tP_{AIS}	AIS propagation delay		70	ns
tP_{INTB}	INTB propagation delay		100	ns
tP_{DLSIG}	DLSIG propagation delay		30	ns
tP_{DLINT}	DLINT assertion propagation delay		100	ns
tP_{DLINTL}	DLINT negation from RDB assertion		70	ns
tP_{DLEOM}	DLEOM assertion from PCLK delay		70	ns
tP_{DLEOMH}	DLEOM assertion (Data Register read)		70	ns
$tP_{RHDLEOM}$	DLEOM negation (Status Register read)		45	ns
$tP_{RLDLEOM}$	DLEOM negation (OVR Status Register read)		70	ns

Fig. 21 SCLK Timing

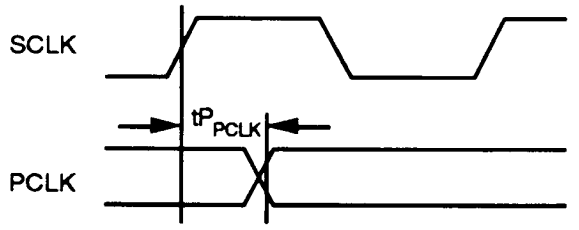


Fig. 22 PCLK Timing

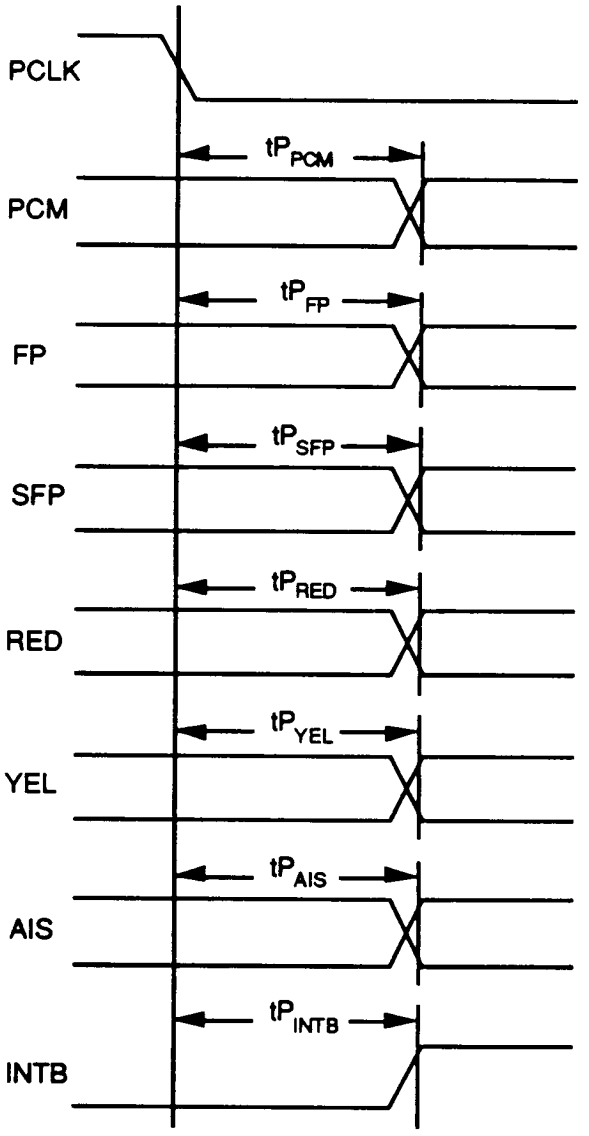


Fig. 23 Data Link Clock and Signal Timing

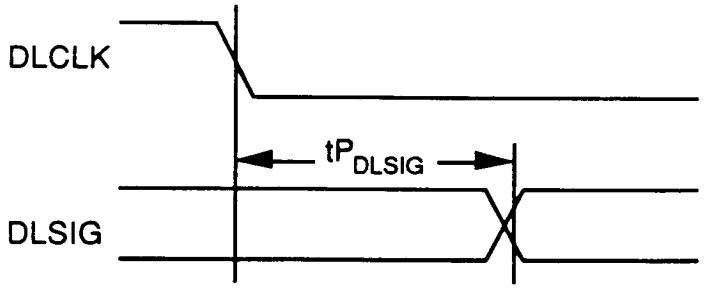


Fig. 24 HDLC Receiver PCLK Associated Timing

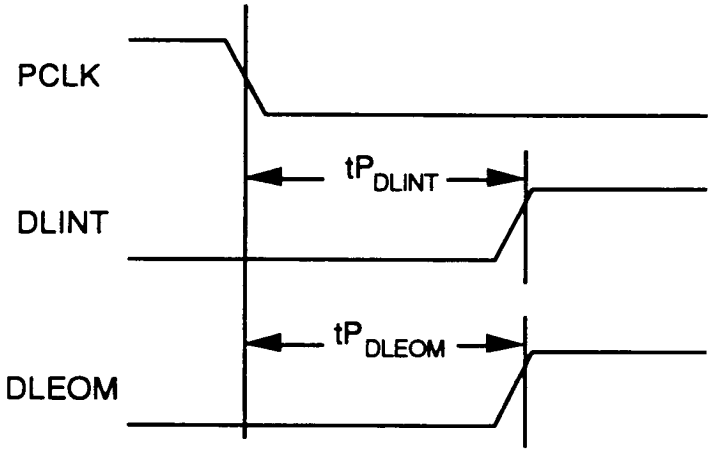
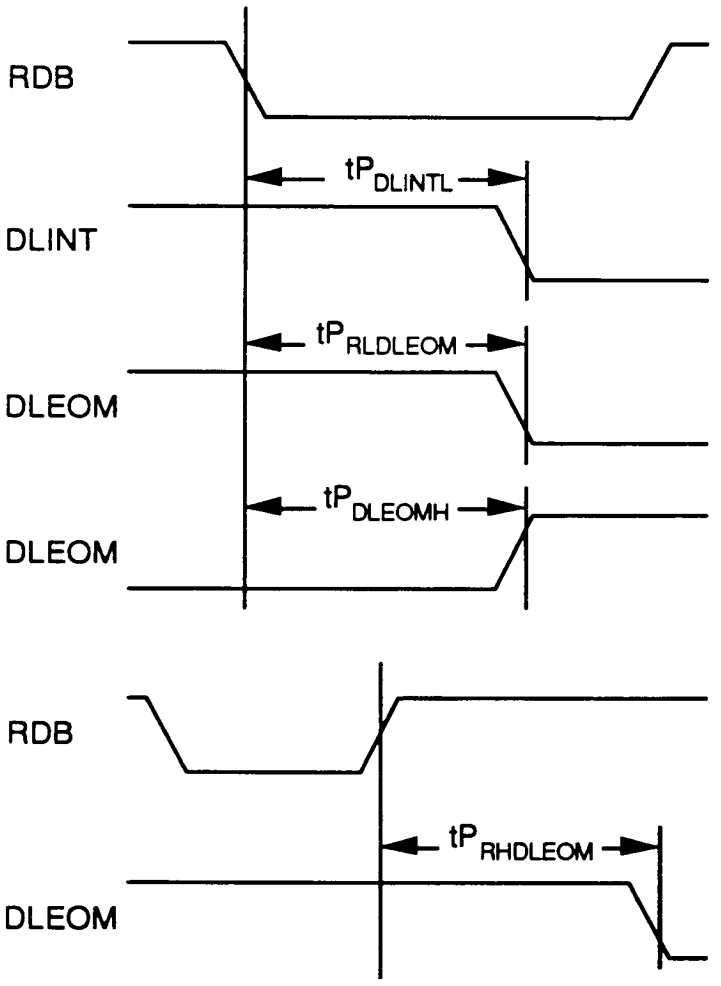


Fig. 25 HDLC Receiver RDB Associated Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

NOTES

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