MC10EL34, MC100EL34

5V ECL ÷2, ÷4, ÷8 Clock Generation Chip

The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 µF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.

The 100 Series contains temperature compensation.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK(s), $\overline{EN}$, and MR
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 191 devices

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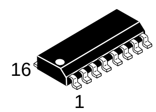
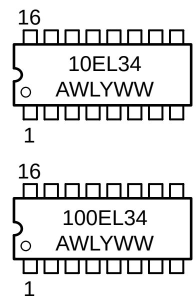
MARKING DIAGRAMS



SO–16
D SUFFIX
CASE 751B

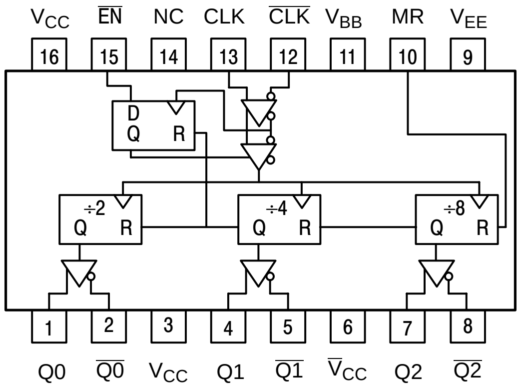


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10EL34D	SO–16	48 Units / Rail
MC10EL34DR2	SO–16	2500 Units / Reel
MC100EL34D	SO–16	48 Units / Rail
MC100EL34DR2	SO–16	2500 Units / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLE

CLK*	$\overline{EN}$*	MR*	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

Z = Low-to-High Transition
ZZ = High-to-Low Transition

* Pins will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
Q0, $\overline{Q0}$	ECL Diff ÷2 Outputs
Q1, $\overline{Q1}$	ECL Diff ÷4 Outputs
Q2, $\overline{Q2}$	ECL Diff ÷8 Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	16 SOIC 16 SOIC	130 75	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	16 SOIC	33 to 36	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 2)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			39	mA
V_{OH}	Output HIGH Voltage (Note 3)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single–Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	3.0		4.6	3.0		4.6	3.0		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
3. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = –5.0 V (Note 5)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			39	mA
V_{OH}	Output HIGH Voltage (Note 6)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 6)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single–Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
6. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 8)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			42	mA
V_{OH}	Output HIGH Voltage (Note 9)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 9)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single–Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
9. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = –5.0 V (Note 11)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			42	mA
V_{OH}	Output HIGH Voltage (Note 12)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 12)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single–Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

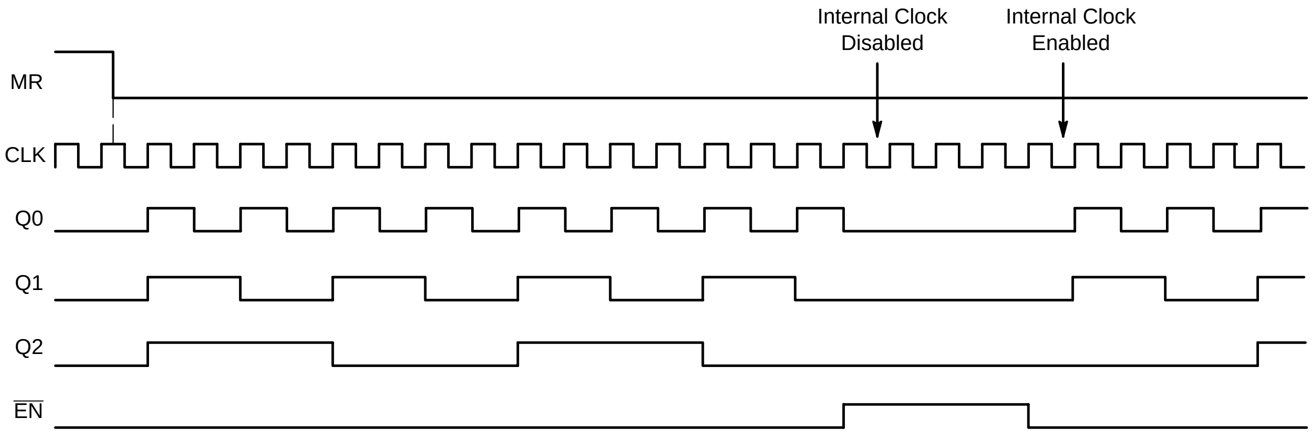
11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
12. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

AC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = –5.0 V (Note 14)

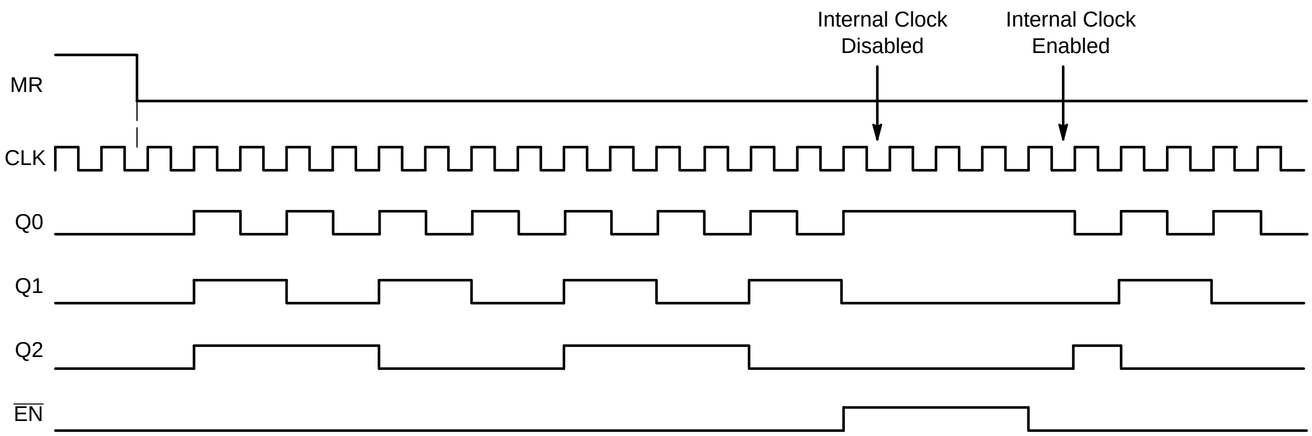
Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.1			1.1			1.1			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q0 CLK to Q1,2 MR to Q	960 900 750		1200 1140 1060	960 900 750		1200 1140 1060	970 910 790		1210 1150 1090	ps
t_{SKEW}	Within-Device Skew (Note 15)		100			100			100		ps
t_{JITTER}	Cycle–to–Cycle Jitter		1.0			1.0			1.0		ps
t_S	Setup Time $\overline{EN}$	400			400			400			ps
t_H	Hold Time $\overline{EN}$	250			250			250			ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
V_{PP}	Input Swing (Note 16)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	275		525	275		525	275		525	ps

14. 10 Series: V_{EE} can vary +0.06 V / –0.5 V.
    100 Series: V_{EE} can vary +0.8 V / –0.5 V.
15. Within-device skew is defined as identical transitions on similar paths through a device.
16. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

There are two distinct functional relationships between the Master Reset and Clock:



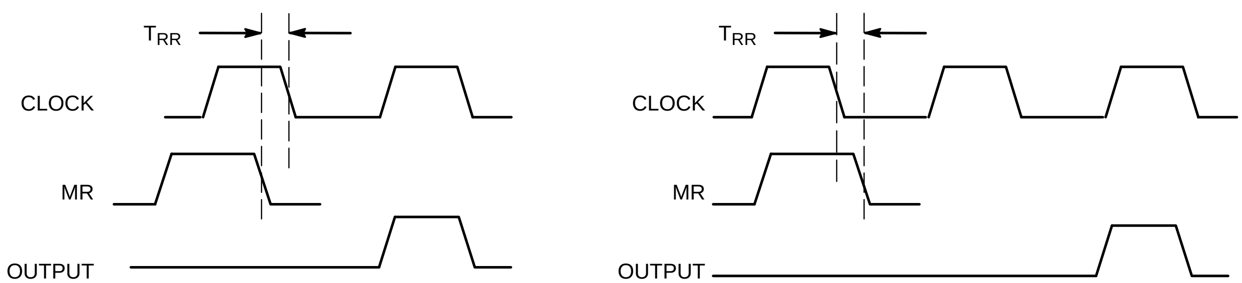
CASE 1: If the MR is de–asserted (L–H), while the Clock is still high, the ouputs will follow the first ensuing clock rising edge.



CASE 2: If the MR is de–asserted (L–H), after the Clock has transitioned low, the outputs will follow the second ensuing clock rising edge.

Figure 1. Timing Diagrams

The $\overline{EN}$ signal will freeze the internal clocks to the flip–flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the $\overline{EN}$ signal not been asserted.



CASE 1 **CASE 2**

Figure 2. Reset Recovery Time

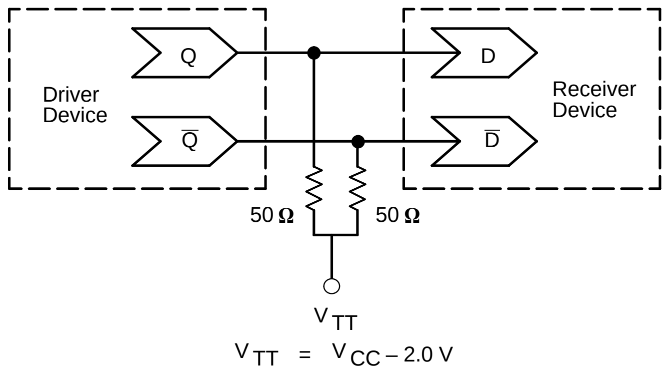


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

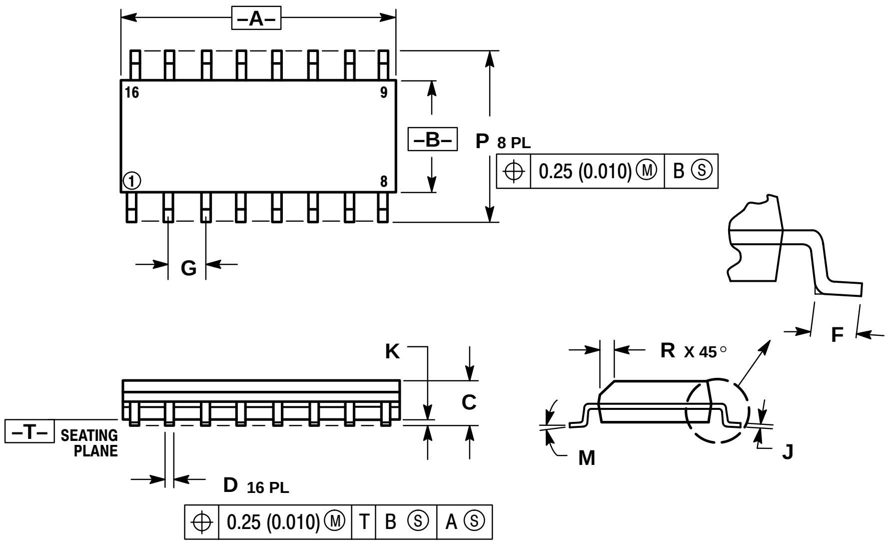
AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

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