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# HM62V16256B Series

4 M SRAM (256-kword × 16-bit)

# HITACHI

ADE-203-933C (Z)  
Rev. 2.0  
Oct. 14, 1999

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## Description

The Hitachi HM62V16256B Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62V16256B Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 70 ns/85 ns (max)
- Power dissipation:
  - Active: 9 mW (typ)
  - Standby: 3 μW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup

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# HM62V16256B Series

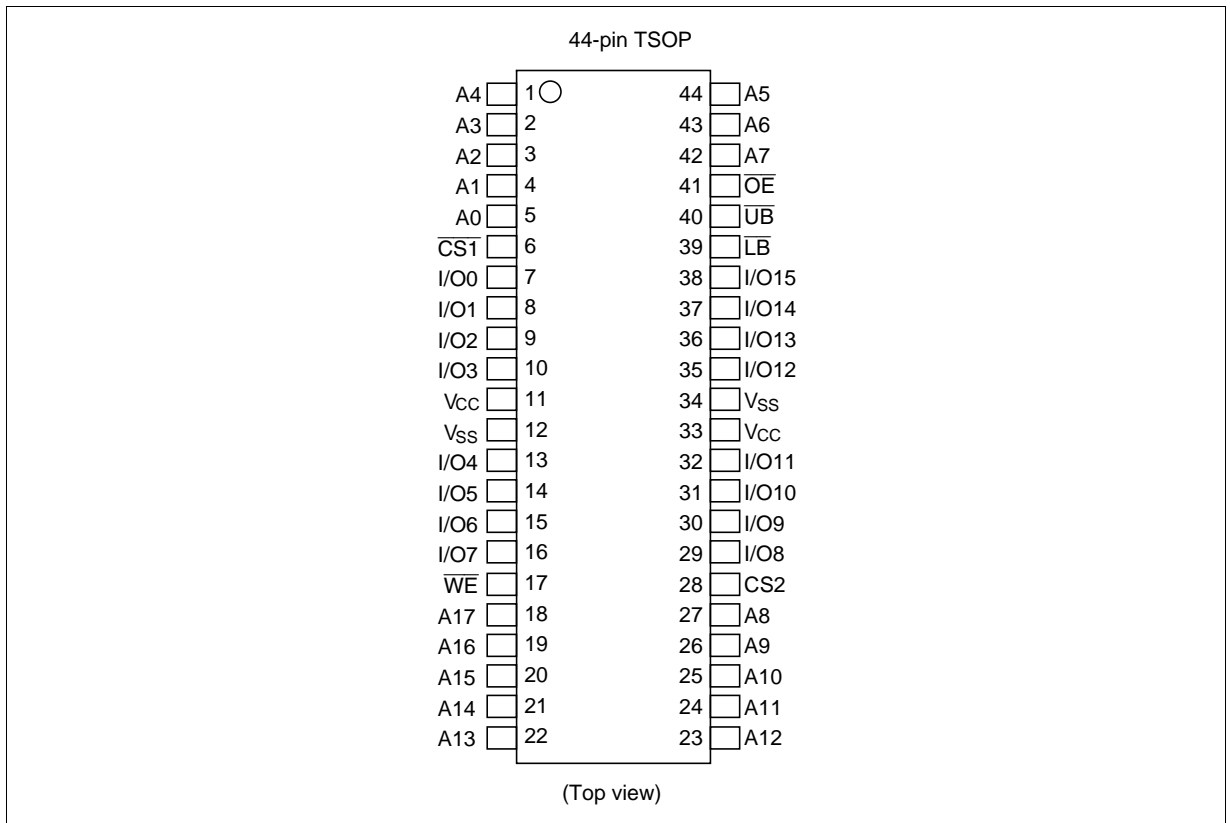
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## Ordering Information

Type No.	Access time	Package
HM62V16256BLTT-7	70 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB)
HM62V16256BLTT-8	85 ns	
HM62V16256BLTT-7SL	70 ns	
HM62V16256BLTT-8SL	85 ns	

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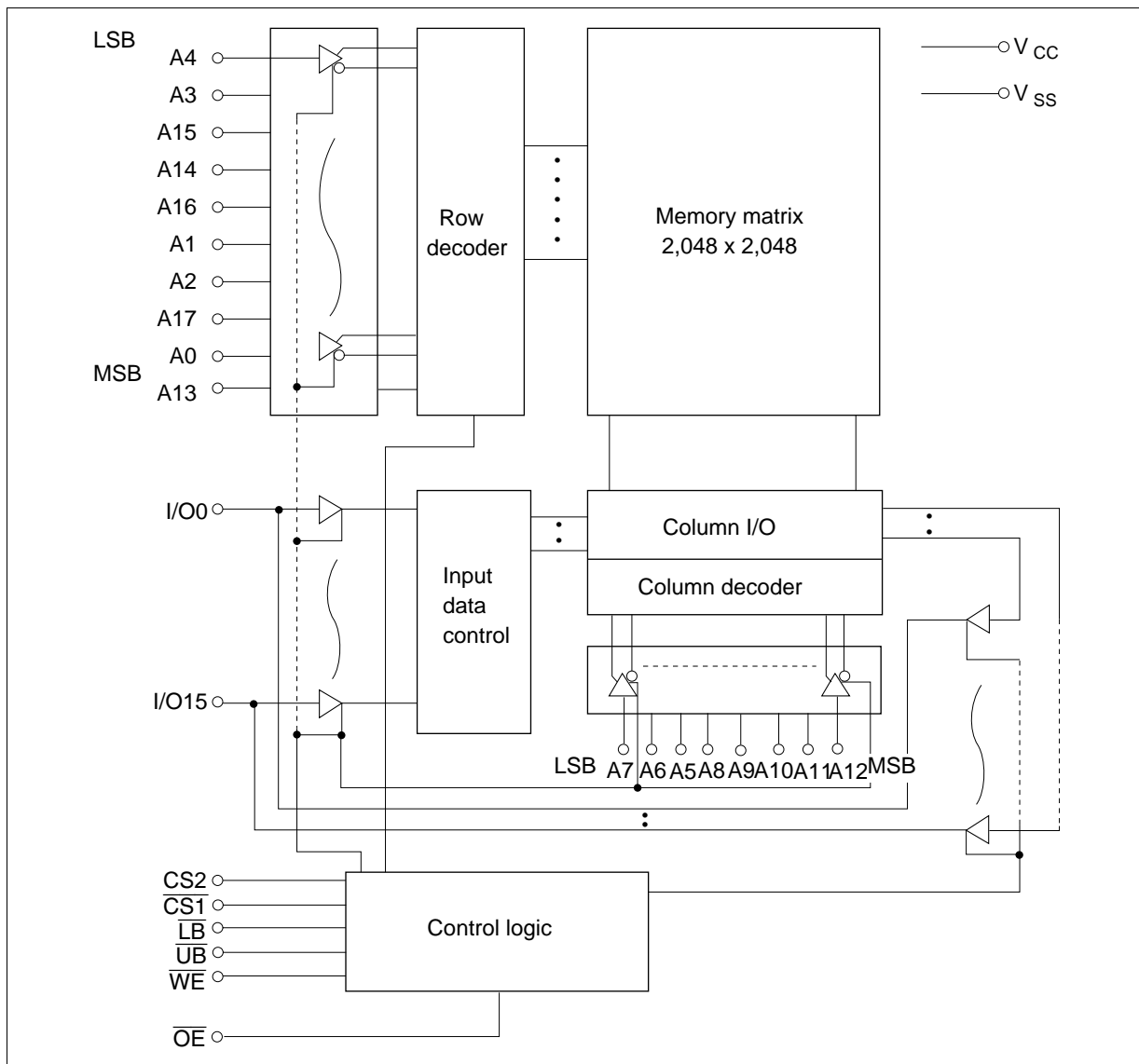
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground

## Block Diagram



**Operation Table**

$\overline{CS1}$	$\overline{CS2}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	$-0.5^{*1}$ to $V_{CC} + 0.3^{*2}$	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-10 to +85	°C

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width  $\leq$  30 ns.

2. Maximum voltage is +4.6 V.

**DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	—	0.6	V	1
Ambient temperature range	$T_a$	0	—	70	°C	

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width  $\leq$  30 ns.

## DC Characteristics

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions	
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS} \text{ to } V_{CC}$	
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , or $\overline{LB} = \overline{UB} = V_{IH}$ $V_{I/O} = V_{SS} \text{ to } V_{CC}$	
Operating current	$I_{CC}$	—	—	20	mA	$\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0 \text{ mA}$	
Average operating current	HM62V16256B-7	$I_{CC1}$	—	—	70	mA	Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}$ , $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$
	HM62V16256B-8	$I_{CC1}$	—	—	65	mA	
		$I_{CC2}$	—	3	15	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{I/O} = 0 \text{ mA}$ , $\overline{CS1} \leq 0.2 \text{ V}$ , $CS2 \geq V_{CC} - 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$
Standby current	$I_{SB}$	—	—	0.3	mA	$CS2 = V_{IL}$	
Standby current	$I_{SB1}^{*2}$	—	1	40	$\mu\text{A}$	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$ , $CS2 \geq V_{CC} - 0.2 \text{ V}$	
		$I_{SB1}^{*3}$	—	1	20	$\mu\text{A}$	
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$	
		$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100 \mu\text{A}$	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$	
		—	—	0.2	V	$I_{OL} = 100 \mu\text{A}$	

Notes: 1. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

## Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1.0 \text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0 \text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0 \text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** (Ta = 0 to +70°C, V<sub>CC</sub> = 2.7 V to 3.6 V, unless otherwise noted.)

**Test Conditions**

- Input pulse levels: V<sub>IL</sub> = 0.4 V, V<sub>IH</sub> = 2.2 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference levels: 1.4 V
- Output load: 1 TTL + 30 pF (HM62V16256B-7) (Including scope and jig)  
1 TTL + 100 pF (HM62V16256B-8) (Including scope and jig)

**Read Cycle**

Parameter	Symbol	HM62V16256B				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	70	—	85	—	ns	
Address access time	t <sub>AA</sub>	—	70	—	85	ns	
Chip select access time	t <sub>ACS1</sub>	—	70	—	85	ns	
	t <sub>ACS2</sub>	—	70	—	85	ns	
Output enable to output valid	t <sub>OE</sub>	—	40	—	45	ns	
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	
$\overline{\text{LB}}$ , $\overline{\text{UB}}$ access time	t <sub>BA</sub>	—	70	—	85	ns	
Chip select to output in low-Z	t <sub>CLZ1</sub>	10	—	10	—	ns	2, 3
	t <sub>CLZ2</sub>	10	—	10	—	ns	2, 3
$\overline{\text{LB}}$ , $\overline{\text{UB}}$ enable to low-z	t <sub>BLZ</sub>	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t <sub>CHZ1</sub>	0	25	0	25	ns	1, 2, 3
	t <sub>CHZ2</sub>	0	25	0	25	ns	1, 2, 3
$\overline{\text{LB}}$ , $\overline{\text{UB}}$ disable to high-Z	t <sub>BHZ</sub>	0	25	0	25	ns	1, 2, 3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	25	0	25	ns	1, 2, 3

## Write Cycle

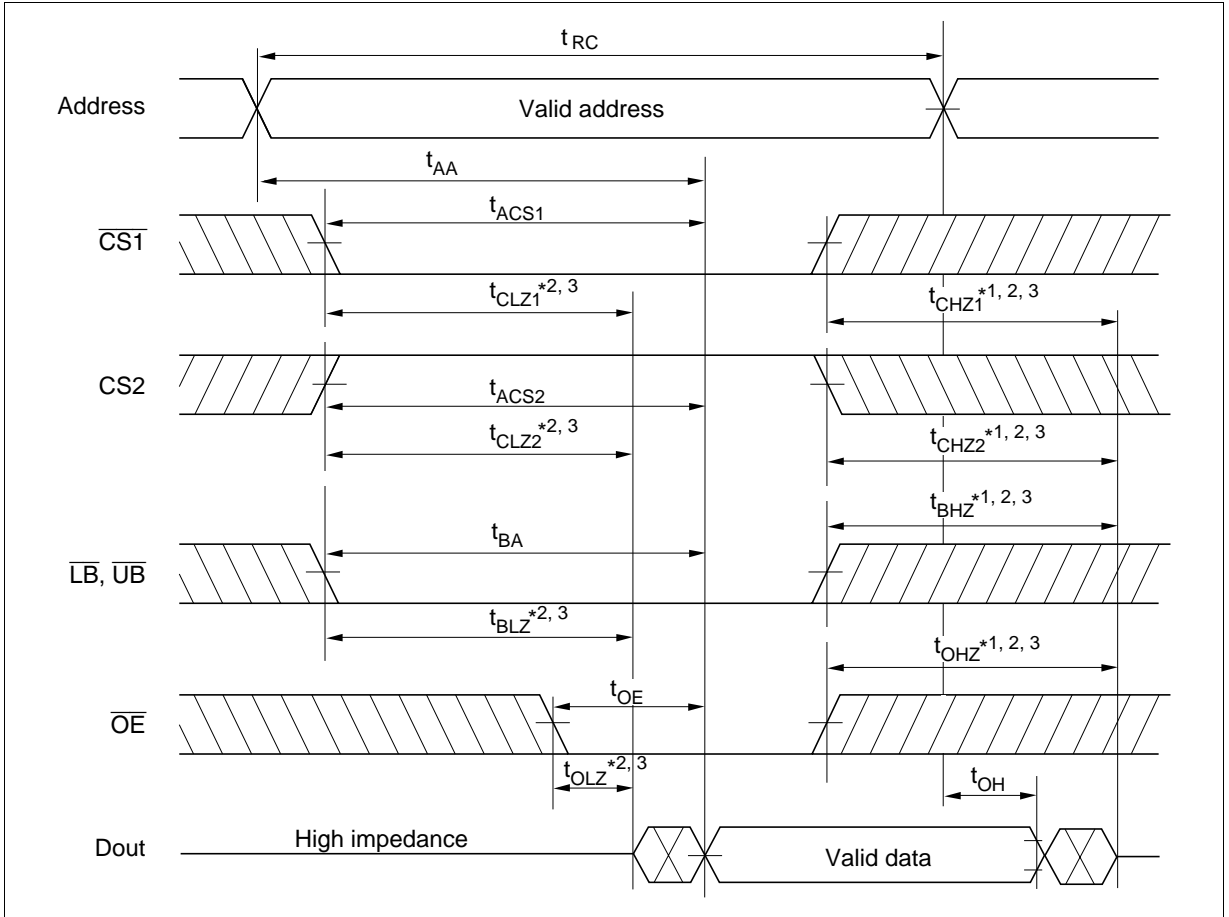
		HM62V16256B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	$t_{WC}$	70	—	85	—	ns	
Address valid to end of write	$t_{AW}$	60	—	70	—	ns	
Chip selection to end of write	$t_{CW}$	60	—	70	—	ns	5
Write pulse width	$t_{WP}$	50	—	55	—	ns	4
$\overline{LB}$ , $\overline{UB}$ valid to end of write	$t_{BW}$	55	—	70	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	30	—	35	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in High-Z	$t_{OHZ}$	0	25	0	25	ns	1, 2
Write to output in high-Z	$t_{WHZ}$	0	25	0	25	ns	1, 2

- Notes:
- $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  - A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, a low  $\overline{WE}$  and a low  $\overline{LB}$  or a low  $\overline{UB}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high,  $\overline{WE}$  going low and  $\overline{LB}$  going low or  $\overline{UB}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low,  $\overline{WE}$  going high and  $\overline{LB}$  going high or  $\overline{UB}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.

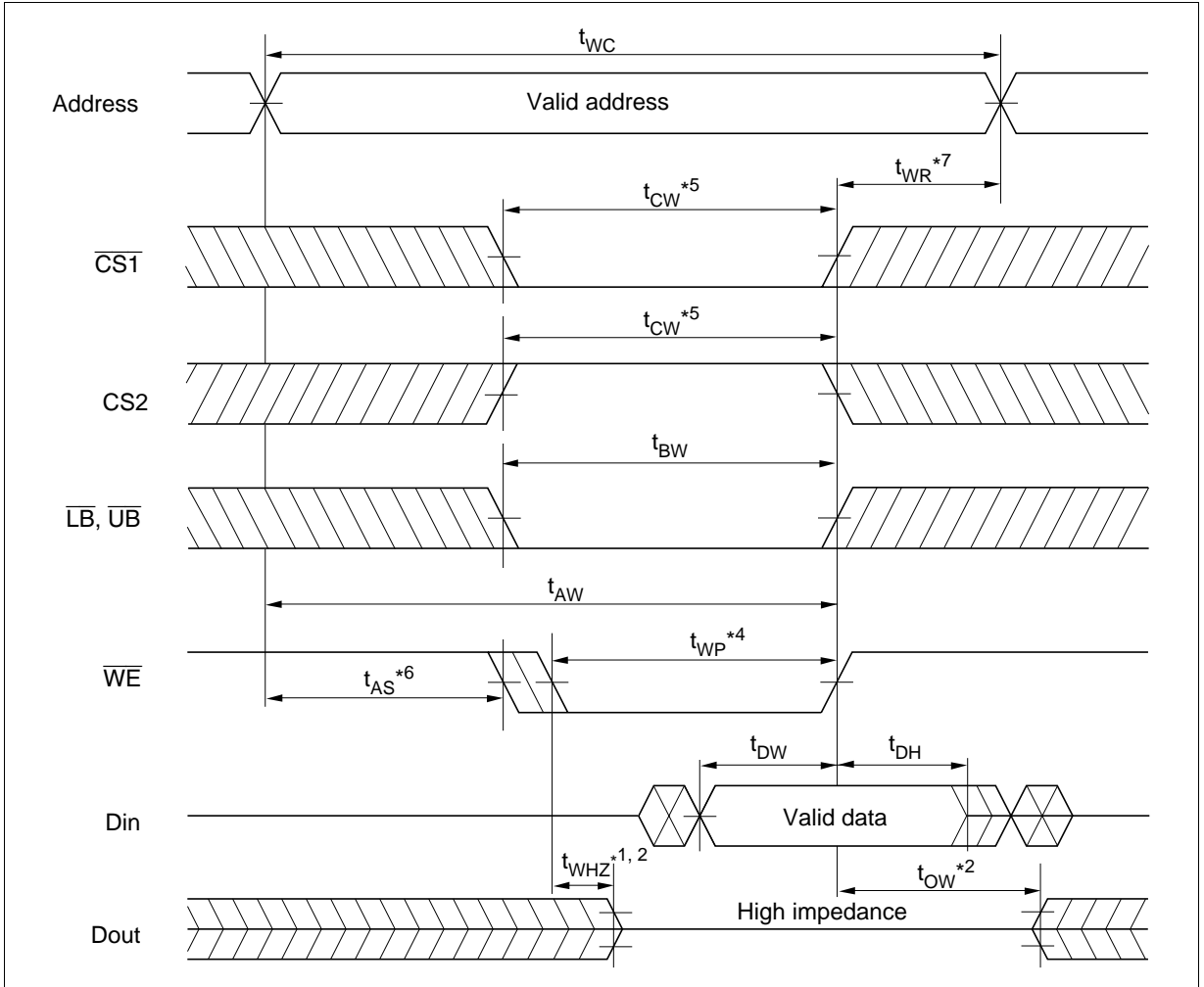


Timing Waveform

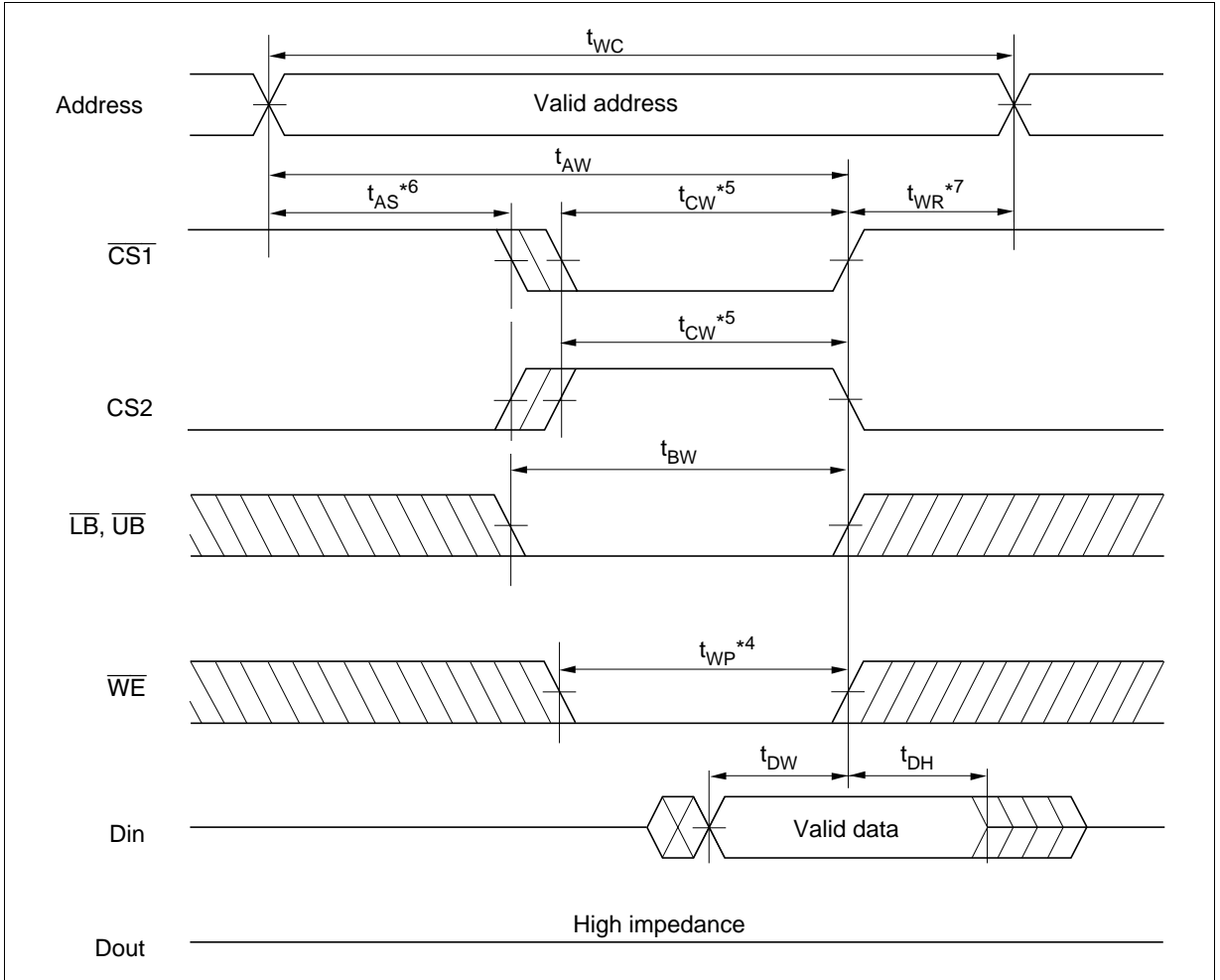
Read Cycle



## Write Cycle (1) ( $\overline{\text{WE}}$ Clock)

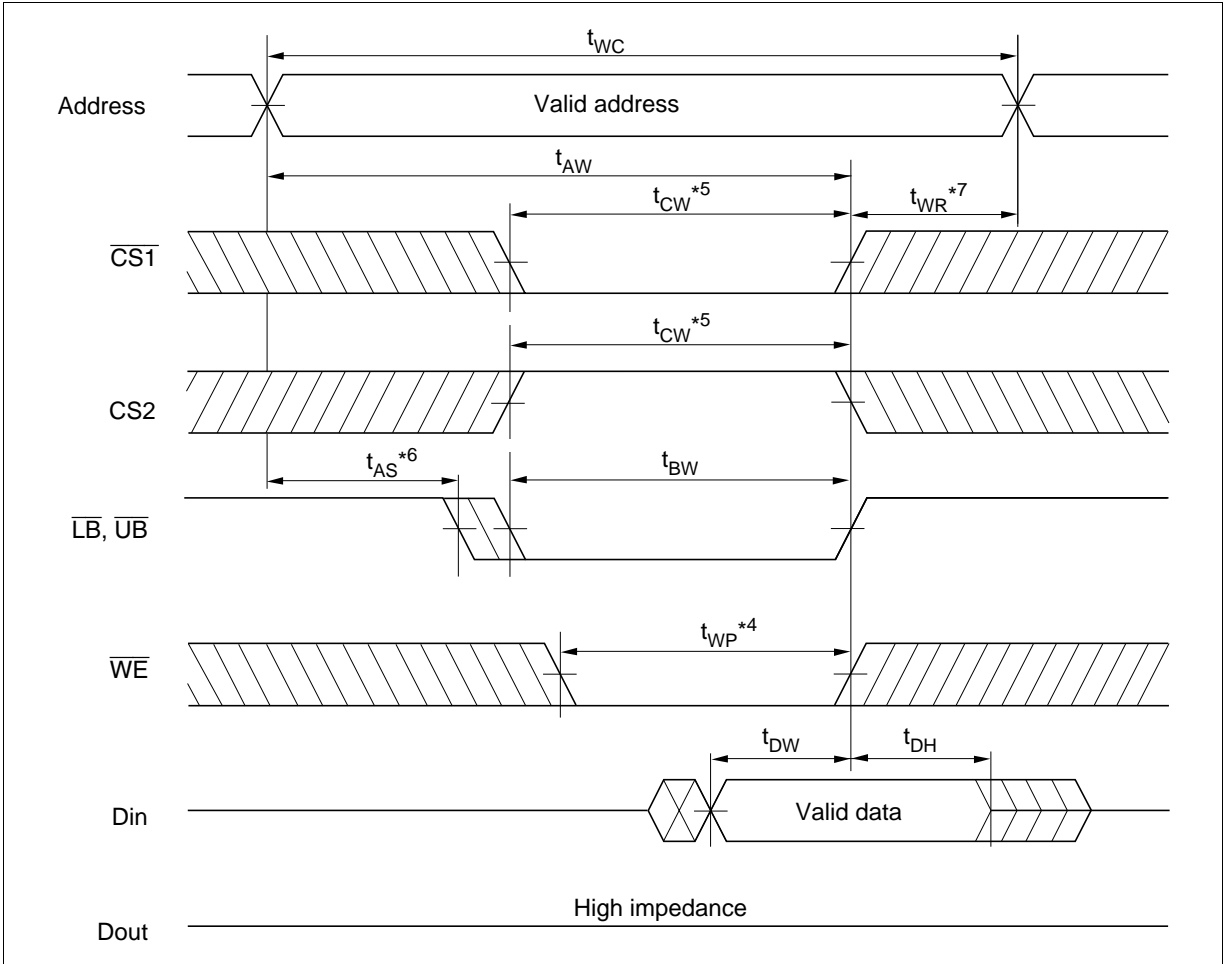


Write Cycle (2) ( $\overline{CS}$  Clock,  $\overline{OE} = V_{IH}$ )



# HM62V16256B Series

Write Cycle (3) ( $\overline{\text{LB}}, \overline{\text{UB}}$  Clock,  $\overline{\text{OE}} = V_{\text{IH}}$ )

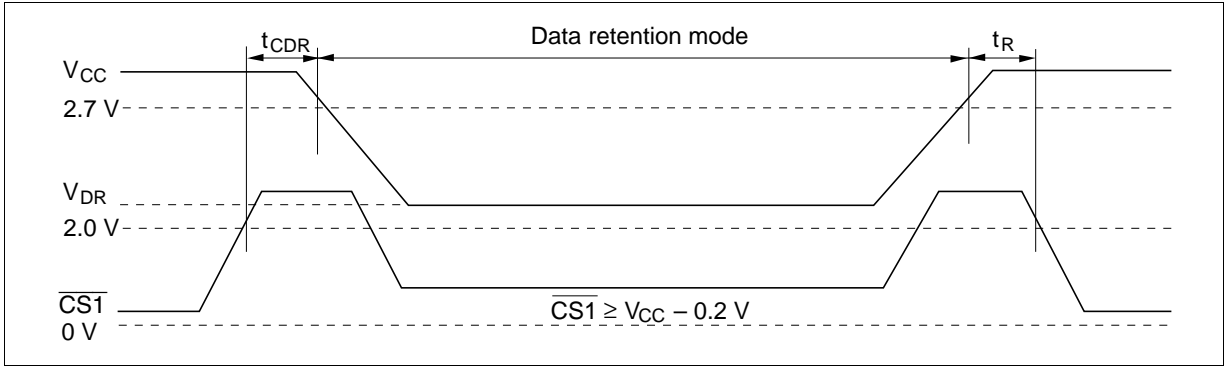


**Low  $V_{CC}$  Data Retention Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ )**

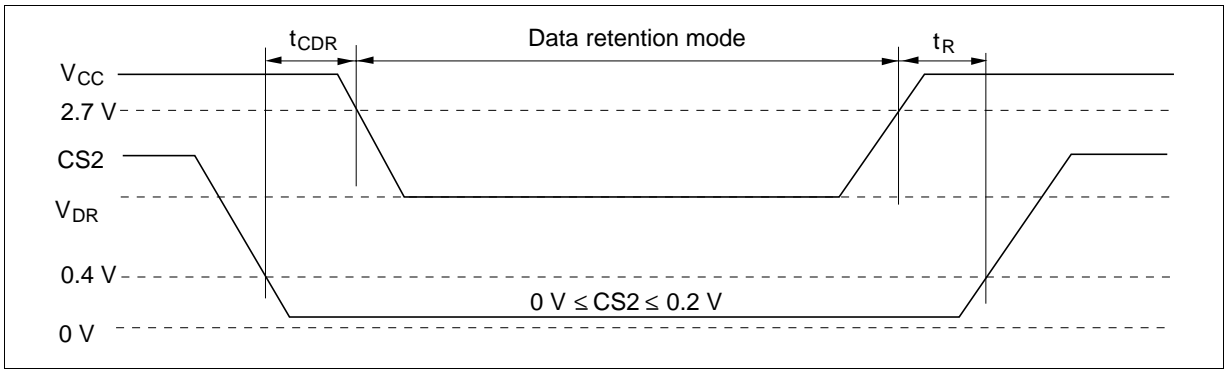
Parameter	Symbol	Min	Typ* <sup>4</sup>	Max	Unit	Test conditions* <sup>3</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V$ $\overline{CS1} \geq V_{CC} - 0.2V$ or (3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ $CS2 \geq V_{CC} - 0.2V$ $\overline{CS1} \leq 0.2V$
Data retention current	$I_{CCDR}$ * <sup>1</sup>	—	0.8	20	$\mu\text{A}$	$V_{CC} = 3.0V, V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V,$ $\overline{CS1} \geq V_{CC} - 0.2V$ or (3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ $CS2 \geq V_{CC} - 0.2V$ $\overline{CS1} \leq 0.2V$
	$I_{CCDR}$ * <sup>2</sup>	—	0.8	10	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}$ * <sup>5</sup>	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L-version, 10  $\mu\text{A}$  max. at  $T_a = 0$  to  $+40^\circ\text{C}$ .
  2. This characteristic is guaranteed only for L-SL version, 5  $\mu\text{A}$  max. at  $T_a = 0$  to  $+40^\circ\text{C}$ .
  3. CS2 controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer,  $\overline{LB}$ ,  $\overline{UB}$  buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{LB}$ ,  $\overline{UB}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode, CS2 must be  $CS2 \geq V_{CC} - 0.2V$  or  $0V \leq CS2 \leq 0.2V$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{LB}$ ,  $\overline{UB}$ , I/O) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 3.0V$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.
  5.  $t_{RC}$  = read cycle time.

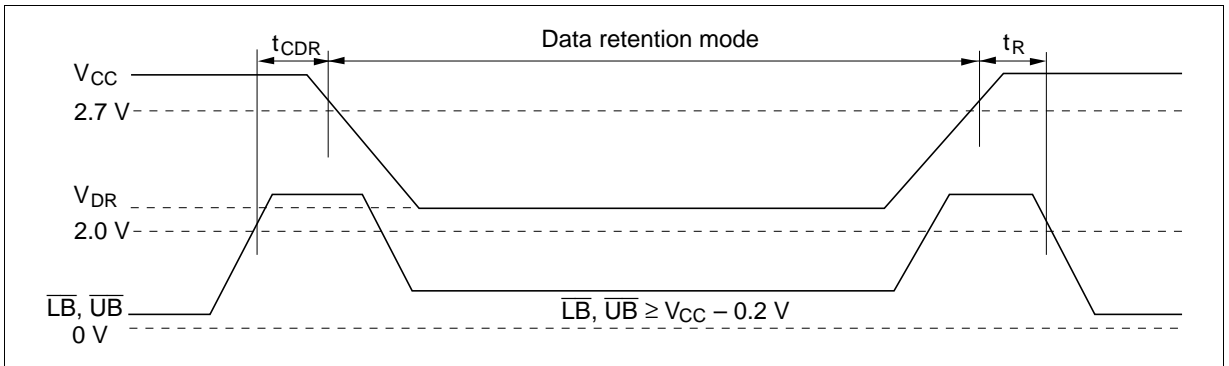
Low  $V_{CC}$  Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (2) ( $CS2$  Controlled)



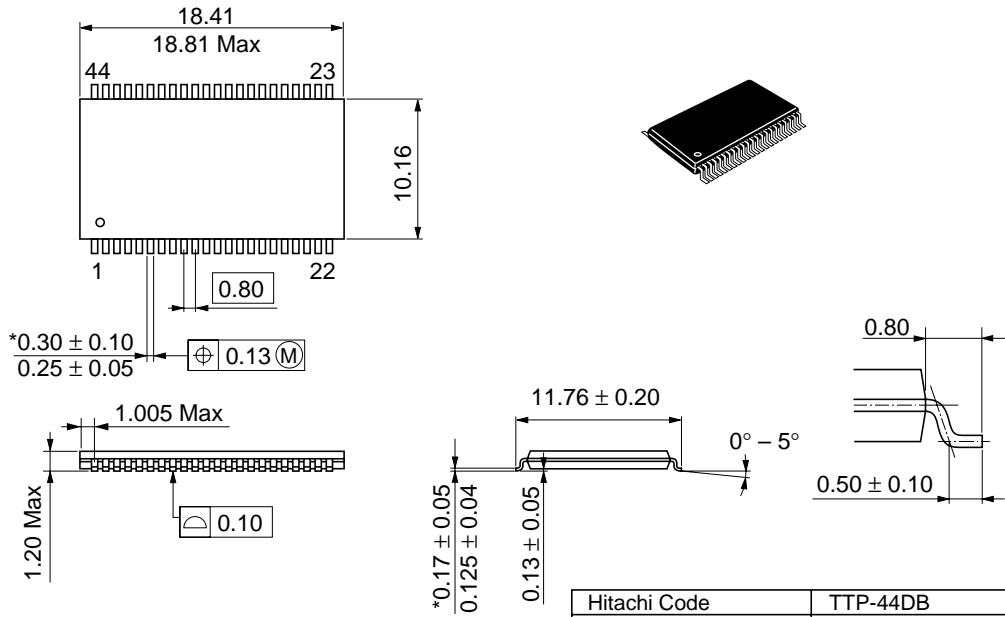
Low  $V_{CC}$  Data Retention Timing Waveform (3) ( $\overline{LB}$ ,  $\overline{UB}$  Controlled)



Package Dimensions

HM62V16256BLTT Series (TTP-44DB)

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-44DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.43 g

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