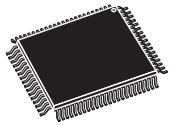
M58BW016BT, M58BW016BB
M58BW016DT, M58BW016DB

16 Mbit (512Kb x32, Boot Block, Burst)
3V Supply Flash Memories

PE4FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 2.7V to 3.6V for Program, Erase and Read
  - V_{DDQ} = V_{DDQIN} = 2.4V to 3.6V for I/O Buffers
  - V_{PP} = 12V for fast Program (optional)
- HIGH PERFORMANCE
  - Access Time: 80, 90 and 100ns
  - 56MHz Effective Zero Wait-State Burst Read
  - Synchronous Burst Reads
  - Asynchronous Page Reads
- HARDWARE BLOCK PROTECTION
  - $\overline{WP}$ pin Lock Program and Erase
- SOFTWARE BLOCK PROTECTION
  - Tuning Protection to Lock Program and Erase with 64 bit User Programmable Password (M58BW016B version only)
- OPTIMIZED for FDI DRIVERS
  - Fast Program / Erase suspend latency time < 6µs
  - Common Flash Interface
- MEMORY BLOCKS
  - 8 Parameters Blocks (Top or Bottom)
  - 31 Main Blocks
- LOW POWER CONSUMPTION
  - 5µA Typical Deep Power Down
  - 60µA Typical Standby
  - Automatic Standby after Asynchronous Read
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code M58BW016xT: 8836h
  - Bottom Device Code M58BW016xB: 8835h

Figure 1. Packages



PQFP80 (T)

LBGA80 (ZA)
10 x 8 ball array

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SUMMARY DESCRIPTION

The M58BW016B/D is a 16Mbit non-volatile Flash memory that can be erased electrically at the block level and programmed in-system on a Double-Word basis using a 2.7V to 3.6V V_{DD} supply for the circuit and a V_{DDQ} supply down to 2.4V for the Input and Output buffers. Optionally a 12V V_{PP} supply can be used to provide fast program and erase for a limited time and number of program/erase cycles.

The devices support Asynchronous (Latch Controlled and Page Read) and Synchronous Bus operations. The Synchronous Burst Read Interface allows a high data transfer rate controlled by the Burst Clock, K, signal. It is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length are configurable and can be easily adapted to a large variety of system clock frequencies and microprocessors. All Writes are Asynchronous. On power-up the memory defaults to Read mode with an Asynchronous Bus.

The device has a boot block architecture with an array of 8 parameter block of 64Kb each and 31 main blocks of 512Kb each. The parameter blocks can be located at the top of the address space, M58BW016BT, M58BW016DT or at the bottom, M58BW016BB, M58BW016DB.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

All blocks are protected during power-up. The M58BW016B features four different levels of block protection to avoid unwanted program/erase operations. The $\overline{WP}$ pin offers an hardware protection on two of the parameter blocks and all of the main blocks. The Program and Erase commands can be password protected by the Tuning Protection command. All Program or Erase operations are blocked when Reset, $\overline{RP}$, is held low. The M58BW016D offers the same protection features with the exception of the Tuning Block Protection which is disabled in the factory.

A Reset/Power-down mode is entered when the $\overline{RP}$ input is Low. In this mode the power consumption is lower than in the normal standby mode, the device is write protected and both the Status and the Burst Configuration Registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

The memory is offered in PQFP80 (14 x 20mm) and LBGA80 (1.0mm pitch) packages and it is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

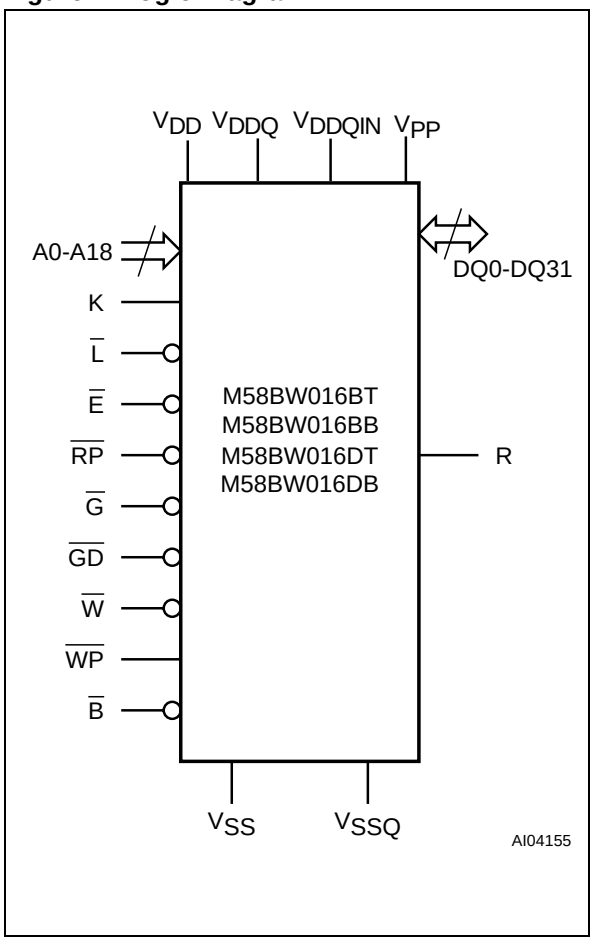


Table 1. Signal Names

A0-A18	Address inputs
DQ0-DQ7	Data Input/Output, Command Input
DQ8-DQ15	Data Input/Output, Burst Configuration Register
DQ16-DQ31	Data Input/Output
$\overline{B}$	Burst Address Advance
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
K	Burst Clock
$\overline{L}$	Latch Enable
R	Valid Data Ready (open drain output)
$\overline{RP}$	Reset/Power-down
$\overline{W}$	Write Enable
$\overline{GD}$	Output Disable
$\overline{WP}$	Write Protect
V_{DD}	Supply Voltage
V_{DDQ}	Power Supply for Output Buffers
V_{DDQIN}	Power Supply for Input Buffers only
V_{PP}	Optional Supply Voltage for Fast Program and Fast Erase Operations
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. LBGA Connections (Top view through package)

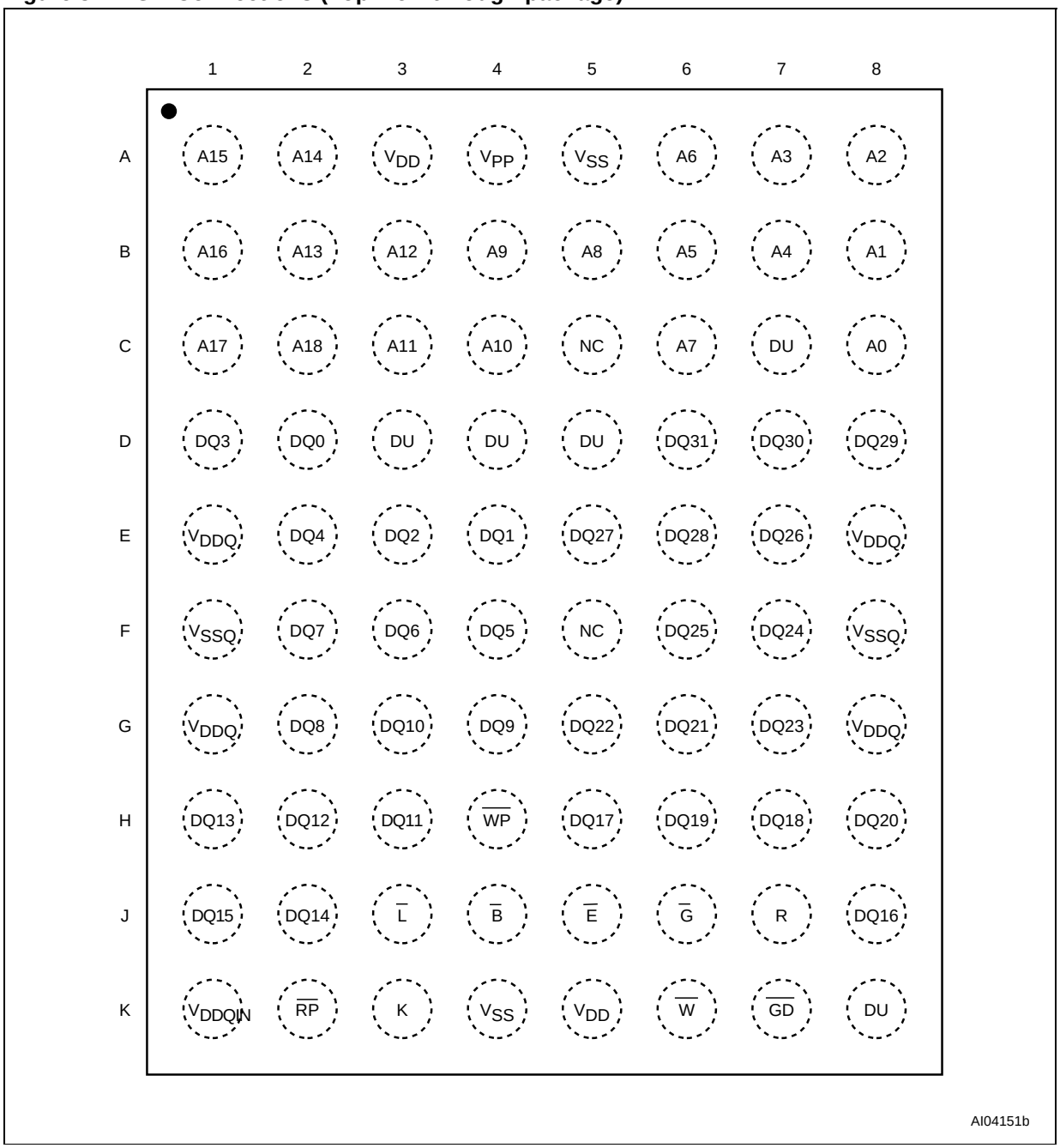
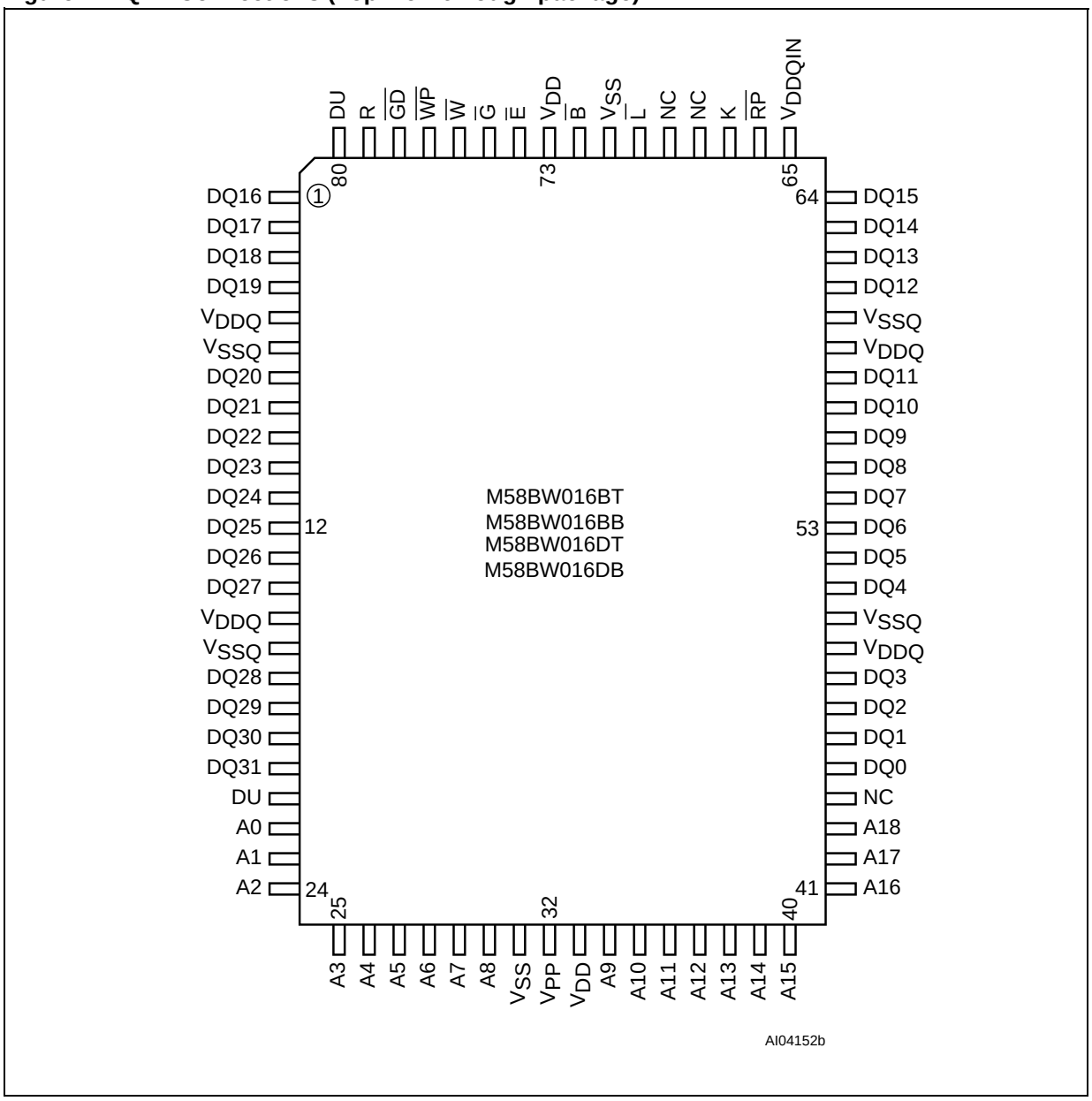


Figure 4. PQFP Connections (Top view through package)



Block Protection

The M58BW016B features four different levels of block protection. The M58BW016D has the same block protection with the exception of the Tuning Block Protection, which is disabled in the factory.

- **Write Protect Pin, $\overline{WP}$, -** When $\overline{WP}$ is low, V_{IL}, all the lockable parameter blocks (two upper (Top) or lower (Bottom)) and all the main blocks are protected. When $\overline{WP}$ is high (V_{IH}) all the lockable parameter blocks and all the main blocks are unprotected.
- **Reset/Power-Down Pin, $\overline{RP}$, -** If the device is held in reset mode ($\overline{RP}$ at V_{IL}), no program or erase operations can be performed on any block.
- Tuning Block Protection: M58BW016B features a 64 bit password protection for program and erase operations for a fixed number of blocks After power-up or reset the device is tuning protected. An Unlock command is provided to allow program or erase operations in all the blocks.

After a device reset the first two kinds of block protection ($\overline{WP}$, $\overline{RP}$) can be combined to give a flexible block protection. They do not affect the Tuning Block Protection. When the two protections are disabled, $\overline{WP}$ and $\overline{RP}$ at V_{IH}, the blocks locked by the Tuning Block Protection cannot be modified. All blocks are protected during power-up.

Tuning Block Protection. The Tuning Block Protection is a software feature to protect certain blocks from program or erase operations. It allows the user to lock program and erase operations with a user definable 64 bit code. It is only available on the M58BW016B version.

The code is written once in the Tuning Protection Register and cannot be erased. When shipped the flash memory will have the Tuning Protection Code bits set to ‘1'. The user can program a ‘0’ in any of the 64 positions. Once programmed it is not possible to reset a bit to ‘1’ as the cells cannot be erased. The Tuning Protection Register can be programmed at any moment (after providing the correct code), however once all bits are set to ‘0’ the Tuning Protection Code can no longer be altered.

The Tuning Protection Code locks the program and erase operations of 2 parameter and 24 main blocks, blocks 0, 1 and 15-38 for the bottom configuration and the blocks 0-23, 37 and 38 for the top configuration.

The tuning blocks are "locked" if the tuning protection code has not been provided, and “unlocked" once the correct code has been provided. The tuning blocks are locked after reset or power-up. The tuning protection status can be monitored in the Status Register. Refer to the Status Register section.

Refer to the Command Interface section for the Tuning Protection Block Unlock and Tuning Protection Program commands. See Appendix B, Figure 25, 26 and 27 for suggested flowcharts for using the Tuning Block Protection commands. For further information on the Tuning Block Protection refer to Application Note, AN1361.

Table 2. Top Boot Block Addresses, M58BW016BT, M58BW016DT

#	Size (Kbit)	Address Range	TP(1)
38	64	7F800h-7FFFFh	yes
37	64	7F000h-7F7FFh	yes
36	64	7E800h-7EFFFh	no
35	64	7E000h-7E7FFh	no
34	64	7D800h-7DFFFh	no
33	64	7D000h-7D7FFh	no
32	64	7C800h-7CFFFh	no
31	64	7C000h-7C7FFh	no
30	512	78000h-7BFFFh	no
29	512	74000h-77FFFh	no
28	512	70000h-73FFFh	no
27	512	6C000h-6FFFFh	no
26	512	68000h-6BFFFh	no
25	512	64000h-67FFFh	no
24	512	60000h-63FFFh	no
23	512	5C000h-5FFFFh	yes
22	512	58000h-5BFFFh	yes
21	512	54000h-57FFFh	yes
20	512	50000h-53FFFh	yes
19	512	4C000h-4FFFFh	yes
18	512	48000h-4BFFFh	yes
17	512	44000h-47FFFh	yes
16	512	40000h-43FFFh	yes
15	512	3C000h-3FFFFh	yes
14	512	38000h-3BFFFh	yes
13	512	34000h-37FFFh	yes
12	512	30000h-33FFFh	yes
11	512	2C000h-2FFFFh	yes
10	512	28000h-2BFFFh	yes
9	512	24000h-27FFFh	yes
8	512	20000h-23FFFh	yes
7	512	1C000h-1FFFFh	yes
6	512	18000h-1BFFFh	yes
5	512	14000h-17FFFh	yes
4	512	10000h-13FFFh	yes
3	512	0C000h-0FFFFh	yes
2	512	08000h-0BFFFh	yes
1	512	04000h-07FFFh	yes
0	512	00000h-03FFFh	yes

Note: 1. TP = Tuning Protected Block, only available for the M58BW016B.

Table 3. Bottom Boot Block Addresses, M58BW016BB, M58BW016DT

#	Size (Kbit)	Address Range	TP(1)
38	512	7C000h-7FFFFh	yes
37	512	78000h-7BFFFh	yes
36	512	74000h-77FFFh	yes
35	512	70000h-73FFFh	yes
34	512	6C000h-6FFFFh	yes
33	512	68000h-6BFFFh	yes
32	512	64000h-67FFFh	yes
31	512	60000h-63FFFh	yes
30	512	5C000h-5FFFFh	yes
29	512	58000h-5BFFFh	yes
28	512	54000h-57FFFh	yes
27	512	50000h-53FFFh	yes
26	512	4C000h-4FFFFh	yes
25	512	48000h-4BFFFh	yes
24	512	44000h-47FFFh	yes
23	512	40000h-43FFFh	yes
22	512	3C000h-3FFFFh	yes
21	512	38000h-3BFFFh	yes
20	512	34000h-37FFFh	yes
19	512	30000h-33FFFh	yes
18	512	2C000h-2FFFFh	yes
17	512	28000h-2BFFFh	yes
16	512	24000h-27FFFh	yes
15	512	20000h-23FFFh	yes
14	512	1C000h-1FFFFh	no
13	512	18000h-1BFFFh	no
12	512	14000h-17FFFh	no
11	512	10000h-13FFFh	no
10	512	0C000h-0FFFFh	no
9	512	08000h-0BFFFh	no
8	512	04000h-07FFFh	no
7	64	03800h-03FFFh	no
6	64	03000h-037FFh	no
5	64	02800h-02FFFh	no
4	64	02000h-027FFh	no
3	64	01800h-01FFFh	no
2	64	01000h-017FFh	no
1	64	00800h-00FFFh	yes
0	64	00000h-007FFh	yes

Note: 1. TP = Tuning Protected Block, only available for the M58BW016B.

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A18). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. Chip Enable must be low when selecting the addresses.

The address inputs are latched on the rising edge of Latch Enable $\overline{L}$ or Burst Clock K, whichever occurs first, in a read operation.The address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a Write operation. The address latch is transparent when Latch Enable is low, V_{IL}. The address is internally latched in an Erase or Program operation.

Data Inputs/Outputs (DQ0-DQ31). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both low, V_{IL}, and Output Disable is at V_{IH}, the data bus outputs data from the memory array, the Electronic Signature, the CFI Information or the contents of the Status Register. The data bus is high impedance when the device is deselected with Chip Enable at V_{IH}, Output Enable at V_{IH}, Output Disable at V_{IL} or Reset/Power-Down at V_{IL}. The Status Register content is output on DQ0-DQ7 and DQ8-DQ31 are at V_{IL}.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the Standby level.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation, when Output Disable $\overline{GD}$ is at V_{IH}. When Output Enable $\overline{G}$ is at V_{IH}, the outputs are high impedance independently of Output Disable.

Output Disable ($\overline{GD}$). The Output Disable, $\overline{GD}$, deactivates the data output buffers. When Output Disable, $\overline{GD}$, is at V_{IH}, the outputs are driven by the Output Enable. When Output Disable, $\overline{GD}$, is at V_{IL}, the outputs are high impedance independently of Output Enable. The Output Disable pin must be connected to an external pull-up resistor as there is no internal pull-up resistor to drive the pin.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, input controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, $\overline{L}$).

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down, $\overline{RP}$, is used to apply a hardware reset to the memory. A hardware reset is achieved by holding Reset/Power-Down Low, V_{IL}, for at least t_{PLPH}. Writing is inhibited to protect data, the Command Interface and the Program/Erase Controller are reset. The Status Register information is cleared and power consumption is reduced to deep power-down level. The device acts as deselected, that is the data outputs are high impedance.

After Reset/Power-Down goes High, V_{IH}, the memory will be ready for Bus Read operations after a delay of t_{PHEL} or Bus Write operations after t_{PHWL}.

If Reset/Power-Down goes low, V_{IL}, during a Block Erase, a Program or a Tuning Protection Program the operation is aborted, in a time of t_{PLRH} maximum, and data is altered and may be corrupted.

During Power-up power should be applied simultaneously to V_{DD} and $V_{DDQ(IN)}$ with $\overline{RP}$ held at V_{IL}. When the supplies are stable $\overline{RP}$ is taken to V_{IH}. Output Enable, $\overline{G}$, Chip Enable, $\overline{E}$, and Write Enable, $\overline{W}$, should be held at V_{IH} during power-up.

In an application, it is recommended to associate Reset/Power-Down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an erase or program operation, the memory may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

See Table 21 and Figure 18, Reset, Power-Down and Power-up Characteristics, for more details.

Latch Enable ($\overline{L}$). The Bus Interface can be configured to latch the Address Inputs on the rising edge of Latch Enable, $\overline{L}$, for Asynchronous Latch Enable Controlled Read or Write or Synchronous Burst Read operations. In Synchronous Burst Read operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL}. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent. Latch Enable, $\overline{L}$, can remain at V_{IL} for Asynchronous Random Read and Write operations.

Burst Clock (K). The Burst Clock, K, is used to synchronize the memory with the external bus dur-

ing Synchronous Burst Read operations. Bus signals are latched on the active edge of the Clock. The Clock can be configured to have an active rising or falling edge. In Synchronous Burst Read mode the address is latched on the first active clock edge when Latch Enable is low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During Asynchronous bus operations the Clock is not used.

Burst Address Advance ($\overline{B}$). The Burst Address Advance, $\overline{B}$, controls the advancing of the address by the internal address counter during Synchronous Burst Read operations.

Burst Address Advance, $\overline{B}$, is only sampled on the active clock edge of the Clock when the X-latency time has expired. If Burst Address Advance is Low, V_{IL}, the internal address counter advances. If Burst Address Advance is High, V_{IH}, the internal address counter does not change; the same data remains on the Data Inputs/Outputs and Burst Address Advance is not sampled until the Y-latency expires.

The Burst Address Advance, $\overline{B}$, may be tied to V_{IL}.

Valid Data Ready (R). The Valid Data Ready output, R, is an open drain output that can be used, during Synchronous Burst Read operations, to identify if the memory is ready to output data or not. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready, at V_{IH}, indicates that new data is or will be available. When Valid Data Ready is Low, V_{IL}, the previous data outputs remain active.

In all Asynchronous operations, Valid Data Ready is high-impedance. It may be tied to other components with the same Valid Data Ready signal to create a unique system Ready signal. The Valid Data Ready output has an internal pull-up resistor of around 1 MΩ powered from V_{DDQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for Valid Data Ready going to V_{IH}.

Write Protect ($\overline{WP}$). The Write Protect, $\overline{WP}$, provides protection against program or erase operations. When Write Protect, $\overline{WP}$, is at V_{IL} the first two (in the bottom configuration) or last two (in the top configuration) parameter blocks and all main blocks are locked. When Write Protect $\overline{WP}$ is at V_{IH} all the blocks can be programmed or erased, if no other protection is used.

Supply Voltage (V_{DD}). The Supply Voltage, V_{DD}, is the core power supply. All internal circuits draw their current from the V_{DD} pin, including the Program/Erase Controller.

Output Supply Voltage (V_{DDQ}). The Output Supply Voltage, V_{DDQ}, is the output buffer power supply for all operations (Read, Program and Erase) used for DQ0-DQ31 when used as outputs.

Input Supply Voltage (V_{DDQIN}). The Input Supply Voltage, V_{DDIN}, is the power supply for all input signal. Input signals are: K, $\overline{B}$, $\overline{L}$, $\overline{W}$, $\overline{GD}$, $\overline{G}$, $\overline{E}$, A0-A18 and D0-D31, when used as inputs.

Program/Erase Supply Voltage (V_{PP}). The Program/Erase Supply Voltage, V_{PP}, is used for program and erase operations. The memory normally executes program and erase operations at V_{PP1} voltage levels. In a manufacturing environment, programming may be speeded up by applying a higher voltage level, V_{PPH}, to the V_{PP} pin.

The voltage level V_{PPH} may be applied for a total of 80 hours over a maximum of 1000 cycles. Stressing the device beyond these limits could damage the device.

Ground (V_{SS} and V_{SSQ}). The Ground V_{SS} is the reference for the internal supply voltage V_{DD}. The Ground V_{SSQ} is the reference for the output and input supplies V_{DDQ}, and V_{DDQIN}. It is essential to connect V_{SS} and V_{SSQ} together.

Note: A 0.1µF capacitor should be connected between the Supply Voltages, V_{DD}, V_{DDQ} and V_{DDIN} and the Grounds, V_{SS} and V_{SSQ} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during all operations of the parts, see Table 15, DC Characteristics, for maximum current supply requirements.

Don't Use (DU). This pin should not be used as it is internally connected. Its voltage level can be between V_{SS} and V_{DDQ} or leave it unconnected.

Not Connected (NC). This pin is not physically connected to the device.

BUS OPERATIONS

Each bus operations that controls the memory is described in this section, see Tables 4, 5 and 6 Bus Operations, for a summary. The bus operation is selected through the Burst Configuration Register; the bits in this register are described at the end of this section.

On Power-up or after a Hardware Reset the memory defaults to Asynchronous Bus Read and Asynchronous Bus Write, no other bus operation can be performed until the Burst Control Register has been configured.

The Electronic Signature, CFI or Status Register will be read in asynchronous mode regardless of the Burst Control Register settings.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Asynchronous Bus Operations

For asynchronous bus operations refer to Table 4 together with the following text.

Asynchronous Bus Read. Asynchronous Bus Read operations read from the memory cells, or specific registers (Electronic Signature, Status Register, CFI and Burst Configuration Register) in the Command Interface. A valid bus operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable and Output Disable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 9, Asynchronous Bus Read AC Waveforms, and Table 16, Asynchronous Bus Read AC Characteristics, for details of when the output becomes valid.

Asynchronous Read is the default read mode which the device enters on power-up or on return from Reset/Power-Down.

Asynchronous Latch Controlled Bus Read. Asynchronous Latch Controlled Bus Read operations read from the memory cells or specific registers in the Command Interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Latch Enable. Once latched, the Address Inputs can change. Set Output Enable Low, V_{IL}, to read the data on the Data Inputs/Outputs; see Figure 1, Asynchronous Latch Controlled Bus Read AC Waveforms and Table 17, Asynchronous Latch Controlled Bus Read AC Characteristics for details on when the output becomes valid.

Note that, since the Latch Enable input is transparent when set Low, V_{IL}, Asynchronous Bus Read operations can be performed when the memory is configured for Asynchronous Latch Enable bus operations by holding Latch Enable Low, V_{IL} throughout the bus operation.

Asynchronous Page Read. Asynchronous Page Read operations are used to read from several addresses within the same memory page. Each memory page is 4 Double-Words and is addressed by the address inputs A0 and A1.

Data is read internally and stored in the Page Buffer. Valid bus operations are the same as Asynchronous Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. Page Read does not support Latched Controlled Read.

See Figure 11, Asynchronous Page Read AC Waveforms and Table 18, Asynchronous Page Read AC Characteristics for details on when the outputs become valid.

Asynchronous Bus Write. Asynchronous Bus Write operations write to the Command Interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Bus Write operation begins by setting the desired address on the Address Inputs, and setting Chip Enable, Write Enable and Latch Enable Low, V_{IL}, and Output Enable High, V_{IH}, or Output Disable Low, V_{IL}. The Address Inputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Commands and Input Data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole Asynchronous Bus Write operation.

See Figure 12, Asynchronous Write AC Waveforms, and Table 19, Asynchronous Write and Latch Controlled Write AC Characteristics, for details of the timing requirements.

Asynchronous Latch Controlled Bus Write. Asynchronous Latch Controlled Bus Write operations write to the Command Interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Latch Controlled Bus Write operation begins by setting the desired address on

the Address Inputs and pulsing Latch Enable Low, V_{IL}. The Address Inputs are latched by the Command Interface on the rising edge of Latch Enable, Write Enable or Chip Enable, whichever occurs first. Commands and Input Data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole Asynchronous Bus Write operation.

See Figure 13, Asynchronous Latch Controlled Write AC Waveforms, and Table 19, Asynchronous Write and Latch Controlled Write AC Characteristics, for details of the timing requirements.

Output Disable. The data outputs are high impedance when the Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}.

Standby. When Chip Enable is High, V_{IH}, and the Program/Erase Controller is idle, the memory enters Standby mode, the power consumption is reduced to the standby level and the Data Inputs/Outputs pins are placed in the high impedance state regardless of Output Enable, Write Enable or Output Disable inputs.

Automatic Low Power. If there is no change in the state of the bus for a short period of time during Asynchronous Bus Read operations the memory enters Auto Low Power mode where the internal Supply Current is reduced to the Auto-Standby Supply Current. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Automatic Low Power is only available in Asynchronous Read modes.

Power-Down. The memory is in Power-down when Reset/Power-Down, $\overline{RP}$, is at V_{IL}. The power consumption is reduced to the power-down level and the outputs are high impedance, independent of the Chip Enable, $\overline{E}$, Output Enable, $\overline{G}$, Output Disable, $\overline{GD}$, or Write Enable, $\overline{W}$, inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory. The Electronic Signature is output by giving the Read Electronic Signature command. The manufacturer code is output when all the Address inputs are at V_{IL}. The device code is output when A1 is at V_{IH} and all the other address pins are at V_{IL}. See Table 5. Issue a Read Memory Array command to return to Read mode.

Table 4. Asynchronous Bus Operations

Bus Operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	$\overline{RP}$	$\overline{L}$	A0-A18	DQ0-DQ31
Asynchronous Bus Read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	Data Output
Asynchronous Latch Controlled Bus Read	Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Address	High Z
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	Data Output
Asynchronous Page Read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Address	Data Output
Asynchronous Bus Write		V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	Address	Data Input
Asynchronous Latch Controlled Bus Write	Address Latch	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	High Z
	Write	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	X	Data Input
Output Disable, $\overline{G}$		V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	High Z
Output Disable, $\overline{GD}$		V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby		V_{IH}	X	X	X	V_{IH}	X	X	High Z
Reset/Power-Down		X	X	X	X	V_{IL}	X	X	High Z

Note: X = Don't Care

Table 5. Asynchronous Read Electronic Signature Operation

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	A18-A0	DQ31-DQ0
Manufacturer	All	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00000h	00000020h
Device	M58BW016xT(1)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00001h	00008836h
	M58BW016xB(1)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00001h	00008835h
Burst Configuration Register		V_{IL}	V_{IL}	V_{IH}	V_{IH}	00005h	BCR (2)

Note: 1. x= B or D version of the device.
2. BCR= Burst Configuration Register.

Synchronous Bus Operations

For synchronous bus operations refer to Table 6 together with the following text.

Synchronous Burst Read. Synchronous Burst Read operations are used to read from the memory at specific times synchronized to an external reference clock. The burst type, length and latency can be configured. The different configurations for Synchronous Burst Read operations are described in the Burst Configuration Register section. Refer to Figures 5 and 6 for examples of synchronous burst operations.

In continuous burst read, one burst read operation can access the entire memory sequentially by keeping the Burst Address Advance $\overline{B}$ at V_{IL} for the appropriate number of clock cycles. At the end of the memory address space the burst read restarts from the beginning at address 000000h.

A valid Synchronous Burst Read operation begins when the Burst Clock is active and Chip Enable and Latch Enable are Low, V_{IL}. The burst start address is latched and loaded into the internal Burst Address Counter on the valid Burst Clock K edge (rising or falling depending on the value of M6) or on the rising edge of Latch Enable, whichever occurs first.

After an initial memory latency time, the memory outputs data each clock cycle (or two clock cycles depending on the value of M9). The Burst Address Advance $\overline{B}$ input controls the memory burst output. The second burst output is on the next clock valid edge after the Burst Address Advance $\overline{B}$ has been pulled Low.

Valid Data Ready, R, monitors if the memory burst boundary is exceeded and the Burst Controller of the microprocessor needs to insert wait states. When Valid Data Ready is Low on the active clock edge, no new data is available and the memory does not increment the internal address counter at the active clock edge even if Burst Address Advance, $\overline{B}$, is Low.

Valid Data Ready may be configured (by bit M8 of Burst Configuration Register) to be valid immediately at the valid clock edge or one data cycle before the valid clock edge.

Synchronous Burst Read will be suspended if Burst Address Advance, $\overline{B}$, goes High, V_{IH}.

If Output Enable is at V_{IL} and Output Disable is at V_{IH}, the last data is still valid.

If Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}, but the Burst Address Advance, $\overline{B}$, is at V_{IL} the internal Burst Address Counter is incremented at each Burst Clock K valid edge.

The Synchronous Burst Read timing diagrams and AC Characteristics are described in the AC and DC Parameters section. See Figures 14, 15, 16 and 17, and Table 20.

Synchronous Burst Read Suspend. During a Synchronous Burst Read operation it is possible to suspend the operation, freeing the data bus for other higher priority devices.

A valid Synchronous Burst Read operation is suspended when both Output Enable and Burst Address Advance are High, V_{IH}. The Burst Address Advance going High, V_{IH}, stops the burst counter and the Output Enable going High, V_{IH}, inhibits the data outputs. The Synchronous Burst Read operation can be resumed by setting Output Enable Low.

Table 6. Synchronous Burst Read Bus Operations

Bus Operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{RP}$	K(3)	$\overline{L}$	$\overline{B}$	A0-A18 DQ0-DQ31
Synchronous Burst Read	Address Latch	V_{IL}	V_{IH}	X	V_{IH}	T	V_{IL}	X	Address Input
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	T	V_{IH}	V_{IL}	Data Output
	Read Suspend	V_{IL}	V_{IH}	X	V_{IH}	X	V_{IH}	V_{IH}	High Z
	Read Resume	V_{IL}	V_{IL}	V_{IH}	V_{IH}	T	V_{IH}	V_{IL}	Data Output
	Burst Address Advance	V_{IL}	V_{IH}	X	V_{IH}	T	V_{IH}	V_{IL}	High Z
	Read Abort, $\overline{E}$	V_{IH}	X	X	V_{IH}	X	X	X	High Z
	Read Abort, $\overline{RP}$	X	X	X	V_{IL}	X	X	X	High Z

Note: 1. X = Don't Care, V_{IL} or V_{IH}.
2. M15 = 0, Bit M15 is in the Burst Configuration Register.
3. T = transition, see M6 in the Burst Configuration Register for details on the active edge of K.

Burst Configuration Register

The Burst Configuration Register is used to configure the type of bus access that the memory will perform.

The Burst Configuration Register is set through the Command Interface and will retain its information until it is re-configured, the device is reset, or the device goes into Reset/Power-Down mode. The Burst Configuration Register bits are described in Table 7. They specify the selection of the burst length, burst type, burst X and Y latencies and the Read operation. Refer to Figures 5 and 6 for examples of synchronous burst configurations.

Read Select Bit (M15). The Read Select bit, M15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to '1', Bus Read operations are asynchronous; when the Read Select but is set to '0', Bus Read operations are synchronous.

On reset or power-up the Read Select bit is set to'1' for asynchronous accesses.

X-Latency Bits (M14-M11). The X-Latency bits are used during Synchronous Bus Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in Table 7, Burst Configuration Register. The X-Latency bits should also be selected in conjunction with Table , Burst Performance to ensure valid settings.

Y-Latency Bit (M9). The Y-Latency bit is used during Synchronous Bus Read operations to set the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in M9.

When the Y-Latency is 1 the data changes each clock cycle; when the Y-Latency is 2 the data changes every second clock cycle. See Table 7, Burst Configuration Register and Table , Burst Performance, for valid combinations of the Y-Latency, the X-Latency and the Clock frequency.

Valid Data Ready Bit (M8). The Valid Data Ready bit controls the timing of the Valid Data Ready output pin, R. When the Valid Data Ready bit is '0' the Valid Data Ready output pin is driven Low for the active clock edge when invalid data is output on the bus. When the Valid Data Ready bit is '1' the Valid Data Ready output pin is driven Low one clock cycle prior to invalid data being output on the bus.

Burst Type Bit (M7). The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' the memory outputs from sequential addresses. See Tables 8, Burst Type Definition, for the sequence of addresses output from a given starting address in each mode.

Valid Clock Edge Bit (M6). The Valid Clock Edge bit, M6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

Wrap Burst Bit (M3). The burst reads can be confined inside the 4 or 8 Double-Word boundary (wrap) or overcome the boundary (no wrap). The Wrap Burst bit is used to select between wrap and no wrap. When the Wrap Burst bit is set to '0' the burst read wraps; when it is set to '1' the burst read does not wrap.

Burst Length Bit (M2-M0). The Burst Length bits set the maximum number of Double-Words that can be output during a Synchronous Burst Read operation before the address wraps. Burst lengths of 4 or 8 are available for both the Sequential and Interleaved burst types, and a continuous burst is available for the Sequential type.

Table 7, Burst Configuration Register gives the valid combinations of the Burst Length bits that the memory accepts; Table 8, Burst Type Definition, gives the sequence of addresses output from a given starting address for each length.

If either a Continuous or a No Wrap Burst Read has been initiated the device will output data synchronously. Depending on the starting address, the device activates the Valid Data Ready output to indicate that a delay is necessary before the data is output. If the starting address is aligned to an 8 Double Word boundary, the continuous burst mode will run without activating the Valid Data Ready output. If the starting address is not aligned to an 8 Double Word boundary, Valid Data Ready is activated to indicate that the device needs an internal delay to read the successive words in the array.

M10, M5 and M4 are reserved for future use.

Table 7. Burst Configuration Register

Bit	Description	Value	Description
M15	Read Select	0	Synchronous Burst Read
		1	Asynchronous Read (Default at power-on)
M14			Reserved
M13-M11	X-Latency (2)	001	Reserved
		010	4, 4-1-1-1 (1)
		011	5, 5-1-1-1, 5-2-2-2
		100	6, 6-1-1-1, 6-2-2-2
		101	7, 7-1-1-1, 7-2-2-2
		110	8, 8-1-1-1, 8-2-2-2
M10			Reserved
M9	Y-Latency (3)	0	One Burst Clock cycle
		1	Two Burst Clock cycles
M8	Valid Data Ready	0	R valid Low during valid Burst Clock edge
		1	R valid Low one data cycle before valid Burst Clock edge
M7	Burst Type	0	Interleaved
		1	Sequential
M6	Valid Clock Edge	0	Falling Burst Clock edge
		1	Rising Burst Clock edge
M5-M4			Reserved
M3	Wrapping	0	Wrap
		1	No wrap
M2-M0	Burst Length	001	4 Double-Words
		010	8 Double-Words
		111	Continuous

Note: 1. 4 - 2 - 2 - 2 is not allowed.
2. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1)\ t_{K.}$ (X is an integer number from 4 to 8 and t_K is the clock period).
3. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y\ t_{K.}$
4. $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation.

Table 8. Burst Type Definition

M 3	Starting Address	x4 Sequential	x4 Interleaved	x8 Sequential	x8 Interleaved	Continuous
0	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10..
0	1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-8-9-10-11..
0	2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-9-10-11-12..
0	3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-10-11-12-13..
0	4	–	–	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-2-13-14..
0	5	–	–	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11-12-13-14..
0	6	–	–	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-13-14-15..
0	7	–	–	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-14-15-16..
0	8	–	–	–	–	8-9-10-11-12-13-14-15-16-17..
1	0	0-1-2-3	–	0-1-2-3-4-5-6-7	–	0-1-2-3-4-5-6-7-8-9-10..
1	1	1-2-3-4	–	1-2-3-4-5-6-7-8	–	1-2-3-4-5-6-7-8-9-10-11..
1	2	2-3-4-5	–	2-3-4-5-6-7-8-9	–	2-3-4-5-6-7-8-9-10-11-12..
1	3	3-4-5-6	–	3-4-5-6-7-8-9-10	–	3-4-5-6-7-8-9-10-11-12-13..
1	4	4-5-6-7	–	4-5-6-7-8-9-10-11	–	4-5-6-7-8-9-10-11-12-13-14..
1	5	5-6-7-8	–	5-6-7-8-9-10-11-12	–	5-6-7-8-9-10-11-12-13-14..
1	6	6-7-8-9	–	6-7-8-9-10-11-12-13	–	6-7-8-9-10-11-12-13-14-15..
1	7	7-8-9-10	–	7-8-9-10-11-12-13-14	–	7-8-9-10-11-12-13-14-15-16..
1	8	8-9-10-11	–	8-9-10-11-12-13-14-15	–	8-9-10-11-12-13-14-15-16-17..

Figure 5. Example Burst Configuration X-1-1-1

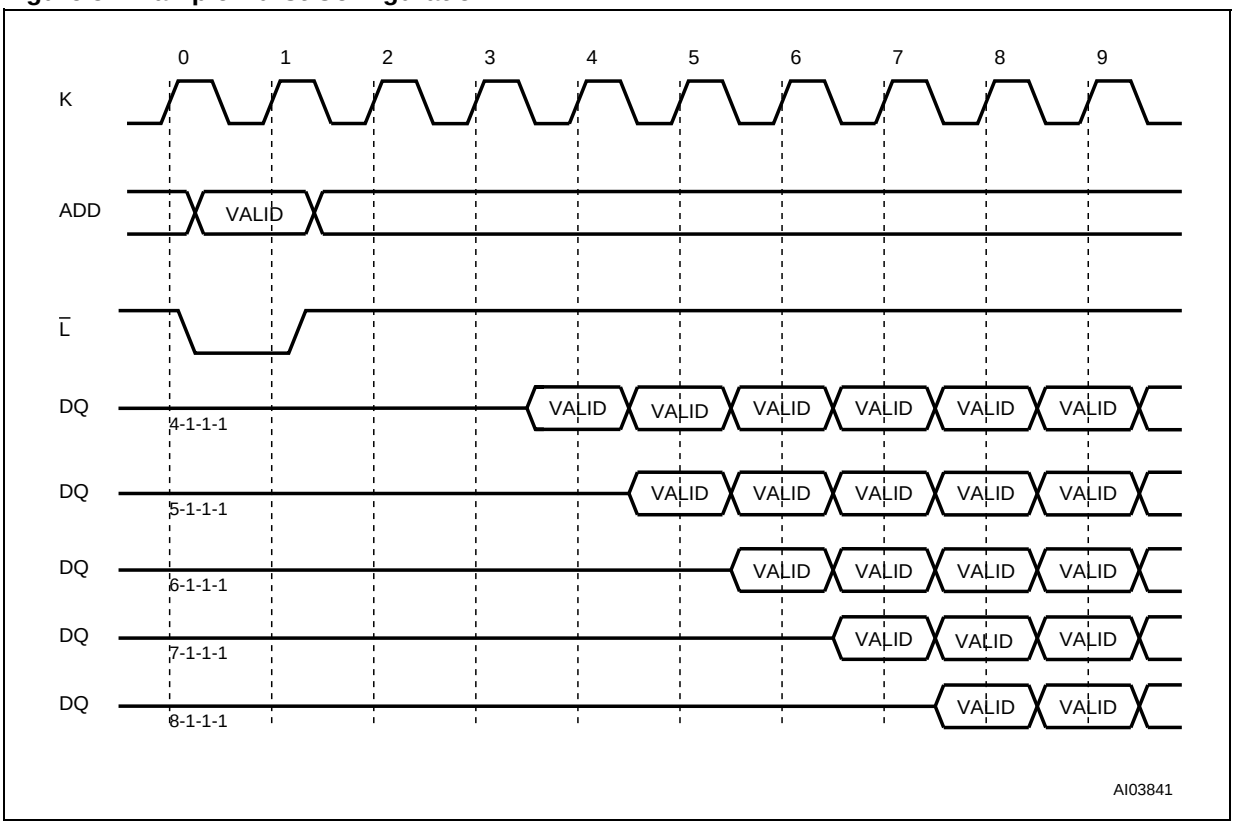
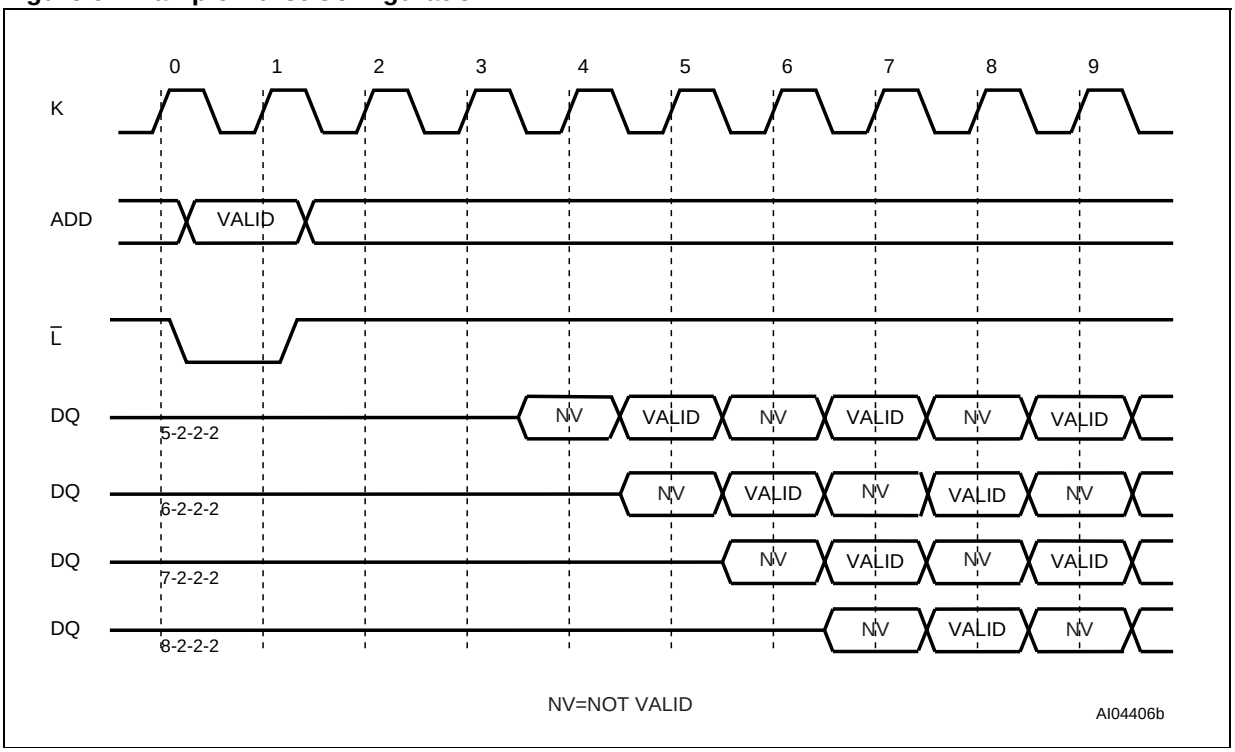


Figure 6. Example Burst Configuration X-2-2-2



COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. The Commands are summarized in Table 9, Commands. Refer to Table 9 in conjunction with the text descriptions below.

Read Memory Array Command

The Read Memory Array command returns the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Subsequent read operations will output the addressed memory array data. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read commands will access the memory array.

Read Electronic Signature Command

The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code or the Burst Configuration Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations, depending on the address specified, read the Manufacturer Code, the Device Code or the Burst Configuration Register until another command is issued; see Table 5, Read Electronic Signature.

Read Query Command.

The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations, depending on the address specified, read from the Common Flash Interface Memory Area. See Appendix A, Tables 26, 27, 28, 29 and 30 for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command

The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ1-DQ7) when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are at V_{IL} and Output Disable is at V_{IH}.

An interactive update of the Status Register bits is possible by toggling Output Enable or Output Disable. It is also possible during a Program or Erase operation, by disactivating the device with Chip Enable at V_{IH} and then reactivating it with Chip Enable and Output Enable at V_{IL} and Output Disable at V_{IH}.

The content of the Status Register may also be read at the completion of a Program, Erase or Suspend operation. During a Block Erase, Program, Tuning Protection Program or Tuning Protection Unlock command, DQ7 indicates the Program/Erase Controller status. It is valid until the operation is completed or suspended.

See the section on the Status Register and Table 11 for details on the definitions of the Status Register bits

Clear Status Register Command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent Bus Read operations continue to output the same data.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Program, Erase, Block Protect or Block Unprotect command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command

The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the first write cycle sets up the Block Erase command, the second write cycle confirms the Block erase command and latches the block address in the internal state machine and starts the Program/Erase Controller. The sequence is aborted if the Confirm command is not given and the device will output the Status Register Data with bits 4 and 5 set to '1'.

Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits. During the Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Erase times are given in Table 10.

See Appendix B, Figure 23, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Block Erase command.

Program Command.

The Program command is used to program the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Program command, the second write cycle latches the address and data to be programmed in the internal state machine and starts the Program/Erase Controller. A program operation can be aborted by writing FFFFFFFFh to any address after the program set-up command has been given.

Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits. During the Program operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored.

The program operation aborts if V_{PP} drops out of the allowed ranges or if Reset/Power-down $\overline{RP}$ falls to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory block must be erased and reprogrammed.

See Appendix B, Figure 21, Program Flowchart and Pseudo Code, for a suggested flowchart on using the Program command.

Program/Erase Suspend Command

The Program/Erase Suspend command is used to pause a Program or Erase operation. The command will only be accepted during a Program or Erase operation. It can be issued at any time during a program or erase operation. The command is ignored if the device is already in suspend mode.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (bit 7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (bit 7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (bit 2) or the Erase Suspend Status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 10.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Program and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See Appendix B, Figure 22, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 24, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command.

See Appendix B, Figure 22, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 24, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Resume command.

Set Burst Configuration Register Command.

The Set Burst Configuration Register command is used to write a new value to the Burst Configuration Control Register which defines the burst length, type, X and Y latencies, Synchronous/Asynchronous Read mode and the valid Clock edge configuration.

Two Bus Write cycles are required to issue the Set Burst Configuration Register command. The first cycle writes the setup command and the address corresponding to the Set Burst Configuration Register content. The second cycle writes the Burst Configuration Register data and the confirm command. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Burst Configuration Register is always presented on A0-A15. M0 is on A0, M1 on A1, etc.; the other address bits are ignored.

Tuning Protection Unlock Command

The Tuning Protection Unlock command unlocks the tuning protected blocks by writing the 64bit

Tuning Protection Code (M58BW016B only). After a reset or power-up the blocks are locked and so a Tuning Protection Unlock command must be issued to allow program or erase operations on tuning protected block or to program a new Tuning Protection Code. Read operations output the Status Register content after the unlock operation has started.

The Tuning Protection Code is composed of 64 bits, but the data bus is 32 bits wide so four (2 x 2) write cycles are required to unlock the device.

- The first write cycle issues the Tuning Protection Unlock Setup command (0x78).
- The second write cycle inputs the first 32 bits of the tuning protection code on the data bus, at address 0x00000.

Bit 7 of the Status Register should now be checked to verify that the device has successfully stored the first part of the code in the internal register. If b7 = '1', the device is ready to accept the second part of the code. This does not mean that the first 32 bits match the tuning protection code, simply that it was correctly stored for the comparing. If b7 = '0', the user must wait for this bit setting (refer to write cycle AC timings).

- The third write cycle re-issues the Tuning Protection Unlock Setup command (0x78).
- The fourth write cycle inputs the second 32 bits of the code at address 0x00001.

Bit 7 of the Status Register should again be checked to verify that the device has successfully stored the second part of the code. When the device is ready (b7 = '1'), the tuning protection status can be monitored on Status Register bit0. If b0 = '0' the device is locked; b0 = '1' the device is unlocked. If the device is still locked a Read Memory Array command must be issued before re-issuing the Tuning Protection Unlock command.

Device locked means that the 64 bit password is wrong. If the unlock operation is attempted using a wrong code on an already unlocked device, the device becomes locked. Status register bit 4 is set to '1' if there has been a verify failure.

Unlocking aborts if V_{PP} drops out of the allowed range or $\overline{RP}$ goes to V_{IL}.

Once the device is successfully unlocked, a Read Memory Array command must be issued to return the memory to read mode before issuing any other commands. The user can then program or erase all blocks, depending on $\overline{WP}$ status and V_{PP} level. At this point, it is also possible to configure a new protection code. To write a new protection code into the device tuning register, the user must perform the Tuning Protection Program sequence. The device can be re-locked with a reset or power-down.

See Appendix B, Figure 25, 26 and 27 for suggested flowcharts for using the Tuning Protection Unlock command.

Tuning Protection Program Command.

The Tuning Protection Program command is used to program a new Tuning Protection Code which can be configured by the designer of the application (M58BW016B only). The device should be unlocked by the Tuning Protection Unlock command before issuing the Tuning Protection Program command.

Read operations output the Status Register content after the program operation has started.

The Tuning Protection Code is composed of 64 bits, but the data bus is 32 bits wide so four (2 x 2) write cycles are required to program the code.

- The first write cycle issues the Tuning Protection Program Setup command (0x48).
- The second write cycle inputs the first 32 bits of the new tuning protection code on the data bus, at address 0x00000.

Bit 7 of the Status Register should now be checked to verify that the device has successfully stored the first part of the code in the internal register. If b7 = '1', the device is ready to accept the second part of the code. If b7 = '0', the user must wait for this bit setting (refer to write cycle AC timings).

- The third write cycle re-issues the Tuning Protection Program Setup command (0x48).
- The fourth write cycle inputs the second 32 bits of the new code at address 0x00001.

Bit 7 of the Status Register should again be checked to verify that the device has successfully stored the second part of the code. When the device is ready (b7 = '1'). After completion Status Register bit 4 is set to '1' if there has been a program failure.

Programming aborts if V_{PP} drops out of the allowed range or $\overline{RP}$ goes to V_{IL}.

A Read Memory Array command must be issued to return the memory to read mode before issuing any other commands. Once the code has been changed a device reset or power-down will make the protection active with the new code.

See Appendix B, Figure 25, 26 and 27 for suggested flowcharts for using the Tuning Protection Program command.

Table 9. Commands

Command	Cycles	Bus Operations											
		1st Cycle			2nd Cycle			3rd Cycle			4th Cycle		
		Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	≥ 2	Write	X	FFh	Read	RA	RD						
Read Electronic Signature (Manufacturer Code)	≥ 2	Write	X	90h	Read	00000h	20h						
Read Electronic Signature (Device Code)	≥ 2	Write	X	90h	Read	00001h	IDh						
Read Electronic Signature (Burst Configuration Register)	≥ 2	Write	X	90h	Read	00005h	BCRh						
Read Status Register	2	Write	X	70h	Read	X	SRDh						
Read Query	≥ 2	Write	X	98h	Read	QAh	QDh						
Clear Status Register	1	Write	X	50h									
Block Erase	2	Write	X	20h	Write	BAh	D0h						
Program	2	Write	X	40h 10h	Write	PA	PD						
Program/Erase Suspend	1	Write	X	B0h									
Program/Erase Resume	1	Write	X	D0h									
Set Burst Configuration Register	2	Write	X	60h	Write	BCRh	03h						
Tuning Protection(2) Program	4	Write	X	48h	Write	TPAh	TPCh	Write	X	48h	Write	TPAh	TPCh
Tuning Protection Unlock(2)	4	Write	X	78h	Write	TPAh	TPCh	Write	X	78h	Write	TPAh	TPCh

Note: 1. X Don't Care; RA Read Address, RD Read Data, ID Device Code, SRD Status Register Data, PA Program Address; PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, BCR Burst Configuration Register value, TPA = Tuning Protection Address, TPC = Tuning Protection Code.
2. Cycles 1 and 2 input the first 32 bits of the code, cycles 3 and 4 the second 32 bits of the code.

Table 10. Program, Erase Times and Program Erase Endurance Cycles

Parameters	M58BW016B/D					Unit
	Min	Typ		Max		
		$V_{PP} = V_{DD}$	V_{PP} = 12V	$V_{PP} = V_{DD}$	V_{PP} = 12V	
Parameter Block (64Kb) Program		0.030	0.016	0.060	0.032	s
Main Block (512Kb) Program		0.23	0.13	0.46	0.26	s
Parameter Block Erase		0.8	0.64	1.8	1.5	s
Main Block Erase		1.5	0.9	3	1.8	s
Program Suspend Latency Time		3		10		µs
Erase Suspend Latency Time		10		30		µs
Program/Erase Cycles (per Block)	100,000					cycles

Note: T_A = –40 to 125°C, V_{DD} = 2.7V to 3.6V, V_{DDQ} = 2.4V to V_{DD}

STATUS REGISTER

The Status Register provides information on the current or previous Program, Erase, Block Protect or Tuning Protection operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Program/Erase Resume commands. The Status Register can be read from any address.

The contents of the Status Register can be updated during an erase or program operation by toggling the Output Enable or Output Disable pins or by dis-activating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}, and Output Disable, V_{IH}.) the device.

The Status Register bits are summarized in Table 11, Status Register Bits. Refer to Table 11 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7)

The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is set to '0', the Program/Erase Controller is active; when bit7 is set to '1', the Program/Erase Controller is inactive.

The Program/Erase Controller Status is set to '0' immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is set to '1'.

During Program and Erase operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is set to '1'.

After the Program/Erase Controller completes its operation the Erase Status (bit5), Program Status and Tuning Protection Unlock status (bit4) bits should be tested for errors.

Erase Suspend Status (Bit 6)

The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is set to '1' (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is set to '0', the Program/Erase Controller is active or has completed its operation; when the bit is set to '1', a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns to '0'.

Erase Status (Bit 5)

The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Erase Status bit is set to '0', the memory has successfully verified that the block has erased correctly. When the Erase Status bit is set to '1', the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly.

Once set to '1', the Erase Status bit can only be reset to '0' by a Clear Status Register command or a hardware reset. If set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status, Tuning Protection Unlock Status (Bit 4)

The Program Status and Tuning Protection Unlock Status bit is used to identify a Program failure or a Tuning Protection Code verify failure. Bit4 should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When bit4 is set to '0' the memory has successfully verified that the device has programmed correctly or that the correct Tuning Protection Code has been written. When bit4 is set to '1' the device has failed to verify that the data has been programmed correctly or that the correct Tuning Protection code has been written.

Once set to 1', the Program Status bit can only be reset to '0' by a Clear Status Register command or a hardware reset. If set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3)

The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is set to '0', the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is set to '1', the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected; Program Erase, operations cannot be performed.

Once set to '1', the V_{PP} Status bit can only be reset to '0' by a Clear Status Register command or a

hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2)

The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is set to ‘1’ (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is set to ‘0’, the Program/Erase Controller is active or has completed its operation; when the bit is set to ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns to ‘0’.

Block Protection Status (Bit 1)

The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is set to ‘0’, no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is set to ‘1’, a Program or Erase operation has been attempted on a protected block.

Once set to ‘1’, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Tuning Protection Status (Bit 0)

The Tuning Protection Status bit indicates if the device is locked (Tuning Protection is enabled) or unlocked (Tuning Protection is disabled).

When the Tuning Protection Status bit is set to ‘0’ the device is locked, when it is set to ‘1’ the device is unlocked. After a reset or power-up the device is locked and so bit0 is set to ‘0’.

The Tuning Protection Status bit is set to ‘1’ for the M58BW016D version.

Table 11. Status Register Bits

Bit	Name	Logic Level	Definition
7	Program/Erase Controller Status	’1’	Ready
		’0’	Busy
6	Erase Suspend Status	’1’	Suspended
		’0’	In Progress or Completed
5	Erase Status	’1’	Erase Error
		’0’	Erase Success
4	Program Status, Tuning Protection Unlock Status	’1’	Program Error
		’0’	Program Success
3	V_{PP} Status	’1’	V_{PP} Invalid, Abort
		’0’	V_{PP} OK
2	Program Suspend Status	’1’	Suspended
		’0’	In Progress or Completed
1	Erase/Program in a Protected Block	’1’	Program/Erase on Protected Block, Abort
		’0’	No Operations to Protected Sectors
0	Tuning Protection Status	’1’	Tuning Protection Disabled(1)
		’0’	Tuning Protection Enabled

Note: 1. For the M58BW016D version the Tuning Protection Status bit is always set to ‘1’.

MAXIMUM RATING

Stressing the device above the ratings listed in Table 12, Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	155	°C
V_{IO}	Input or Output Voltage	–0.6	V_{DDQ} +0.6 V_{DDQIN} +0.6	V
V_{DD}, V_{DDQ}, V_{DDQIN}	Supply Voltage	–0.6	4.2	V
V_{PP}	Program Voltage	–0.6	13.5 (1)	V

Note: Cumulative time at a high voltage level of 13.5V should not exceed 80 hours on V_{PP} pin.

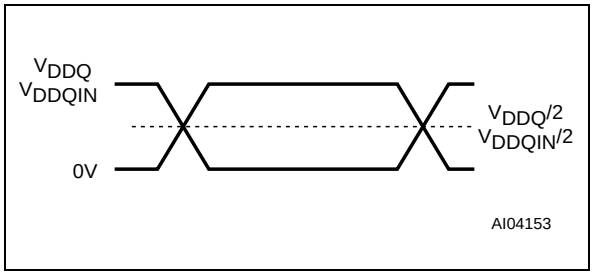
DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 13, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating and AC Measurement Conditions

Parameter		Value		Units
		Min	Max	
Supply Voltage (V_{DD})		2.7	3.6	V
Input/Output Supply Voltage (V_{DDQ})		2.4	V_{DD}	V
Ambient Temperature (T_A)	Grade 6	–40	90	°C
	Grade 3	–40	125	°C
Load Capacitance (C_L)		60		pF
Clock Rise and Fall Times			4	ns
Input Rise and Fall Times			4	ns
Input Pulses Voltages		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages		$V_{DDQ}/2$		V

Figure 7. AC Measurement Input Output Waveform



Note: $V_{DD} = V_{DDQ}$.

Figure 8. AC Measurement Load Circuit

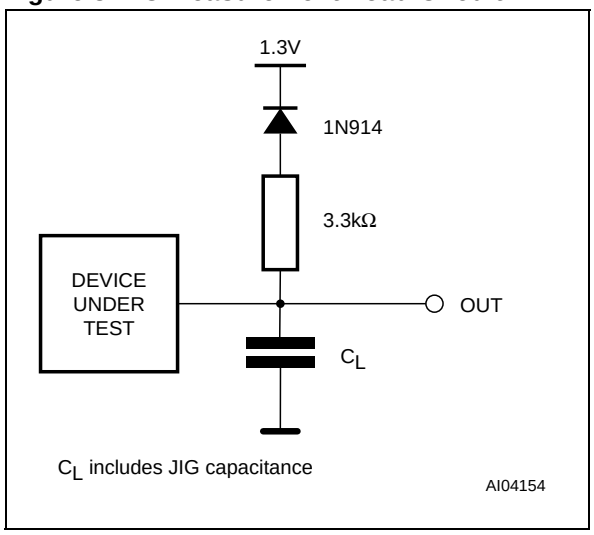


Table 14. Device Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Note: 1. T_A = 25°C, f = 1 MHz
2. Sampled only, not 100% tested.

Table 15. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$		±5	µA
I_{DD}	Supply Current (Random Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{add} = 6MHz		20	mA
I_{DDB}	Supply Current (Burst Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{clock} = 56MHz		30	mA
I_{DD1}	Supply Current (Standby)	$\overline{E} = \overline{RP} = V_{DD} \pm 0.2V$		60	µA
	Supply Current (Auto Low-Power)	$\overline{E} = V_{SS} \pm 0.2V$, $\overline{RP} = V_{DD} \pm 0.2V$		60	µA
I_{DD2}	Supply Current (Reset/Power-down)	$\overline{RP} = V_{SS} \pm 0.2V$		60	µA
I_{DD3}	Supply Current (Program or Erase, Set Lock Bit, Erase Lock Bit)	Program, Block Erase in progress		30	mA
I_{DD4}	Supply Current (Erase/Program Suspend)	$\overline{E} = V_{IH}$		40	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} \ge V_{PP1}$		± 30	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{PP1}$		± 30	µA
I_{PP2}	Program Current (Power-down)	$\overline{RP} = V_{IL}$		± 5	µA
I_{PP3}	Program Current (Program) Program in Progress	$V_{PP} = V_{PP1}$		200	µA
		$V_{PP} = V_{PPH}$		20	mA
I_{PP4}	Program Current (Erase) Erase in Progress	$V_{PP} = V_{PP1}$		200	µA
		$V_{PP} = V_{PPH}$		20	mA
V_{IL}	Input Low Voltage		–0.5	$0.2V_{DDQIN}$	V
V_{IH}	Input High Voltage (for DQ lines)		$0.8V_{DDQIN}$	V_{DDQ} +0.3	V
V_{IH}	Input High Voltage (for Input only lines)		$0.8V_{DDQIN}$	3.6	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA		0.1	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{DDQ} –0.1		V
V_{PP1}	Program Voltage (Program or Erase operations)		2.7	3.6	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)			2.2	V

Figure 9. Asynchronous Bus Read AC Waveforms

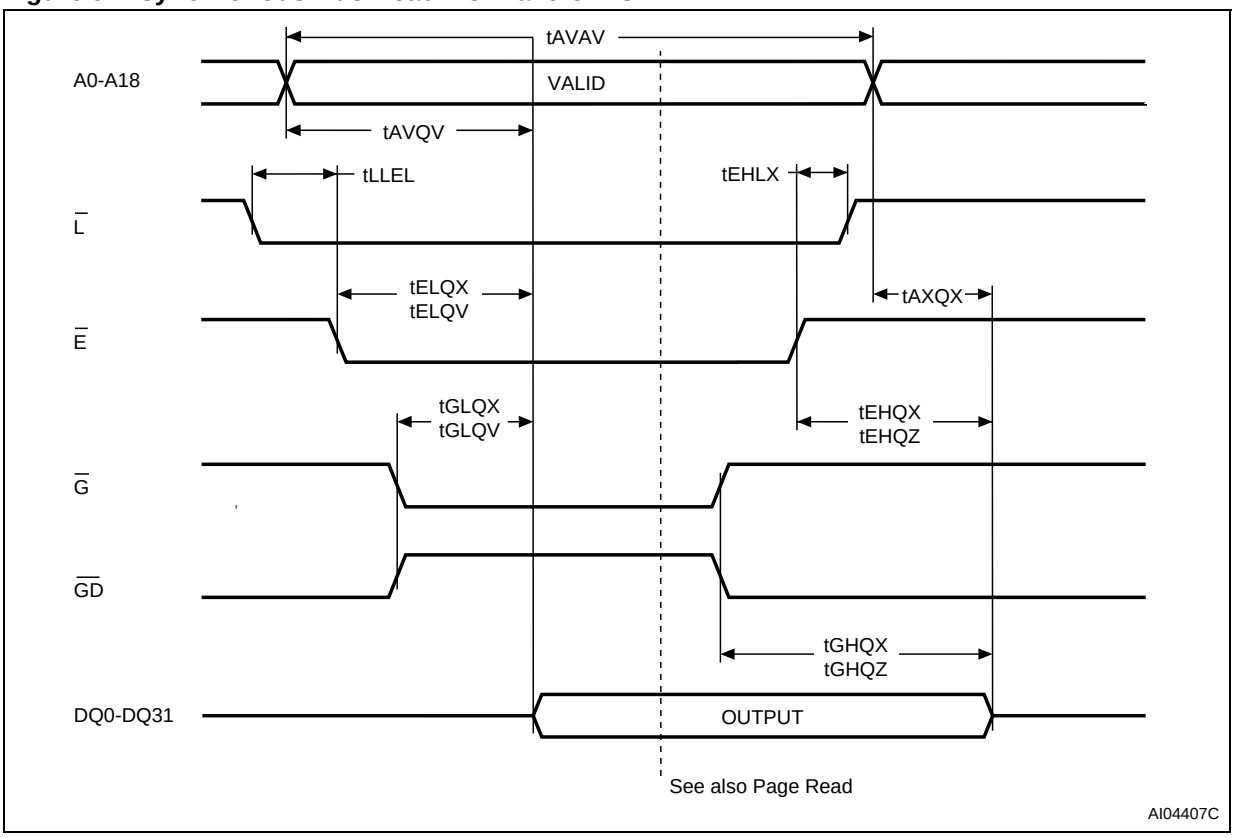


Table 16. Asynchronous Bus Read AC Characteristics.

Symbol	Parameter	Test Condition		M58BW016			Unit
				80	90	100	
t_{AVAV}	Address Valid to Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	80	90	100	ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	80	90	100	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	0	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	0	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	20	20	20	ns
t_{ELQV}(1)	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	80	90	100	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	0	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	15	15	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	25	25	ns
t_{GLQX}	Output Enable to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{LLEL}	Latch Enable Low to Chip Enable Low		Min	0	0	0	ns

Note: 1. Output Enable $\overline{G}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of Chip Enable $\overline{E}$ without increasing t_{ELQV}.

Figure 10. Asynchronous Latch Controlled Bus Read AC Waveforms

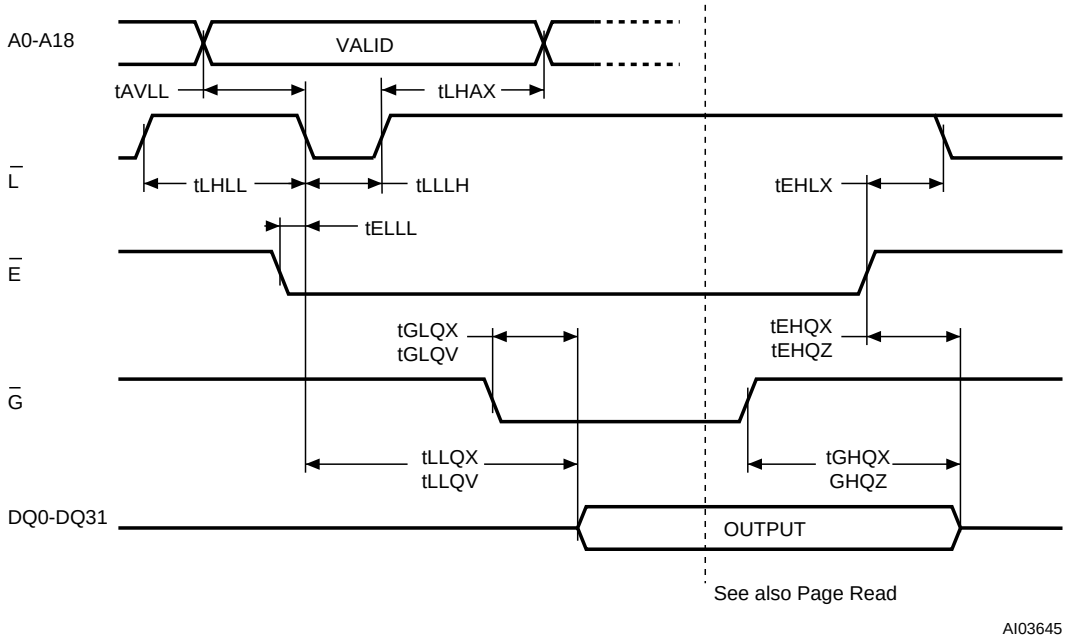


Table 17. Asynchronous Latch Controlled Bus Read AC Characteristics

Symbol	Parameter	Test Condition		M58BW016			Unit
				80	90	100	
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	0	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	20	20	20	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	0	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	15	15	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	25	25	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	5	5	5	ns
t_{LHLL}	Latch Enable High to Latch Enable Low		Min	10	10	10	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	10	ns
t_{LLQV}	Latch Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	80	90	100	ns
t_{LLQX}	Latch Enable Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	0	ns

Figure 11. Asynchronous Page Read AC Waveforms

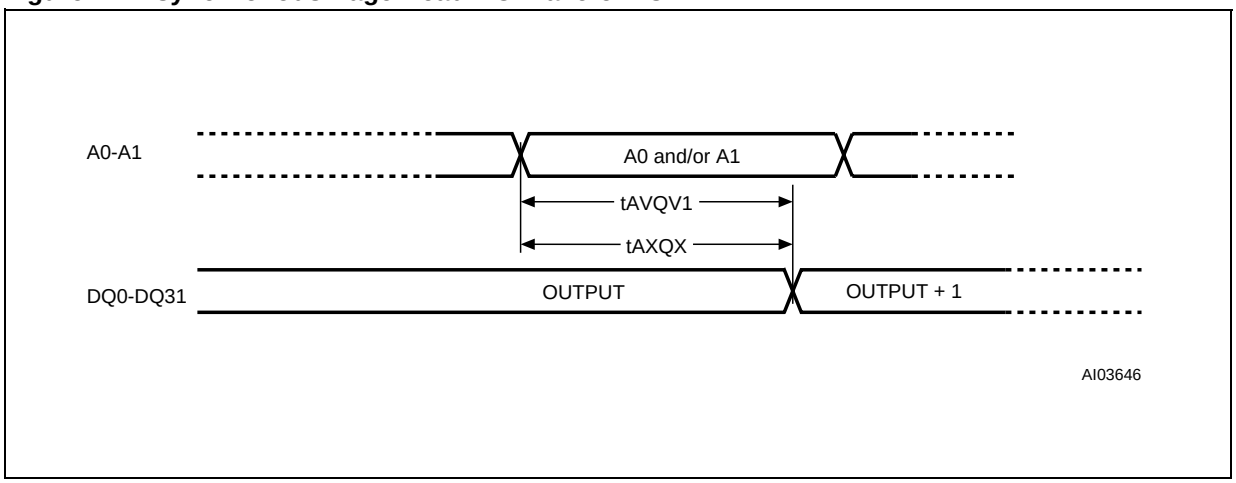


Table 18. Asynchronous Page Read AC Characteristics

Symbol	Parameter	Test Condition		M58BW016			Unit
				80	90	100	
t_{AVQV1}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	25	25	25	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	6	6	6	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 12. Asynchronous Write AC Waveform

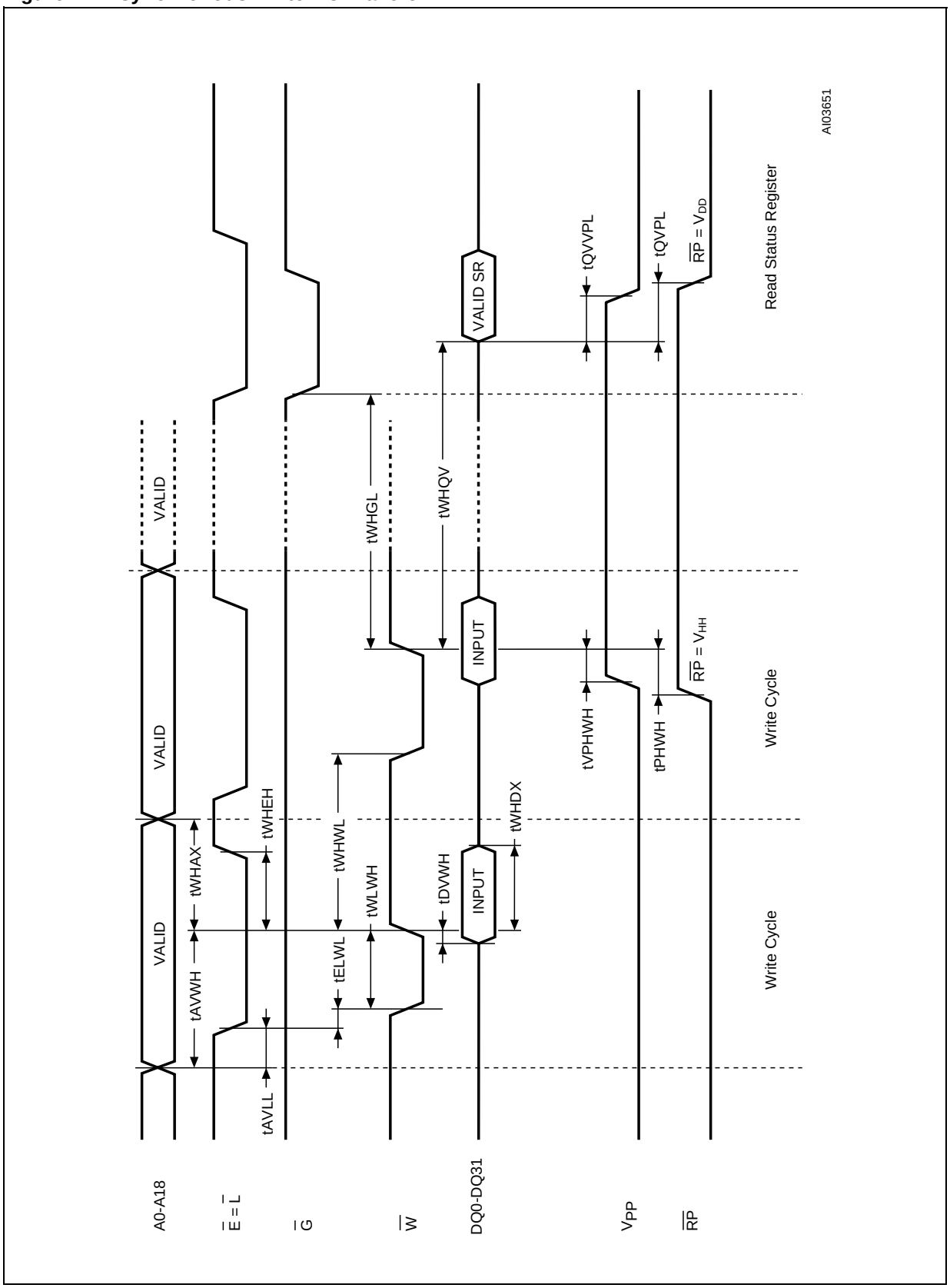


Figure 13. Asynchronous Latch Controlled Write AC Waveform

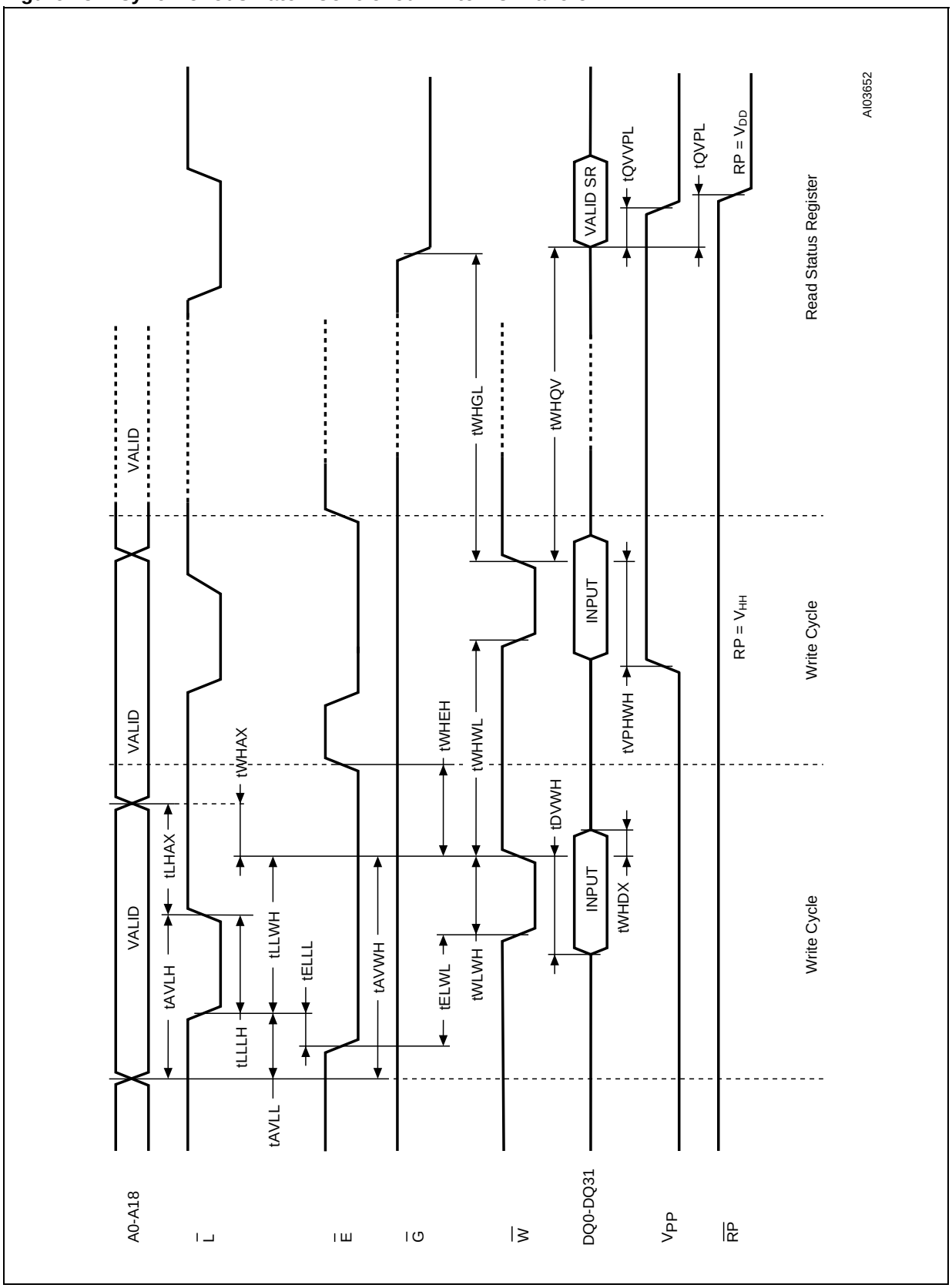


Table 19. Asynchronous Write and Latch Controlled Write AC Characteristics

Symbol	Parameter	Test Condition		M58BW016			Unit
				80	90	100	
t_{AVLL}	Address Valid to Latch Enable Low		Min	0	0	0	ns
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	50	ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	50	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	0	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	5	5	5	ns
t_{LLLH}	Latch Enable Low to Latch Enable High		Min	10	10	10	ns
t_{LLWH}	latch Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	50	ns
t_{QVVPL}	Output Valid to V_{PP} Low		Min	0	0	0	ns
t_{VPHWH}	V_{PP} High to Write Enable High		Min	0	0	0	ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	0	0	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	150	150	150	ns
t_{WHQV}	Write Enable High to Output Valid		Min	175	175	175	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	20	20	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	60	60	60	ns
t_{QVPL}	Output Valid to Reset/Power-down Low		Min	0	0	0	ns

Figure 14. Synchronous Burst Read (Data Valid from 'n' Clock Rising Edge)

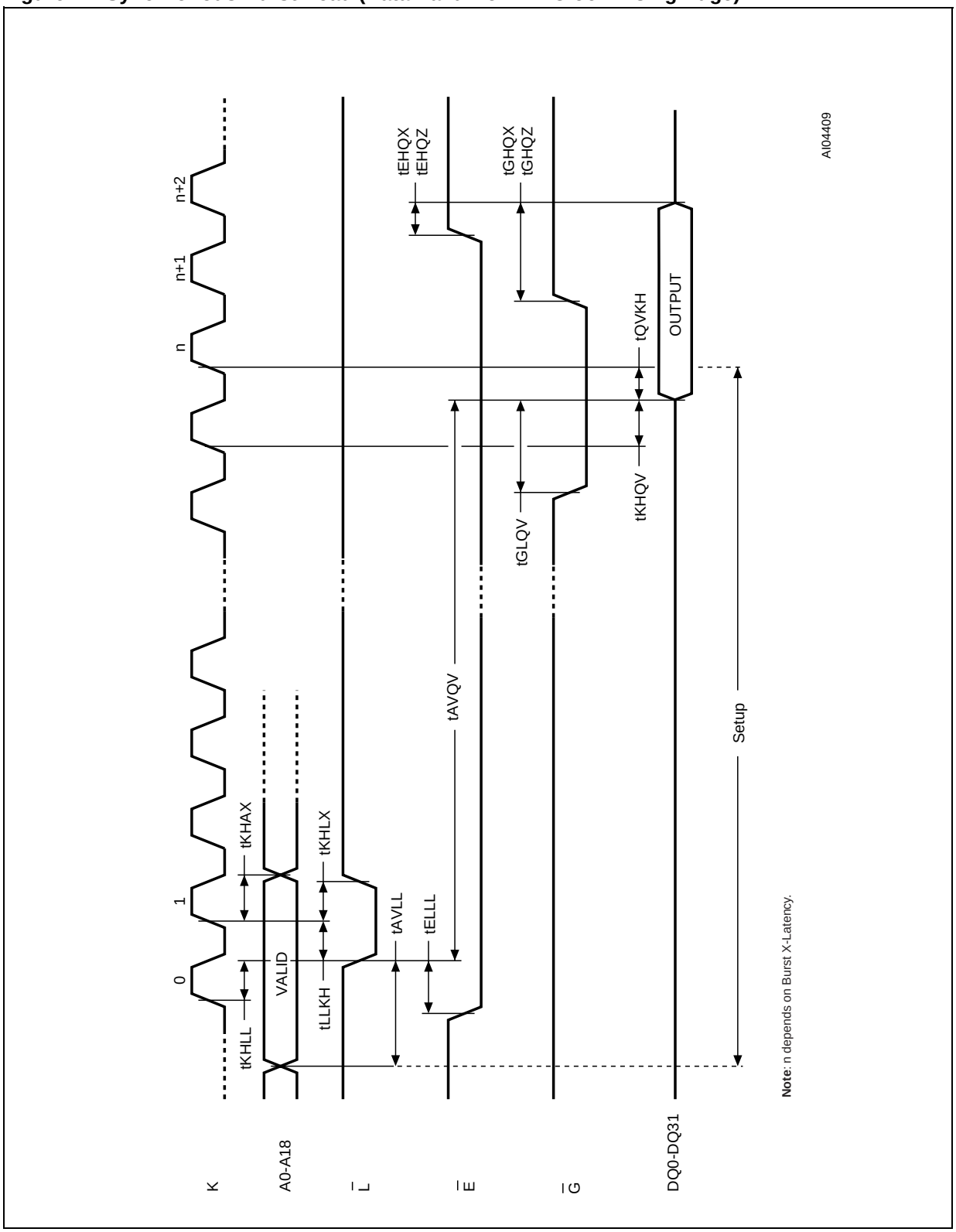
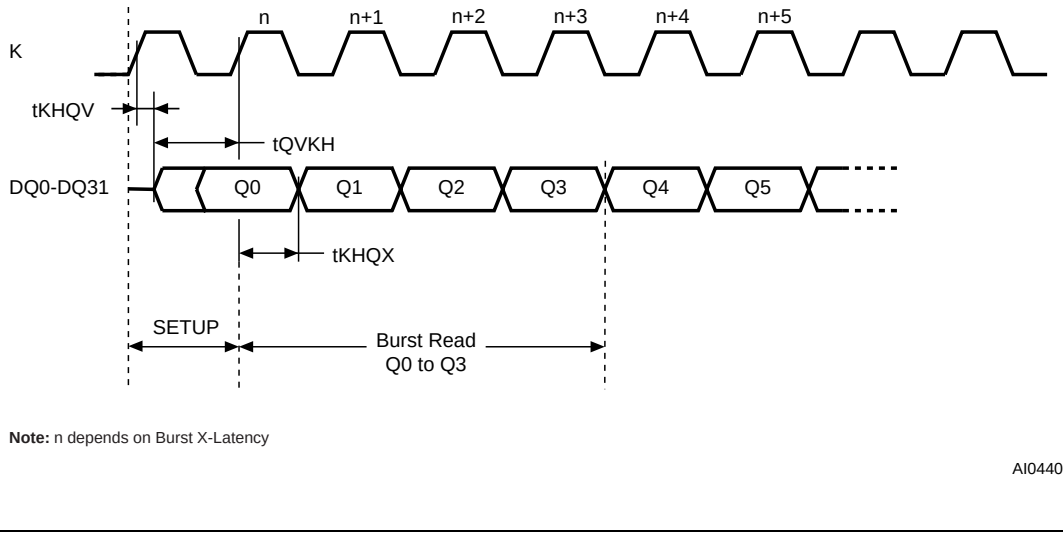


Table 20. Synchronous Burst Read AC Characteristics

Symbol	Parameter	Test Condition		M58BW016			Unit
				80	90	100	
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{BHKH}	Burst Address Advance High to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	8	8	8	ns
t_{BLKH}	Burst Address Advance Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	8	8	8	ns
t_{ELLL}	Chip Enable Low to Latch Enable low		Min	0	0	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{L} = V_{IH}$	Min	25	25	25	ns
t_{KHAX}	Valid Clock Edge to Address Transition	$\overline{E} = V_{IL}$	Min	5	5	5	ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{KHLX}	Valid Clock Edge to Latch Enable Transition	$\overline{E} = V_{IL}$	Min	0	0	0	ns
t_{KHQX}	Valid Clock Edge to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	3	3	3	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$	Min	6	6	6	ns
t_{QVKH}(1)	Output Valid to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	6	6	6	ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	6	6	6	ns
t_{KHQV}	Valid Clock Edge to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Max	10	10	10	ns

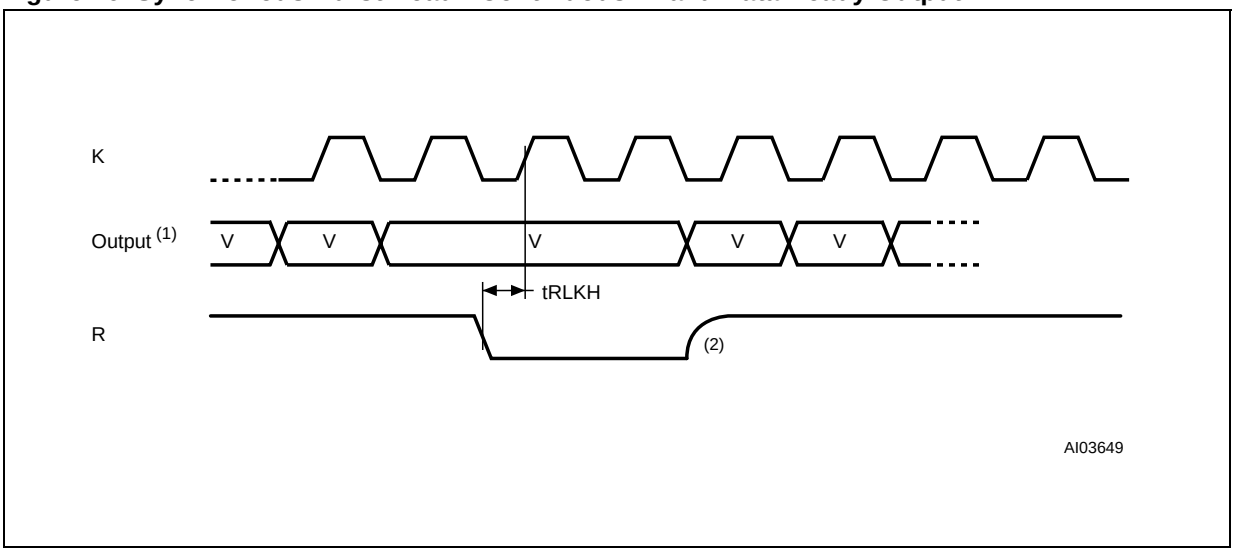
Note: 1. Data output should be read on the valid clock edge.
2. For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 15. Synchronous Burst Read (Data Valid from 'n' Clock Rising Edge)



Note: For set up signals and timings see Synchronous Burst Read.

Figure 16. Synchronous Burst Read - Continuous - Valid Data Ready Output



Note: Valid Data Ready = Valid Low during valid clock edge

1. V= Valid output.
2. R is an open drain output with an internal pull up resistor of 1MΩ. The internal timing of R follows DQ. An external resistor, typically 300kΩ. for a single memory on the R bus, should be used to give the data valid set up time required to recognize that valid data is available on the next valid clock edge.

Figure 17. Synchronous Burst Read - Burst Address Advance

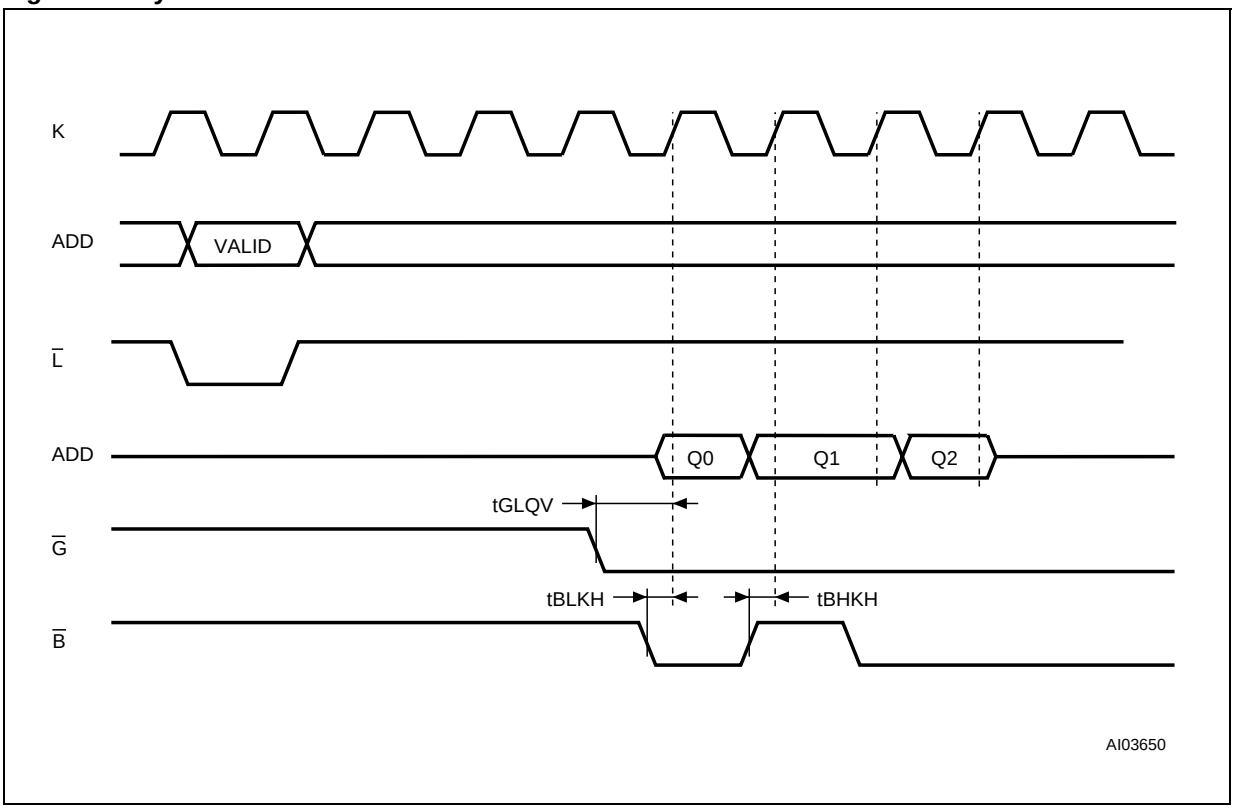


Figure 18. Reset, Power-Down and Power-up AC Waveform

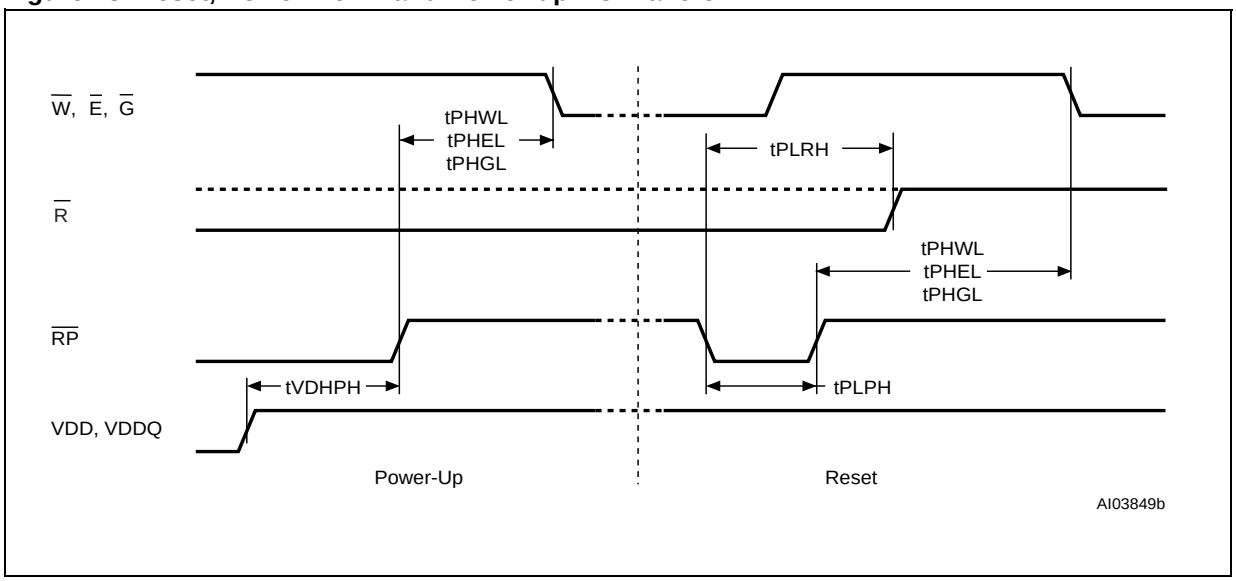


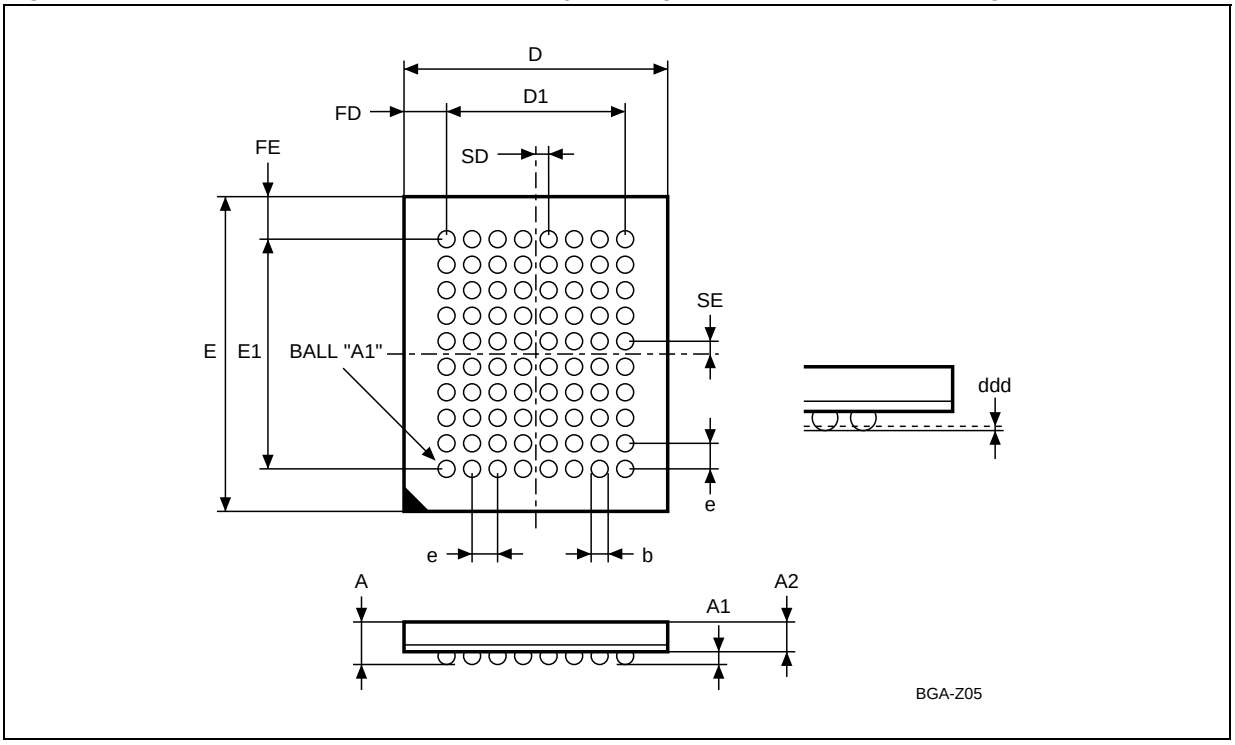
Table 21. Reset, Power-Down and Power-up AC Characteristics

Symbol	Parameter	Min	Max	Unit
t_{PHEL}	Reset/Power-down High to Chip Enable Low	50		ns
t_{PHQV} (1)	Reset/Power-down High to Output Valid		130	ns
t_{PHWL}	Reset/Power-down High to Write Enable Low	50		ns
t_{PHGL}	Reset/Power-down High to Output Enable Low	50		ns
t_{PLPH}	Reset/Power-down Low to Reset/Power-down High	100		ns
t_{PLRH}	Reset/Power-down Low to Valid Data Ready High	2	30	µs
t_{VDHPH}	Supply Voltages High to Reset/Power-down High	10		µs

Note: 1. This time is $t_{PHEL} + t_{AVQV}$ or $t_{PHEL} + t_{ELQV}$.

PACKAGE MECHANICAL

Figure 19. LBGA80 10x12mm - 8x10 ball array, 1mm pitch, Bottom View Package Outline

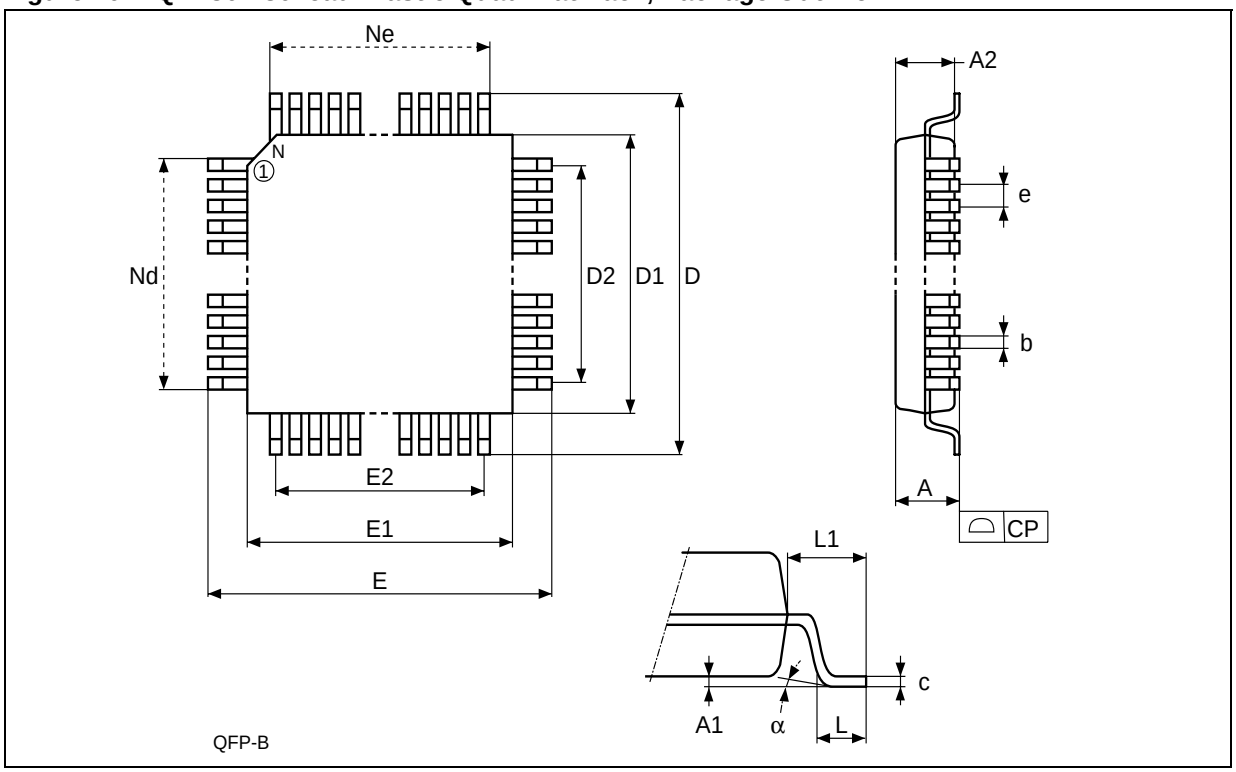


Note: Drawing is not to scale.

Table 22. LBGA80 10x12mm - 8x10 ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.700			0.0669
A1	0.400	0.350	0.450	0.0157	0.0138	0.0177
A2	1.100			0.0433		
b	0.500	–	–	0.0197	–	–
D	10.000	–	–	0.3937	–	–
D1	7.000	–	–	0.2756	–	–
ddd			0.150			0.0059
E	12.000	–	–	0.4724	–	–
E1	9.000	–	–	0.3543	–	–
e	1.000	–	–	0.0394	–	–
FD	1.500	–	–	0.0591	–	–
FE	1.500	–	–	0.0591	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

Figure 20. PQFP80 - 80 lead Plastic Quad Flat Pack, Package Outline



Note: Drawing is not to scale.

Table 23. PQFP80 - 80 lead Plastic Quad Flat Pack, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.400			0.1339
A1		0.250			0.0098	
A2	2.800	2.550	3.050	0.1102	0.1004	0.1201
b		0.300	0.450		0.0118	0.0177
c		0.130	0.230		0.0051	0.0091
D	23.200	22.950	23.450	0.9134	0.9035	0.9232
D1	20.000	19.900	20.100	0.7874	0.7835	0.7913
D2	18.400	–	–	0.7244	–	–
e	0.800	–	–	0.0315	–	–
E	17.200	16.950	17.450	0.6772	0.6673	0.6870
E1	14.000	13.900	14.100	0.5512	0.5472	0.5551
E2	12.000	–	–	0.4724	–	–
L	0.800	0.650	0.950	0.0315	0.0256	0.0374
L1	1.600	–	–	0.0630	–	–
α		0°	7°		0°	7°
N	80			80		
Nd	24			24		
Ne	16			16		

PART NUMBERING

Table 24. Ordering Information Scheme

Example: M58BW016B T 80 T 3 T

Device Type
M58

Architecture
B = Burst Mode

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = V_{DDQIN} =2.4 to V_{DD}

Device Function
016B = 16 Mbit (x32), Boot Block, Burst Tuning Protection
016D = 16 Mbit (x32), Boot Block, Burst no Tuning Protection

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
80 = 80ns
90 = 90ns
100 = 100ns

Package
T = PQFP80
ZA = LBGA80: 1.0mm pitch

Temperature Range
3 = –40 to 125 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 25. Document Revision History

Date	Version	Revision Details
January-2001	-01	First Issue.
05-Jun-2001	-02	Major rewrite and restructure.
15-Jun-2001	-03	Nd and Ne values changed in PQFP80 Package Mechanical Table
17-Jul-2001	-04	PQFP80 Package Outline Drawing and Mechanical Data Table updated
17-Dec-2001	-05	tLEAD removed from Absolute Maximum Ratings (Table 12) 80, 90 and 100ns Speed classes defined (Tables 16, 17, 18, 19 and 20 clarified accordingly) Figures 14, 15, 16 and 17 clarified Temperature range 3 and 6 added Tables 13, 14, 15, 21 and CFI Tables 27, 28, 29, 30 clarified Document status changed from Product Preview to Preliminary Data
17-Jan-2002	-06	DC Characteristics I_{PP}, I_{PP1} and I_{DD1} clarified AC Bus Read Characteristics timing t_{GHQZ} clarified
30-Aug-2002	6.1	Revision numbering modified: a minor revision will be indicated by incrementing the tenths digit, and a major revision, by incrementing the units digit of the previous version (e.g. revision version 06 becomes 6.0). References of V_{PP} pin used for block protection purposes removed. Figure 9 modified.
4-Sep-2002	7.0	Datasheet status changed from Preliminary Data to full Datasheet. t_{WLWH} parameter modified in Table 19, Asynchronous Write and Latch Controlled Write AC Characteristics.

APPENDIX A. COMMON FLASH INTERFACE - CFI

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 26, 27, 28, 29 and 30 show the addresses used to retrieve the data.

Table 26. Query Structure Overview

Offset	Sub-section Name	Description
00h		Manufacturer Code
01h		Device Code
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash memory layout
P(h)(1)	Primary Algorithm-specific Extended Query Table	Additional information specific to the Primary Algorithm (optional)
A(h)(2)	Alternate Algorithm-specific Extended Query Table	Additional information specific to the Alternate Algorithm (optional)

Note: 1. Offset 15h defines P which points to the Primary Algorithm Extended Query Address Table.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.

Table 27. CFI - Query Address and Data Output

Address A0-A18	Data		Instruction
10h	51h	"Q"	Query ASCII String 51h; "Q" 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	03h		Primary Vendor: Command Set and Control Interface ID Code
14h	00h		
15h	35h		Primary algorithm extended Query Address Table: P(h)
16h	00h		
17h	00h		Alternate Vendor: Command Set and Control Interface ID Code
18h	00h		
19h	00h		Alternate Algorithm Extended Query address Table
1Ah	00h		

Note: 1. The x8 or Byte Address and the x16 or Word Address mode are not available.
2. Query Data are always presented on DQ7-DQ0. DQ31-DQ8 are set to '0'.

Table 28. CFI - Device Voltage and Timing Specification

Address A0-A18	Data	Description
1Bh	27h (1)	V_{DD} min, 2.7V
1Ch	36h (1)	V_{DD} max, 3.6V
1Dh	B4h (2)	V_{PP} min
1Eh	C6h (2)	V_{PP} max
1Fh	00h (3)	2^n ms typical time-out for Word, DWord prog – Not Available
20h	00h (3)	2^n ms, typical time-out for max buffer write – Not Available
21h	0Ah	2^n ms, typical time-out for Erase Block
22h	00h (3)	2^n ms, typical time-out for chip erase – Not Available
23h	00h (3)	2^n x typical for Word Dword time-out max – Not Available
24h	00h	2^n x typical for buffer write time-out max – Not Available
25h	04h	2^n x typical for individual block erase time-out maximum
26h	00h (3)	2^n x typical for chip erase max time-out – Not Available

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.
2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volts while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
3. Not supported.

Table 29. Device Geometry Definition

Address A0-A18	Data	Description
27h	15h	2^n number of bytes memory size
28h	03h	Device Interface Sync./Async.
29h	00h	Organization Sync./Async.
2Ah	00h	Page size in bytes, 2^n
2Bh	00h	
2Ch	02h	Bit7-0 = number of Erase Block Regions in device
2Dh	1Eh	Number (n-1) of blocks of identical size; n=31
2Eh	00h	
2Fh	00h	Erase Block region information x 256 bytes per Erase Block (64Kbytes)
30h	01h	
31h	07h	Number (n-1) of blocks of identical size; n=8
32h	00h	
33h	20h	Erase Block region information x 256 bytes per Erase Block (8Kbytes)
34h	00h	

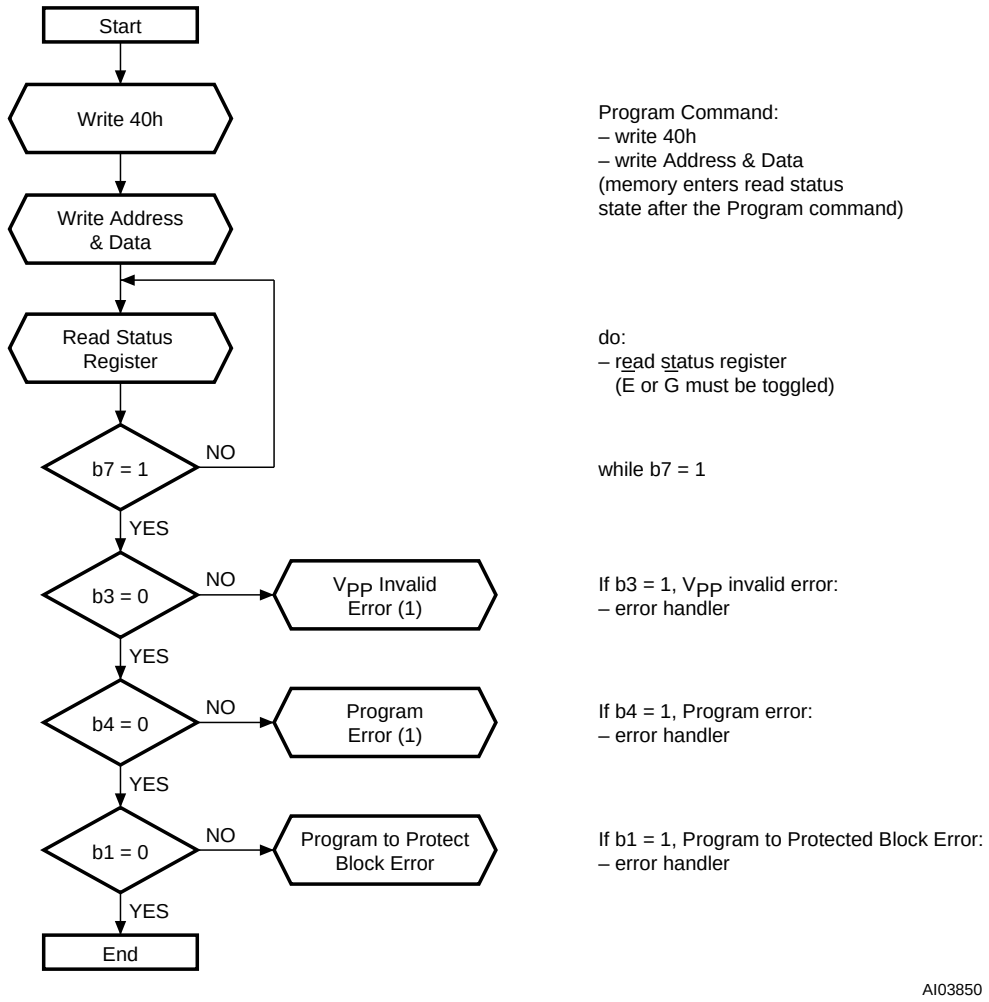
Table 30. Extended Query information

Address offset	Address A18-A0	Data (Hex)		Description
(P)h	35h	50h	"P"	Query ASCII string - Extended Table
(P+1)h	36h	52h	"R"	
(P+2)h	37h	49h	"Y"	
(P+3)h	38h	31h		Major version number
(P+4)h	39h	31h		Minor version number
(P+5)h	3Ah	86h		Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Lock/Unlock Supported (1=yes) bit4, Queue Erase Supported (0=no) Bit 31-5 reserved for future use
(P+6)h	3Bh	01h		Optional Features: Synchronous Read supported
(P+7)h	3Ch	00h		
(P+8)h	3Dh	00h		
(P+9)h	3Eh	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h	3Fh	00h (1)		Block Status Register Mask – Not Available

Note: 1. Not supported.

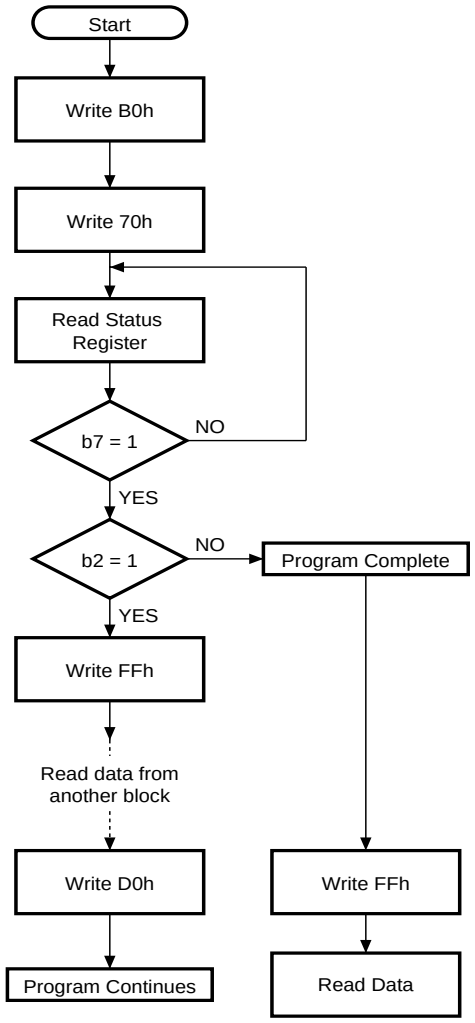
APPENDIX B. FLOW CHARTS

Figure 21. Program Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared before further P/E operations.

Figure 22. Program Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while b7 = 1

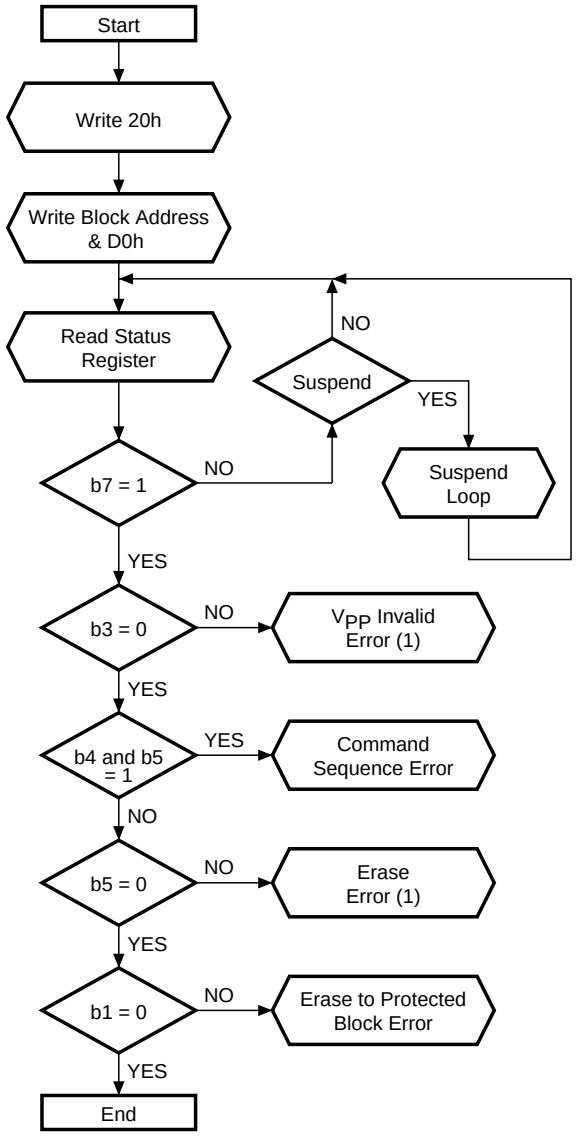
If b4 = 0, Program completed

Read Memory Array Command:
– write FFh
– one or more data reads from other blocks

Program Erase Resume Command:
– write D0h to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase Suspend command was not issued).

AI00612

Figure 23. Block Erase Flowchart and Pseudo Code



Erase Command:
– write 20h
– write Block Address
(A11-A18) & D0h
(memory enters read status state after the Erase command)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)
if Erase command given execute suspend erase loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4, b5 = 1, Command Sequence error:
– error handler

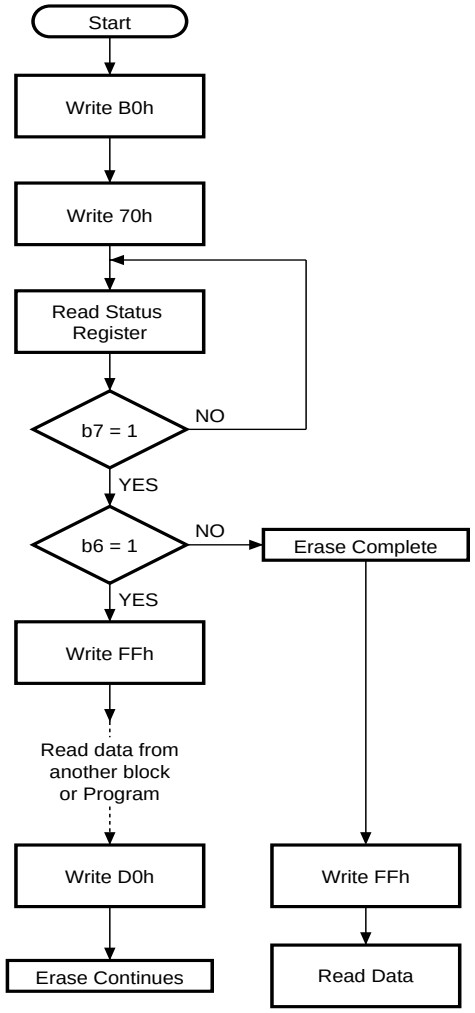
If b5 = 1, Erase error:
– error handler

If b1 = 1, Erase to Protected Block Error:
– error handler

AI03851

Note: 1. If an error is found, the Status Register must be cleared before further P/E operations.

Figure 24. Erase Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while b7 = 1

If b6 = 0, Erase completed

Read Memory Array command:
– write FFh
– one or more data reads from other blocks

Program/Erase Resume command:
– write D0h to resume the Erase operation
– if the Program operation completed then this is not necessary. The device returns to Read mode as normal (as if the Program/Erase suspend was not issued).

AI00615

Figure 25. Unlock Device and Change Tuning Protection Code Flowchart

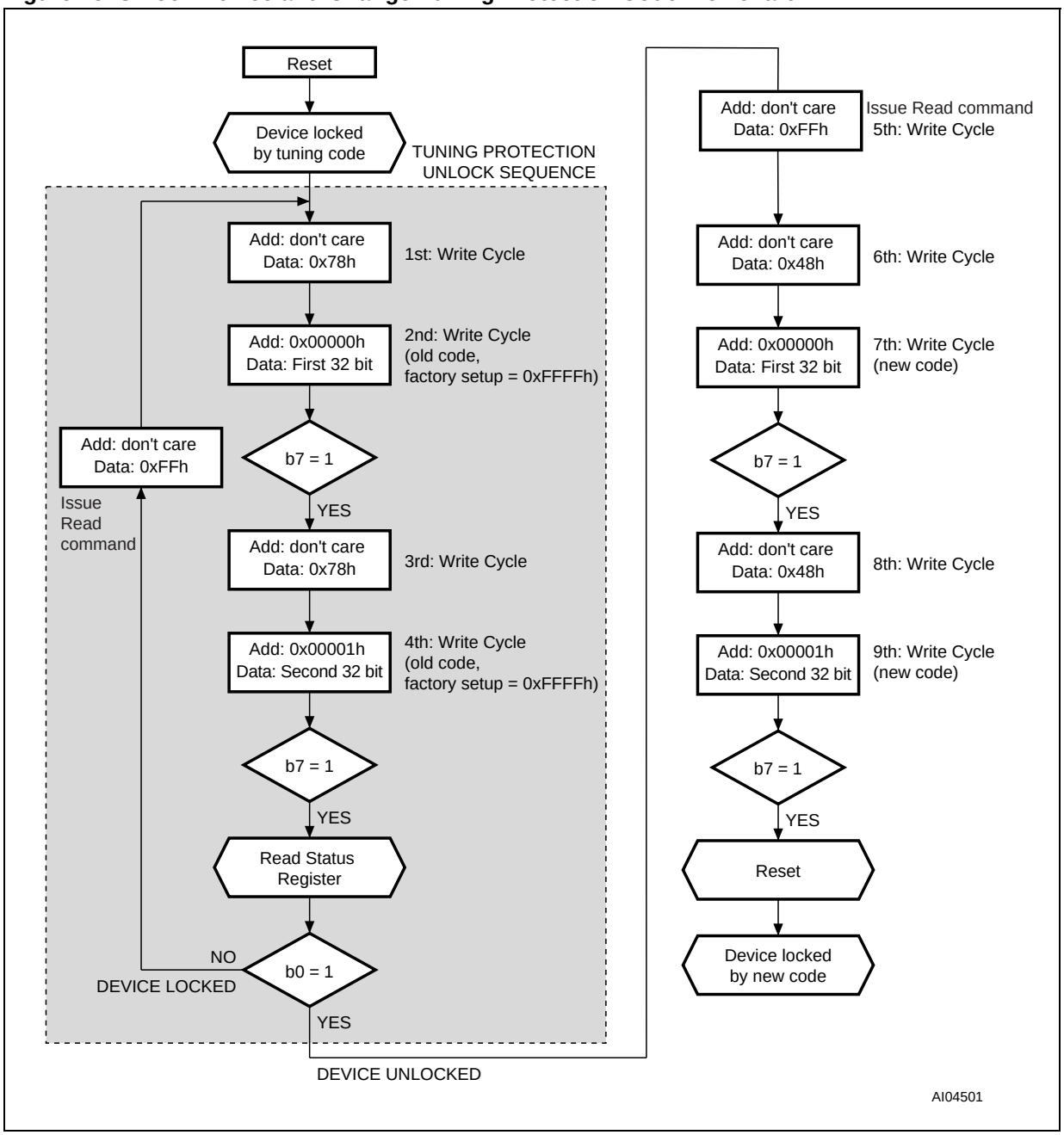


Figure 26. Unlock Device and Program a Tuning Protected Block Flowchart

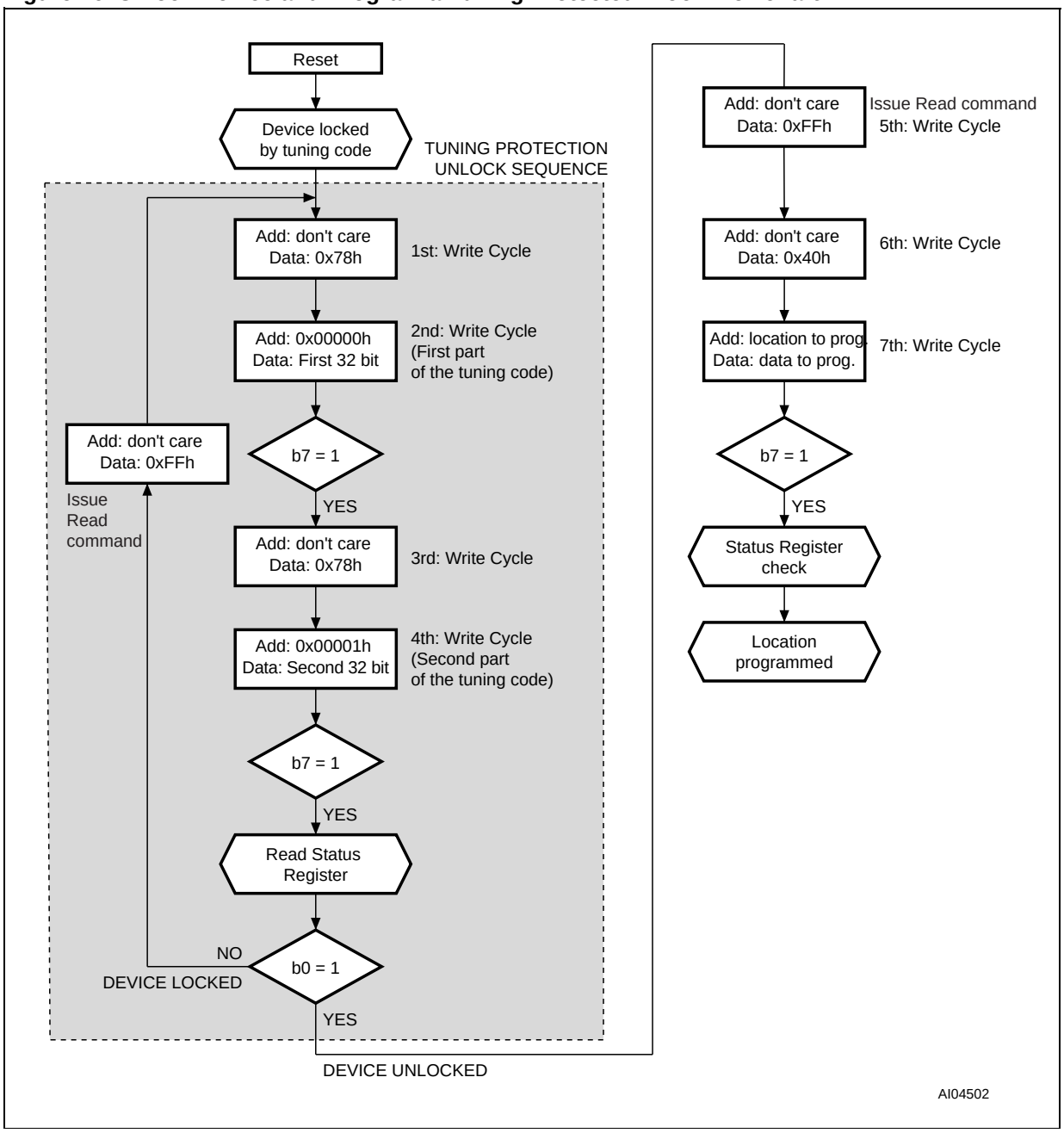


Figure 27. Unlock Device and Erase a Tuning Protected Block Flowchart

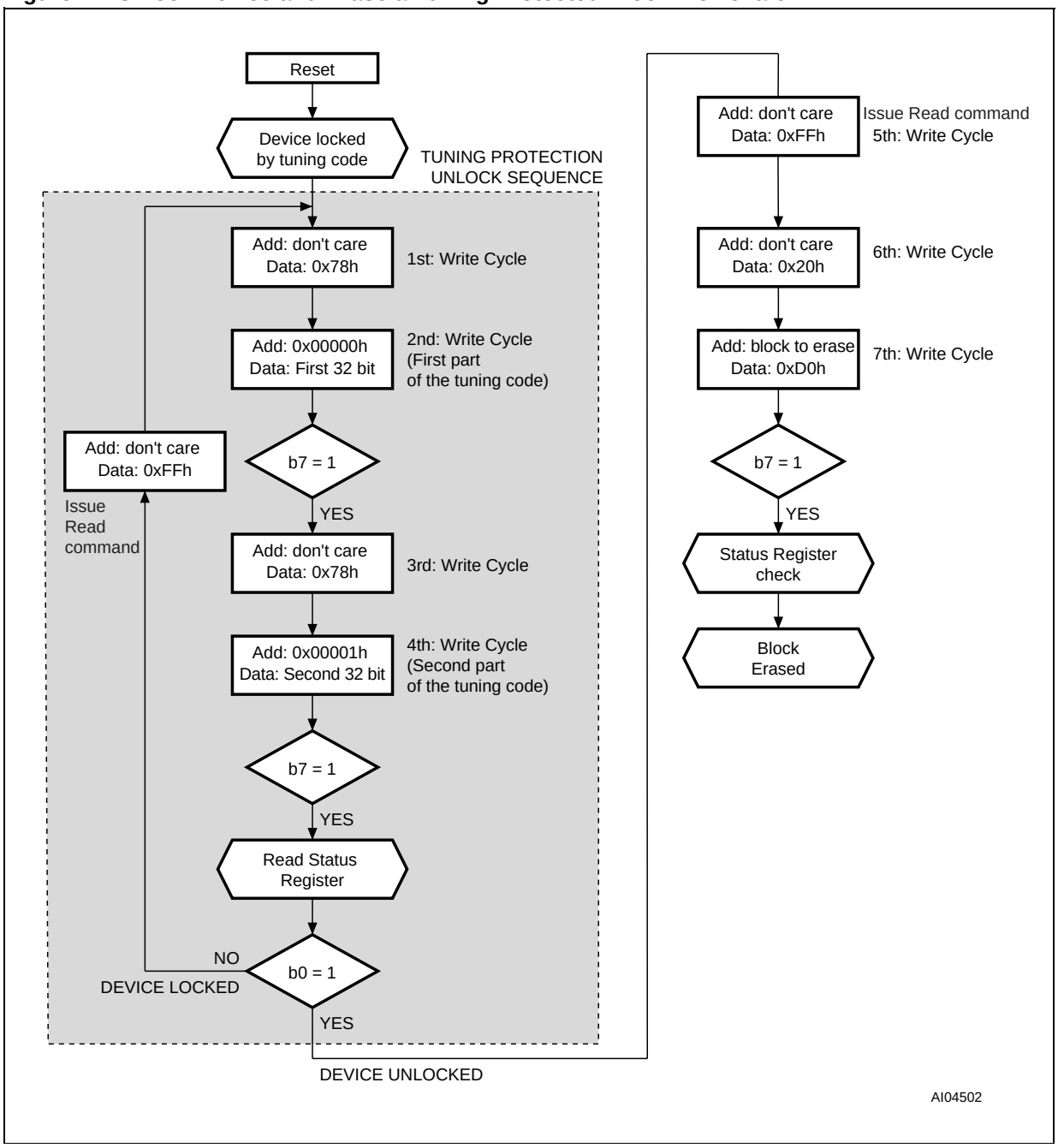


Figure 28. Power-up Sequence to Burst the Flash

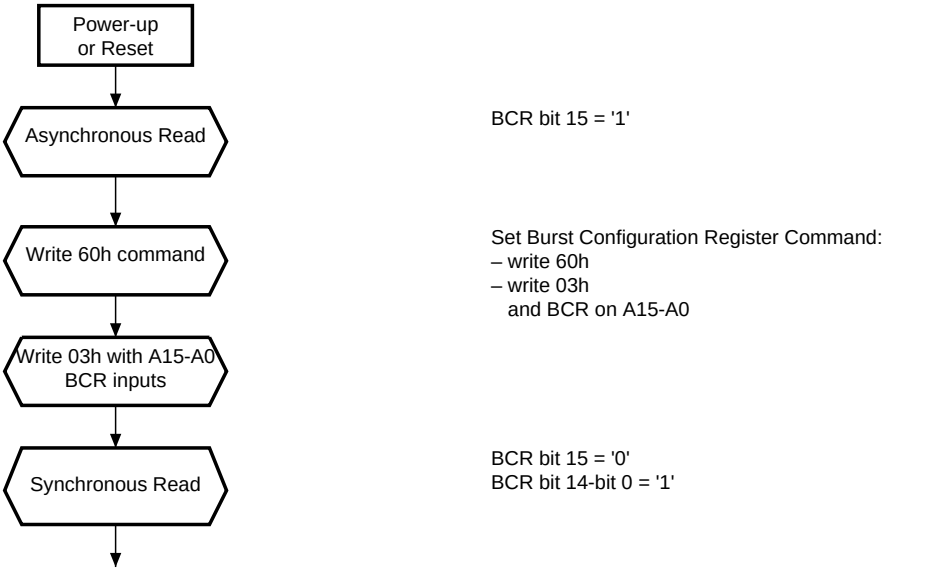


Figure 29. Command Interface and Program Erase Controller Flowchart (a)

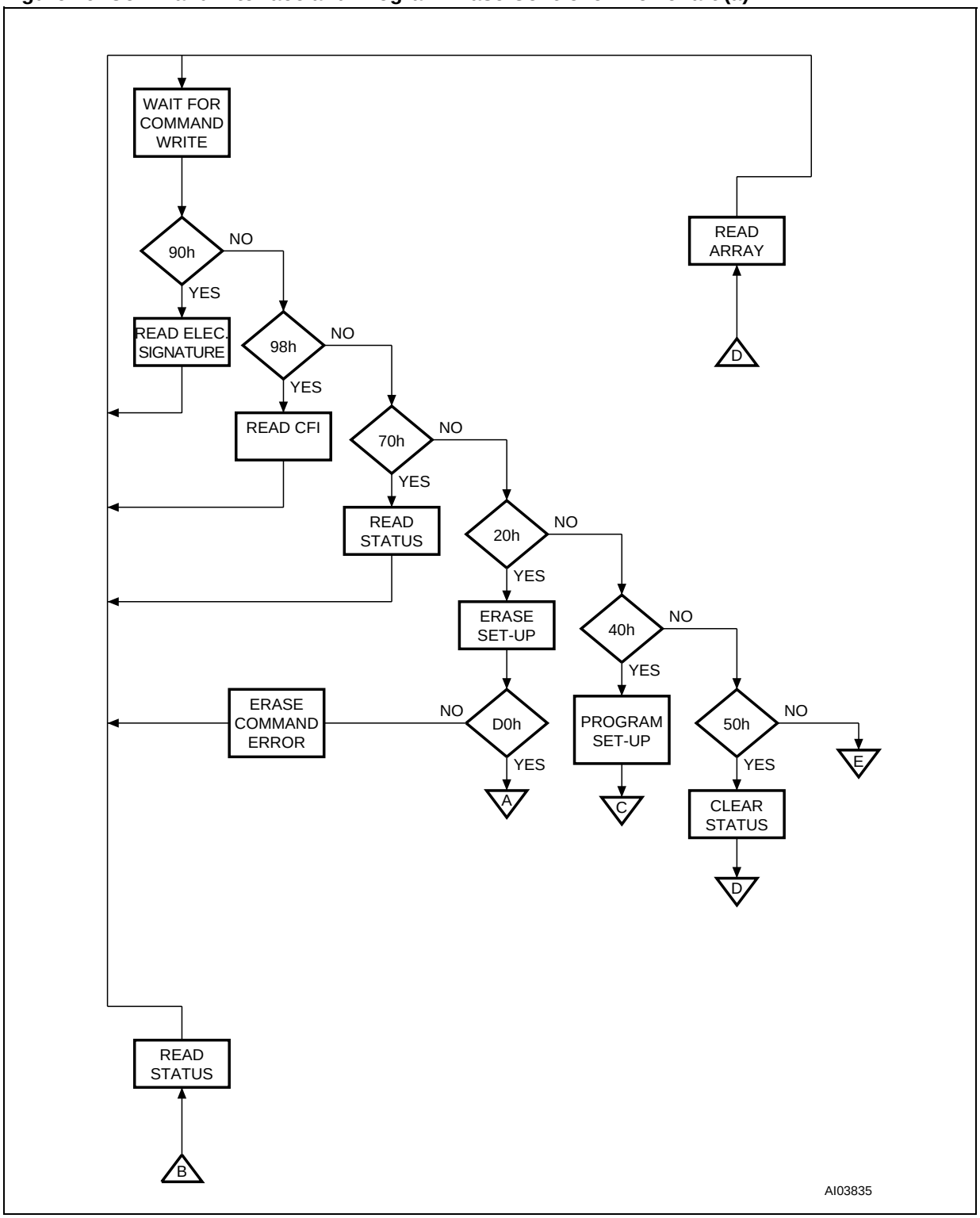


Figure 30. Command Interface and Program Erase Controller Flowchart (b)

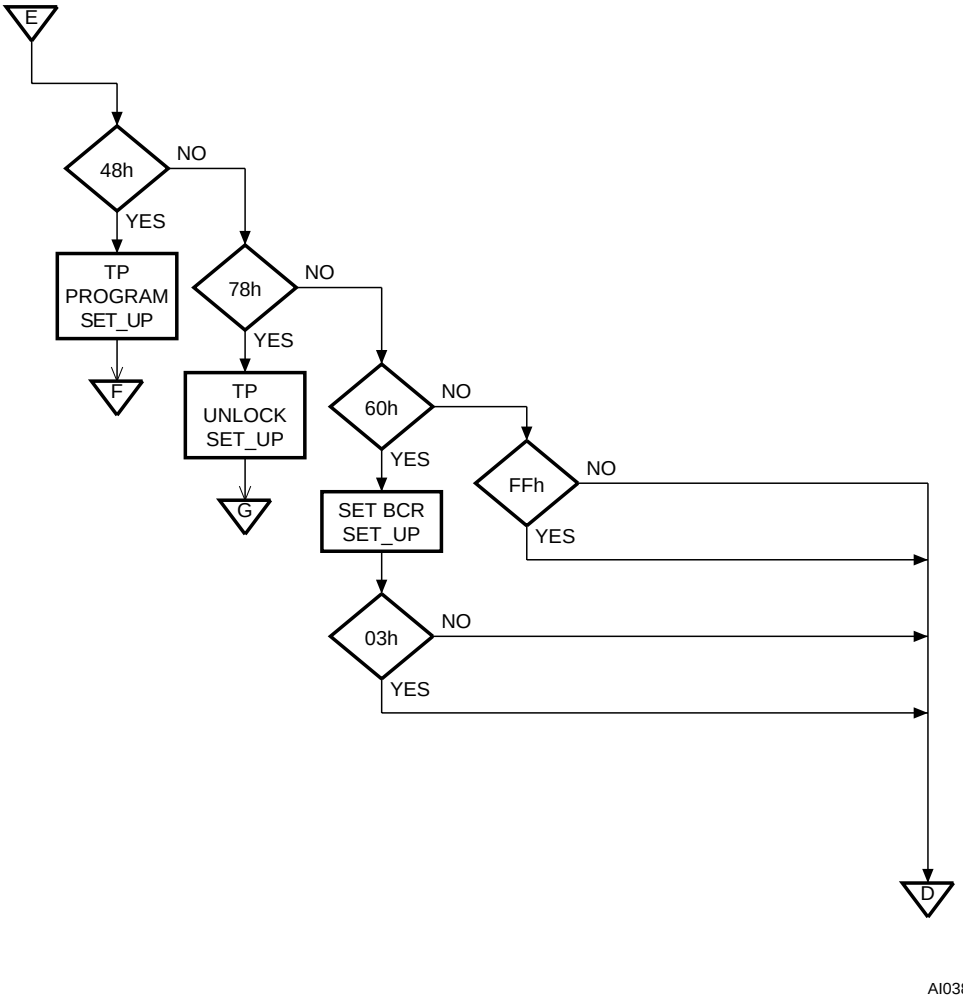


Figure 31. Command Interface and Program Erase Controller Flowchart (c)

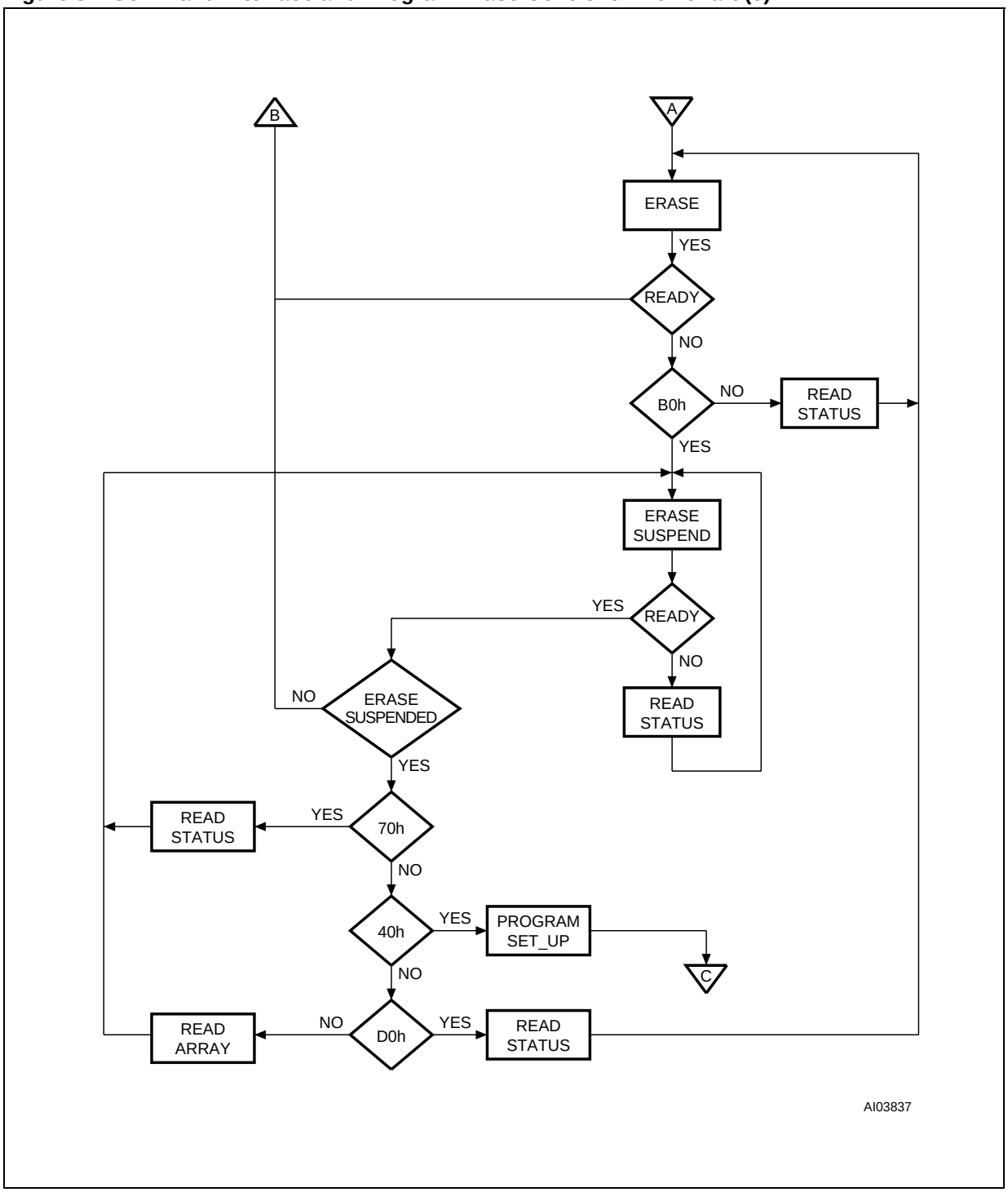


Figure 32. Command Interface and Program Erase Controller Flowchart (d)

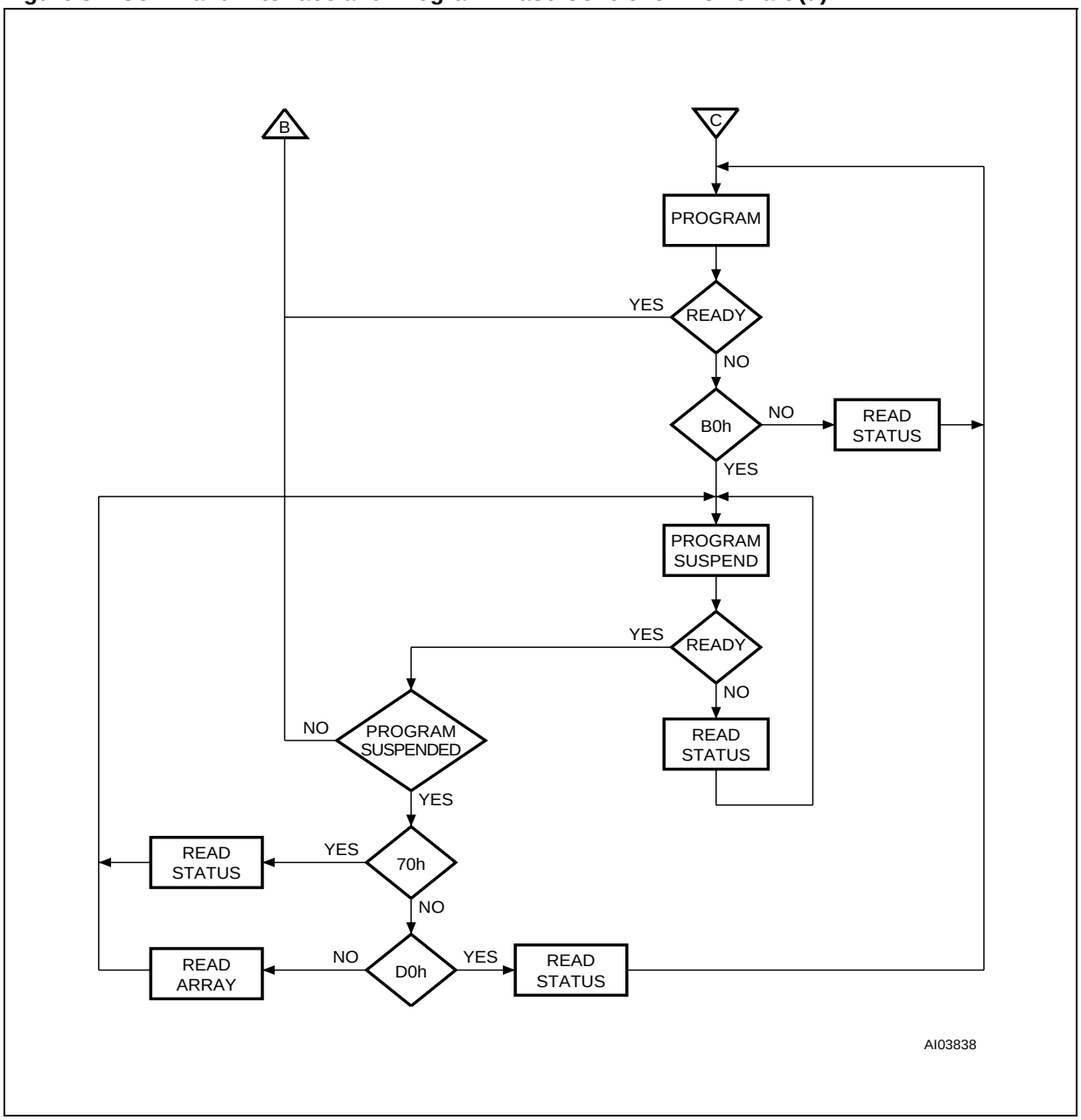
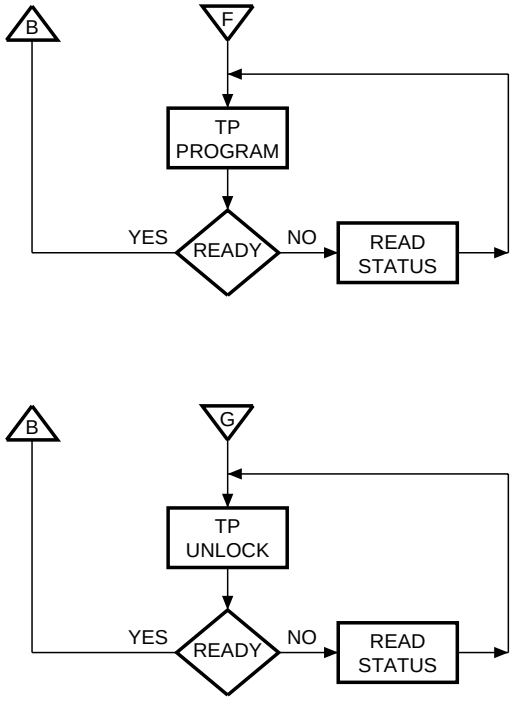


Figure 33. Command Interface and Program Erase Controller Flowchart (e)



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