Engineering Specification

Type 20.8 QXGA Monochrome TFT/LCD Module
Model Name:ITQX21H

Document Control Number : OEM I-921H-02

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
November 10,2000	OEM921H-01	All	First Edition for customer. Based on Internal Spec. EC F79103.
February 28,2002	OEM I-921H-01	 1,5,6 8 9 15 32	Updated by establishment of the New Company as "International Display Technology". To avoid using "inch" indication. To update Min. value of Backlight on signal. To update Note of Minimum White Luminance. To correct Figure of LVDS Data Order. To update Max. value of Temperature for X-Driver.
March 13,2002	OEM I-921H-02	8 10 23 28,29	To update value of Shock Test Criteria. To update J1/J2 Connector (X-cards). To correct the value of the following Timing Characteristics items. (There is no design changes.) (Min. value) : Total line (Max. value) : H-front porch H-active level H-back porch To udpate Reference Drawings.

1.0 Handling Precautions

- Damage to the panel or the panel electronics may result from any deviation from the recommended power on/off sequencing. The panel should not be hot plugged. Refer to the Power On/Off Sequence section in this Specification.
- Handle the panel with care. The LCD panel and CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may crack or break if dropped or subjected to excessive force.
- The CCFLs contain a small amount of Mercury so should not be disposed of to landfill. Dispose of as required by local ordinances or regulations.
- The LCD module contains small amounts of material having no flammability grade. The exemption conditions of the flammability requirements (4.4.3.3, IEC60950 or UL1950) should be applied.
- The panel may be damaged by the application of twisting or bending forces to the module assembly.Care should be taken in the design of the monitor housing and the assembly procedure to prevent stress damage to the panel especially the lamp cable and the lamp connector..
- Use standard earthing/grounding procedures to prevent damage to the CMOS LSI while handling the module.
- Use earthing/grounding procedures, an ionic shower, or similar to prevent static damage while removing the protective front sheet.
- The front polarizer can be easily damaged. Take care not to scratch the front surface with any hard or abrasive material. Dust, finger marks, grease etc. can be removed with a soft damp cloth (a small amount of mild detergent can be used on the damp cloth). Do not apply water or datergent directly to the front surface as this may cause staining or damage the electronic components.
- Never use any solvent on the front polarizer or module as this may cause permanent damage.
- Do not open or modify the module assembly.
- Continuous operation of the panel with the same screen content may result in some image sticking. Over 10 hours operation with the same content is not recommended.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

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2.0 General Description

This specification applies to the Type 20.8 Monochrome TFT/LCD Module 'ITQX21H'.

This module is designed for a LCD monitor style display unit.This module includes an inverter card for backlight.

The screen format and electrical interface are intended to support the QXGA (2048(H) x 1536(V)) screen.

Supported gray scale is 8-bit per 1(one) sub-pixel.

All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.

2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

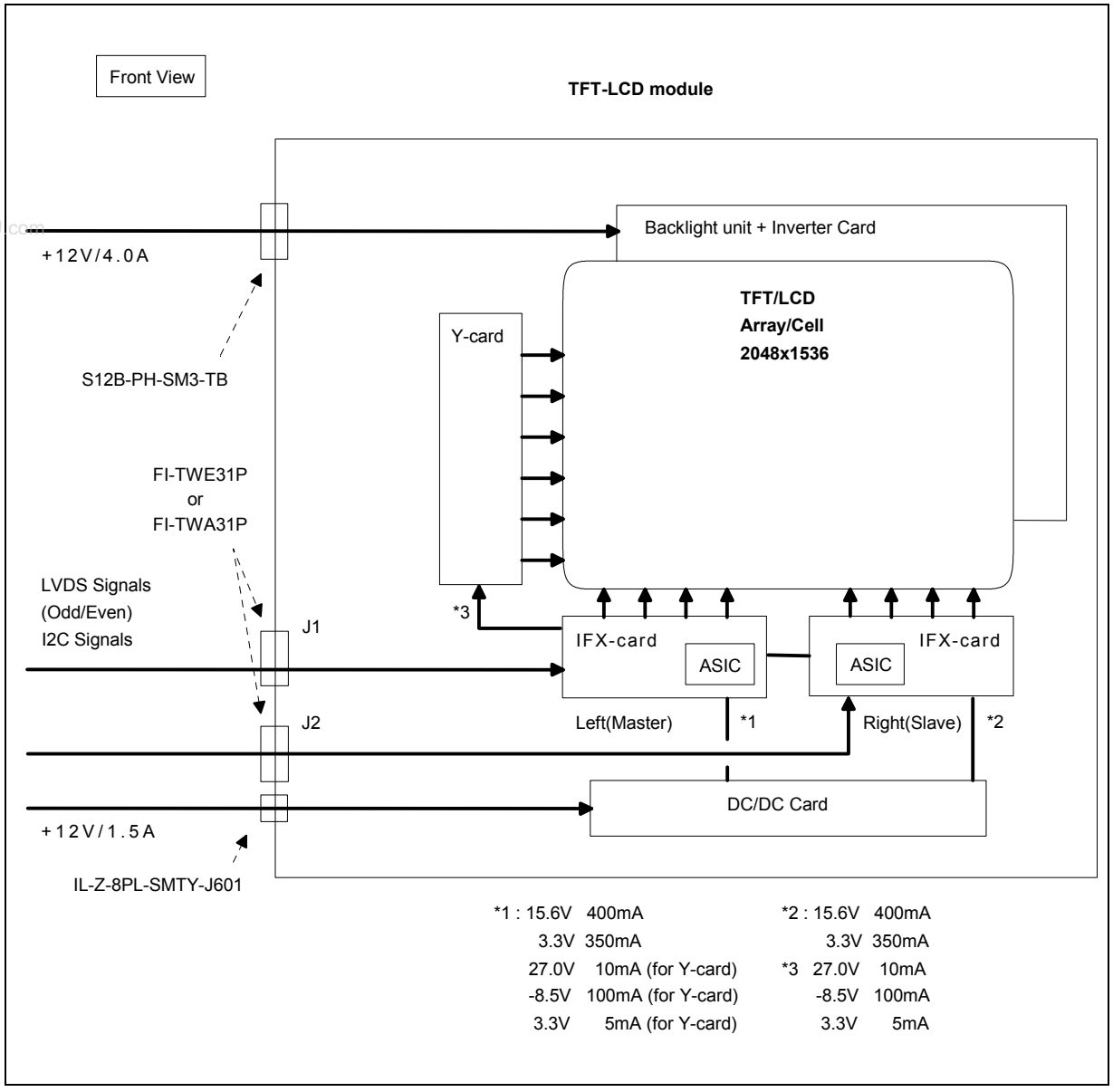
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	528
Pixels H x V	2048(x3) x 1536
Active Area [mm]	423.9(H) x 318.0(V)
Pixel Pitch [mm]	0.207 x 0.207
Pixel Arrangement	Sub-pixel Vertical Stripe
Weight [grams]	2,300 Typ.
Physical Size [mm]	457.0(W) x 350.0(H) x 45.0(D) Typ.(w/inverter)
Display Mode	Normally Black
Supported Monochrome	8-bit per 1(one) sub-pixel
White Luminance [cd/m^2]	800 Typ.
Contrast Ratio	600 : 1 Typ.(In the Dark room)
Optical Rise Time/Fall Time [msec]	50 Typ.
Input Voltage [V]	+12 +/- 5%
Power Consumption [W]	64 max
Electrical Interface	LVDS (5 Pairs) x 4 (Right x 2, Left x 2)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 **Note** -20 to +60

Note : Max. Operating Temperature 50 degree C in the Spec means the temperature measured for the point of the front surface of the LCD glass cell.

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 20.8 Monochrome TFT/LCD Module.

Type 20.8 Monochrome TFT-LCD Module Functional Block Diagram



2.2.1 Interface Summary

- 4 sets of LVDS interface for Video input (65MHz Typ per set, 24 bits total)
- Voltage control or I2C interface (3.3V) control for Brightness and Contrast Control
- Power (+12V) for Logic
- Power (+12V) for Backlight

ITQX21H TFT-LCD module does not have any frame buffer. Image expansion (Scaling) should be managed by a device driving this module and the device should supply constant timings with the frame locked to this module.

ITQX21H has 4 sets of LVDS interface and they are bundled to two channels. The screen is divided into two half-size screens (Left and Right) and each channel controls one of the half-size screens.

Each LVDS interface is named as :

- LVDS-LE (Left screen, even dot) : Left channel
- LVDS-LO (Left screen, odd dot) : Left channel
- LVDS-RE (Right screen, even dot) : Right channel
- LVDS-RO (Right screen, odd dot) : Right channel

The Left channel consists of LVDS-LE and LVDS-LO and the Right channel consists of LVDS-RE and LVDS-RO.

Each channel has the following signals.

- 4 pairs of Video and timing signals for Even dots (8 bits per pixel)
- 4 pairs of Video signals for Odd dots (8 bits per pixel)
- 1 pair of Dot Clock for Even dots
- 1 pair of Dot Clock for Odd dots

3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+13.2	V	
Backlight Voltage	VBL	-0.3	+13.2	V	
Brightness control	VDIM	-0.3	+5.3	V	
Backlight on signal	BLON	-1	+5.3	V	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Humidity	HOP	8	80	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	**(Note 2)**
Shock			50 11	G ms	**(Note 2)** Half sine wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.

Note 2 : Vibration Specification

- Sign Vibration:10-200-10Hz, 1.5G, 30 min, X, Y, Z Axis, Each One Time.

Shock Specification

- Half sine wave:50G 11msec. -X+/-, -Y+/-, -Z+/- (Total 6 directions), Each One Time Shock.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≥10 (Left) Vertical (Upper) K≥10 (Lower)	85 85 85 85	- - - -
Contrast ratio		600	-
Response Time (ms)	Rising	25	-
	Falling	25	-
White Balance	White x	0.294	-
	White y	0.309	-
Maximum White Luminance (cd/m^2)	VDIM-IN = 0V **(*1)**	800	-
Minimum White Luminance (%)	VDIM-IN = 3.0V	10	20 Max

Note:Measure center of the screen.

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

J1/J2 Connector (On X-cards)

J1/J2 Connector

Connector Name / Designation	Signal Connector
Manufacturer	JAE
Type / Part Number	FI-TWE31P-VF(Metal Shell) or FI-TWA31P-VF(Plastic Shell)
Mating connector	FI-W31S, FI-WE31M**(*1)**, FI-WE31MV**(*1)** FI-W31MV-A **(*1)**

Important Notice:
For the J1/J2 connector and there Mating connector, following combination is ***mandatory*** requirement.

J1/J2 Connector	Mating Connector (FPC side)
FI-TWE31P-VF(Metal Shell)	FI-W31S FI-WE31MV**(*1)** FI-WE31M**(*1)**
FI-TWA31P-VF(Plastic Shell)	FI-W31S FI-W31MV-A **(*1)**

Note : For pin assignment, please refer to '5.1.2 LCD Drive Connector Description'.
(*1) If you use the FPC type plug, please connect the FPC GND plane to the GND pins instead of connecting to the shell Frame Ground. Because the connectors on the PCB side are going to be changed to Plastic Mold type(FI-TWA31P-VF) those do not have the metallic shell.

Inverter Connector (CN-1 on Inverter Card)

Connector Name / Designation	Signal Connector
Manufacturer	JST
Type / Part Number	S12B-PH-SM3-TB
Mating connector	PHR-12

DC/DC Connector Type (J601 on DC/DC Card)

Connector Name / Designation	Signal Connector
Manufacturer	JAE
Type / Part Number	IL-Z-8PL-SMTY
Mating connector	IL-Z-8S-S125C3

5.2 Interface Signal Description

The module uses a pair of LVDS receiver macro which is equivalent to THC63LVDF84A/R84A(THine Electronics, Inc.). LVDS is a differential signal transfer technology for LCD interface and high speed data transfer device. Transmitter shall be THC63LVDF83A/M83A(THine Electronics, Inc.) or equivalent.

J1 (Master) : Left side (Front View)

Signal Description (J1)

PIN #	SIGNAL NAME	Description
1	(RESERVED)	This pin must be kept 'OPEN'.
2	(RESERVED)	
3	(RESERVED)	
4	(RESERVED)	
5	(RESERVED)	
6	DGND	Digital Ground
7	SDATA	I2C Data for Contrast/Brightness (3.3V typ)
8	SCLK	I2C Clock (3.3V typ)
9	DGND	Digital Ground
10	LGND	LVDS GND
11	RxOIN3+	Positive LVDS differential data input (Odd data)
12	RxOIN3-	Negative LVDS differential data input (Odd data)
13	RxOCLKIN+	Positive LVDS differential clock input (Odd Clock)
14	RxOCLKIN-	Negative LVDS differential clock input (Odd Clock)
15	RxOIN2+	Positive LVDS differential data input (Odd data)
16	RxOIN2-	Negative LVDS differential data input (Odd data)
17	RxOIN1+	Positive LVDS differential data input (Odd data)
18	RxOIN1-	Negative LVDS differential data input (Odd data)
19	RxOIN0+	Positive LVDS differential data input (Odd data)
20	RxOIN0-	Negative LVDS differential data input (Odd data)
21	RxEIN3+	Positive LVDS differential data input (Even data)
22	RxEIN3-	Negative LVDS differential data input (Even data)
23	RxECLKIN+	Positive LVDS differential clock input (Even Clock)
24	RxECLKIN-	Negative LVDS differential clock input (Even Clock)
25	RxEIN2+	Positive LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG)
26	RxEIN2-	Negative LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG)
27	RxEIN1+	Positive LVDS differential data input (Even data)

28	RxEIN1-	Negative LVDS differential data input (Even data)
29	RxEIN0+	Positive LVDS differential data input (Even data)
30	RxEIN0-	Negative LVDS differential data input (Even data)
31	LVDSGND	Ground for LVDS clock/data signals

Note:
I2C address for Brightness and Contrast is '0101101'b.
DAC for them is DALLAS DS1803 or equivalent.
Its port-0 is for Contrast and the Port-1 is for Brightness.
Reserved address of I2C is from '0010000'b to '0011111'b, and from '0110000'b to '0111111'b for another reserved function.

J2 (Slave) : Right side (Front View)
Signal Description (J2)

PIN #	SIGNAL NAME	Description
1	BLON	Backlight on/off signal(Hi:backlight ON, Low:backlight OFF)
2	VDIM-IN	Brightness Dimming Control Voltage (0-3V, 0V:MaxBrightness)
3	VDIM-OUT	Brightness Dimming Control Voltage Output Generated by I2C command
4	VCONT-IN	Contrast Control Voltage (0-1.6V, 1.0Vtyp for Gamma2.2, 0V:Brighter side)
5	VCONT-OUT	Contrast Control Voltage Output Generated by I2C command
6	DGND	Digital Ground
7	(RESERVED)	
8	(RESERVED)	
9	DGND	Digital Ground
10	LGND	LVDS GND
11	RxOIN3+	Positive LVDS differential data input (Odd data)
12	RxOIN3-	Negative LVDS differential data input (Odd data)
13	RxOCLKIN+	Positive LVDS differential clock input (Odd Clock)
14	RxOCLKIN-	Negative LVDS differential clock input (Odd Clock)
15	RxOIN2+	Positive LVDS differential data input (Odd data)
16	RxOIN2-	Negative LVDS differential data input (Odd data)
17	RxOIN1+	Positive LVDS differential data input (Odd data)
18	RxOIN1-	Negative LVDS differential data input (Odd data)
19	RxOIN0+	Positive LVDS differential data input (Odd data)
20	RxOIN0-	Negative LVDS differential data input (Odd data)
21	RxEIN3+	Positive LVDS differential data input (Even data)

22	RxEIN3-	Negative LVDS differential data input (Even data)
23	RxECLKIN+	Positive LVDS differential clock input (Even Clock)
24	RxECLKIN-	Negative LVDS differential clock input (Even Clock)
25	RxEIN2+	Positive LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG)
26	RxEIN2-	Negative LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG)
27	RxEIN1+	Positive LVDS differential data input (Even data)
28	RxEIN1-	Negative LVDS differential data input (Even data)
29	RxEIN0+	Positive LVDS differential data input (Even data)
30	RxEIN0-	Negative LVDS differential data input (Even data)
31	LVDSGND	Ground for LVDS clock/data signals

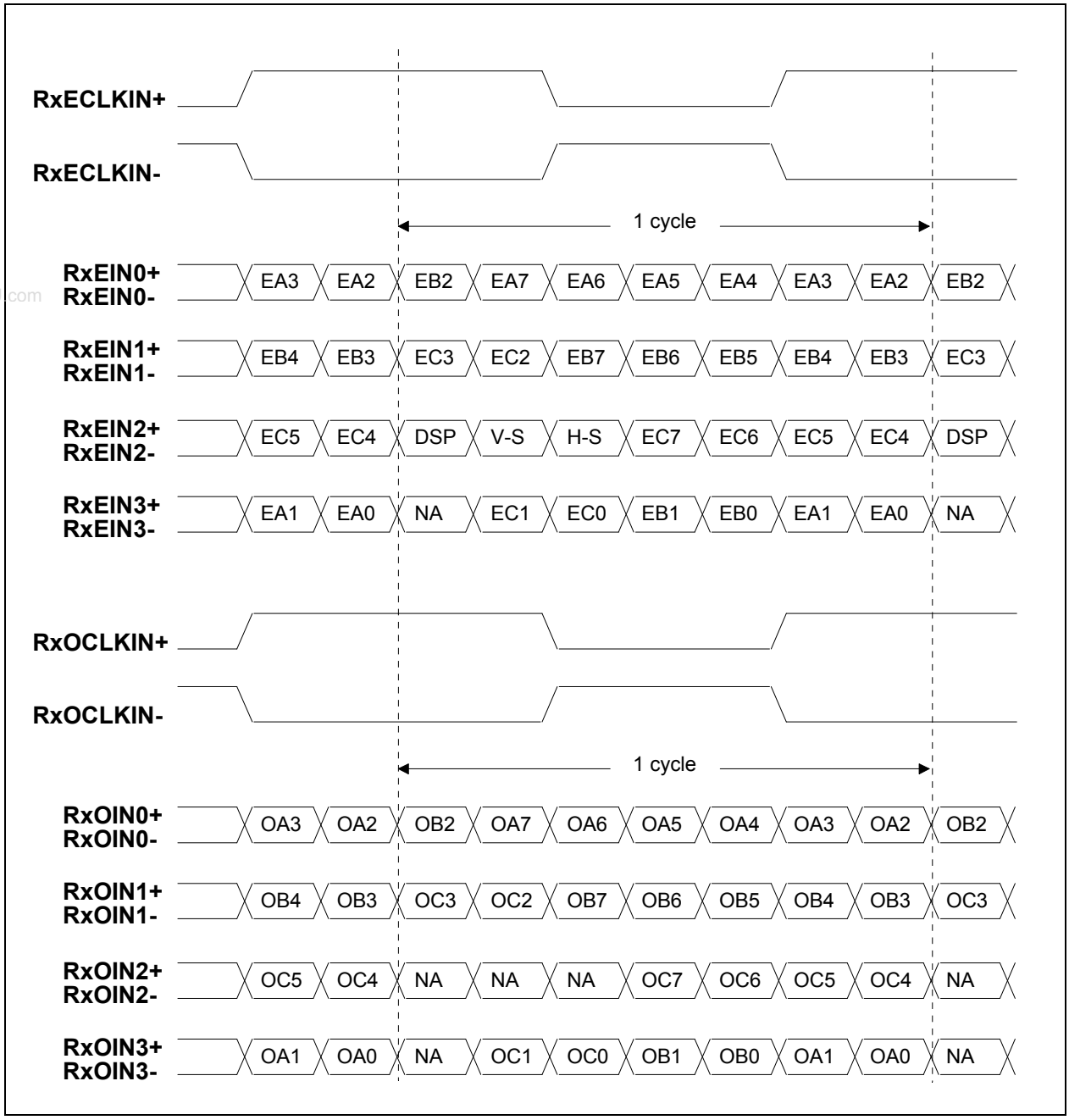
Note:
To use I2C digital control for Contrast/Brightness, connect VCONT-OUT to VCONT-IN, VDIM-OUT to VDIM-IN.
To use analogue voltage control, set VCONT-OUT and VDIM-OUT open, then supply appropriate analogue voltage to VCONT-IN and VDIM-IN.

The following is LVDS Signal description;

SIGNAL NAME	Description	
DTCLK	**Data Clock**	The typical frequency is 65 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	When the signal is high, the pixel data shall be valid to be displayed. The signal is synchronized to DTCLK.
V-Sync	**Vertical Sync**	The signal is synchronized to DTCLK.
H-Sync	**Horizontal Sync**	The signal is synchronized to DTCLK.

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

The following is LVDS Data Order;



Note: A/B/C 7: MSB , A/B/C 0: LSB, DSP = DSPTMG, V-S = V-Sync, H-S = H-Sync
'NA' : Both high and low data are ignored.

5.3 Interface Signal Electrical Characteristics

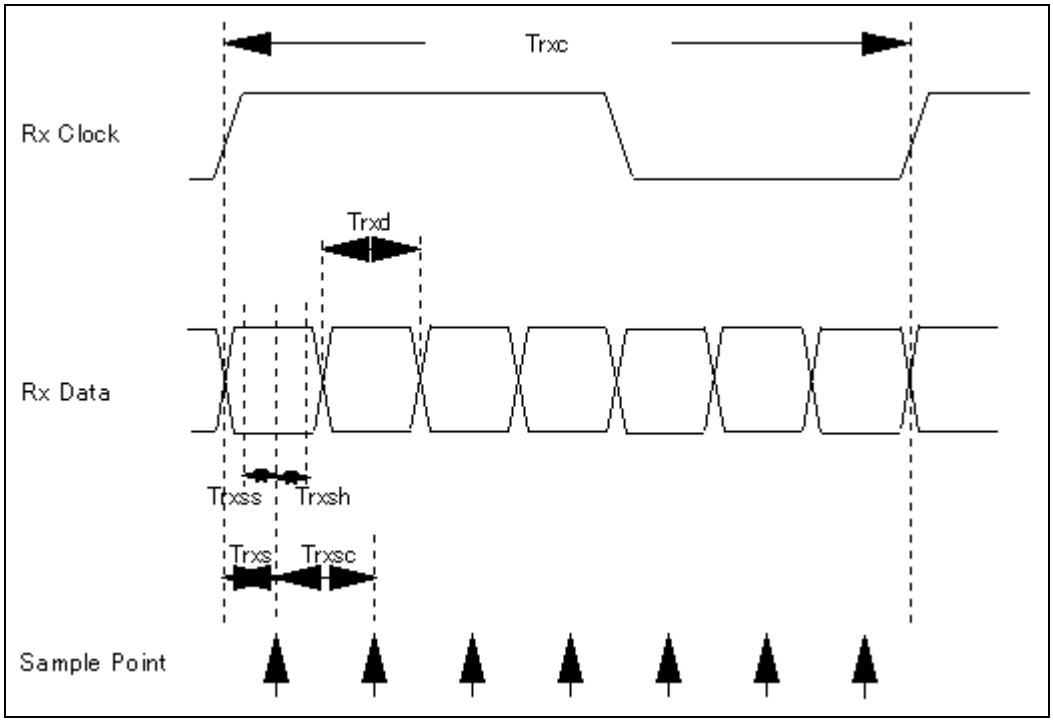
Each signal characteristics are as follows;

Electrical Characteristics

Parameter	Condition	Min	Max	unit
Vth	Differential Input High Voltage (Vcm=+1.2V)		100	mV
Vtl	Differential Input High Voltage (Vcm=+1.2V)	-100		mV

Note : It is recommended to refer to the specifications of THC63LVDF84A/R84A(THine Electronics, Inc.) for the detail.

LVDS Timing



LVDS Macro AC characteristics

Parameter	Symbol	Min	Typ	Max	Unit
LVDS Clock Cycle	Trxc	15.15	15.38	16.66	[ns]
LVDS Data Cycle	Trxd		Trxc/7		[ns]
Sample Data Setup Time (Trxc=Typ.)	Trxss	600			[ps]
Sample Data Hold Time (Trxc=Typ.)	Trxsh	600			[ps]
Data Sample Time	Trxs		Trxc/14		[ns]
Data Sample Cycle	Trxsc		Trxc/7		[ns]

Inverter Input Signal Electrical Characteristics

NAME	**Description**	**Min**	**Typ**	**Max**	**Unit**	**Note**
BLON	High voltage	2.0	3.3	5.25	V	
	Low voltage	-0.1	0.0	0.8	V	
	Current	-1.0	-	1.0	mA	
Vcont-IN	Input Voltage range	0.2	1.0	1.6	V	*1
	Current	-1.0	-	1.0	mA	
VDIM-IN	Input Voltage range	0.0	-	3.0	V	0V:Brightness Max 3V:Brightness Min
	Current	-1.0	-	1.0	mA	

Note:

*1)

0.2V : To pull the GAMMA curve toward darker side (ex. GAMMA 3.0)
When x'00' is written by I2C, Vcont-OUT voltage is about 0.2V

1.0V : GAMMA 2.2
When x'50' is written by I2C, Vcont-OUT voltage is about 1.0V

1.6V : To pull the GAMMA curve toward brighter side (ex. GAMMA 1.5)
When x'D0' is written by I2C, Vcont-OUT voltage is about 1.6V

Those numbers are approximate values.

*2)

I2C address for Brightness and Contrast is '0101101'b and the port-0 is for Contrast and port-1 is for Brightness.

5.4 Inverter Connector Signal Description

Inverter Connector Signal Description

PIN #	SIGNAL NAME	Description
1-5	VBL	+12.0V Power Source for backlight
6-10	RTN	Ground for VBL line
11	(RESERVED)	
12	(RESERVED)	

Inverter Input Signal Electrical Characteristics

NAME	Description	Min	Typ	Max	Unit	Note
VBL	B/L Unit Drive Voltage	11.4	12	12.6	V	

5.5 DC/DC Connector Singal Description

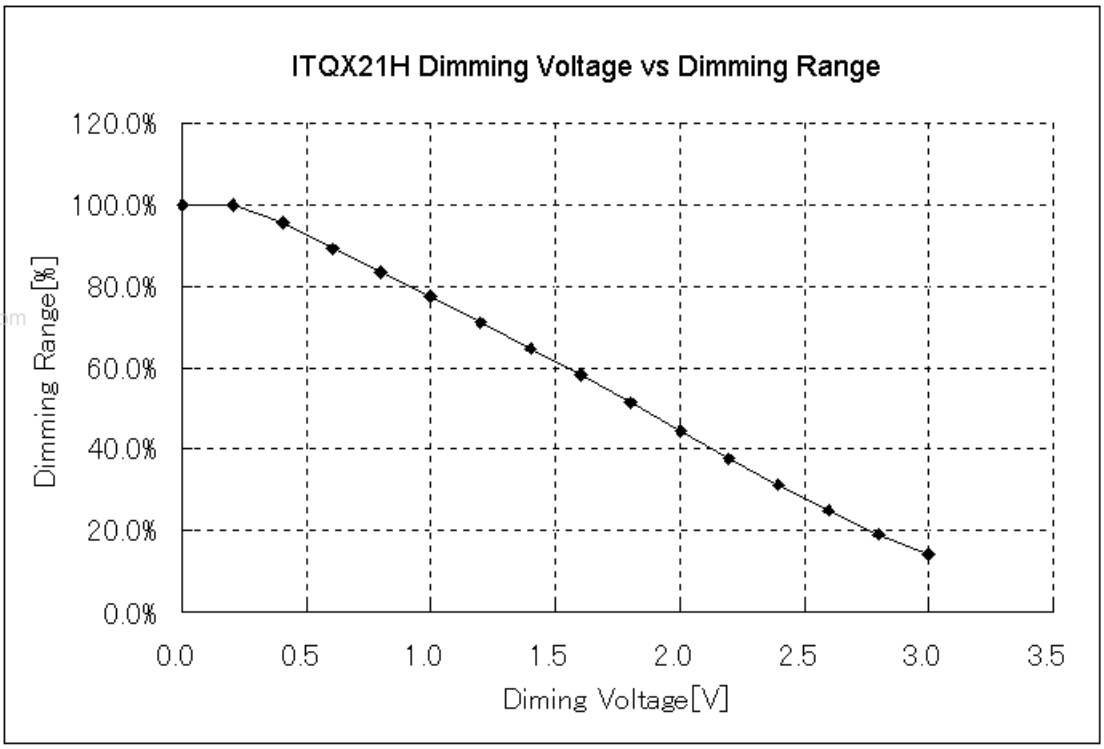
DC/DC Connector Signal Description

PIN #	SIGNAL NAME	Description
1-4	RTN	Ground for Vin line
5-8	Vin	+12.0V Power Supply for LCD Driver Cards (Except Inverter and Backlight)

DC/DC Input Signal Electrical Characteristics

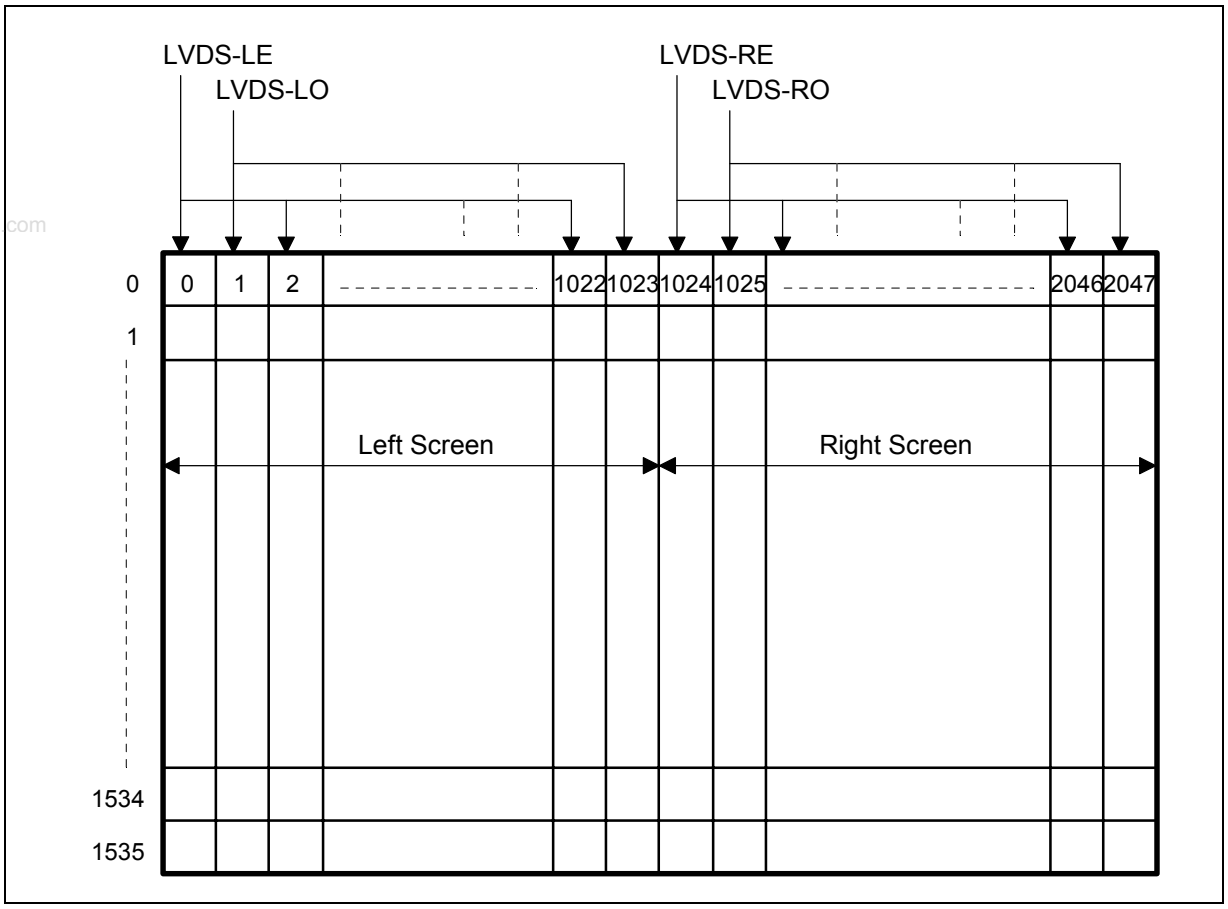
NAME	Description	Min	Typ	Max	Unit	Note
Vin	Logic/LCD Drive Voltage	11.4	12	12.6	V	

The following chart is the VDIM vs Dimming Range for your reference.



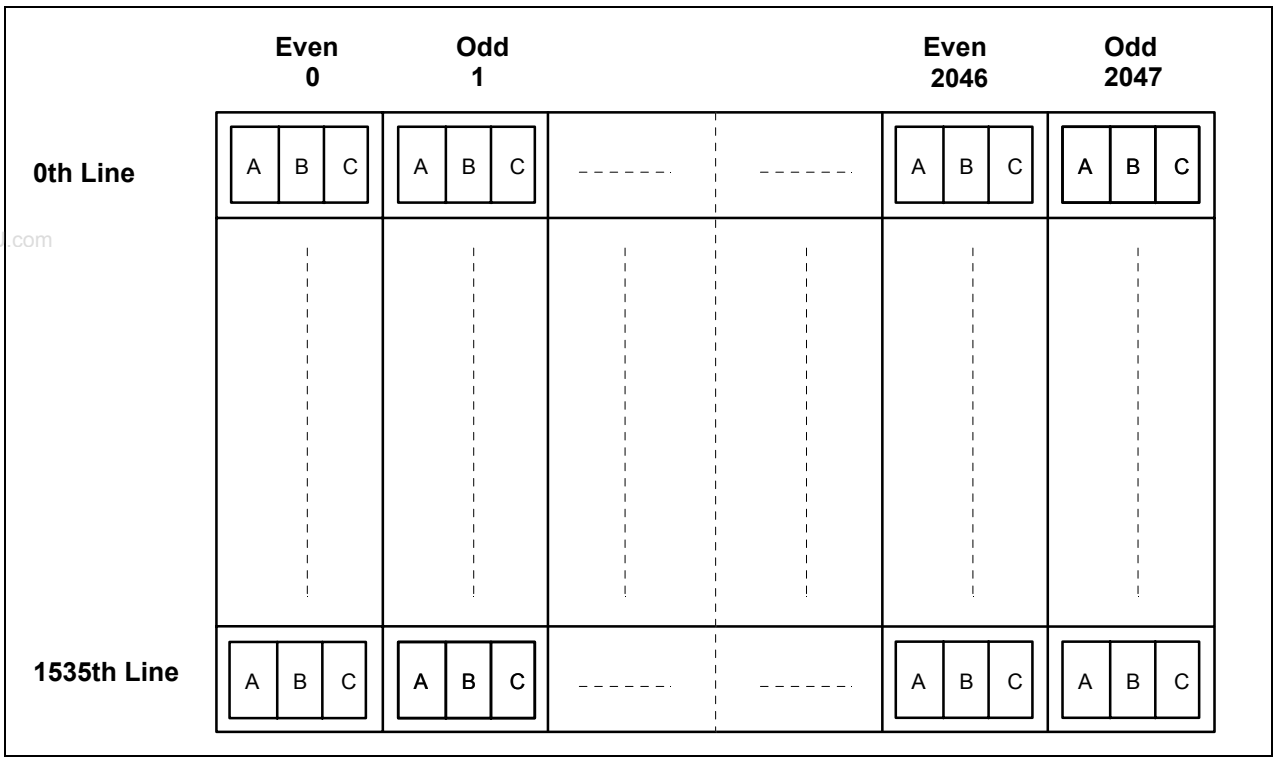
6.0 Pixel format image

Screen Format



Following figure shows the relationship between the input signals and the LCD pixel format image. Each sub-pixel data(A,B,C) of an Even and the right adjacent Odd pixel unit are sampled at the same time.

Pixel Arrangement



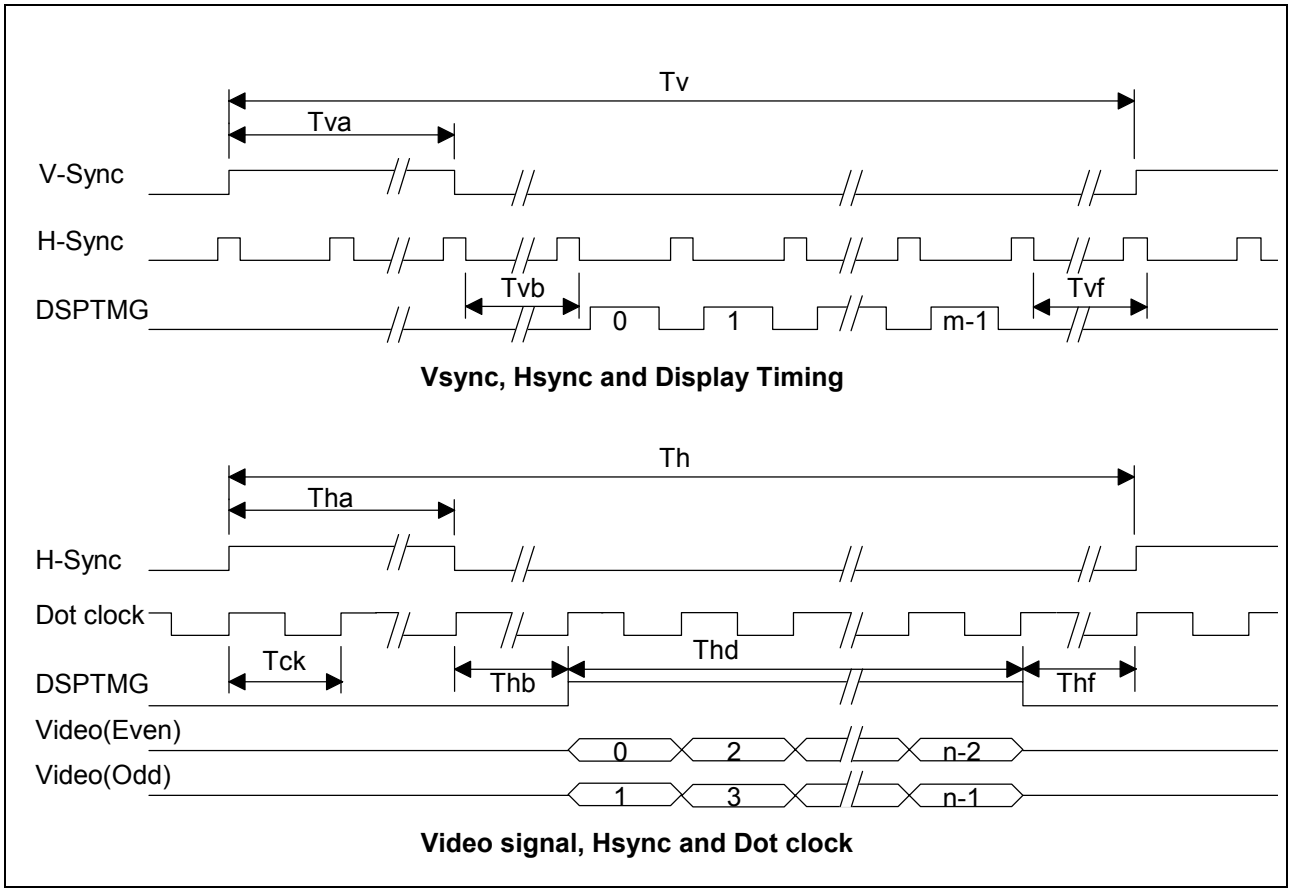
7.0 Interface Timings

Following is the Video timing diagrams per channel (a half screen refresh) to be converted to/from the LVDS interface signals.

7.1 Timing Characteristics

EVEN for LVDS-LE or LVDS-RE
ODD for LVDS-LO or LVDS-RO.

Interface Timing Definition



Vsync, Hsync and Display Timing

Video signal, Hsync and Dot clock

Timing Characteristics

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Dot Clock Freq.	Fdck	60	65	66	MHz
DTCLK	Dot Clock period	Tck	15.15	15.38	16.66	ns
V-Sync	Refresh Rate	1/Tv		60		Hz
V-Sync	Frame period	Tv		16.67		ms
V-Sync	Total line	Tv	1547	1612	1628	lines
V-Sync	V-front porch	Tvf	2	6	14	lines
V-Sync	V-active level	Tva	2	12	14	lines
V-Sync	V-back porch	Tvb	7	58	64	lines
V-Sync	V-Blank	Tvf+Tva+Tvb	11	76	92	lines
DSPTMG	Display Lines	m	-	1536	-	lines
H-Sync	H-Scan Rate	1/Th	92.86	96.72	96.72	KHz
H-Sync	H-Scan Rate	Th	10.34	***1**	10.77	us
H-Sync	Cycle	Th	640	672	700	Tck
H-Sync	H-front porch	Thf	8	12	172	Tck
H-Sync	H-active level	Tha	8	68	172	Tck
H-Sync	H-back porch	Thb	8	80	172	Tck
H-Sync	H-Blank	Thf+Tha+Thb	128	160	188	Tck
DSPTMG	Display clocks	Thd	-	512	-	Tck
DSPTMG	Display Pixels	n	-	1024	-	pixels

Note: Typical value is based on VESA STANDARD (XGA 60Hz).
H/V-Sync Polarity can be both Positive and Negative.
DSPTMG should be Active High.

V-Sync should not be changed at H-Sync leading edge (+/- 6 Tck).

Even Dot clock and Odd Dot clock in each channel should have completely the same clock source. The skew should be within +/- 2ns.

Dot Clocks of the Left and Right channels should have completely the same clock source. But the skew between those clocks does not need to be cared.

The skews of all the other signals (H-Sync, V-Sync, DSPTMG and Video data) should be synchronized between Left and Right channels and should be within +/- 4 dot clocks, respectively.

***1** For this value, the smaller, the better.

8.0 Power Consumption

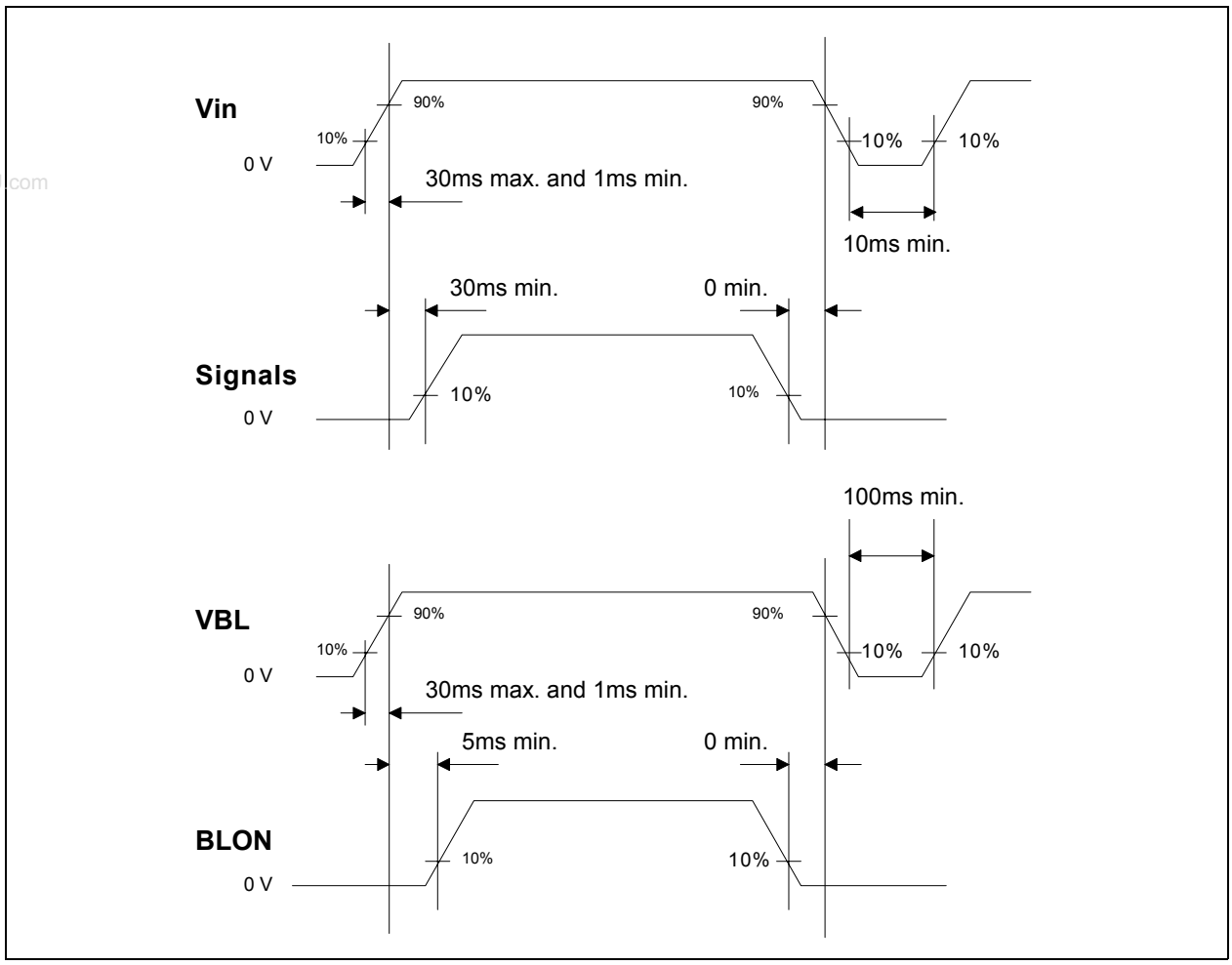
Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
Vin	Logic/LCD Drive Voltage	11.4	12	12.6	V	
Iin	Vin Current		1.2	1.4	A	Vin=12V
Pin	Vin Power		14.4	16	W	Vin=12V All White Pattern
Vin rp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
Vin ns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	
VBL	Backlight power Voltage	11.4	12	12.6	V	
PBL	Backlight Power consumption		44	48	W	Brightness=max

9.0 Power ON/OFF Sequence

Vin power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin is off.

Vin/VBL/Signals Power On/Off Sequence Requirements



10.0 I2C Specification

Following describes the I2C specifications equipped in the LCD module. Since the DAC (DALLAS DS1803) is used for Brightness and Contrast, please refer to its own specifications in detail. 2 signals (SCLK and SDATA) in the LCD module interface are used for the DAC.
The address for DAC is '0101101'b. Its port-0 is for Contrast and its port-1 is for Brightness.
Reserved addresses are from '0010000'b to '0011111'b and from '0110000'b to '0111111'b.

10.1 I2C Feature Summary

- Standard mode (100KHz max) support
- 3.3V interface
- Slave mode operation only

10.2 Electrical Specification

2 signals (SCLK and SDATA) are equipped at the LCD module interface. SCLK is the clock input as SCL and SDATA is the data input/output as SDA. These signals should be driven by Open-Drain or Open-Collector without any pull-up resister. Both signals are pulled up by 5.1K ohm resisters to 3.3V typ respectively in the LCD module.

Electrical Specification of C/A

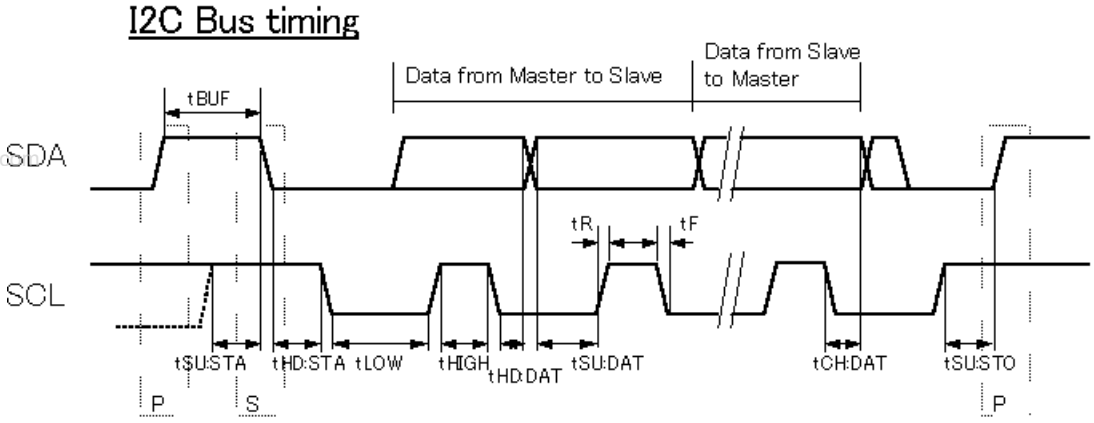
	Symbol	Min	Max	Unit
Input Low voltage (*1)	Vil	-0.5	0.5	V
Input High voltage (*2)	Vih	2.3	3.6	V
Input Hysteresis voltage	Vhys	0.4	-	V
Input leakage current @ Vil-Min or Vih-Max (*3)	Ii	-30	30	uA
Output Low voltage	Vol	-	0.5	V
Output High impedance leakage current(*3)	Ioh	-30	30	uA
Input capacitance	Ci	-	35	pF

NOTE :
*1 : Vil (typ) = 0.9V
*2 : Vih (typ) = 1.8V
*3 : without pull up resisters (5.1K ohm)

10.3 Timing Specification

In the following figure and table, Slave is the control ASICs in the LCD module and Master is the controller to drive the LCD module.
"S" is the START condition and "P" is the STOP condition.

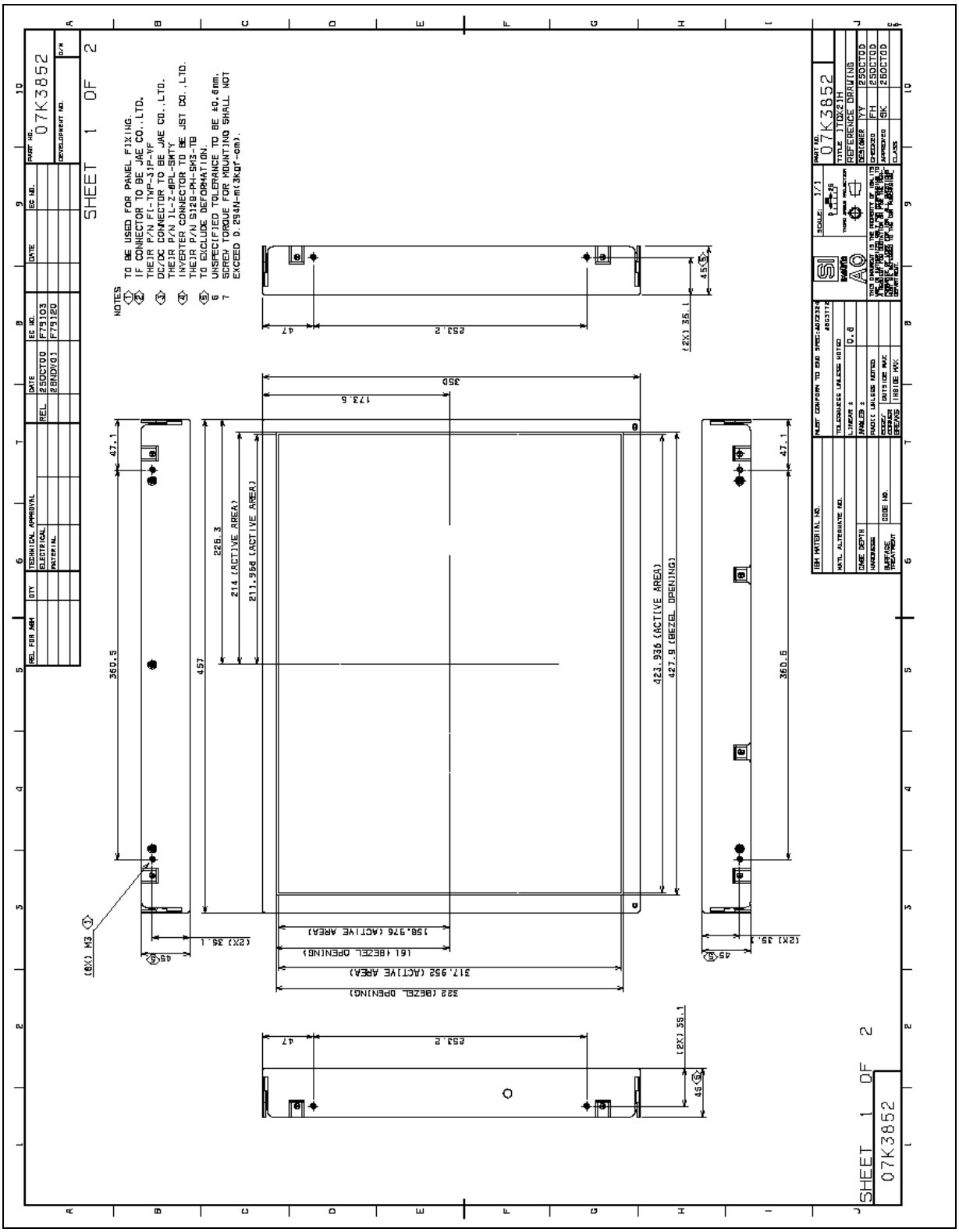
I2C Bus timing

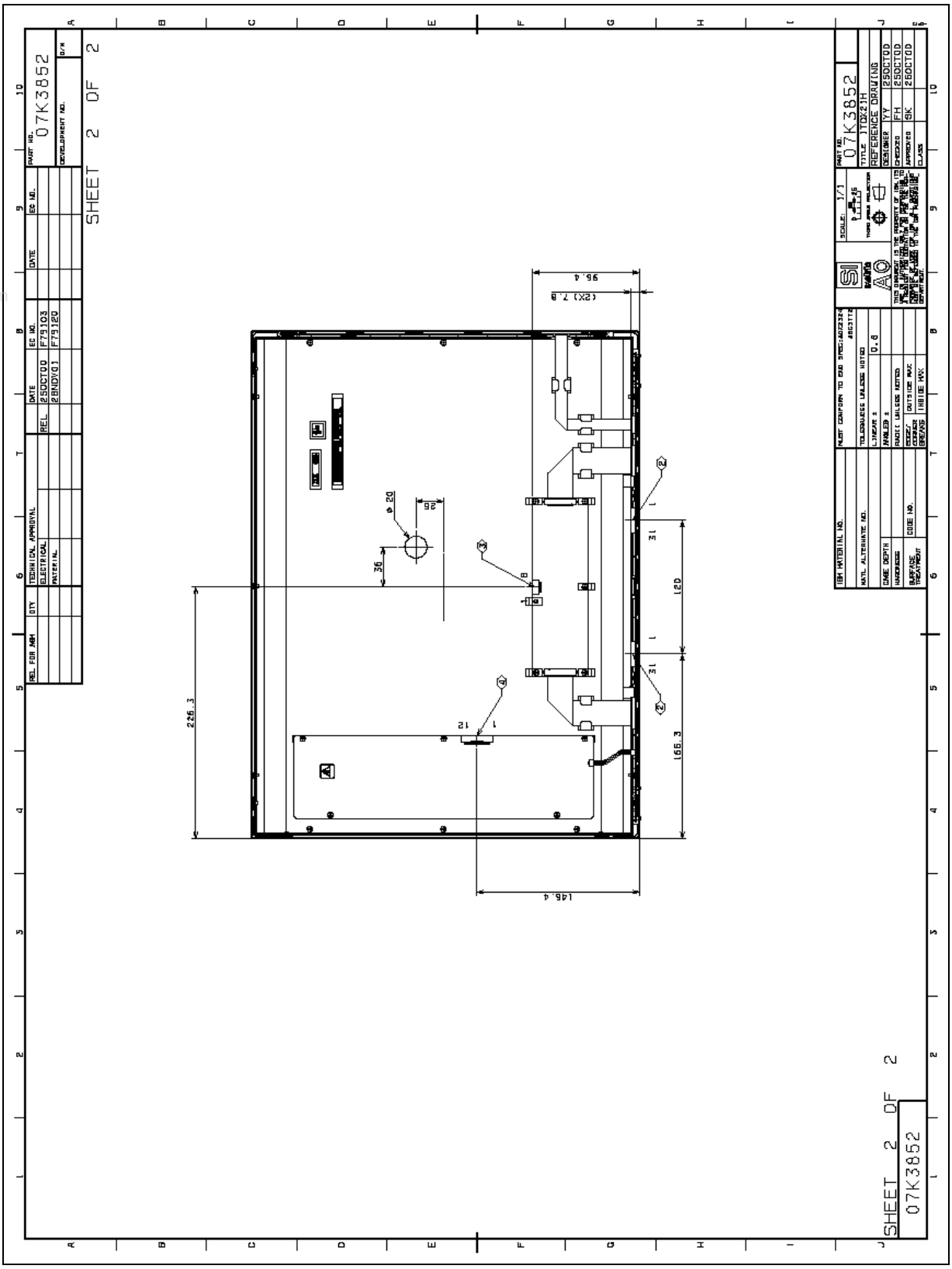


Timing Specification of C/A

	Symbol	Min	Max	Unit
Frequency of SCL	fSCL	0	100	KHz
Bus Free Time from STOP to START	tBUF	4.7	-	us
Setup time of START	tSU:STA	4.7	-	us
Hold time of START	tHD:STA	4.0	-	us
Low time of SCL	tLOW	4.7	-	us
High time of SCL	tHIGH	4.0	-	us
Data hold time for Slave	tHD:DAT	0	-	us
Data setup time for Slave	tSU:DAT	250	-	ns
Data change from SCL falling edge (to Master)	tCH:DAT	300	900	ns
Rise time Vil-Max --> Vih-Min	tR	-	1000	ns
Fall time Vil-Max <-- Vih-Min	tF	-	300	ns
Setup time of STOP	tSU:STO	4.0	-	us
Spike suppression	tSP	-	50	ns

11.0 Mechanical Characteristics





12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

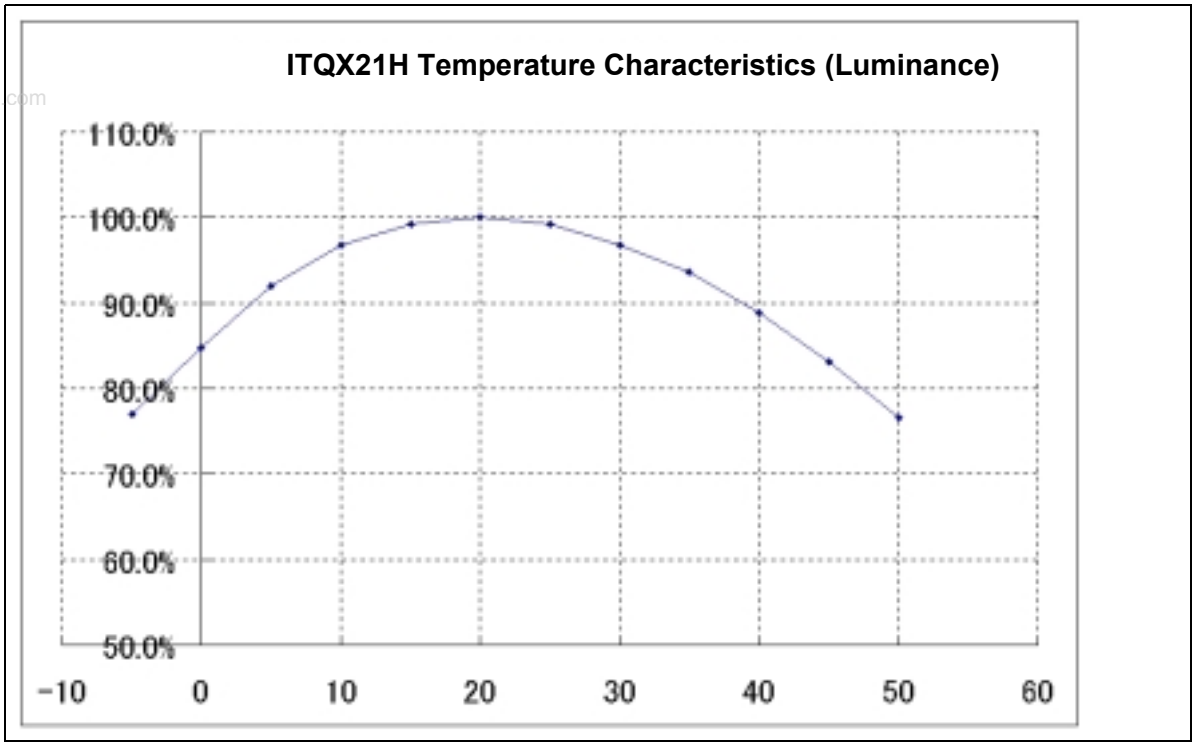
- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-95 *UL 1950, Third Edition, including revisions through revision date March 1,1998, which are based on the Fourth Amendment to IEC 950, Second Edition, which would cover the component itself if submitted for Listing.
- The inverter output circuit supplied with this model is a limited Current Circuit.
- The units are intended to be supplied by SELV.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

13.0 Application Note

This section describes some outstanding characteristics of ITQX21H module and also describes some design recommendations.

13.1 Luminance vs Temperature

The following chart shows the initial luminace transition coming along with the module temperature.



13.2 Design Recommendation

This chapter describes the recommendation when monitor frame is designed.

13.2.1 Recommendations for cooling

The ITQX21H is a high luminance and high resolution panel and produces some heat. Inadequate cooling can result in damage to the module or the monitor unit.

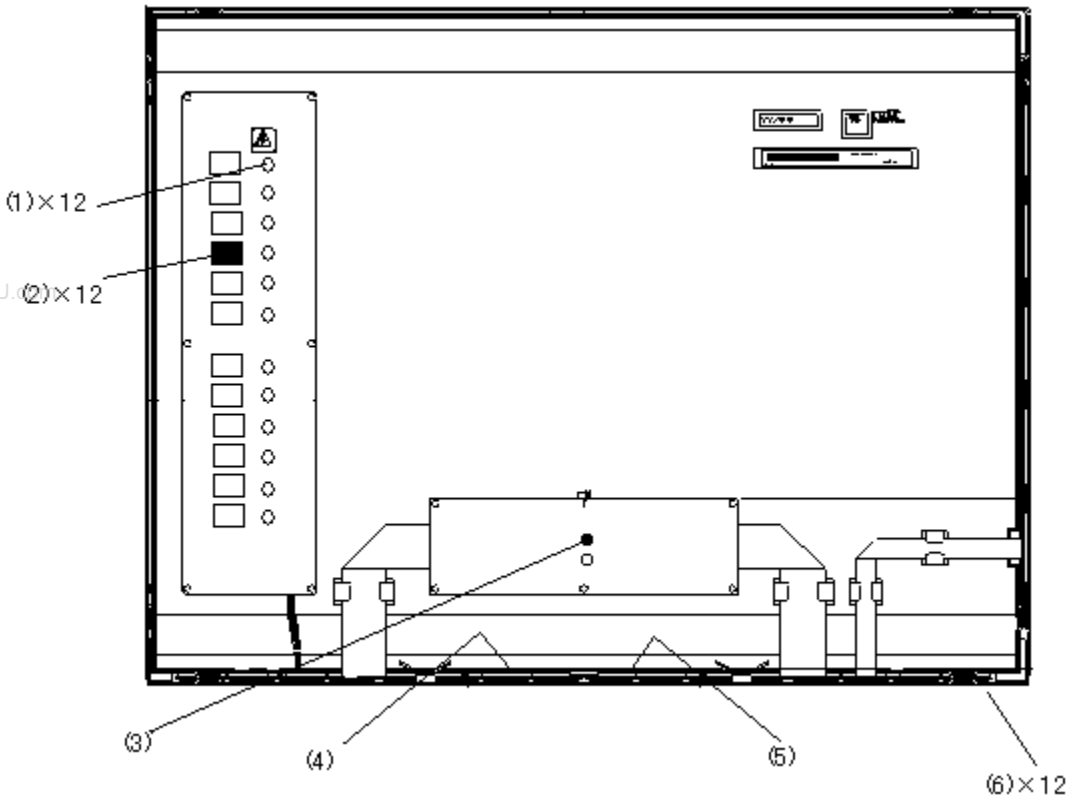
COOLING FANS ARE STRONGLY RECOMMENDED TO ENSURE CORRECT TEMPERATURE OPERATION.

Because of the large panel size the use of 2 fans is recommended.

The recommended position of the fans is to supplement the normal convective flow. The optimum configuration would be to input cool air at the base of the panel and exhaust hot air at the top. The exact size, position, and flow rates are a function of the monitor enclosure design. Please refere to the maximum operating temperatures of the various components to verify the design.

*** Reference ***

See the rear side of module below;



- ABSOLUTELY NECESSARY POINTS are next two components.
(6) X-DRIVER (Will get very hot.)
and
(1) Choke Coil

- Backlight Inverter
(2) Transformer

- DC/DC Card
(3) Choke Coil

- PCB-X
(4), (5) Gate Array

The table below shows the maximum component temperature Spec.

Component	Max. Temperature Spec. (degree C)
Gate Array	100
X-Driver	85
Choke Coil(Inverter)	105
Transformer(Inverter)	100
Choke Coil(DC/DC)	105
Polarizer(Cell)	60

13.2.2 Mechanical recommendation for monitor enclosure design.

This TFT module uses IPS technology to enhance viewing angle, this technology is weak against twisting and bending forces.
These forces cause bad FOS quality, such a un uniformity.
In order to keep original FOS quality, please following instruction at manufacturing and designing.

1. After installation of the TFT Module into an enclosure, do not twist nor bent the TFT Module even momentary.

2. At designing the enclosure, it should be taken into below consideration. otherwise the TFT Module occur uniformity problem.

2-1. Material of chassis or bracket to mounting TFT module should be hard material, stainless or SECC or SPCC.
Material thickness should be exceeded 1mm.

2-2. No bending/ twisting forces are applied to the TFT Module from out side.

2-3. No pushing force for EMI grounding using metal fingers or gasket TFT metal bezel, to push glass surface by TFT metal bezel opening edge, is applied to TFT module metal bezel wall.

2-4. At designing system front plastic bezel, do not touch and push glass surface to avoid un uniformity.

13.2.3 Recommendation of designing monitor which uses ITQX21H for EMC Compliance

A. Chassis and Frame Ground of Monitor

1. LCD Module should be covered by metal chasis over all except front side. the chasis of the monitor's interface card should be designed as separate parts with the chasis of the LCD module.
Holes on the partition wall between the two chasis shold be as small as possible to pass through the cables.
The two chassis should be contacted each other with low impedance.

2. Monitor's chasis(equal chasis of LCD module)should have the contact with the frame ground of voltage source(Power FG) with low impedance.

3. The chasis of LCD module should have the contact with the surrounding of front bezel by finger or something at intervals of less than 1 inch.

4. The ground of the monitor's interface card should be contacted with its chasis with low impedance.

5. The holes for thermal radiation, on chasis of LCD module or monitor's interface card, should be less than 1 inch in diameter, at intervals of less than 1 inch. We recommend the holes are about 5mm in diameter, at intervals of about 10mm to 15mm.

B. LVDS cabel(assumption as wire type, not FPC or FFC)

1. Signal pairs of the differential signals should be twisted each other with more than a turn per a centimeter.

2. The ground line would wind around the set of LVDS cables(1 channel).

3. The set of LVDS cables would be covered by shield mesh.
   To make the shield mesh contacted with the signal ground, it is possible to strip the cover of ground line wound around LVDS signals.

4. Ferrite Core would be added to LVDS cables at the point near signal source.
   We recommend the above works at that priority(1. is the highest).

C. A ferrite core would be added to the power cable which supply +12volt to LCD module.

****** End Of Page ******