HDMI 1.3 Splitter

EP9132

User Guide

V0.1

Revised Date: Jan. 04, 2008

Original Release Date: Apr. 19, 2007

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Apr/19/2007	Jerry Chen	Initial Version
0.1	Jan/04/2008	Ether Lai	Revise Feature List; Add Power Consumption;

Section 1 Introduction

1.1 Overview

The EP9132 is an DVI/HDMI splitter with integrated HDCP decryption/encryption engines and is compliant with HDMI Rev 1.3b and HDCP Rev 1.2 specifications. The EP9132 receives DVI/HDMI inputs, process HDCP decryption and encryption and transmits the data to 2 DVI/HDMI ports. The chip uses an external EE to store the encrypted HDCP receiver/transmitter keys.

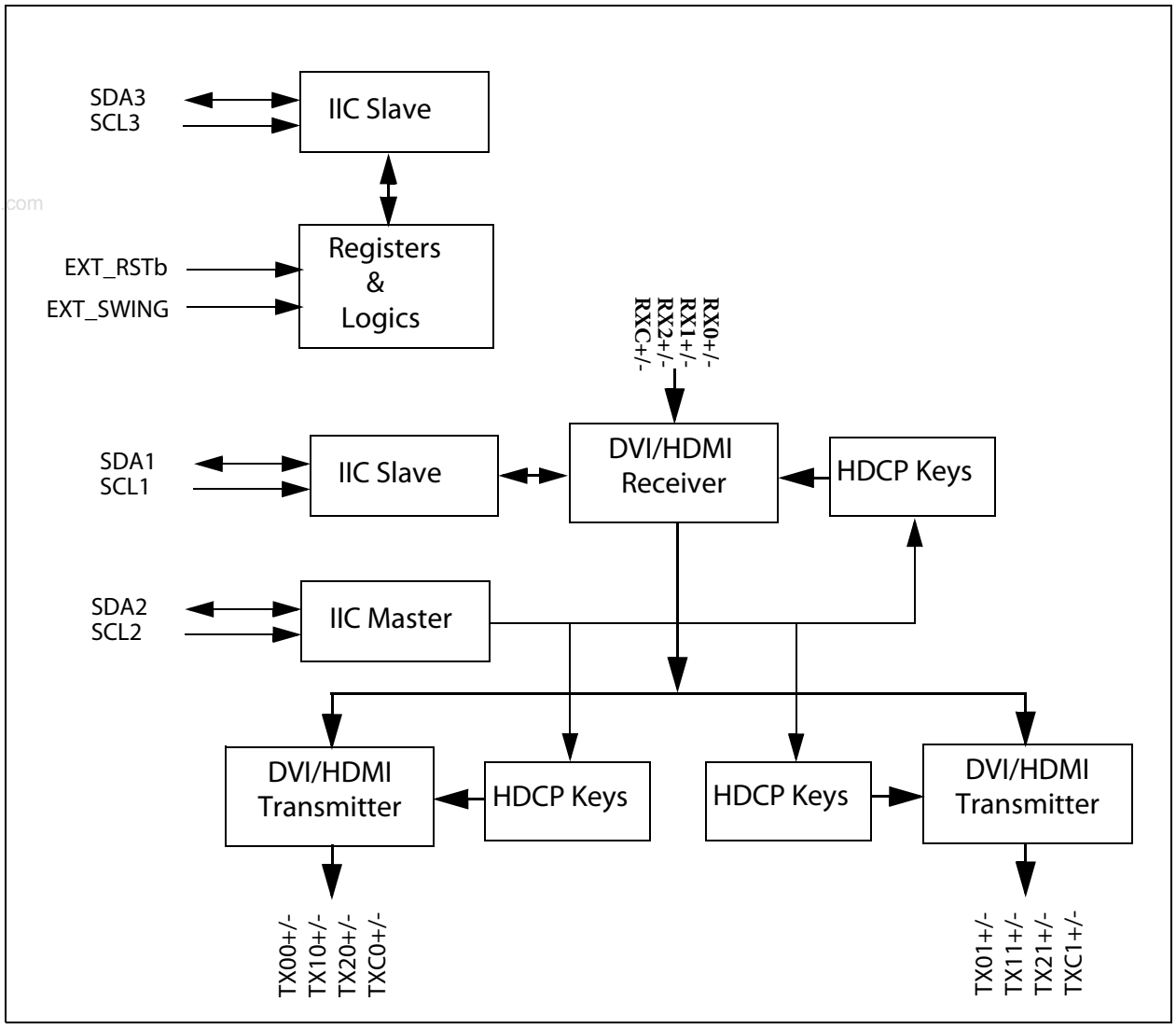
1.2 Features

- DVI Specification 1.0 Compliant
- HDMI Specification 1.3b Compliant
- Integrated HDCP decryption/encryption engines which are compliant with HDCP Rev 1.2 specification
- Encrypted HDCP keys store in external serial EE
- Wide Frequency Range: 25MHz - 225MHz
- Support 12-bit Deep Color up to 1080p
- Supports 1 DVI/HDMI input port and 2 DVI/HDMI output ports
- Supports conversion of HDMI signaling to DVI signaling
- Supports HDCP Repeater
- Re-Sample architecture to filter input noise and recover the input data
- Re-Drive architecture to regenerate clean TMDS signal
- Cascadable to make more than 2 output ports
- Single 3.3V CMOS Design
- 80-Pin LQFP (Pb-Free)

Section 2 Overview

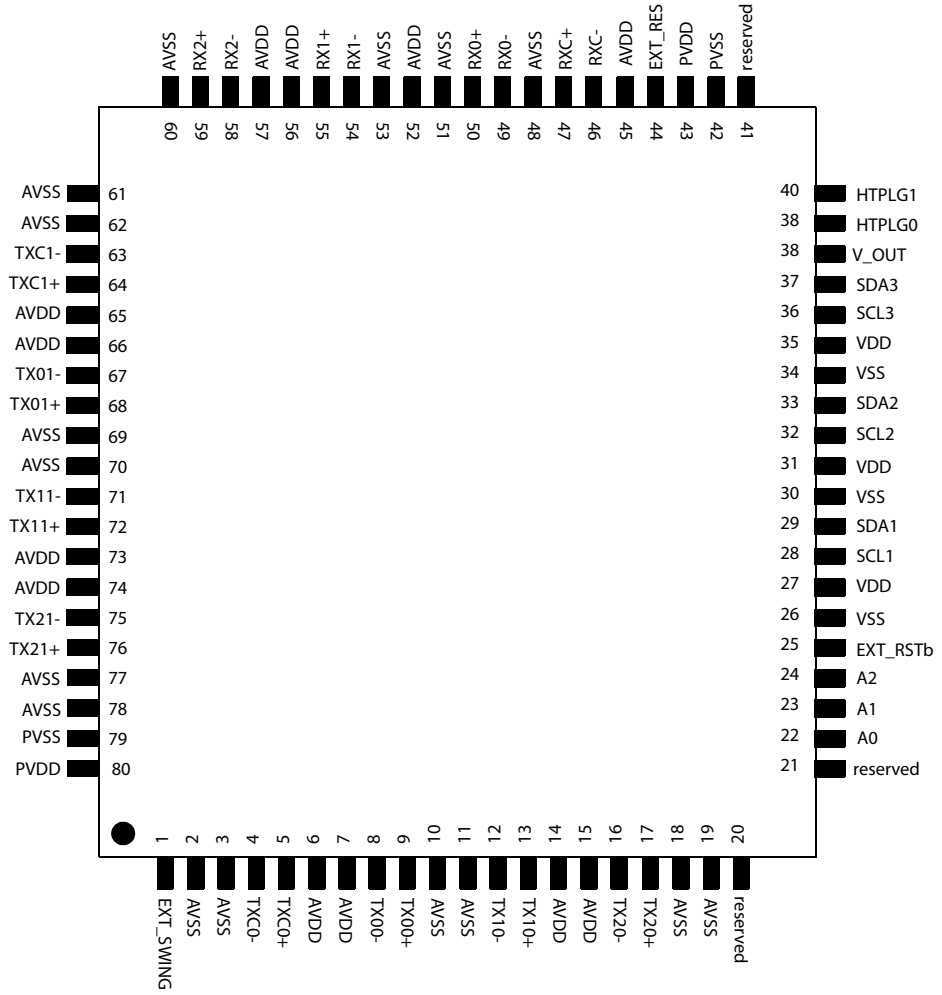
2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram

Figure 2-2 Pin Diagram



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 IIC Pins

NAME	IN / OUT	DESCRIPTION
SCL1	IN	IIC SCL signal for receiver port DDC
SDA1	IO	IIC SDA signal for receiver port DDC (open drain)
SCL2	OUT	IIC SCL signal for EE interface (open drain)
SDA2	IO	IIC SDA signal for EE interface (open drain)
SCL3	IN	IIC SCL signal for internal registers access
SDA3	IO	IIC SDA signal for internal registers access (open drain)
A2, A1, A0	IN	Determine the lowest 3-bit of the IIC addrress for IIC Port 3 (SCL3/SDA3)

Table 2-2 Misc. Pins

NAME	IN / OUT	DESCRIPTION
EXT_RSTb	IN	External Reset (Active LOW). A HIGH level indicates normal operation and a LOW level causes all the logic on the chip to be reset.
V_OUT	OUT	Polarity corrected vertical sync pulse (active high) derived from receiver input
reserved	IN	Must be tied LOW for normal operation.

Table 2-3 Receiver Pins

NAME	IN / OUT	DESCRIPTION
RX0- RX0+ RX1- RX1+ RX2- RX2+	Analog	Differential Data Input Pairs for receiver port
RXC- RXC+		Differential Clock Input Pairs for receiver port
EXT_RES	Analog	DVI/HDMI External Termination Resistor

Table 2-4 Transmitter Pins

NAME	IN / OUT	DESCRIPTION
TX00- TX00+ TX10- TX10+ TX20- TX20+	Analog	Differential Data Output Pairs for transmitter port 0
TXC0- TXC0+		Differential Clock Output Pairs for transmitter port 0
HTPLG0	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for tansmitter port 0. Note: This input is only 3.3V tolerant and has no internal debouncer circuit.

Table 2-4 Transmitter Pins

NAME	IN / OUT	DESCRIPTION
TX01- TX01+ TX11- TX11+ TX21- TX21+	Analog	Differential Data Output Pairs for transmitter port 1
TXC1- TXC1+		Differential Clock Output Pairs for transmitter port 1
HTPLG1	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for tansmitter port 1. Note: This input is only 3.3V tolerant and has no internal debouncer circuit.
EXT_SWING	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistance determines the amplitude of the voltage swing. 300Ω is recommended.

Table 2-5 Power and Ground Pins

NAME	IN / OUT	DESCRIPTION
VDD	PWR	Digital Power, 3.3V
VSS	GND	Digital Ground
AVDD	PWR	Analog Power, 3.3V
AVSS	GND	Analog Ground
PVDD	PWR	Analog Power for PLL, 3.3V
PVSS	GND	Analog Ground for PLL

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		165	°C
P_{PD}	Package Power Dissipation		1.6		W

1 Permanent device damage may occur if absolute maximum conditions are exceeded.

2 Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

1 Guaranteed by design.

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA
V_{ID}	Differential Input Voltage, Single Ended Amplitude		150		1000	mV

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm R_{EXT_SWING} = 750 ohm	510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]			AVCC		mV
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V			5	V
I_{PD}	Power-Down Current[2]	25°C Ambient, V_{CC}=3.3V		2		mA
I_{CCD}	Supply Current (25°C Ambient, R_{EXT_SWING} = 300 ohm, TX0/TX1 are Active)	Typical Case Pattern[3] 1080i Resolution (8-bit)		306		mA
		Worst Case Pattern[4] 1080i Resolution (8-bit)		310		mA
		Typical Case Pattern[3] 1080p Resolution (8-bit)		364		mA
		Worst Case Pattern[4] 1080p Resolution (8-bit)		373		mA
		Typical Case Pattern[3] UXGA Resolution (8-bit)		374		mA
		Worst Case Pattern[4] UXGA Resolution (8-bit)		382		mA
		Typical Case Pattern[3] 1080p Resolution (12-bit)		421		mA
		Worst Case Pattern[4] UXGA Resolution (12-bit)		423		mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are scilent.

3 The typical Pattern contains a gray scale area, checkerboard area and text.

4 Black and White checkboard pattern, each checker is one pixel wide.

Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
T_{PDL}	Delay from OUT_EN Low to High Impedance outputs				10	ns

T_{HSC}	Link Disabled (Tx power down) to LINK_ON Low[4]				250	ms
T_{FSC}	Link Enabled (DE Active) to LINK_ON High[1]			25	40	DE edges

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronical Measurement Procedures*
4. Measured when transmitter was powered down.

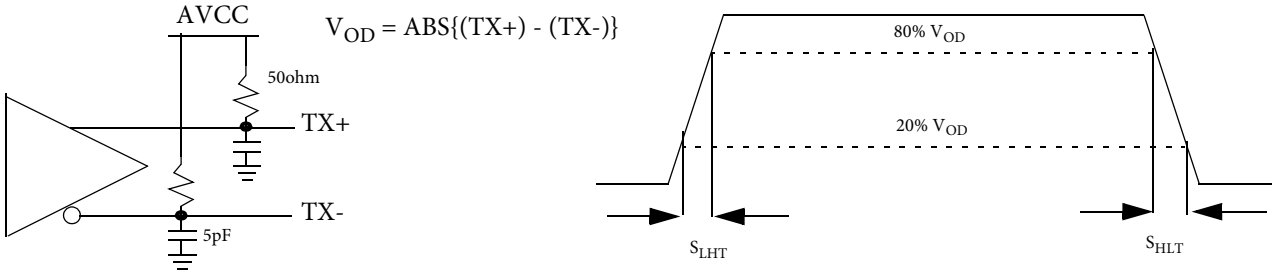
Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 300 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 300 ohm	170	200	230	ps

2 Jitter can be estimated by 1) triggering a digital scope at the rising of input clock and 2) measuring the peak to peak time spread of the rising edge of the input clock at both 0.5us and 1.0us after the trigger.

3 Actual jitter tolerance may be higher depending on the frequency of the jitter.

Figure 2-3 Differential Output Timing Definition



Section 3 Detail Functional Descriptions

3.1 General

The chip provides an IIC (SCL3/SDA3) serial bus interface to communicate with the host. The IIC address for this slave IIC interface is "0111_A2_A1_A1_x" (where x=1 for read and x=0 for write). A2, A1 and A0 are programmable by pins

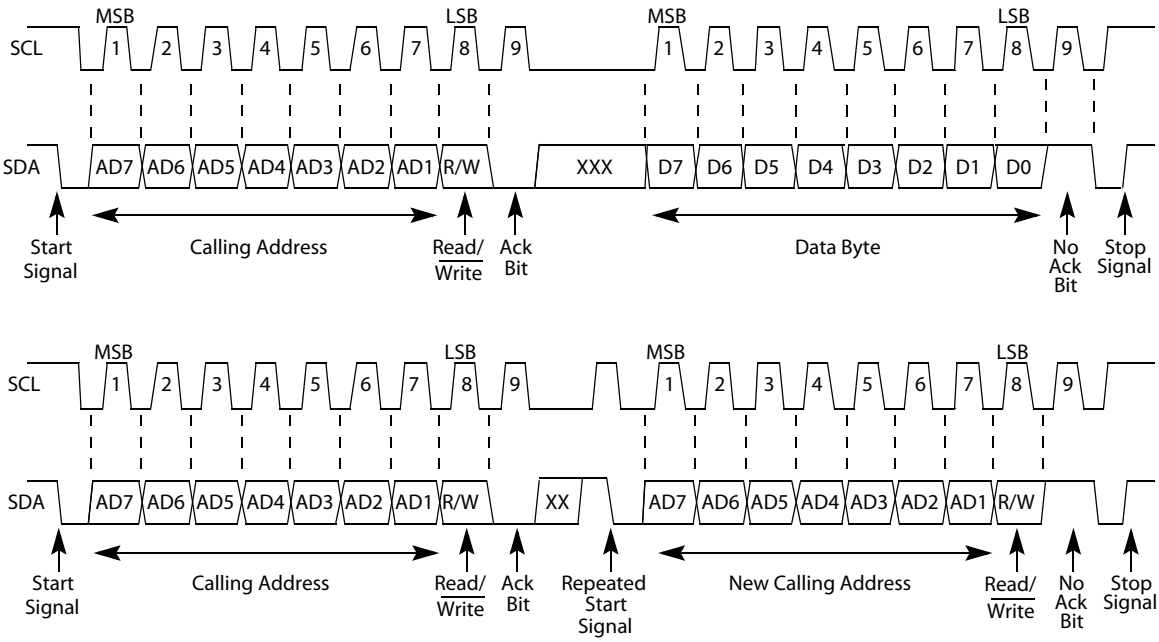
3.2 IIC Interface

The IIC bus interface uses a Serial Data line (SDA at pin SDA3) and a Serial Clock Line (SCL at pin SCL3) for data transfer. The chip acts as a slave for receiving and transmitting data over the serial interface. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

The standard IIC traffic protocol is illustrated in the following Figure:

Figure 3-1 IIC Bus Transmission Protocol



3.2.1 Basic Protocol

For EP9132, there are six components to serial bus operation:

- START Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte for Read/Write
- STOP Signal

When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the EP9132 sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the EP9132 does not assert the acknowledge.

Writing data to specific control registers of the chip requires that the 8-bits address of the control register is written after the slave address has been acknowledged. This control register address is the base address for the subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

Data are read from the control registers of the chip in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the chip, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus.

3.2.2 Examples of the read/write sequence

Write to One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte

- Data Byte to Base Address
- STOP Signal

Write to Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- .....
- Data Byte to (Base Address + N)
- STOP Signal

Read from One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- STOP Signal (Optional)
- START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- STOP Signal

Read from Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- STOP Signal (Optional)
- START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- .....

- Data Byte from (Base Address + N)
- STOP Signal

3.3 Description of the Control Registers

The following table shows all the control registers of the DVI/HDMI Transmitter EP9132:

Table 3-1 IIC Control Registers

Addr	Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RESET
$05	R/W	-	-	TMDS_SAMP[5:0]						04h
$06	R/W	TMDS_CTL1[7:0]								00h
$07	R/W	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	-	-	RX_PU	TX_SEL	02h
$08	R/W	TX_MUTE	RX_VSYNC	-	-	-	-	TX_ENC_OPT	TX_PU	01h
$09	R	-	-	-	-	-	TX_RSEN	TX_HTPLG	-	00h
$0E	R/W	-	-	-	-	-	-	TX_EESS	TX_HDMI	01h
$0F	R/W	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN	00h
$10	R/W	TX_BKSV_1								XXh
$11	R/W	TX_BKSV_2								XXh
$12	R/W	TX_BKSV_3								XXh
$13	R/W	TX_BKSV_4								XXh
$14	R/W	TX_BKSV_5								XXh
$15	R/W	TX_AN_1								XXh
$16	R/W	TX_AN_2								XXh
$17	R/W	TX_AN_3								XXh
$18	R/W	TX_AN_4								XXh
$19	R/W	TX_AN_5								XXh
$1A	R/W	TX_AN_6								XXh
$1B	R/W	TX_AN_7								XXh
$1C	R/W	TX_AN_8								XXh
$1D	R	TX_AKSV_1								XXh
$1E	R	TX_AKSV_2								XXh
$1F	R	TX_AKSV_3								XXh
$20	R	TX_AKSV_4								XXh

$21	R	TX_AKSV_5	XXh
$22	R	TX_RI_1	XXh
$23	R	TX_RI_2	XXh

3.3.1 Register Descriptions

Detailed usage of these IIC registers is described in the following section.

3.3.1.1 TMDS Control Register 0

Table 3-2 TMDS Control Register 0

$05

	6	5	4	3	2	1	0
R W	0	0	TMDS_SAMP[5:0]				
Reset:	0	0	0	0	0	1	0	0

TMDS_SAMP[5:0] — TMDS Sampling Logic Control Parameters

This register has to be programmed with the value 0x08 after the power on sequence if the expected supported TMDS clock frequency is up to 225MHz (1080p, 12 bits deep color).

3.3.1.2 TMDS Control Register 1

Table 3-3 TMDS Control Register 1

$06

	6	5	4	3	2	1	0
R W	TMDS_CTL1[7:0]						
Reset:	0	0	0	0	0	0	0	0

TMDS_CTL1[7:0] — TMDS Control Register 1

This register has to be programmed with the value 0xA6 after the power on sequence if the expected supported TMDS clock frequency is up to 225MHz (1080p, 12 bits deep color).

3.3.1.3 Control Register 0

Table 3-4 Control Register 0

$07	6	5	4	3	2	1	0
R	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	-	-	RX_PU	TX_SEL
W	-	-	-	-				
Reset:	-	-	-	-	-	-	1	0

RX_LINK_ON — Receiver Link On

This bit indicates whether a valid signal appears at the clock input of the receiver port. This bit is valid even when the receiver is powered off.

1 = Clock presents at the input of the receiver port

0 = No clock is detected at the input of the receiver port

RX_DE_ON — Receiver DE On

This bit indicates whether DE signal is toggling at the receiver port. This bit is valid only when the receiver is powered on.

1 = DE signal is toggling at the receiver port

0 = DE signal is not toggling at the receiver port

RX_HDMI — Receiver HDMI signal

This bit indicates whether the receiver port is receiving DVI or HDMI signal

1 = HDMI

0 = DVI

RX_ENC_ON — Receiver Decryption On

This bit indicates whether the HDCP decryption is active at the receiver port.

1 = HDCP decryption at the receiver port is active

0 = HDCP decryption at the receiver port is not active

RX_PU — Receiver Power Down Control Bit

This bit controls the power of the receiver port

1 = Normal operation.

0 = Power down Mode.

TX_SEL — Transmitter Port Select for IIC Access

The 2 transmitter ports share the same IIC register address. This bit is used to select which transmitter port is addressed for IIC access.

1 = Port 1 is selected

0 = Port 0 is selected

3.3.1.4 Control Register 1

Table 3-5 Control Register 1

$08

	6	5	4	3	2	1	0
R	TX_MUTE	RX_VSYNC	-	-	-	-	-TX_ENC_OPT	TX_PU
W		-						
Reset:	0	-	-	0	-	-	0	1

TX_MUTE — Video Mute Transmitter

The bit is used to mute the video for the selected transmitter port.

1 = Selected transmitter port is video muted

0 = Normal

VSYNC — Vertical Sync Status Bit

The VSYNC bit gives the current status of the vertical sync signal received by the receiver.

TX_ENC_OPT — Transmitter Encryption Option

1 = Not affected by RX encryption status.

0 = Force not to encrypt if RX is not encrypted.

TX_PU — Transmitter Power Down Control Bit

This bit controls the power of the selected transmitter port

1 = Normal operation.

0 = Put the selected transmitter port in power down mode.

3.3.1.5 Control Register 2

Table 3-6 Control Register 2

$09

	6	5	4	3	2	1	0
R	-	-	-	-	-	TX_RSEN	TX_HTPLG	-
W						-	-	
Reset:	-	-	-	-	-	-	-	-

TX_RSEN — Transmitter Analog Output Status Bit

The TX_RSEN bit indicates the analog output status at the selected transmitter port.

1 = The selected transmitter analog outputs are connected to the receiver

0 = The selected transmitter analog outputs are disconnected

TX_HTPLG — Transmitter Hot Plug Status Bit

The TX_HTPLG bit indicates the hot plug status at the selected transmitter port.

1 = Hot Plug detected at the selected transmitter port.

0 = Hot Plug not detected at the selected transmitter port.

3.3.1.6 Control Register 3

Table 3-7 Control Register 3

$0A

	6	5	4	3	2	1	0
R/W	DK[3:1]		DKEN	-	-	-	-
Reset:	1	0	0	0	-	-	-	-

DK[3:1] — De-skewing Setting Control Bits

The DK[3:1] setting the clock to data timing for de-skew purpose. Eight steps can be selected and the time difference for each step is 200 ps. The default is 0 step.

000 = -4 step
001 = -3 step
010 = -2 step
011 = -1 step
100 = 0 step
101 = +1 step
110 = +2 step
111 = +3 step

DKEN — De-Skew (Clock to Data De-skewing) Enable Bit

1 = De-Skew Enabled
0 = De-Skew Disabled, 0 step is selected

3.3.1.7 Control Register 4

Table 3-8 Control Register 4

$0E

	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	TX_EESS	TX_HDMI
Reset:	-	-	-	-	-	-	0	1

TX_EESS — Enable Enhanced Encryption Signalling for the selected transmitter port

1 = Using Enhanced Encryption Signalling for the selected transmitter port.
0 = Using Original Encryption Signalling for the selected transmitter port. This is only valid if the selected transmitter is working in DVI mode (TX_HDMI = 0).

TX_HDMI — Set HDMI mode for the selected transmitter port

1 = Put the selected transmitter port working in HDMI mode. This is valid only if the receiver is receiving HDMI signal.
0 = Put the selected transmitter port working in DVI mode.

3.3.1.8 Control Register 5

Table 3-9 Control Register 5

$0F

	6	5	4	3	2	1	0
R	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN
W								
	-	-	-	0	-	-	-	0

TX_AKSV_RDY — Transmitter AKSV Ready

The TX_AKSV_RDY bit indicates whether the HDCP keys and AKSV has been successfully downloaded from external EE or not for the selected transmitter port. This bit is read only.

1 = HDCP keys and AKSV has been successfully downloaded from external EE. AKSV is ready for read.

0 = HDCP keys and AKSV downloading has not been completed. AKSV is not ready for read.

TX_ENC_ON — Transmitter HDCP Encryption On

The TX_ENC_ON bit indicates whether the HDCP encryption for the selected transmitter port is active or not. This bit is read only.

1 = HDCP encryption is active.

0 = HDCP encryption is not active.

TX_RPTR — Transmit to Repeater

The TX_RPTR bit should be set if the receiver side which is connected to the selected transmitter port is a repeater. It should be cleared otherwise.

1 = The selected transmitter port is connecting to a repeater.

0 = The selected transmitter port is not connecting to a repeater.

TX_RI_RDY — Transmitter RI Ready

This bit indicates that the first Ri value is available for the selected transmitter port. This bit is read only.

1 = First Ri value is available for the selected transmitter port.

0 = First Ri value is not available for the selected transmitter port.

TX_ENC_EN — Transmitter ENC Enable

1 = Enable HDCP encryption for the selected transmitter port.

0 = Disable HDCP encryption the selected transmitter port.

3.3.1.9 TX_BKSV Registers - TX_BKSV_1 ~ TX_BKSV_5

These 5 registers for the selected transmitter port should be programmed with receiver's Key Selection Vector. TX_BKSV_1 is the LSB and TX_BKSV_5 is the MSB. TX_BKSV_5 should be written last, as it triggers the authentication process.

3.3.1.10 TX_AN Registers - TX_AN_1 ~ TX_AN_8

These 8 registers for the selected transmitter port should be programmed with a 64-bit pseudo-random value before triggering the authentication process. TX_AN_1 is the LSB and TX_AN_8 is the MSB.

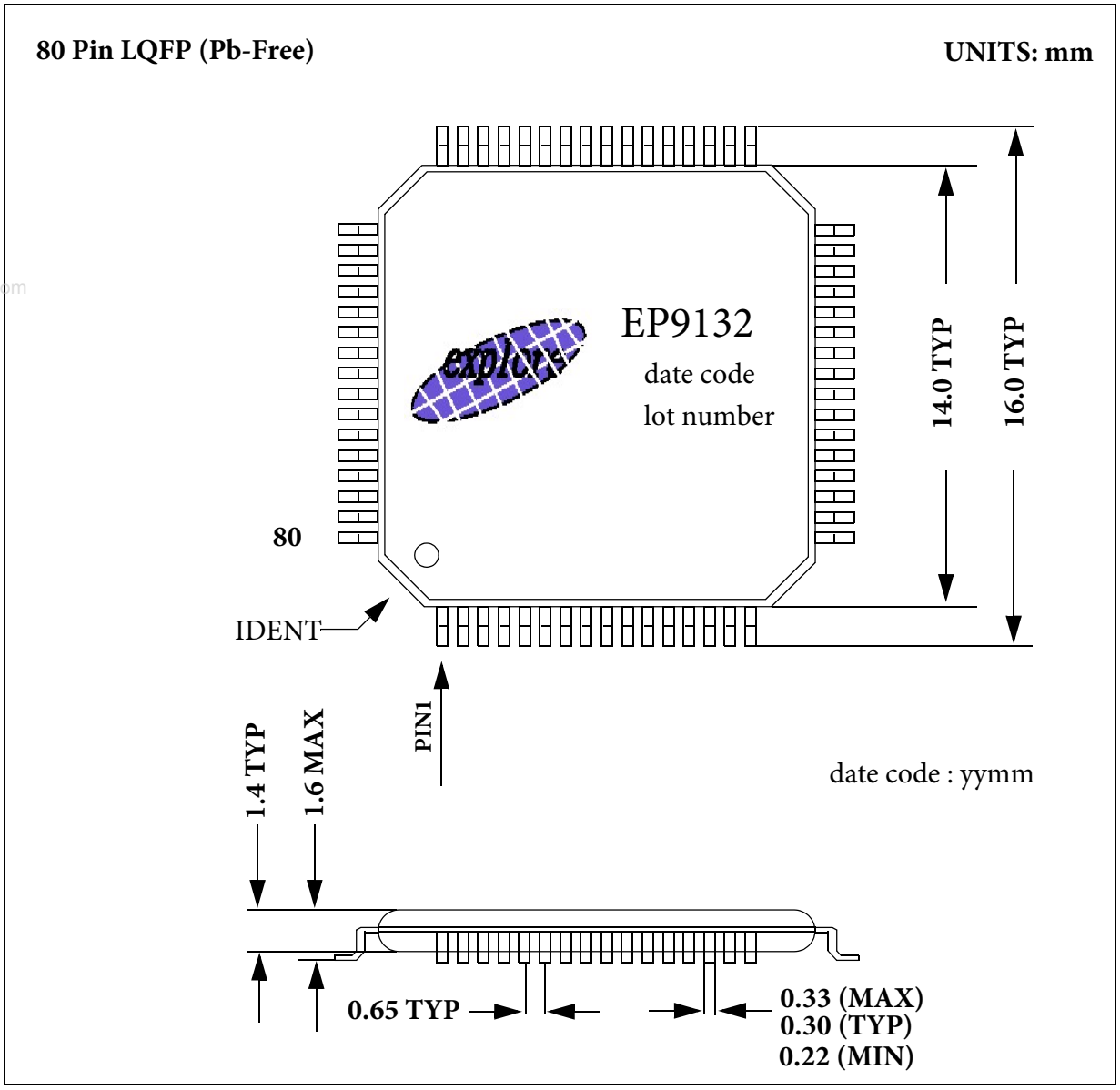
3.3.1.11 TX_AKSV Registers - TX_AKSV_1 ~ TX_AKSV_5

These 5 registers are read only which hold transmitter's Key Selection Vector for the selected transmitter port. TX_AKSV_1 is the LSB and TX_AKSV_5 is the MSB. All five bytes should be read from here and then written to the receiver. Byte 5 should be written last to the receiver, as it will trigger authentication there. These 5 registers should not be read until TX_AKSV_RDY bit is 1.

3.3.1.12 TX_RI Registers - TX_RI_1 ~ TX_RI_2

These 2 registers hold transmitter's Ri value for the selected transmitter port. They should be read and compared against the Ri value of the receiver to ensure that the encryption process on the transmitter and receiver is synchronized.

Section 4 Package



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