CYPRESS

# Three-PLL General Purpose
# EPROM Programmable Clock Generator

| Features | Benefits |
|---|---|
| • **Three integrated phase-locked loops** | Provides all necessary system clocks in a single package |
| • **EPROM programmability** | Easy customization and fast turnaround time |
| • **Low skew, low jitter, high accuracy outputs** | Meets critical timing requirements in complex system designs |
| • **Power management options (Shutdown, OE, Suspend)** | Supports low power applications |
| • **Frequency select option** | Enables design flexibility and margin testing |
| • **Smooth slewing on CPUCLK** | Allows downstream PLLs to stay locked on CPUCLK output |
| • **3.3V or 5V operation** | Enables application compatibility |

| Part Number | Outputs | Input Frequency Range | Output Frequency Range | Specifics |
|---|---|---|---|---|
| CY2291 | 8 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–100 MHz (5V) 76.923 kHz–80 MHz (3.3V) | Factory Programmable Commercial Temperature |
| CY2291I | 8 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V) | Factory Programmable Industrial Temperature |
| CY2291F | 8 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V) | **Field Programmable** Commercial Temperature |
| CY2292 | 6 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–100 MHz (5V) 76.923 kHz–80 MHz (3.3V) | Factory Programmable Commercial Temperature |
| CY2292I | 6 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V) | Factory Programmable Industrial Temperature |
| CY2292F | 6 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V) | **Field Programmable** Commercial Temperature |
| CY2295 | 8 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–100 MHz (5V) 76.923 kHz–80 MHz (3.3V) | Factory Programmable Commercial Temperature |
| CY2295I | 8 | 10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock) | 76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V) | Factory Programmable Industrial Temperature |

## Logic Block Diagram

CY2291/CY2291F/CY2291I
CY2292/CY2292F/CY2292I
CY2295/CY2295I

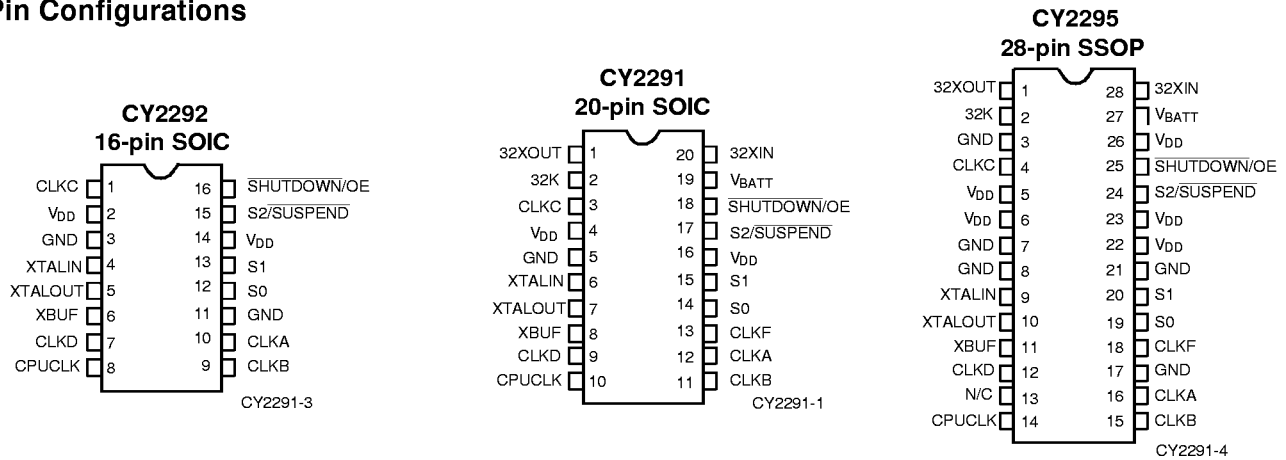## Pin Configurations

**CY2292**
**16-pin SOIC**

```
CLKC    [ 1      16 ]  SHUTDOWN/OE
VDD     [ 2      15 ]  S2/SUSPEND
GND     [ 3      14 ]  VDD
XTALIN  [ 4      13 ]  S1
XTALOUT [ 5      12 ]  S0
XBUF    [ 6      11 ]  GND
CLKD    [ 7      10 ]  CLKA
CPUCLK  [ 8       9 ]  CLKB
                          CY2291-3
```

**CY2291**
**20-pin SOIC**

```
32XOUT  [ 1      20 ]  32XIN
32K     [ 2      19 ]  VBATT
CLKC    [ 3      18 ]  SHUTDOWN/OE
VDD     [ 4      17 ]  S2/SUSPEND
GND     [ 5      16 ]  VDD
XTALIN  [ 6      15 ]  S1
XTALOUT [ 7      14 ]  S0
XBUF    [ 8      13 ]  CLKF
CLKD    [ 9      12 ]  CLKA
CPUCLK  [ 10     11 ]  CLKB
                          CY2291-1
```

**CY2295**
**28-pin SSOP**

```
32XOUT  [ 1      28 ]  32XIN
32K     [ 2      27 ]  VBATT
GND     [ 3      26 ]  VDD
CLKC    [ 4      25 ]  SHUTDOWN/OE
VDD     [ 5      24 ]  S2/SUSPEND
VDD     [ 6      23 ]  VDD
GND     [ 7      22 ]  VDD
GND     [ 8      21 ]  GND
XTALIN  [ 9      20 ]  S1
XTALOUT [ 10     19 ]  S0
XBUF    [ 11     18 ]  CLKF
CLKD    [ 12     17 ]  GND
N/C     [ 13     16 ]  CLKA
CPUCLK  [ 14     15 ]  CLKB
                          CY2291-4
```

## Pin Summary

| Name | Pin Number CY2291 | Pin Number CY2292 | Pin Number CY2295 | Description |
|---|---|---|---|---|
| 32XOUT | 1 | — | 1 | 32.768 kHz crystal feedback |
| 32K | 2 | — | 2 | 32.768 kHz output (always active if $V_{BATT}$ is present) |
| CLKC | 3 | 1 | 4 | Configurable clock output C |
| $V_{DD}$ | 4, 16 | 2, 14 | 5, 6, 22, 23, 26 | Voltage supply |
| GND | 5 | 3, 11 | 3, 7, 8, 17, 21 | Ground |
| XTALIN[1] | 6 | 4 | 9 | Reference crystal input or external reference clock input |
| XTALOUT[1, 2] | 7 | 5 | 10 | Reference crystal feedback |
| XBUF | 8 | 6 | 11 | Buffered reference clock output |
| CLKD | 9 | 7 | 12 | Configurable clock output D |
| CPUCLK | 10 | 8 | 14 | CPU frequency clock output |
| CLKB | 11 | 9 | 15 | Configurable clock output B |
| CLKA | 12 | 10 | 16 | Configurable clock output A |
| CLKF | 13 | — | 18 | Configurable clock output F |
| S0 | 14 | 12 | 19 | CPU clock select input, bit 0 |
| S1 | 15 | 13 | 20 | CPU clock select input, bit 1 |
| S2/SUSPEND | 17 | 15 | 24 | CPU clock select input, bit 2. Optionally enables suspend feature when LOW [3] |
| SHUTDOWN/OE | 18 | 16 | 25 | Places outputs in three-state[4] condition and shuts down chip when LOW. Optionally, only places outputs in three-state[4] condition and does not shut down chip when LOW |
| $V_{BATT}$ | 19 | — | 27 | Battery supply for 32.768-kHz circuit |
| 32XIN | 20 | — | 28 | 32.768-kHz crystal input |

**Notes:**
1. For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF or 18 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
3. Please refer to application note "Understanding the CY2291, CY2292 and CY2295" for more information.
4. The CY2291 has weak pull-downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

## Operation

The CY2291, CY2292 and CY2295 are a third-generation family of clock generators. The CY2291 is upwardly compatible with the industry standard ICD2023 and ICD2028 and continues their tradition by providing a high level of customizable features to meet the diverse clock generation needs of modern motherboards and other synchronous systems. The CY2292 differs from the CY2291 in that it comes in a 16-pin 150-mil SOIC package, and does not provide either the 32-kHz or CLKF outputs. The CY2295 is available in a space-saving 28-pin SSOP package.

All parts provide a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs (CLKA–CLKD) can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same or related[3] frequencies will have low ($\leq$500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2291, CY2292, and CY2295 can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing full customization of output frequencies. The reference oscillator has been designed for 10-MHz to 25-MHz crystals, providing additional flexibility. No external components are required with this crystal. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used. Customers using the 32-kHz oscillator on the CY2291 or CY2295 should connect a 10-M$\Omega$ resistor in parallel with the 32-kHz crystal.

## Output Configuration

The CY2291 and CY2295 (and CY2292) have five (four) independent frequency sources on chip. These are the 32-kHz oscillator (not available on CY2292), the reference oscillator, and three Phase Locked Loops (PLLs). Each PLL has a specific function. The System PLL (SPLL) drives the CLKF output (not available on CY2292) and provides fixed output frequencies on the configurable outputs. The SPLL offers the most output frequency divider options. The CPU PLL (CPLL) is controlled by the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. The Utility PLL (UPLL) provides the most accurate clock. It is often used for miscellaneous frequencies not provided by the other frequency sources.

All configurations are EPROM programmable, providing short sample and production lead times. Please refer to the application note "Understanding the CY2291, CY2292, and CY2295" for information on configuring the part.

## Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW (the 32-kHz clock output is not affected). If system shutdown is enabled (the default), a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the $V_{DD}$ pins will be less than 50 µA (for Commercial Temp. or 100 µA for Industrial Temp.) plus 15 µA max. for the 32-kHz subsystem and is typically 10 µA. After leaving shutdown mode, the PLLs will have to re-lock. All outputs except 32K have a weak pull-down so that the outputs do not float when three-stated.[4]

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs except 32K can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.[3]

The CPUCLK can slew (transition) smoothly between 8 MHz and the maximum output frequency (100 MHz at 5V/80 MHz at 3.3V for Commercial Temp. parts or 90 MHz at 5V/66.6 MHz at 3.3V for Industrial Temp. and for field-programmed parts). This feature is extremely useful in "Green" PC and laptop applications, where reducing the frequency of operation can result in considerable power savings. This feature meets all 486 and Pentium processor slewing requirements.

## CyClocks™ Software

CyClocks is an easy-to-use application that allows you to configure any one of the EPROM programmable clocks offered by Cypress. You may specify the input frequency, PLL & output frequencies, and different functional options. Please note the output frequency ranges in this datasheet when specifying them in CyClocks to ensure that you stay within the limits. CyClocks also has a power calculation feature that allows you to see the power consumption of your specific configuration. You can download a copy of CyClocks for free on Cypress's website at www.cypress.com.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ................................................ –0.5V to +7.0V

DC Input Voltage ........................................... –0.5V to +7.0V

Storage Temperature ................................. –65°C to +150°C

Max. Soldering Temperature (10 sec) ......................... 260°C

Junction Temperature ................................................... 150°C

Package Power Dissipation ..................................... 750 mW

Static Discharge Voltage .......................................... >2000V
(per MIL-STD-883, Method 3015)

## Operating Conditions[5]

| Parameter | Description | Part Numbers | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage, 5.0V (3.3V) operation | All | 4.5 (3.0) | 5.5 (3.6) | V |
| $V_{BATT}$ | Battery Backup Voltage | All | 2.0 | 5.5 | V |
| $T_A$ | Operating Temperature, Ambient | CY2291/CY2291F CY2292/CY2292F CY2295 | 0 | +70 | °C |
| | | CY2291I CY2292I CY2295I | –40 | +85 | °C |
| $C_{LOAD}$ | Max. Load Capacitance 5.0V (3.3V) Operation | All | | 25 (15) | pF |
| $f_{REF}$ | Reference Frequency | All | 10.0 | 25.0 | MHz |
| $f_{REF}$ | Reference Frequency, External Reference Clock[6, 7, 8] | All | 1 | 30 | MHz |

## Electrical Characteristics

| Parameter | Description | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$[9] | HIGH-Level Output Voltage | $I_{OH} = 4.0$ mA | | 2.4 | | | V |
| $V_{OL}$[9] | LOW-Level Output Voltage | $I_{OL} = 4.0$ mA | | | | 0.4 | V |
| $V_{OH-32}$ | 32.768-kHz HIGH-Level Output Voltage | $I_{OH} = 0.5$ mA | | $V_{BATT}$ 0.5 | | | V |
| $V_{OL-32}$ | 32.768-kHz LOW-Level Output Voltage | $I_{OL} = 0.5$ mA | | | | 0.4 | V |
| $V_{IH}$ | HIGH-Level Input Voltage[10] | Except crystal pins | | 2.0 | | | V |
| $V_{IL}$ | LOW-Level Input Voltage[10] | Except crystal pins | | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN} = V_{DD}$–0.5V | | | < 1 | 10 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN} = +0.5$V | | | < 1 | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | Three-state outputs | | | | 250 | µA |
| $I_{DD}$ | $V_{DD}$ Supply Current[11] | $V_{DD} = V_{DD}$ max., 5V (3.3V) operation | | | 75(50) | 100(65) | mA |
| $I_{DDS}$ | $V_{DD}$ Power Supply Current in Shutdown Mode[11] | Shutdown active, excluding $V_{BATT}$ | CY2291/CY2291F CY2292/CY2292F CY2295 | | 10 | 50 | µA |
| | | | CY2291I CY2292I CY2295I | | 10 | 100 | µA |
| $I_{BATT}$ | $V_{BATT}$ Power Supply Current | $V_{BATT} = 3.0$V | | | 5 | 15 | µA |

Notes:
5. Electrical parameters are guaranteed with these operating conditions.
6. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}$/2.
7. Please refer to application note "Crystal Oscillator Topics" for information on AC-coupling the external input reference clock.
8. The oscillator circuit is optimized for a crystal reference and for external reference clocks up to 20 MHz. For external reference clocks above 20 MHz, it is recommended that a 150-ohm pull-up resistor to $V_{DD}$ be connected to the Xout pin.
9. All outputs swing rail to rail.
10. Xtal inputs have CMOS thresholds.
11. Load = Max., $V_{IN}$ = 0V or $V_{DD}$, Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations will vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.06 \cdot (F_{CPLL}+F_{UPLL}+2 \cdot F_{SPLL})+0.27 \cdot (F_{CLKA}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CPUCLK}+F_{CLKF}+F_{XBUF})$.

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## Switching Characteristics[12]

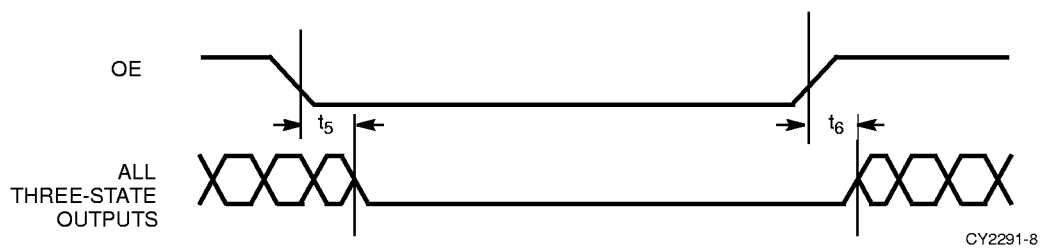| Parameter | Name | Description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_1$ | Output Period | Clock output range, 5V operation | CY2291 CY2292 CY2295 | 10 (100 MHz) | | 13000 (76.923 kHz) | ns |
| | | | CY2291F/CY2291I CY2292F/CY2291I CY2295I | 11.1 (90 MHz) | | 13000 (76.923 kHz) | ns |
| $t_1$ | Output Period | Clock output range, 3.3V operation | CY2291 CY2292 CY2295 | 12.5 (80 MHz) | | 13000 (76.923 kHz) | ns |
| | | | CY2291F/CY2291I CY2292F/CY2291I CY2295I | 15 (66.6 MHz) | | 13000 (76.923 kHz) | ns |
| | Output Duty Cycle[13] | Duty cycle for outputs, defined as $t_2 \div t_1$[14] $f_{OUT} \geq 66$ MHZ | | 40% | 50% | 60% | |
| | | Duty cycle for outputs, defined as $t_2 \div t_1$[14] $f_{OUT} < 66$ MHZ | | 45% | 50% | 55% | |
| $t_3$ | Rise Time | Output clock rise time[15] | | | 3 | 5 | ns |
| $t_4$ | Fall Time | Output clock fall time[15] | | | 2.5 | 4 | ns |
| $t_5$ | Output Disable Time | Time for output to enter three-state mode after SHUTDOWN/OE goes LOW | | | 10 | 15 | ns |
| $t_6$ | Output Enable Time | Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH | | | 10 | 15 | ns |
| $t_7$ | Skew | Skew delay between any identical or related outputs[3, 14] | | | < 0.25 | 0.5 | ns |
| $t_8$ | CPUCLK Slew | Frequency transition rate | | 1.0 | | 20.0 | MHz/ ms |
| $t_{9A}$ | Clock Jitter[16] | Peak-to-peak period jitter ($t_{9A}$ max. $- t_{9A}$ min.), % of clock period ($f_{OUT} \leq 4$ MHz) | | | <0.5 | 1 | % |
| $t_{9B}$ | Clock Jitter[16] | Peak-to-peak period jitter ($t_{9B}$ max. $- t_{9B}$ min.) (4 MHz $\leq f_{OUT} \leq 16$ MHz) | | | <0.7 | 1 | ns |
| $t_{9C}$ | Clock Jitter[16] | Peak-to-peak period jitter (16 MHz $< f_{OUT} \leq 50$ MHz) | | | <400 | 500 | ps |
| $t_{9D}$ | Clock Jitter[16] | Peak-to-peak period jitter ($f_{OUT} > 50$ MHz) | | | <250 | 350 | ps |
| $t_{10A}$ | Lock Time for CPLL | Lock Time from Power-up | | | <25 | 50 | ms |
| $t_{10B}$ | Lock Time for UPLL and SPLL | Lock Time from Power-up | | | <0.25 | 1 | ms |
| | Slew Limits | CPU PLL Slew Limits | CY2291 CY2292 CY2295 | 8 | | 100 (5V) 80 (3.3V) | MHz |
| | | | CY2291F/CY2291I CY2292F/CY2291I CY2295I | 8 | | 90 (5V) 66.6 (3.3V) | MHz |

Notes:
12. Guaranteed by design and characterization, not 100% tested in production.
13. XBUF duty cycle depends on XTALIN duty cycle.
14. Measured at 1.4V.
15. Measured between 0.4V and 2.4V.
16. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the application note: "Jitter in PLL-Based Systems."
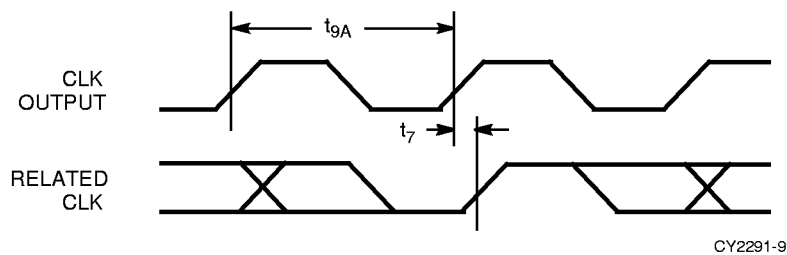
## Switching Waveforms

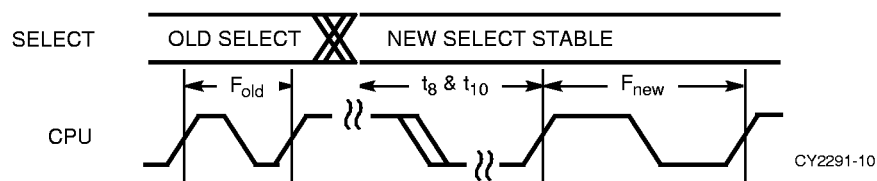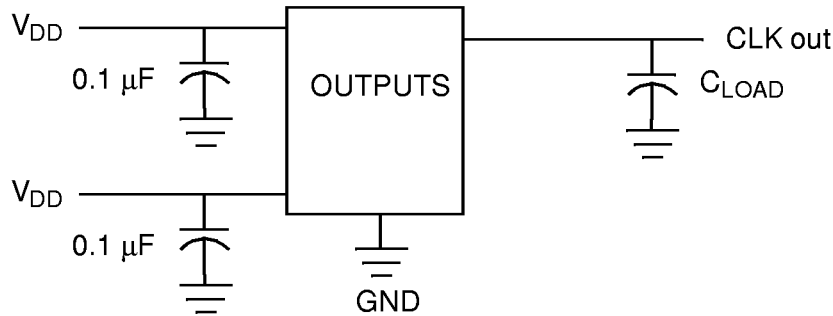### All Outputs, Duty Cycle and Rise/Fall Time

OUTPUT

t

$t_2$

$t_3$

$t_4$
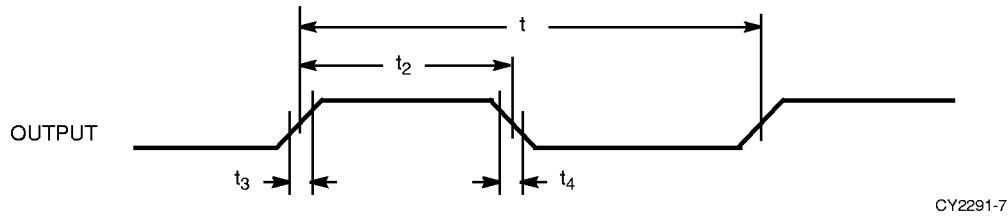
CY2291-7

### Output Three-State Timing[4]

OE

ALL
THREE-STATE
OUTPUTS

$t_5$

$t_6$

CY2291-8

### CLK Outputs Jitter and Skew

CLK
OUTPUT

RELATED
CLK

$t_{9A}$

$t_7$

CY2291-9

### CPU Frequency Change

SELECT

OLD SELECT    NEW SELECT STABLE

CPU

$F_{old}$

$t_8$ & $t_{10}$

$F_{new}$

CY2291-10

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## Test Circuit



CY2291-11

## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltage |
|---|---|---|---|---|
| CY2291SC–XXX | S5 | 20-Pin SOIC | Commercial | 5.0V |
| CY2292SC–XXX | S16 | 16-Pin SOIC | Commercial | 5.0V |
| CY2295PVC–XXX | O28 | 28-Pin SSOP | Commercial | 5.0V |
| CY2291SL–XXX | S5 | 20-Pin SOIC | Commercial | 3.3V |
| CY2292SL–XXX | S16 | 16-Pin SOIC | Commercial | 3.3V |
| CY2295PVL–XXX | O28 | 28-Pin SSOP | Commercial | 3.3V |
| CY2291F | S5 | 20-Pin SOIC | Commercial | 3.3V or 5.0V |
| CY2292F | S16 | 16-Pin SOIC | Commercial | 3.3V or 5.0V |
| CY2291SI–XXX | S5 | 20-Pin SOIC | Industrial | 3.3V or 5.0V |
| CY2292SI–XXX | S16 | 16-Pin SOIC | Industrial | 3.3V or 5.0V |
| CY2295PVI–XXX | O28 | 28-Pin SSOP | Industrial | 3.3V or 5.0V |

Document #: 38–00410–E

## Custom Configuration Request Procedure

The CY229x are EPROM-programmable devices which may be configured in the factory or in the field by a Cypress Field Application Engineer (FAE). The output frequencies requested will be matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress FAE or sales representative. There are two methods to use to request custom configurations:

1. Use CyClocks™ software. This software automatically calculates the output frequencies that can be generated by the CY229x devices and provides a print-out of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative. The CyClocks software is available free-of-charge from the Cypress website (http://www.cypress.com) or from your local sales representative.

2. Use the custom configuration form attached. All areas must be filled in with the exception of shaded cells and the form submitted to the appropriate Cypress FAE or sales representative.

If requesting samples through the factory:

Once the custom request has been processed you will receive a part number with a 3-digit extension (e.g., CY2292SC-128) specific to the frequencies and pinout of your device. This will be the part number used for samples requests and production orders.

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# CY2291/CY2291F/CY2291I
# CY2292/CY2292F/CY2292I
# CY2295/CY2295I

**CYPRESS**

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## CY2291/2/5 CUSTOM CONFIGURATION REQUEST FORM
### (Please submit to your local FAE or sales representative)

Company _____  Engineer _____  FAE/Sales _____

Phone# _____  Fax# _____

**CIRCLE ONE**          **CY2291**          **CY2292**          **CY2295**

The CY2291, CY2295, and CY2292 are the industry's most flexible frequency synthesizers, offering a high degree of config-urability due to their unique internal programmable EPROM array. Of the CY2291/2/5's outputs, six (five on the CY2292) may be defined within the scope of the PLL frequencies and divider criteria described in the following. Shaded areas are for Cypress use only. Contact your local Cypress representative for assistance.

1. **OPERATING VOLTAGE** (Circle one)          **3.3V**          **5.0V**

2. **INPUT REFERENCE FREQUENCY** (Circle one)          **Crystal**          **External Clock**          **14.31818 MHz** (Default)
   If a different reference is required, specify the frequency in the box to the right
   (must be between 10 MHz and 25 MHz for crystal, 1 MHz and 30 MHz for external clock):

3. **CPU-PLL (CPLL) FREQUENCIES** ("Off" is a valid selection for any address and will automatically be entered for blanks.)

| Select S2 S1 S0 | Requested | Actual |
|---|---|---|
| 0 0 0 | | |
| 0 0 1 | | |
| 0 1 0 | | |
| 0 1 1 | | |
| 1 0 0 | | |
| 1 0 1 | | |
| 1 1 0 | | |
| 1 1 1 | | |

If the Suspend Option is specified in #7 below, the Select MSB (S2) serves a dual function as both the MSB CPU address and as the Suspend select pin. The CPU frequencies speci-fied for addresses 000–011 will be active unless the CPU-PLL is shut down during the suspend mode (CPU-PLL is circled in #7). Also, any outputs derived from a non-suspended CPU-PLL (assigned in #5 as options 5–8) that are not circled in #7 will remain active during the suspend mode.

Range: 8–100 MHz at 5V; 8–80 MHz at 3.3V (Commercial)
8–90 MHz at 5V, 8–66.6 MHz at 3.3V (Industrial/Field-Prog)
Default = "Off" for all selections

4. **UTILITY-PLL (UPLL) AND SYSTEM-PLL (SPLL) FREQUENCIES** ("Off" is a valid frequency selection for either PLL.)
   To minimize harmonic effects, avoid setting any PLL to an equal or multiple frequency of another PLL.

| | Requested | Actual |
|---|---|---|
| UPLL | | |
| SPLL | | |

(Commercial)
8–90 MHz at 5V, 8–66.6 MHz at 3.3V (Industrial/Field-Prog)
Default = 96 MHz at 5V; 48 MHz at 3.3V

Range: 8–100 MHz at 5V; 8–80 MHz at 3.3V (Commercial)
8–90 MHz at 5V, 8–66.6 MHz at 3.3V (Industrial/Field-Prog)
Default = 96 MHz at 5V; 48 MHz at 3.3V

5. **OUTPUT CONFIGURATION** ("Off" is a valid selection for any output and will automatically be entered for blanks.)
   Assign by number from the Output Options Table below and fill in the Frequency column as a double-check.

**Output Options Table**

| | | | | | |
|---|---|---|---|---|---|
| 1. Ref | 6. CPLL/2 | 11. UPLL/4 | 16. SPLL/4 | 21. SPLL/12 | 26. SPLL/40 |
| 2. Ref/2 | 7. CPLL/4 | 12. UPLL/8 | 17. SPLL/5 | 22. SPLL/13 | 27. SPLL/48 |
| 3. Ref/4 | 8. CPLL/8 | 13. SPLL | 18. SPLL/6 | 23. SPLL/20 | 28. SPLL/52 |
| 4. Ref/8 | 9. UPLL | 14. SPLL/2 | 19. SPLL/8 | 24. SPLL/24 | 29. SPLL/96 |
| 5. CPLL | 10. UPLL/2 | 15. SPLL/3 | 20. SPLL/10 | 25. SPLL/26 | 30. SPLL/104 |

CLKF (Options 14–16, Off)
XBUF (Option 1 only)
CPUCLK (Options 5–7, Off)

CLKA (Options 1–30, Off)
CLKB (Options 1–30, Off)
CLKC (Options 1–30, Off)
CLKD (Options 1–30, Off)

*32K and CLKF are not available on the CY2292.*          *For CLKD only: option #4 (Ref/8) is replaced with Ref/3.*

6. **SHUTDOWN OPTION** (Circle Yes or No)          **Yes**          **No**

7. **SUSPEND OPTION** (Circle Yes or No)          **Yes**          **No**

IF SUSPEND = "Yes": Circle each resource to be shut down when the Suspend mode is active (S2=0). Note that suspending a PLL automatically suspends its outputs.

| CPU-PLL | XBUF | CLKA |
|---|---|---|
| UTIL-PLL | CPUCLK | CLKB |
| SYS-PLL | CLKF | CLKC |
| | | CLKD |

**FOR CYPRESS USE ONLY** (Shaded Areas above and below)

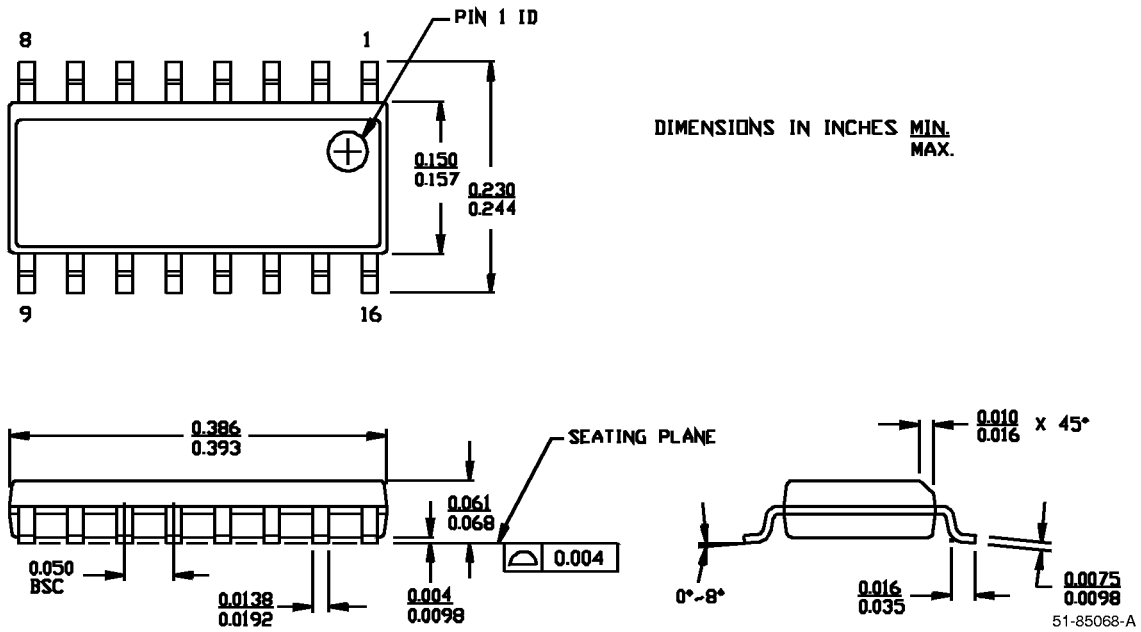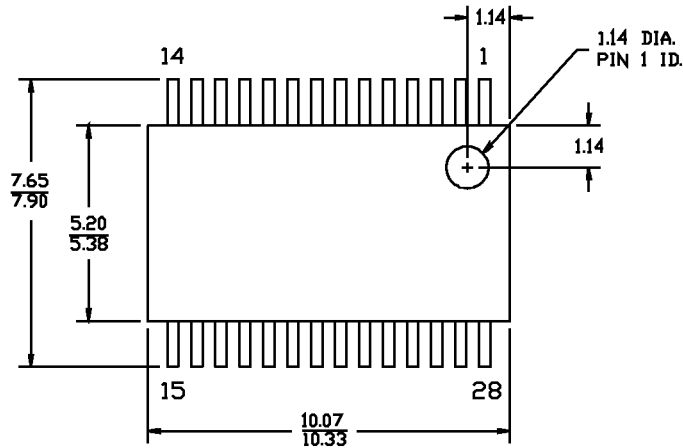| Customer Configuration | Marking |
|---|---|
| Date | Quantity |

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## Package Diagrams

### 20-Lead (300-Mil) Molded SOIC S5

PIN 1 ID

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$

51-85024-A
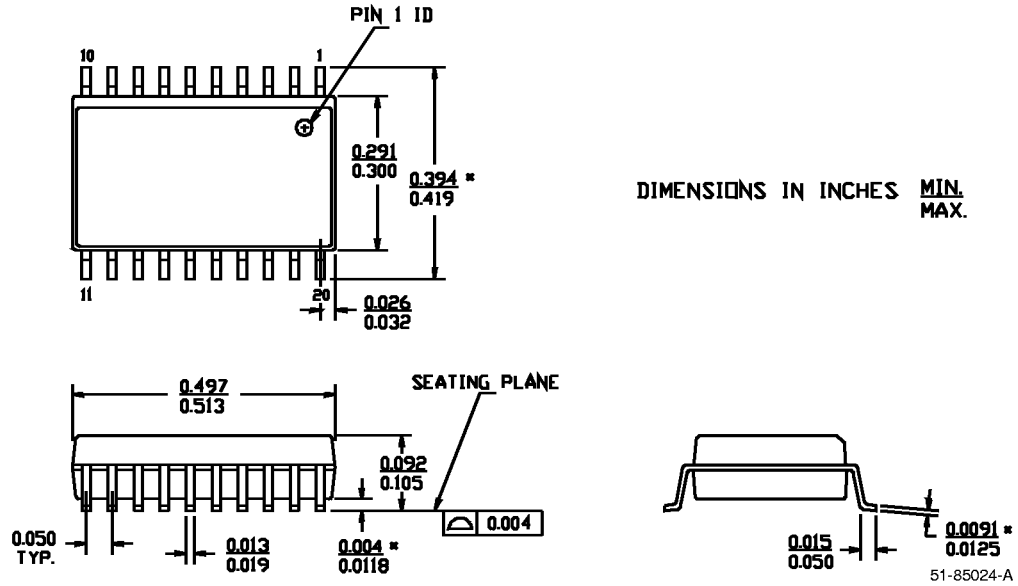
### 16-Lead (150-Mil) Molded SOIC S16

PIN 1 ID

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$

51-85068-A

9

**Package Diagrams** (continued)

### 28-Lead (210-Mil) Shrunk Small Outline Package O28



DIMENSIONS IN MILLIMETERS $\frac{\text{MIN.}}{\text{MAX.}}$

51-85079-B