ANALOG DEVICES

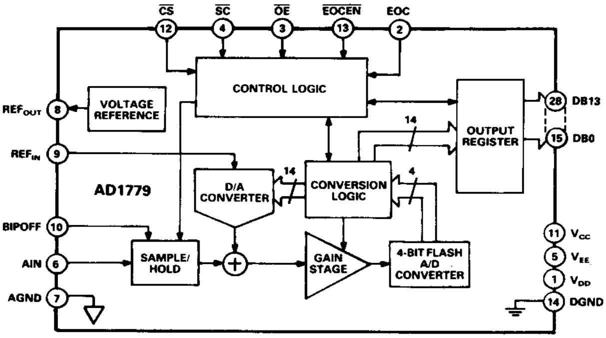
14-Bit 100 KSPS Complete Sampling ADC

AD1779

FEATURES

AC Characterized and Specified
100k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
80 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
16-Bit Bus Interface (See AD1679 for 8-Bit Interface)
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD1779 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1779 is a complete, 14-bit monolithic analog-to-digital converter consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The 14 data bits are accessed by a 16-bit bus in a single read operation. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm, which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD1779 operates from +5 V and ±12 V supplies and dissipates 720 mW. A 28-pin plastic DIP and a 0.6″ wide ceramic DIP are available. Contact factory for surface-mount package options.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD1779 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. PERFORMANCE: The AD1779 provides a throughput of 100k conversions per second. S/N+D is 80 dB (K grade) at 10 kHz and remains flat beyond the Nyquist frequency.
3. SPECIFICATIONS: The AD1779 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD. These parameters are important in signal processing applications as they indicate the AD1779's effect on the spectral content of the input signal.
4. EASE OF USE: The pinout is designed for easy board layout, and the single read output provides compatibility with 16-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
5. RELIABILITY: The AD1779 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = + 5 V ±10%, f_{SAMPLE} = 100 KSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD1779J			AD1779K			Units
	Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
−0.5 dB Input (Referred to −0 dB Input)	78	79		**80**	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−90	**−84**		−90	**−84**	dB
		0.003	**0.006**		0.003	**0.006**	%
T_{min} to T_{max}		−88	**−82**		−88	**−82**	dB
		0.004	**0.008**		0.004	**0.008**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	**−84**		−90	**−84**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

NOTES

[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full-scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.

[2] See Figure 7 for higher frequencies and other input amplitudes.

[3] See Figures 5 and 6 for other conditions.

[4] f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 KSPS. See Figure 9 and Definition of Specifications section.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter	Test Conditions	Min	Max	Units
LOGIC INPUTS				
V_{IH} High Level Input Voltage		2.4		V
V_{IL} Low Level Input Voltage			**0.8**	V
I_{IH} High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL} Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN} Input Capacitance			10	pF
LOGIC OUTPUTS				
V_{OH} High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
	I_{OH} = 0.5 mA	2.4		V
V_{OL} Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ} High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{OZ} High Z Output Capacitance			10	pF

NOTES

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

DC SPECIFICATIONS (@ +25°C, V_{CC}=+12 V ±5%, V_{EE}=−12 V ±5%, V_{DD}=+5 V ±10% unless otherwise indicated)

Parameter	AD1779J			AD1779K			Units
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error		±1			±1		LSB
Differential Linearity							
T_{min} to T_{max} (No Missing Codes)	**14**			**14**			Bits
Unipolar Zero Error[1]		±10			±10		LSB
Bipolar Zero Error[1]		±10			±10		LSB
Unipolar Gain Error[1,2]		±12			±12		LSB
Bipolar Gain Error[1,2]		±12			±12		LSB
Temperature Drift (Coefficients)[3]							
Unipolar Zero		±8 (10)			±8 (10)		LSB (ppm/°C)
Bipolar Zero		±8 (10)			±8 (10)		LSB (ppm/°C)
Unipolar Gain		±16 (20)			±16 (20)		LSB (ppm/°C)
Bipolar Gain		±16 (20)			±16 (20)		LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	µs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[4]	**4.95**		**5.05**	**4.95**		**5.05**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
Power Supply Rejection		1			1		mV/V
POWER SUPPLIES (T_{min} to T_{max})							
Operating Voltages							
V_{CC}	+11.4	+12	+12.6	+11.4	+12	+12.6	V
V_{EE}	−12.6	−12	−11.4	−12.6	−12	−11.4	V
V_{DD}	+4.5	+5	+5.5	+4.5	+5	+5.5	V
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	720		560	720	mW

NOTES

[1] Adjustable to zero; see Figures 11 and 12.

[2] Includes internal voltage reference error.

[3] Includes internal voltage reference drift.

[4] With maximum external load applied.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (All device types T_{min} to T_{max}, $V_{CC} = +12$ V ±5%, $V_{EE} = -12$ V ±5%, $V_{DD} = +5$ V ±10%)

Parameter	Symbol	Min	Max	Units
Conversion Rate[1]	t_{CR}		10	µs
Convert Pulse Width	t_{CP}	150		ns
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		8.5	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2]	t_{BA}		100	ns
Float Delay[3]	t_{FD}	10	80	ns
Update Delay	t_{UD}		200	ns
$\overline{\text{OE}}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	150		ns
Conversion Delay	t_{CD}	400		ns

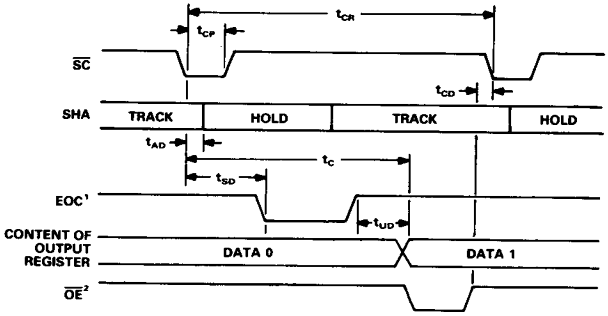
NOTES

[1] Includes Acquisition Time.

[2] Measured from the falling edge of $\overline{\text{OE/EOCEN}}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4; C_{OUT} = 100 pF.

[3] Measured from the rising edge of $\overline{\text{OE/EOCEN}}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 4; C_{OUT} = 10 pF.

Specifications subject to change without notice.



NOTES
¹$\overline{\text{EOCEN}}$ = LOW.
²DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

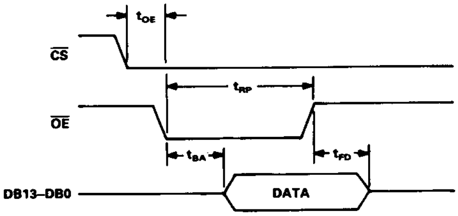


Figure 2. Output Timing

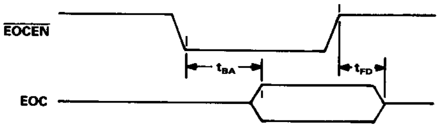


Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

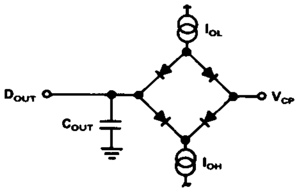


Figure 4. Load Circuit for Bus Timing Specifications

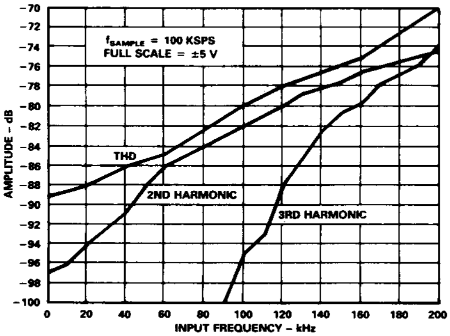


Figure 5. Harmonic Distortion vs. Input Frequency (−0.5 dB Input)

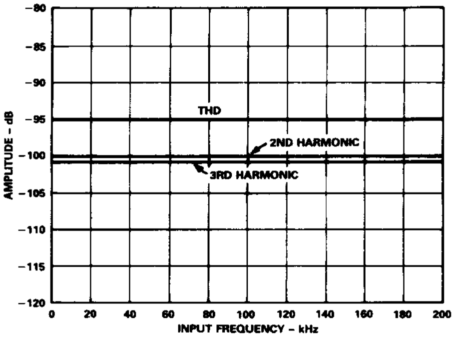


Figure 6. Harmonic Distortion vs. Input Frequency (−20 dB Input)

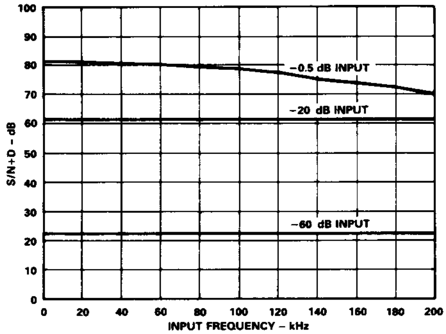


Figure 7. S/N+D vs. Input Frequency and Amplitude

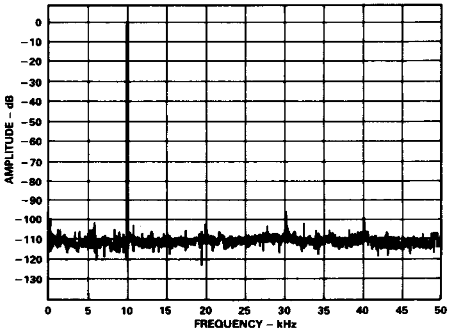


Figure 8. 5-Plot Averaged 2048 Point FFT at 100 KSPS, f_{IN} = 10.009 kHz

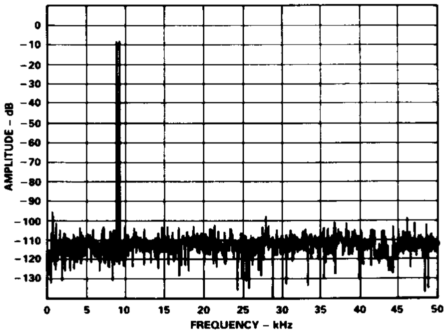


Figure 9. Nonaveraged IMD Plot for f_{IN} = 9.08 kHz (f_a), 9.58 kHz (f_b) at 100 KSPS

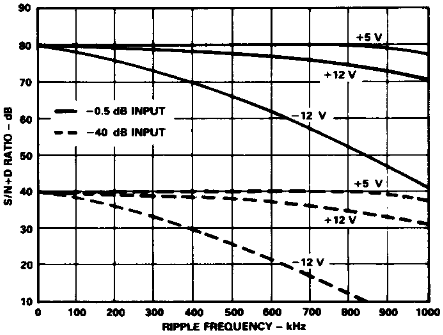


Figure 10. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 100 KSPS, V_{RIPPLE} = 0.1 V p-p)

CONVERSION CONTROL

Before a conversion is started, End Of Convert (EOC) is HIGH and the sample-hold is in track mode. A conversion is started by bringing $\overline{\text{SC}}$ LOW, regardless of the state of $\overline{\text{CS}}$.

After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 μs maximum. The acquisition time does not affect the throughput rate as the AD1779 goes back into track mode more than 2 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

When the conversion is finished, EOC goes HIGH and the result is loaded into the output register after a period of time t_{UD}. Bringing $\overline{\text{OE}}$ LOW makes the output register contents available on the output data bits (DB13–DB0). A period of time t_{CD} is required after $\overline{\text{OE}}$ is brought HIGH before the next $\overline{\text{SC}}$ instruction is issued. This is to allow internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

If $\overline{\text{SC}}$ is held LOW, conversions will occur continuously. EOC will go HIGH for approximately 1.5 μs between conversions.

END-OF-CONVERT

End-of-Convert (EOC) is a three-state output which is enabled by End-of-Convert ENable $\overline{\text{EOCEN}}$.

OUTPUT ENABLE OPERATION

The data bits (DB13–DB0) are three-state outputs that are enabled by Chip Select ($\overline{\text{CS}}$) and Output Enable ($\overline{\text{OE}}$). $\overline{\text{CS}}$ should be LOW t_{OE} before $\overline{\text{OE}}$ is brought LOW. $\overline{\text{OE}}$ must be toggled to update the output register. The output is read in a single cycle as a 14-bit word.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REFOUT), output coding is twos complement binary.

POWER-UP

A conversion sequence, consisting of one $\overline{\text{SC}}$ instruction, is required after power-up to reset internal logic.

14-BIT MODE CODING FORMAT (1 LSB = 0.61 mV)

Unipolar Coding (Straight Binary)		**Bipolar Coding (Twos Complement)**	
V_{IN}	**Output Code**	**V_{IN}**	**Output Code**
0	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

CONVERSION TRUTH TABLE

	INPUTS				OUTPUTS		
Mode	**$\overline{\text{SC}}$**	**$\overline{\text{EOCEN}}$**	**$\overline{\text{CS}}$**	**$\overline{\text{OE}}$**	**EOC**	**DB13 . . . DB0**	**Status**
Start Conversion	1	X	X	X			No Conversion
	↓	X	X	X			Start Conversion
	0	X	X	X			Continuous Conversion
Conversion Status	X	0	X	X	0		Converting
	X	0	X	X	1		Not Converting
	X	1	X	X	High Z		Either
Data Access	X	X	X	1		High Z	Three-State
	X	X	1	X		High Z	Three-State
	X	X	0	0		MSB . . . LSB	Data Out

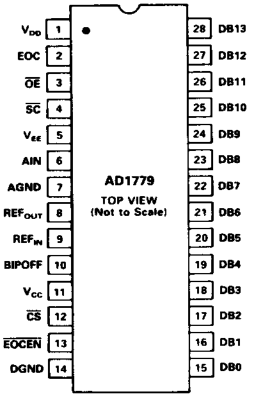
NOTES
U = Logical OR.
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay LOW for t = t_{CP}.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature		0	+70	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ESD SENSITIVITY

The AD1779 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1779 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

WARNING!
ESD SENSITIVE DEVICE

ORDERING GUIDE

Model	Package	S/N+D[1]	Temperature Range	Digital Interface Format[2]	Package Options[3]
AD1779JN	28-Pin Plastic DIP	79 dB	0 to +70°C	1 Cycle Read (14 Bits)	N-28A
AD1779KN	28-Pin Plastic DIP	81 dB	0 to +70°C	1 Cycle Read (14 Bits)	N-28A
AD1779JD	28-Pin Ceramic DIP	79 dB	0 to +70°C	1 Cycle Read (14 Bits)	D-28A
AD1779KD	28-Pin Ceramic DIP	81 dB	0 to +70°C	1 Cycle Read (14 Bits)	D-28A

NOTES

[1] Typical @ 10 kHz, −0.5 dB input.

[2] For 2 cycle read (8+6 bits) interface to 8-bit buses, see AD1679.

[3] See Section 14 for package outline information.

AD1779 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	A1	Analog Signal Input.
BIPOFF	10	A1	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos complement binary output coding.
$\overline{\text{CS}}$	12	D1	Chip Select. Active LOW.
DGND	14	P	Digital Ground.
DB13–DB0	28–15	DO	Data Bits. These pins provide all 14 bits in one 14 bit parallel output. Active HIGH.
EOC	2	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. EOC is a three-state output. See $\overline{\text{EOCEN}}$ pin for information on EOC gating.
$\overline{\text{EOCEN}}$	13	DI	End-of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{\text{OE}}$	3	DI	Output Enable. A down-going transition on $\overline{\text{OE}}$ enables data bits. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{\text{SC}}$	4	DI	Start Convert. Active LOW.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	1	P	+5 V Digital Power.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are tri-state drivers.
P = Power.

FREQUENCY DOMAIN TESTING

The AD1779 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral number of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency domain response of the converter.

NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of a full-scale input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a −0 dB input signal.

BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD1779 has been designed to optimize input bandwidth, allowing it to undersample input signal frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY

Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME

Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

For the AD1779, this specification is 14 bits from T_{min} to T_{max}, which guarantees that all 16,384 codes are present over temperature.

UNIPOLAR ZERO ERROR

In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR

In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR

The full-scale transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD1779 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 11. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the specified AD1779 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9997 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 0000 0000 0001). Then perform the gain error trim as outlined above.

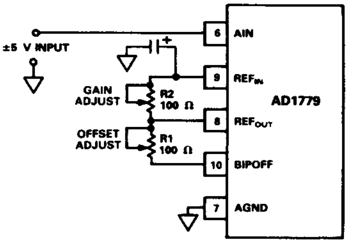


Figure 11. Bipolar Input Connections with Gain and Offset Trims

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 12. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF$_{OUT}$ is connected directly to REF$_{IN}$, the additional gain error will be approximately 1%.

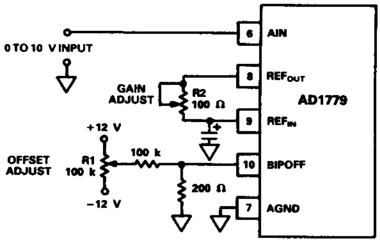


Figure 12. Unipolar Input Connections with Gain and Offset Trims

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF$_{IN}$ (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broad-band noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD1779 incorporates several features to help the user's layout. Analog pins (V$_{EE}$, AIN, AGND, REF$_{OUT}$, REF$_{IN}$, BIPOFF, V$_{CC}$) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB13–DB0 and EOC.

SUPPLY DECOUPLING

The AD1779 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor provides adequate decoupling .

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1779, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1779 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD1779 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1779. If multiple AD1779s are used or the AD1779 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.

INTERFACING THE AD1779 TO MICROPROCESSORS

The I/O capabilities of the AD1779 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD1779 interface configurations.

AD1779 TO TMS320C25

In Figure 13 the AD1779 is mapped into the TMS320C25 I/O space. AD1779 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{\text{IS}}$, Port 8 and $\overline{\text{MSC}}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD1779 read instruction.

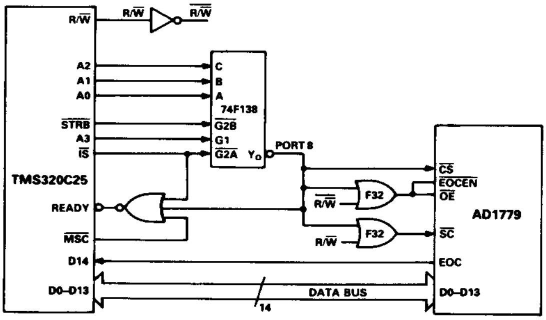


Figure 13. AD1779 to TMS320C25 Interface

AD1779 TO 80186

Figure 14 shows the AD1779 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD1779 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

The AD1779 is asynchronous which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD1779 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ sequences the high and low byte AD1779 data and resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

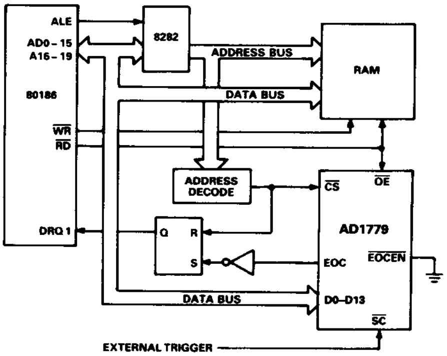


Figure 14. AD1779 to 80186 DMA Interface

AD1779 TO Z80

The AD1779 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O configuration, where the AD1779 occupies several port addresses to allow separate polling of the EOC status and reading of the data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD1779 to be used with Z80 processors having clock speeds up to 8 MHz.

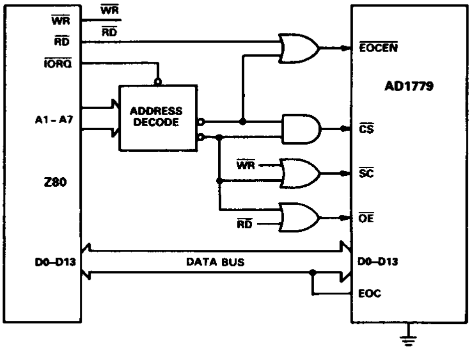


Figure 15. AD1779 to Z80 Interface

AD1779 TO ANALOG DEVICES ADSP-2100A

Figure 16 demonstrates the AD1779 interfaced to an ADSP-2100A. With a clock frequency of 1.25 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD1779 data memory interface with two wait states.

The converter runs asychronously using a sampling clock. The EOC output of the AD1779 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns).

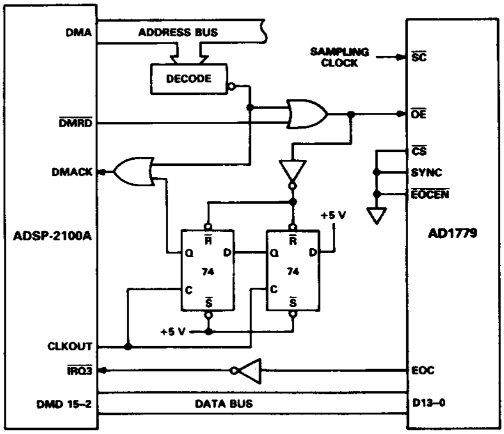


Figure 16. AD1779 to ADSP-2100A Interface