Changing from the ST14xxx to the M14xxx I²C EEPROM Memory Card Products in Your Application

STMicroelectronics I²C EEPROM Memory Card products range from the low density ST14C02C (2 Kbit) up to the high density M14256 (256 Kbit). Near the middle of this range, the ST14xxx memories, fabricated using the low density technology, are being superseded by the corresponding M14xxx memories, fabricated using ST's high density technology.

This document describes the main differences between memories fabricated in the two technologies, with the aim of helping the user to make the transition as smoothly as possible (in the application software and hardware) from the old family to the new one.

The M14xxx devices have new features, over and above those previously supported. Not least, they are able to work up to an I²C bus frequency of 400 kHz, with a power supply voltage value as low as 2.5 V. This document, therefore, is also aimed at helping the user to make optimum use of the new features of the new family.

Table 1.

Device	Memory Capacity	Interface	Fabrication Technology		
ST14C02C	2 Kbit EEPROM (256 x 8)	I²C	ST's Hi-Endurance Single Polysilicon CMOS technology	Low density	1.2 µm
ST14C04C	4 Kbit EEPROM (512 x 8)	I²C			1.2 µm
ST14E32	32 Kbit EEPROM (4K x 8)	XI²C			1.0 µm
M14C04	4 Kbit EEPROM (512 x 8)	I²C	ST's Hi-Endurance Single Polysilicon CMOS technology which guarantees an endurance well above one million erase/write cycles with a data retention of 40 years	High density	0.6 µm
M14C16	16 Kbit EEPROM (2K x 8)	I²C			0.6 µm
M14C32	32 Kbit EEPROM (4K x 8)	XI²C			0.6 µm
M14C64	64 Kbit EEPROM (8K x 8)	XI²C			0.6 µm
M14128	128 Kbit EEPROM (16K x 8)	XI²C	ST's Hi-Endurance Double Polysilicon CMOS technology which guarantees an endurance well above 100,000 erase/write cycles with a data retention of 10 years		0.6 µm
M14256	256 Kbit EEPROM (32K x 8)	XI²C			0.6 µm

Figure 1. ST14C02C I²C EEPROM

Memory Addressing

Start | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | Ack | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 | Ack | .....

Parameters	Range
V_{CC}	3V to 5.5V
Cycling	1 million
Data Retention	10 Years
Contact 2	Not Connected
Contact 8	MODE
EEPROM Page size	8 bytes
Bus Frequency	100 kHz
Write Protection	Not available

V_{CC} GND

SCL   SDA

MODE

AI02491
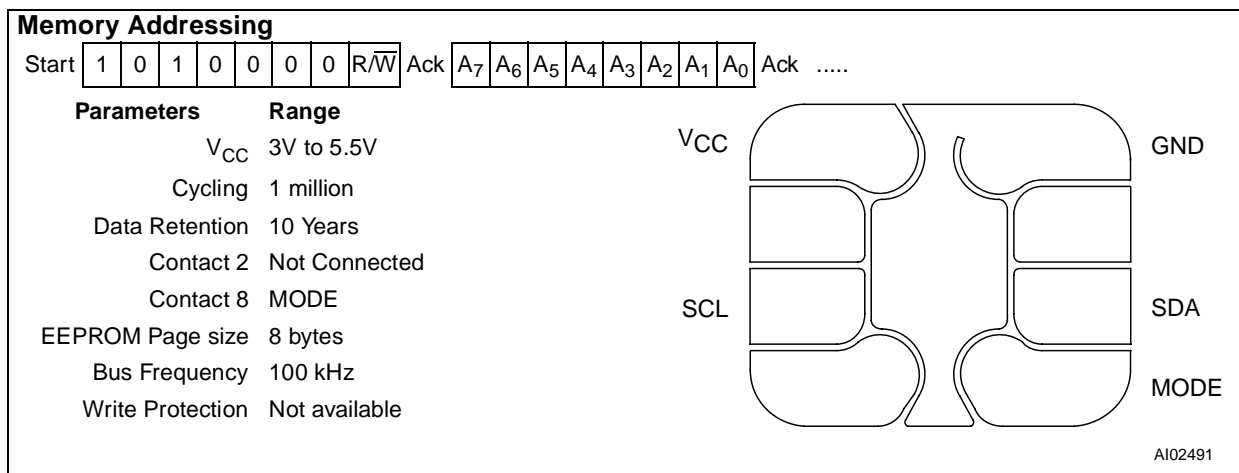
Figure 2. ST14C04C I²C EEPROM

Memory Addressing

Start | 1 | 0 | 1 | 0 | 0 | 0 | A_8 | R/$\overline{W}$ | Ack | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 | Ack | .....

Parameters	Range
V_{CC}	3V to 5.5V
Cycling	1 million
Data Retention	10 Years
Contact 2	PRE
Contact 8	MODE
EEPROM Page size	8 bytes
Bus Frequency	100 kHz
Write Protection	Top Half of the memory using the PRE pad + Address Pointer

V_{CC} GND

PRE

SCL   SDA

MODE

AI02456
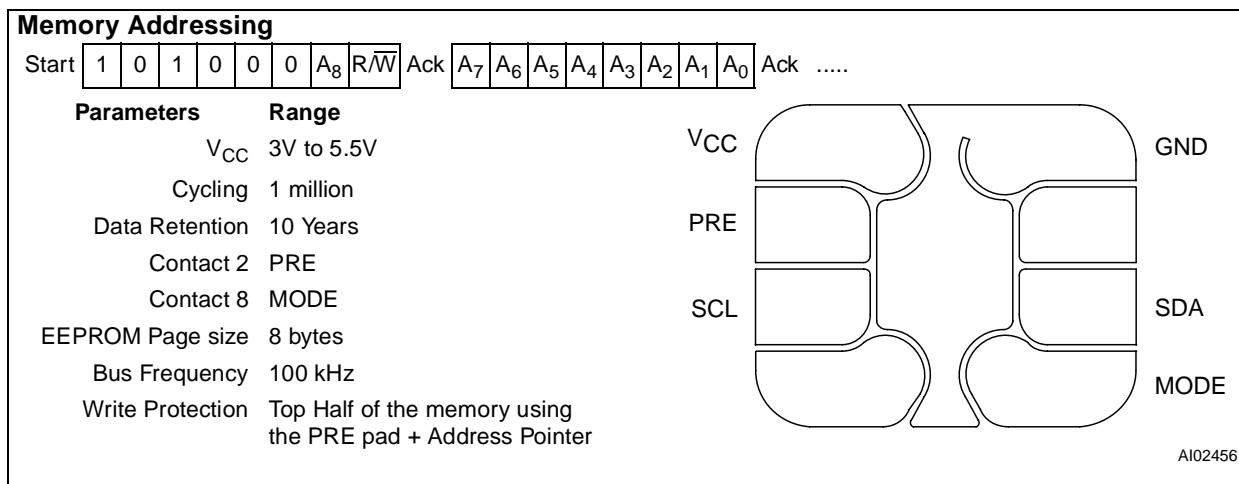
Figure 3. M14C04 I²C EEPROM

Memory Addressing

Start | 1 | 0 | 1 | 0 | 0 | 0 | A_8 | R/$\overline{W}$ | Ack | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 | Ack | .....

Parameters	Range
V_{CC}	2.5V to 5.5V
Cycling	1 million
Data Retention	40 Years
Contact 2	$\overline{WC}$
Contact 8	Not Connected
EEPROM Page size	16 bytes
Bus Frequency	400 kHz
Write Protection	Full memory using the $\overline{WC}$ pad

V_{CC} GND

$\overline{WC}$

SCL   SDA

AI02168
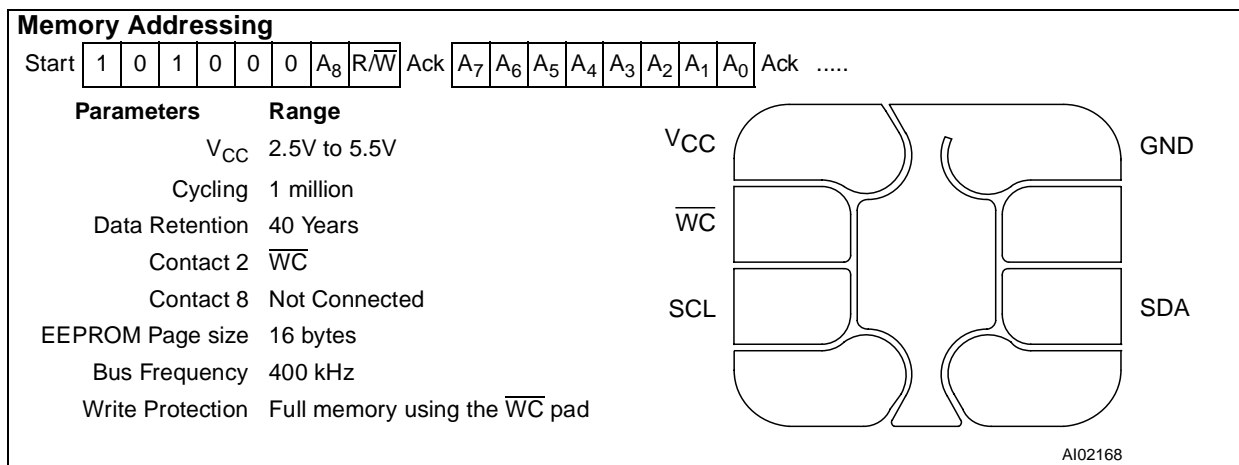
Figure 4. M14C16 I²C EEPROM

Memory Addressing

Start | 1 | 0 | 1 | 0 | A_{10} | A_9 | A_8 | $R/\overline{W}$ | Ack | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 | Ack .....

Parameters	Range
V_{CC}	2.5V to 5.5V
Cycling	1 million
Data Retention	40 Years
Contact 2	$\overline{WC}$
Contact 8	Not Connected
EEPROM Page size	16 bytes
Bus Frequency	400 kHz
Write Protection	Full memory using the $\overline{WC}$ pad

V_{CC} GND
$\overline{WC}$
SCL   SDA

AI02168
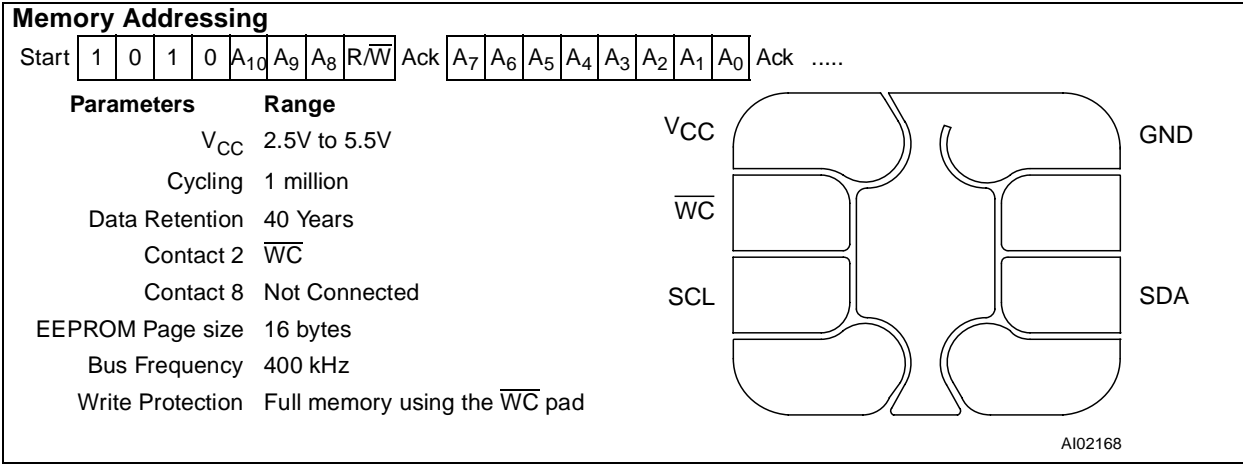
Figure 5. ST14E32/ST15E32 XI²C EEPROM

Memory Addressing

Start | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $R/\overline{W}$ | Ack | A_{15} | A_{14} | A_{13} | A_{12} | A_{11} | A_{10} | A_9 | A_8 | Ack | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 | Ack .....

Parameters	Range
V_{CC}	2.7V to 5.5V
Cycling	100,000
Data Retention	10 Years
Contact 2	$\overline{WC}$
Contact 8	Not Connected
EEPROM Page size	32 bytes
Bus Frequency	400 kHz
Write Protection	Full memory using the $\overline{WC}$ pad

V_{CC} GND
$\overline{WC}$
SCL   SDA

AI02168
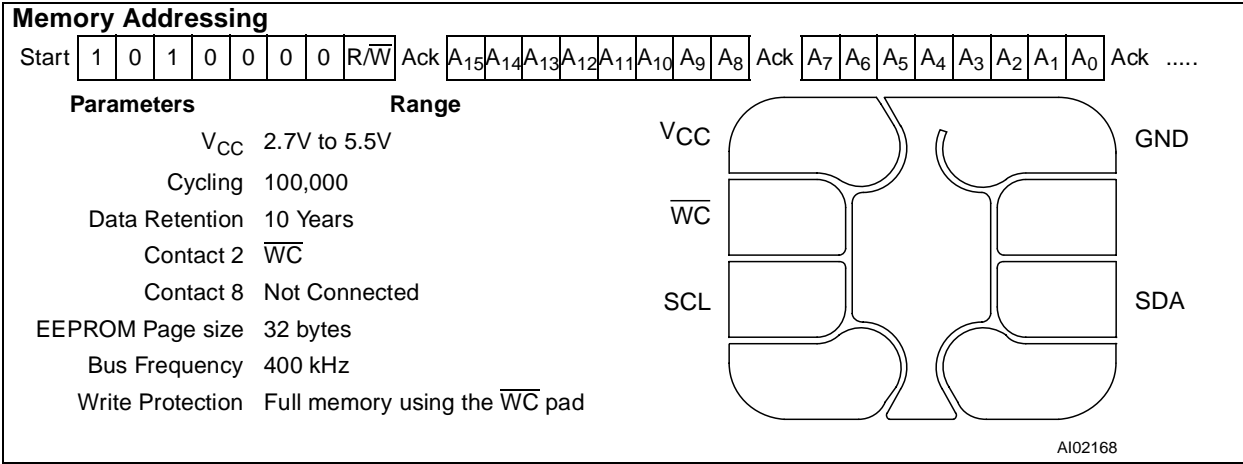
Figure 6. M14C32 XI²C EEPROM

Memory Addressing

Start | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $R/\overline{W}$ | Ack | A_{15} | A_{14} | A_{13} | A_{12} | A_{11} | A_{10} | A_9 | A_8 | Ack | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 | Ack .....

Parameters	Range
V_{CC}	2.5V to 5.5V
Cycling	1 million
Data Retention	40 Years
Contact 2	$\overline{WC}$
Contact 8	Not Connected
EEPROM Page size	32 bytes
Bus Frequency	400 kHz
Write Protection	Full memory using the $\overline{WC}$ pad

V_{CC} GND
$\overline{WC}$
SCL   SDA

AI02168
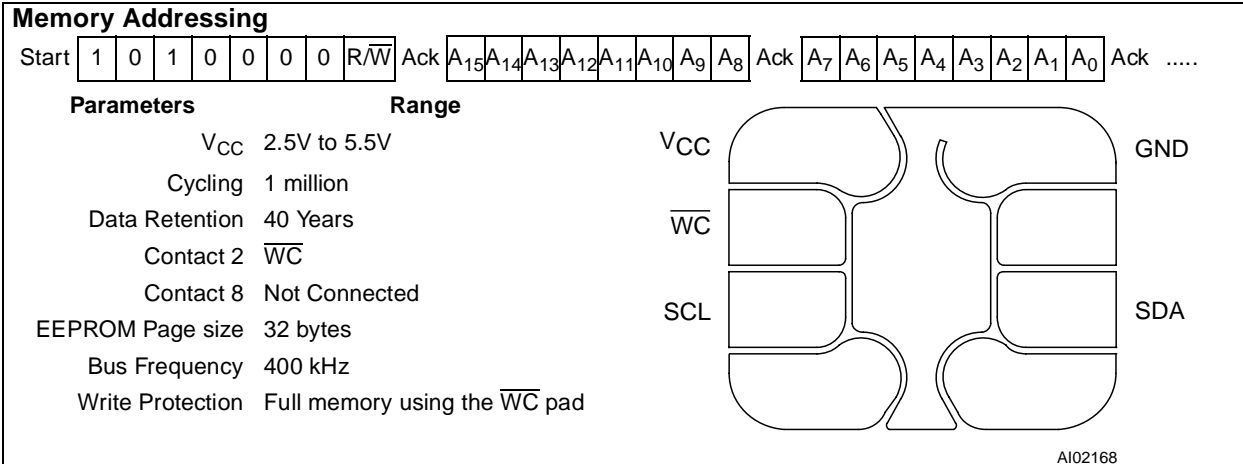
SIGNAL DESCRIPTION

Serial Clock (SCL)

Available on all the standard I²C devices, this signal is used to synchronize all data in and out of the device. A pull up resistor can be connected from Serial Clock (SCL) to V_{CC}.

Serial Data (SDA)

Available on all the standard I²C devices, this signal is bi-directional, and is used to transfer data in and out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}.

Figure 7. ST14C04C Write Protection
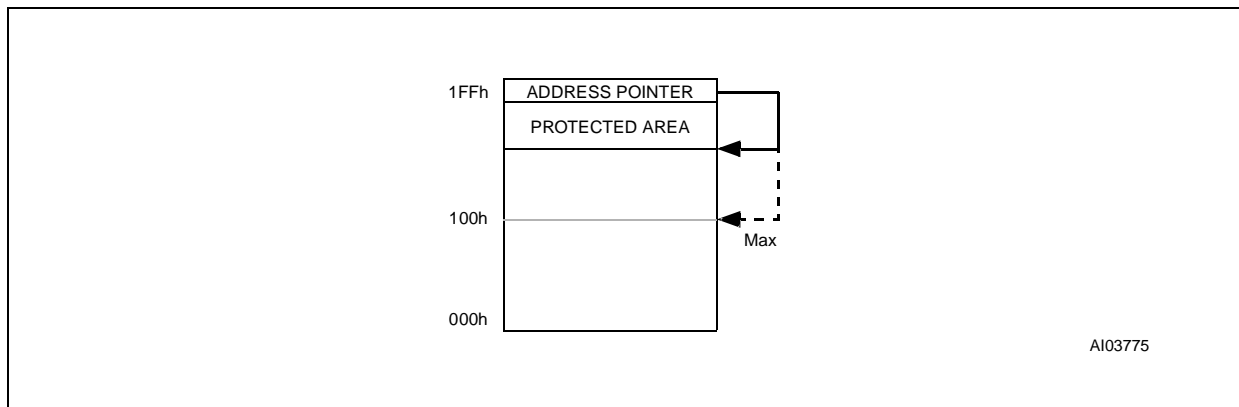
Protect Enable (PRE)

This signal is available on the ST14C04C only, and is not provided on the new M14xxx memories.

The Block Address Pointer byte (as shown in Figure 7) is used to point to a page of memory. All the memory locations in this page, and above, are write-protected when bit b2 (Protect Flag in location 1FFh) is reset to 0, and Protect Enable (PRE) is driven High (PRE=V_{IH}). To unprotect, PRE is held at V_{IL}.

This mechanism allows from 8 to 256 bytes of the top of the memory to be write-protected. The bottom of the memory cannot be write-protected. (Please see the *ST14C04C* data sheet, and the *AN1006* application note, for more details).

Mode (MODE)

The MODE input is available on the ST14C02C and ST14C04C, and is not provided in the new M14xxx memories. This input is used to select between the Multibyte Write mode (MODE=V_{IH}) and the Page Write mode (MODE=V_{IL}).

Figure 8. Wrap-round in Page Write Mode and Multibyte Write Mode
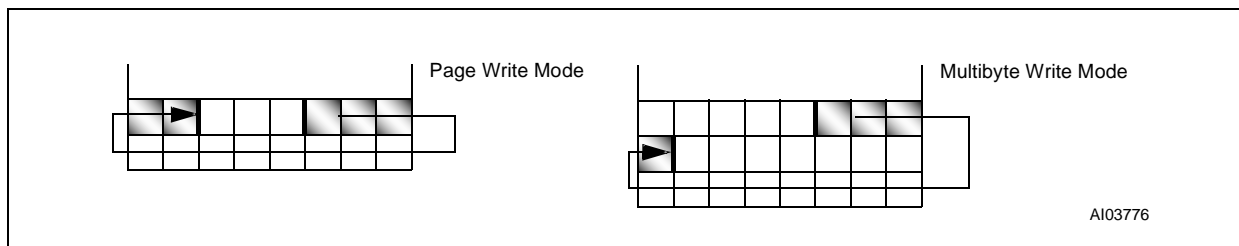
In Page Write mode, it is possible to write from 1 to 8 bytes in one programming cycle, assuming that all writes are to the same physical row of memory. An attempt to write beyond the end of the row causes the address to wrap round to the beginning of the same row, as shown in the left half of Figure 8, and not to increment to the next row, as might have been expected.

In Multibyte Write mode, it is possible to write from 1 to 4 bytes. This time, though, the address register is incremented to the start of the next row after writing to the end of the current row, as shown in the right half of Figure 8. However, the cost of doing this is to increase the programming time. If all writes are within a single row of memory, the instruction is executed in one programming cycle. If the row boundary is crossed, though, the instruction is executed in two programming cycles (one programming cycle for each row).

When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode). The MODE pin is treated as Don't Care for the Byte Write mode.

Write Control ($\overline{WC}$)

The Write Control input is available on the M14C04, M14C16, ST14E32 and M14C32. This is the standard use of the C2 module pad, according to ISO 7813, and is used for all the M14xxx I²C EEPROM products.

The Write Control input is used to enable ($\overline{WC}=V_{IL}$) or inhibit ($\overline{WC}=V_{IH}$) writing to the entire memory area. When left unconnected, the $\overline{WC}$ input is internally read as V_{IL} and write operations are allowed.

AC PARAMETERS

The same I²C specifications are used for both ST14Cxx and M14xxx EEPROM family products. Two I²C standards are available, depending on the bus frequency: one specified at 100 kHz and one at 400 kHz (see Table 2). Note that a product specified at 400 kHz is backward compatible with the 100 kHz specification. The main significance of this is in respect of the differences in the rise times for the two specifications.

Table 2. I²C timings specifications

Symbol	Alt.	Parameter	Fast I²C 400 kHz		I²C 100 kHz		Unit
			Min.	Max.	Min.	Max.	
t_{CH1CH2}	t_R	Clock Rise Time		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2}	t_R	SDA Rise Time	20	300	20	1000	ns
t_{DL1DL2}	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX}	$t_{SU:STA}$	Clock High to Input Transition	600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		4000		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		4000		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		4700		ns
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1300		4700		ns
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid		1000		3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		100	kHz
t_W	t_{WR}	Write Time		10		10	ms

MEMORY REPLACEMENT

Converting from Using the ST14C02C or ST14C04C to the M14C04
The replacement, in an application, of a ST14C02C or a ST14C04C by a M14C04 is straightforward under the following conditions:

– If the application does not currently use the Multibyte Write mode of the ST14Cxx, and has the MODE pin connected to GND.

– If the application does not currently use the Protect Enable feature of the ST14C04C, and has the PRE pin connected to GND, or left floating.

– If the application software does not currently use the Page Write roll-over feature of the ST14Cxx. (As the page size is different between the ST14Cxx and the M14C04, data will not be written at the right locations).

Converting from Using the ST14E32 to the M14C32
The ST14E32 and the M14C32 are fully compatible. They have the same pin out, the same page size and can both work at 400 kHz.

Converting from Using One Member of the M14xxx family to Another
All members of the new M14xxx I²C EEPROM family have standardized on the pin outs shown in Figure 9. Thus, upgrading from one member of the family to another is particularly straightforward. Moreover, they all off the same V_{CC} range (2.5 V to 5.5 V) and the same I^{2}C bus frequency (400 kHz).

Figure 9. M14xxx Module Pin Out
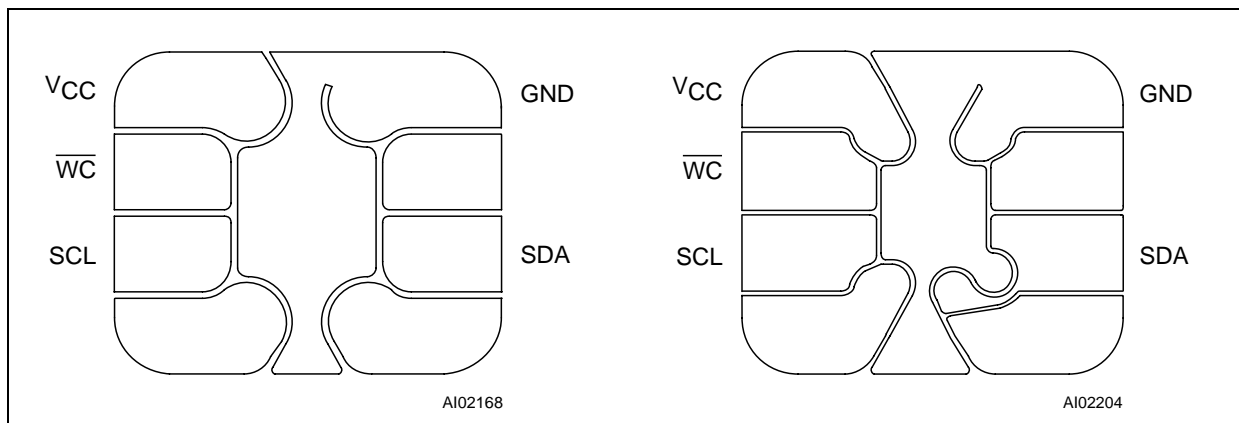
If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.memcard@st.com   (for application support)

ask.memory@st.com   (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.