SONY

CXA2032Q

2-channel REC/PB Amplifier for 8 mm VTR

Description

The CXA2032Q is a bipolar IC designed as recording/playback amplifiers for 8 mm VTRs.

Features

Recording system

- Supports EVR control for recording Y/low-band recording level
- Feedback damping circuit provided in the recording amplifier

Playback system

- Feedback damping circuit provided in the playback amplifier facilitates printed circuit board design
- RFAGC and dropout detection circuit

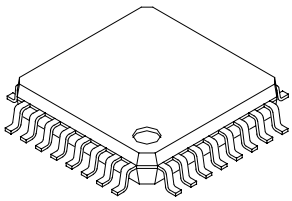
Applications

8 mm VTR

Structure

Bipolar silicon monolithic IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

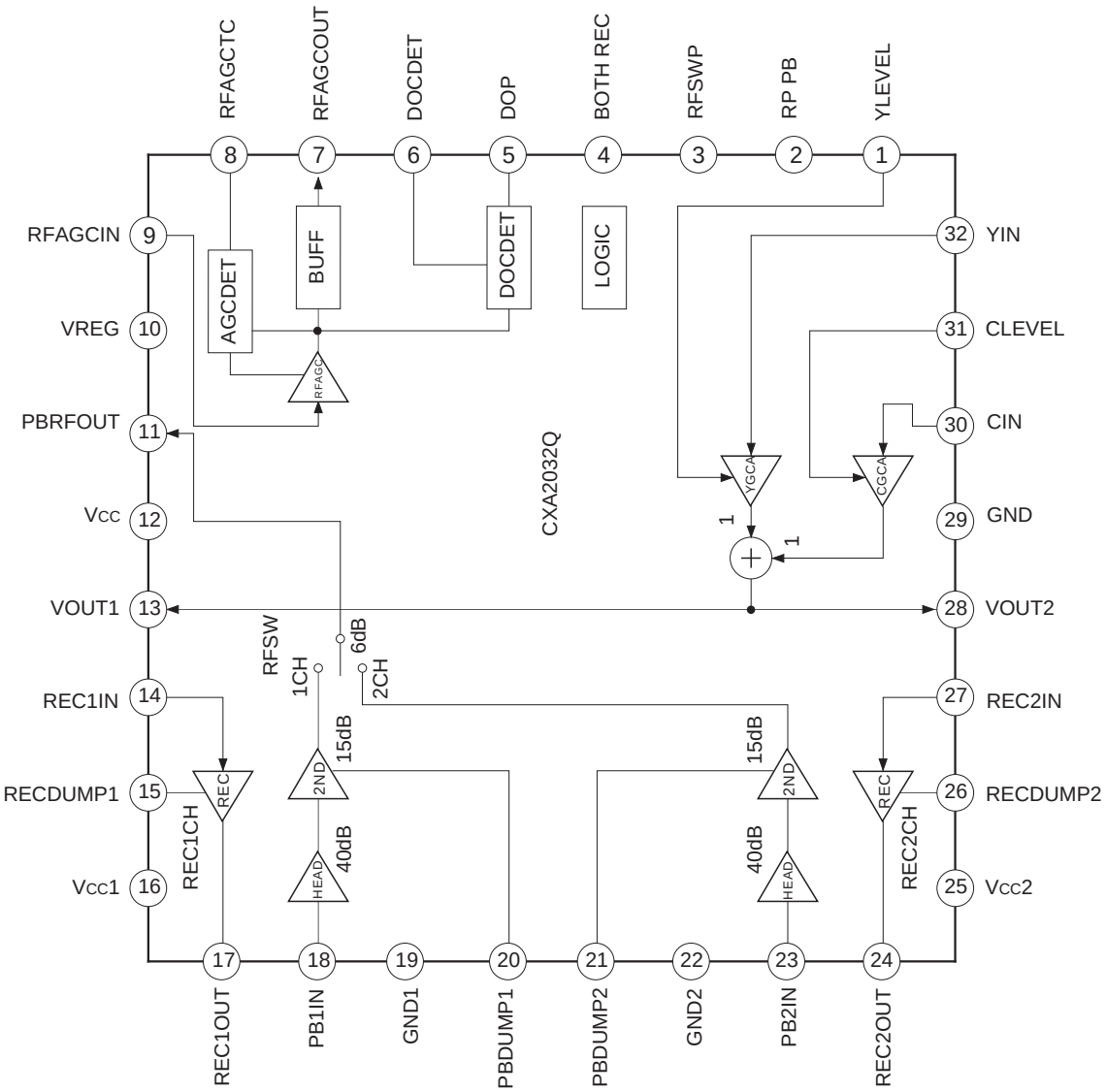
• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–10 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	450	mW

Operating Condition

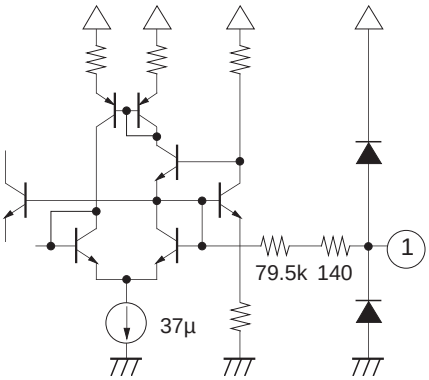
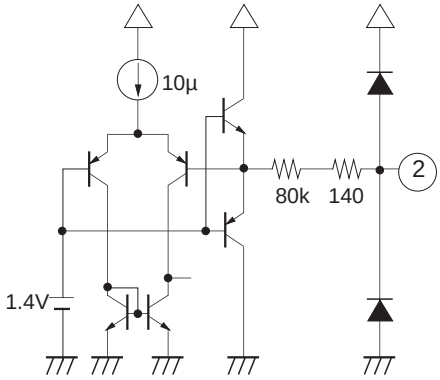
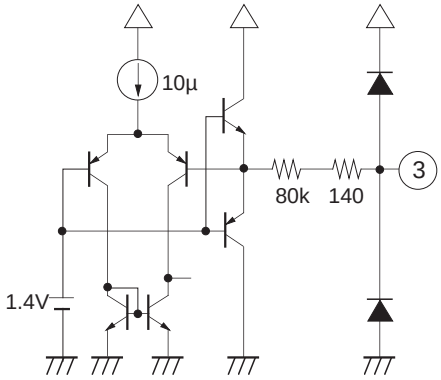
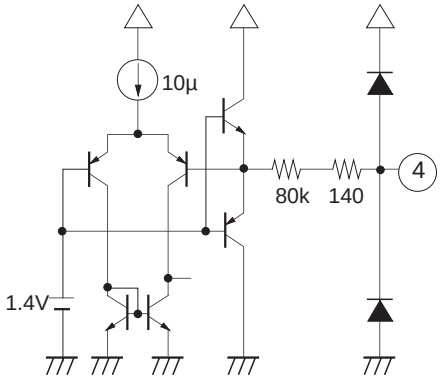
Supply voltage	V_{CC}	4.5 to 5.25	V

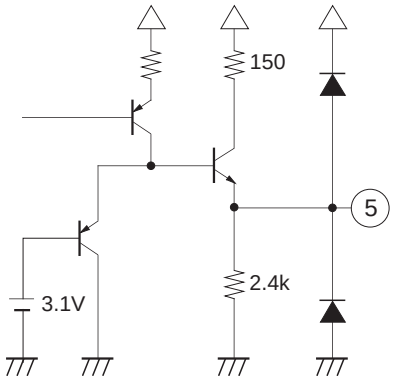
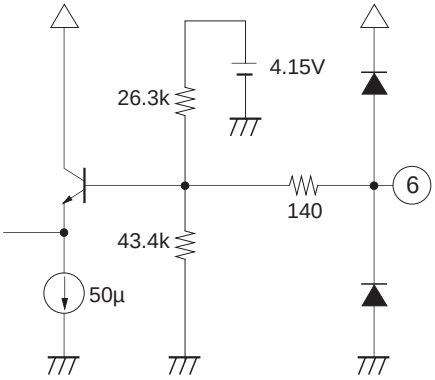
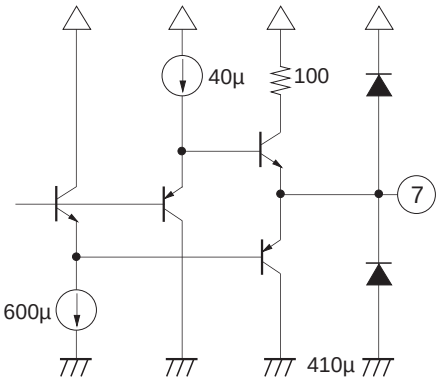
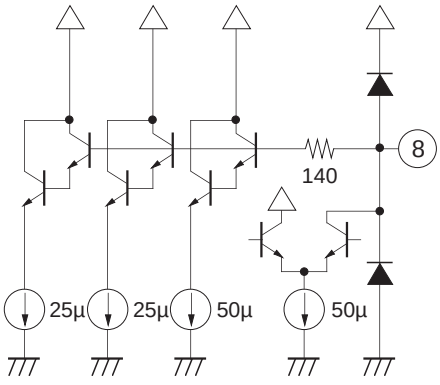
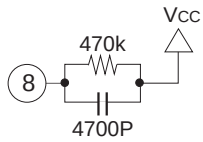
E95840-TE

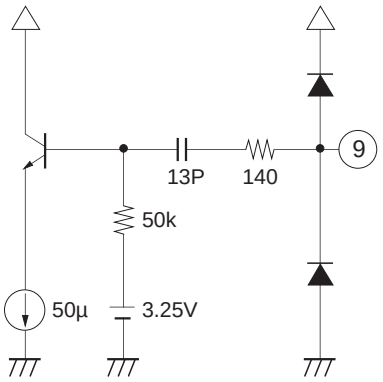
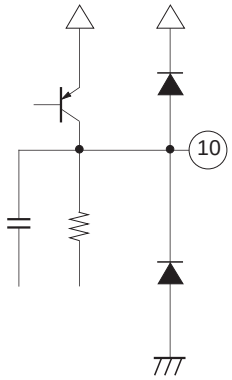
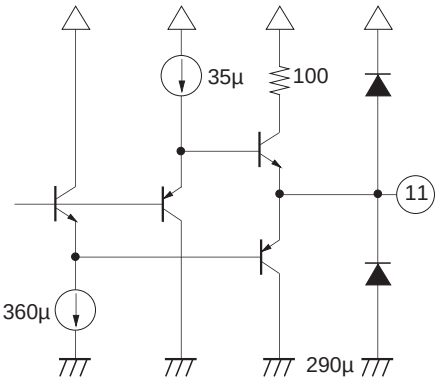
Block Diagram and Pin Configuration

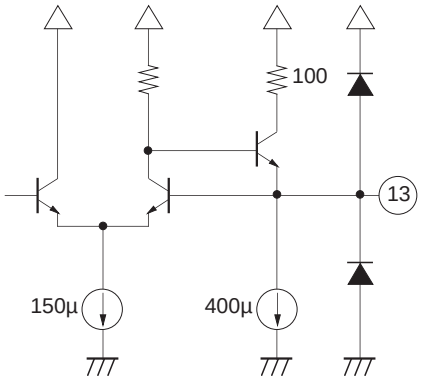
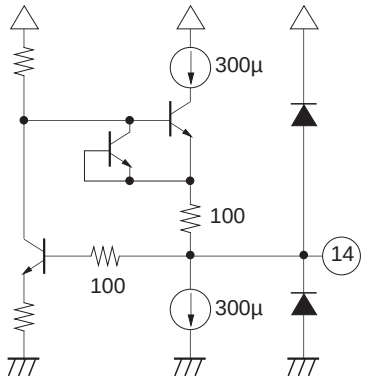
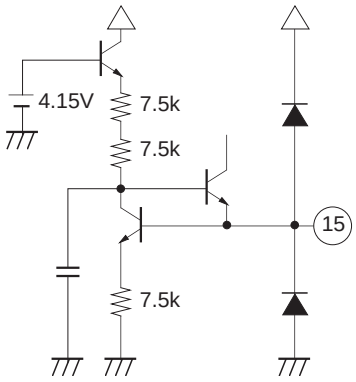


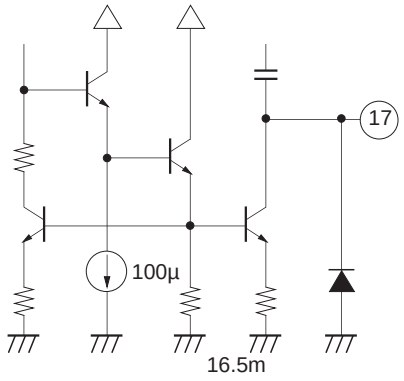
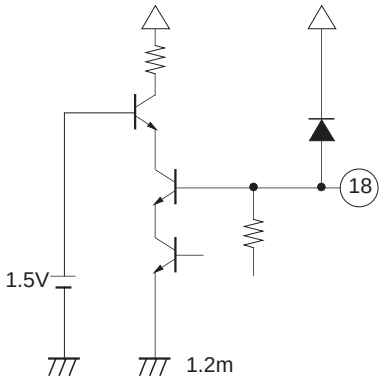
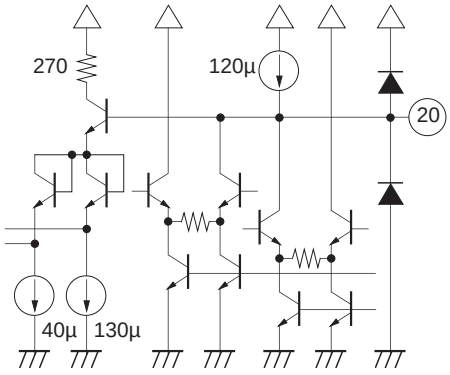
Pin Description (Vcc, Vcc1ch, Vcc2ch=4.75 V Ta=25 °C)

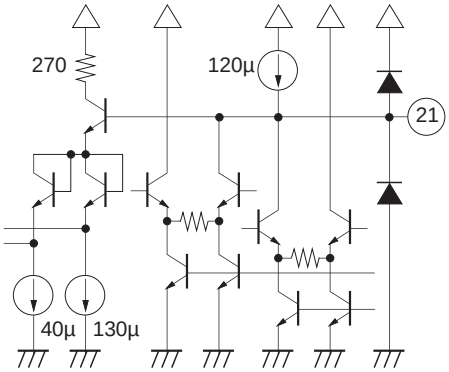
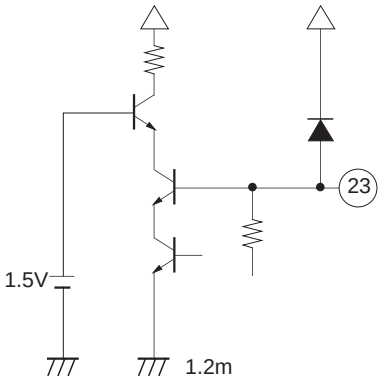
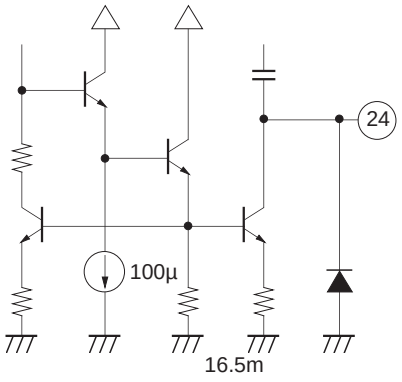
Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	Description
1	YLEVEL	0 V to 4.75 V input	—		EVR adjusting pin for Y signal level during recording. The control voltage is from 0 V to 4.75 V. Increasing the input voltage increases the Y signal level.
2	RP PB	H: 2.3 V or more L: 0.6 V or less input	—		Input pin for REC/PB mode switching signal. H: PB L: REC
3	RFSWP	H: 2.3 V or more L: 0.6 V or less input	—		Input pin for RFSWP signal.
4	BOTH REC	H: 2.3 V or more L: 0.6 V or less input	—		Alternate recording/both channel recording switching pin. H: Both channel recording L: Alternate recording

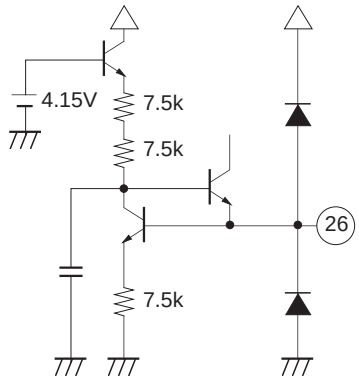
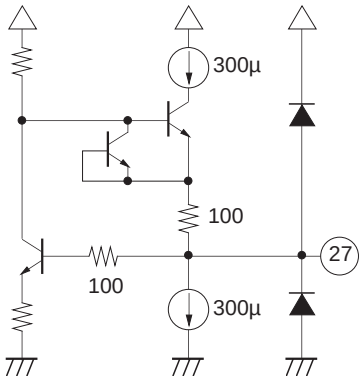
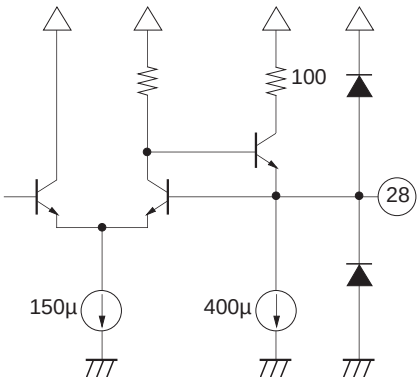
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
5	DOP	H: 3.15 V L: 0.0 V output	—		Output pin for dropout detection signal. Goes High during dropout.
6	DOCDET	2.6 V (when pin is open)	—		Pin for deciding dropout detection level. Connect decoupling capacitance between this pin and GND. For adjustment, input voltage proportional to Pin 10 (VREG) output voltage. Increasing the input voltage increases the detection level.
7	RFAGCOUT	2.8 V	400mVp-p output		Output pin for playback Y signal.
8	RFAGCTC	2.5 V to 4.75 V input (during EVR adjustment)	—		RFAGC time constant pin.  RFAGC gain can be adjusted by EVR. Increasing the input voltage increases the gain.

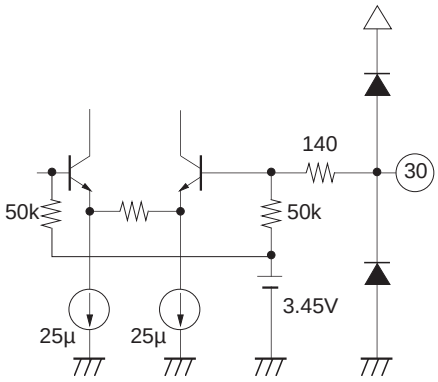
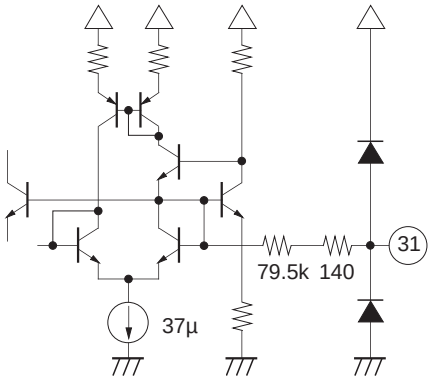
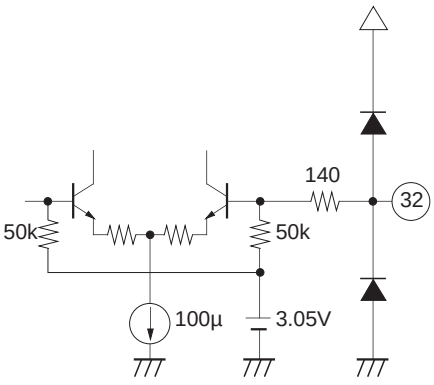
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
9	RFAGCIN	—	220mVp-p input		Input pin for playback Y signal. Playback Y signal is separated from playback video signal output to Pin 11 (PBRFOUT), then input to Pin 9 (RFAGCIN).
10	VREG	4.15 V	—		Output pin for 4.15 V regulator. Connect decoupling capacitance between this pin and GND.
11	PBRFOUT	2.0 V	220mVp-p (playback Y signal output)		Output pin for playback video signal.
12	V_{CC}	4.75 V	—		Power supply pin for main blocks excluding recording and head amplifiers.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
13	VOUT1	3.4 V	184mVp-p (recording Y signal output)		Recording video signal 1ch output pin. The signal obtained by mixing the recording Y, recording C, recording AFM and recording ATF signals is output.
14	REC1IN	0.7 V	120 µAp-p input		Recording video signal 1ch REC AMP input pin. Pin 13 (VOUT1) output is V/I converted by external resistor, then input to Pin 14 (REC1IN).
15	RECDUMP1	1.4 V	—		Damping adjusting pin for 1ch recording amplifier. Damping is adjusted by attaching damping resistor between Pin 15 and GND. Decreasing the resistance value increases the damping.
16	$V_{CC}1$	4.75 V	—		Power supply pin for 1ch recording and head amplifiers.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
17	REC1OUT	16.5 mA output	19 mAp-p output		Recording signal 1ch output pin. This pin is an open collector.
18	PB1IN	0.7 V	200 µVp-p input		Playback signal 1ch input pin.
19	GND1	0 V	—		GND pin for 1ch recording and head amplifiers.
20	PBDUMP1	2.6 V	—		Damping adjusting pin for 1ch head amplifier.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
21	PBDUMP2	2.6 V	—		Damping adjusting pin for 2ch head amplifier.
22	GND2	0 V	—		GND pin for 2ch recording and head amplifiers.
23	PB2IN	0.7 V	200 µVp-p input		Playback signal 2ch input pin.
24	REC2OUT	16.5 mA output	19 mAp-p output		Recording signal 2ch output pin. This pin is an open collector.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
25	$V_{CC}2$	4.75 V	—		Power supply pin for 2ch recording and head amplifiers.
26	RECDUMP2	1.4 V	—		Damping adjusting pin for 2ch recording amplifier. Damping is adjusted by attaching damping resistor between Pin 26 and GND. Decreasing the resistance value increases the damping.
27	REC2IN	0.7 V	120 µAp-p input		Recording video signal 2ch REC AMP input pin. Pin 28 (VOUT2) output is V/I converted by external resistor, then input to Pin 27 (REC2IN).
28	VOUT2	3.4 V	184mVp-p (recording Y signal output)		Recording video signal 2ch output pin. The signal obtained by mixing the recording Y, recording C, recording AFM and recording ATF signals is output.

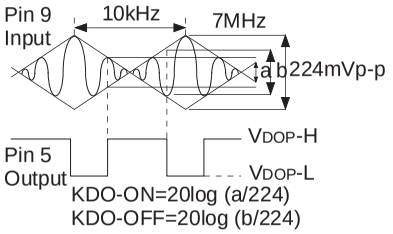
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
29	GND	0 V	—		GND pin for main blocks excluding recording and head amplifiers.
30	CIN	3.45 V	136mVp-p (recording C signal input)		Input pin for recording C, recording AFM and recording ATF signals. These three signals are mixed by external resistor, then input to Pin 30 (CIN).
31	CLEVEL	0.0 V to 4.75 V input	—		EVR adjusting pin for low-band recording signal (C, AFM, ATF) level. The control voltage is from 0 V to 4.75 V. Increasing the input voltage increases the low-band recording signal level.
32	YIN	3.05 V	500mVp-p		Input pin for recording Y signal.

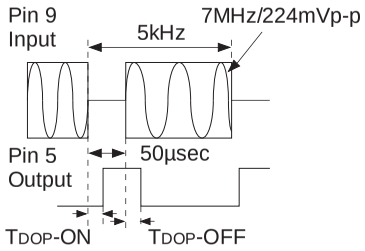
Electrical Characteristics Target Values

∗See the Control Logic Truth Table for control logic.

(V_{CC}=4.75 V, Ta=25 °C, See the Electrical Characteristics Measurement Circuit.)

No.	Item	Symbol	Measurement conditions				Measurement pin or ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input conditions			Logic						
			Pin	Level	Frequency							
1	Circuit current during recording	I rec	—	—	—	B	I_{VCC}	Current consumption inside IC during switching recording ∗1	20	29	38	mA
2	Circuit current during playback	I pb	—	—	—	F	I_{VCC}	Current consumption inside IC during playback	16	23	30	mA
3	VREG pin voltage	V REG	—	—	—	B	10	Pin voltage measurement	3.95	4.15	4.35	V
Recording system								(∗1: Including recording amplifier 1ch output bias current)				
4	Recording Y signal GCA minimum gain	G YMIN	32	1120 mVp-p	300 kHz	B	13	Pin 1 (YLEVEL) = 0 V	—	–17.2	–15.7	dB
5	Recording Y signal GCA maximum gain	G YMAX	32	225 mVp-p	300 kHz	B	13	Pin 1 (YLEVEL) = 4.75 V	–1.7	0.9	—	dB
6	Recording Y signal GCA frequency response (center)	V FY	32	500 mVp-p	10 MHz	B	13	10 MHz level/300 kHz level Pin 1 (YLEVEL) = Vylev (center gain)	–1.3	–0.3	0.7	dB
7	Recording Y signal GCA secondary distortion (center gain)	DY	32	500 mVp-p	7 MHz	B	13	Pin 1 (YLEVEL) = Vylev (center gain)	—	–50	—	dB
8	Recording C signal GCA minimum gain	G CMIN	30	305 mVp-p	300 kHz	B	13	Pin 31 (CLEVEL) = 0 V	—	–17.8	–16.4	dB
9	Recording C signal GCA maximum gain	G CMAX	30	60 mVp-p	300 kHz	B	13	Pin 31 (CLEVEL) = 4.75 V	–2.4	0.6	—	dB
10	Recording C signal GCA frequency response (center)	VFC	30	136 mVp-p	2 MHz	B	13	2 MHz level/300 kHz level Pin 31 (CLEVEL) = Cylev (center gain)	–0.5	0	0.5	dB
11	Recording C signal GCA secondary distortion (maximum gain)	DC	30	90 mVp-p	700 kHz	B	13	Pin 31 (CLEVEL) = 4.75 V	—	–56	—	dB

No.	Item	Symbol	Measurement conditions				Measurement pin or ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input conditions			Logic						
			Pin	Level	Frequency							
12	Recording AFM signal secondary distortion (maximum gain)	D AFM	30	90 mVp-p	1.7 MHz	B	13	Pin 31 (CLEVEL) = 4.75 V	—	–55	—	dB
13	Recording amplifier output bias current	IB1, 2	—	—	—	B	IB1, 2	DC current measurement	12.7	16.5	20.2	mA
14	Recording amplifier output current	I R1 I R2	14 27	184 mVp-p 184 mVp-p	1 MHz 1 MHz	B B	17 24	Output level (mVp-p)/51 Ω Output level (mVp-p)/51 Ω	16.6	19	21.4	mA p-p
15	Recording amplifier frequency response	ΔR1 ΔR2	14 27	184 mVp-p 184 mVp-p	10 MHz 10 MHz	B B	17 24	10 MHz level/1 MHz level 10 MHz level/1 MHz level	—	0	—	dB
Playback system												
16	Playback amplifier, RFSW gain	GV1 GV2	18 23	200 µVp-p 200 µVp-p	300 kHz 300 kHz	F E	11 11		57.9	61.4	64.9	dB
17	RFAGC standard output	V AGC1	9	224 mVp-p	7 MHz	F	7	Measure output level, applying time constant to Pin 8 (RFAGCTC).	330	400	470	mV p-p
18	RFAGC cover range High	V AGC2	9	56 mVp-p	7 MHz	F	7		310	375	—	
19	RFAGC cover range Low	V AGC3	9	896 mVp-p	7 MHz	F	7		—	425	495	
20	Dropout detection ON level	K DO-ON	See Measurement method (figure to right).			F	5	Apply time constant to Pin 8 (RFAGCTC).	–13.5	–10.5	–7.5	dB
21	Dropout detection OFF level	K DO-OFF				F	5		–8.5	–5.5	–2.5	
22	Dropout pulse Low level	V DOP-L				F	5		0	0.01	0.2	V
23	Dropout pulse High level	V DOP-H				F	5		2.9	3.15	3.4	

No.	Item	Symbol	Measurement conditions				Measurement pin or ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input conditions			Logic						
			Pin	Level	Frequency							
24	Dropout ON detection time	T DOP -ON	See Measurement method (figure to right).			F	5	Apply time constant to Pin 8 (RFAGCTC). 	—	1	—	µs
25	Dropout OFF detection time	T DOP -OFF				F	5		—	2	—	

Control Logic Truth Table

Input conditions and operation / Name of control logic conditions	Control logic input conditions			Operation of each section under respective input conditions									Operation	Mode
				Recording system				Playback system						
	RPPB	RFSWP	BOTHREC	VOUT1	VOUT2	REC1OUT	REC2OUT	PB1chAMP	PB2chAMP	PBRFOUT	RFAGCOUT	DOCDET		
	2	3	4	13	28	17	24			11	7			
A	L	L	L	V	V	Δ	V	×	×	×	×	×	VIDEO EACH REC ↓	REC
B	L	H	L	V	V	V	Δ	×	×	×	×	×	↓	
C	L	L	H	V	V	V	V	×	×	×	×	×	VIDEO BOTH REC ↓	
D	L	H	H	V	V	V	V	×	×	×	×	×	↓	
E	H	L	—	×	×	×	×	O	O	CH2	O	O	PB ↓	PB
F	H	H	—	×	×	×	×	O	O	CH1	O	O	↓	

(Description of input conditions)

H · · · Control logic input voltage of 2.3 V or more

L · · · Control logic input voltage of 0.6 V or less

— · · · Don't care.

(Description of operation mode)

O · · · Operating

× · · · Not operating

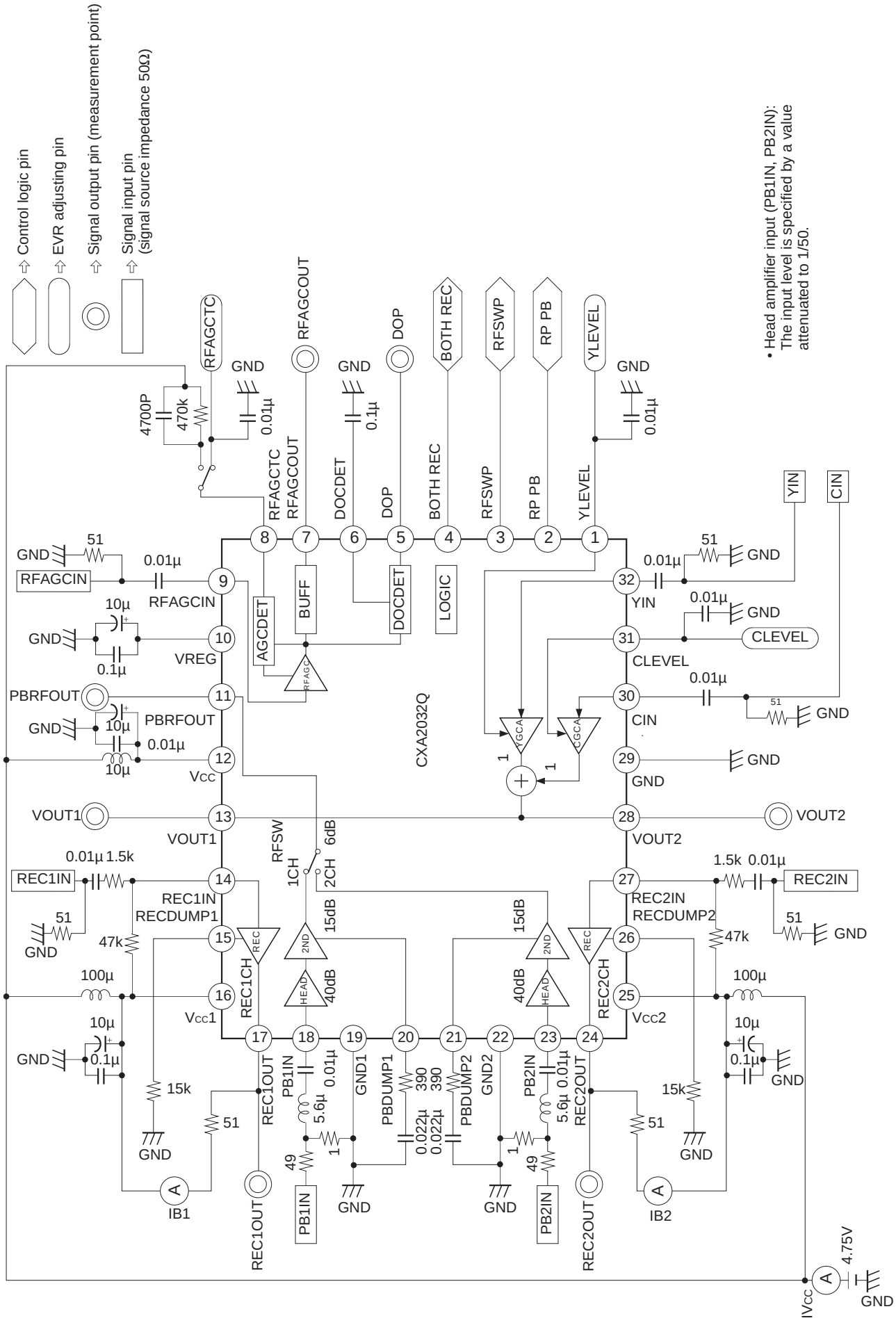
V · · · Video signal is output.

Δ · · · Operating but bias current is OFF.

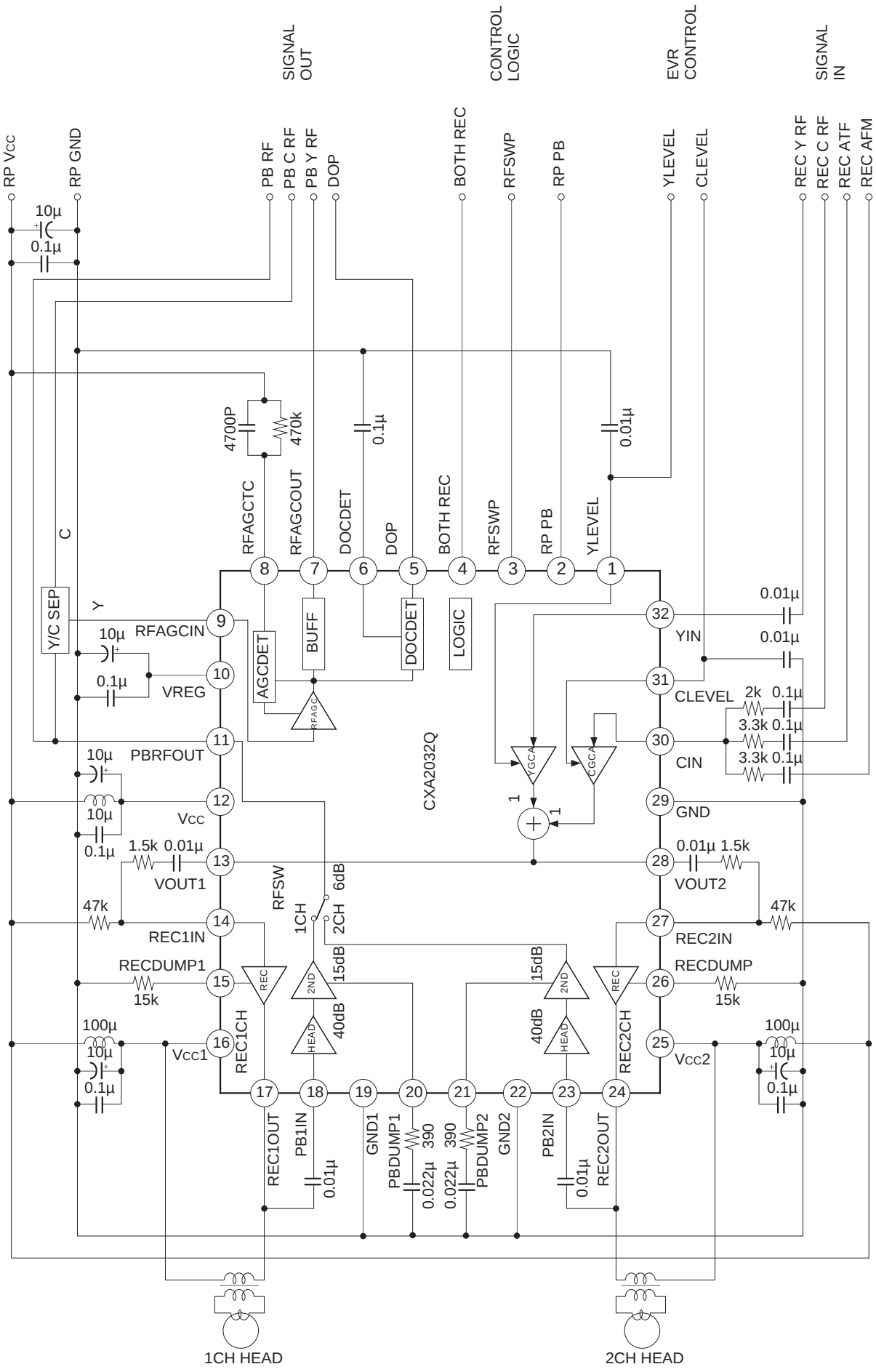
CH1 · · · CH1 signal is output.

CH2 · · · CH2 signal is output.

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

<Recording level adjustment>
Y, chroma, AFM and ATF signals are adjusted at specified levels so that they are mixed internally to achieve an appropriate value at the head, then output to Pins 13 (VOUT1) and 28 (VOUT2). The Y level is EVR adjusted at Pin 1 (YLEVEL) and the low-band level (chroma, AFM, ATF) at Pin 31 (CLEVEL).

<Recording amplifier>
The signal, which underwent recording level adjustment, is V/I converted by external resistor, then input to Pins 14 (REC1IN) and 27 (REC2IN). The current of the input signal is amplified by the recording amplifier, and this signal is then output from Pins 17 (REC1OUT) and 24 (REC2OUT) to drive the head. A feedback damping circuit is incorporated into the recording amplifier to inhibit head resonance, and the peaking amount can be adjusted by external resistors attached to Pins 15 (RECDUMP1) and 26 (RECDUMP2).
During recording, the output capacitance is about 12 pF including that of the playback amplifier.

<Playback amplifier>
The playback signal from the head is amplified with low noise and high gain. A feedback damping circuit is incorporated to inhibit head resonance, and the peaking amount can be adjusted by external resistors attached to Pins 20 (PBDUMP1) and 21 (PBDUMP2).
During playback, the output capacitance is approximately 20 pF including that of the recording amplifier.

<RFSW>
This section switches the playback signals of channels 1 and 2 at the correct timing and outputs the playback video signal to Pin 11 (PBRFOUT). Switching is performed at Pin 3 (RFSWP).

<RFAGC>
This section inputs the playback Y signal separated from playback video signal using an external circuit and outputs it at a constant level of 400 mVp-p.

<Dropout detection>
A dropout is detected in the playback Y signal, and a dropout pulse is output. The detection level is optimized using 224 mVp-p input as a reference.

<Control logic>
In order to save power consumption, this IC exercises power-saving control of circuit blocks which are not in need for operation depending on the mode. The IC also incorporates a logic circuit for controlling the built-in switches which change inputs and outputs.
The combinations of input and output required for basic operation are shown in the Control Logic Truth Table.

<Reference voltage in the IC>
VREG 4.15 V is generated as the reference voltage used in the IC.

Notes on Operation

1. This IC is characterized by high-voltage gain (approximately 61 dB in the playback system). Be careful of the following when using the IC.

   1) Use a reinforced power supply and ground lines. Decouple the power supply pin with a coil and a capacitor. Connect each decoupling capacitor as close to the pin as possible.

   2) Use of a regulator power supply is recommended.

   3) Connecting a capacitive load to the output may cause oscillation.

   4) Take particular care not to make capacitive coupling between the head amplifier input and the playback output. Also be careful not to make capacitive coupling between the recording input and the recording amplifier output.

   5) Use of decoupling capacitors is recommended between the following DC voltage input pins and GND. When the control voltage source is at high impedance, aggravation of cross talk or oscillation may occur.

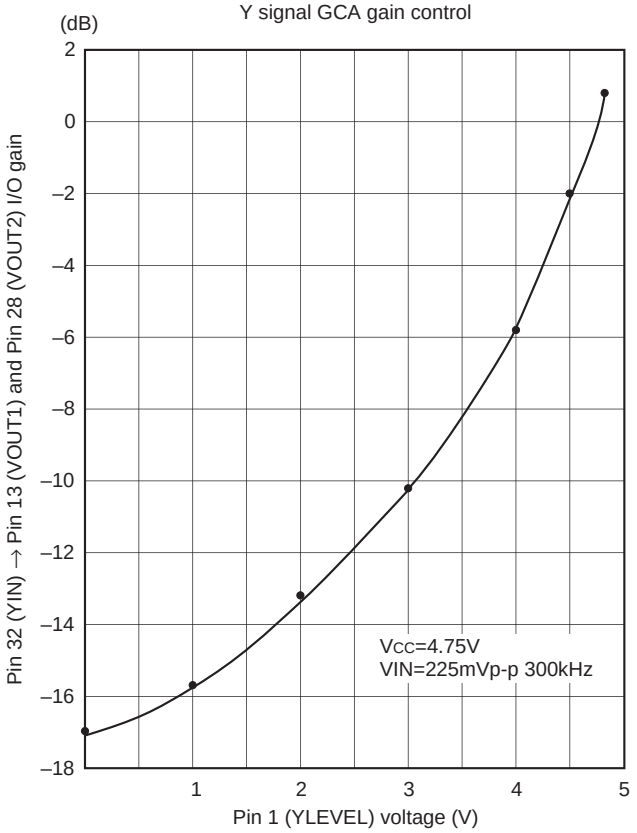
      Pin 1 (YLEVEL), Pin 31 (CLEVEL)

   6) When a decoupling capacitor is necessary for other pins (not power supply pin), it is recommended to connect each decoupling capacitor as close to the pin as possible.

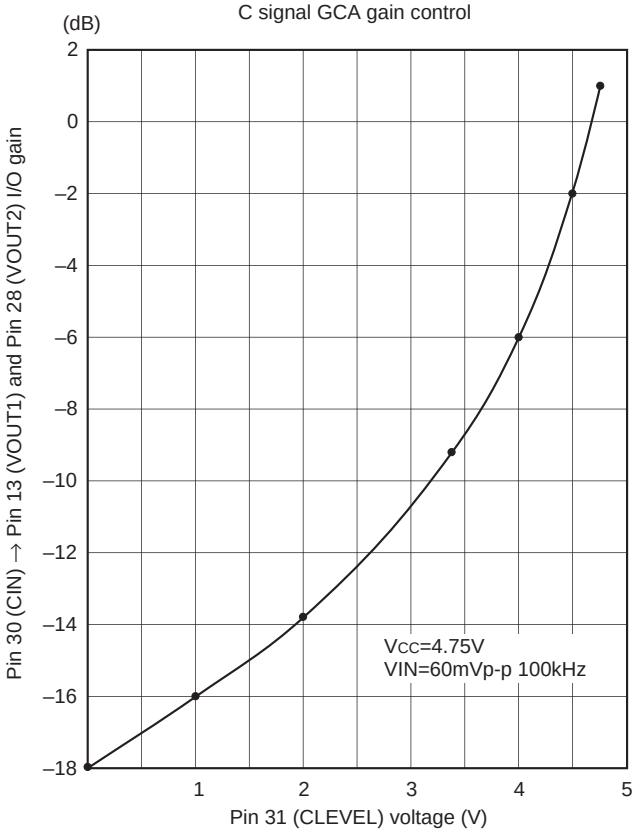
   7) The voltage input to EVR adjusting pins should be proportional to the supply voltage V_{CC}. Control the input voltage in the range from 0 to 4.75 V when V_{CC} = 4.75 V.
      For EVR adjustment at Pin 8 (RFAGCTC), control the input voltage in the range of 2.5 V to 4.75 V.

Characteristics Graphs

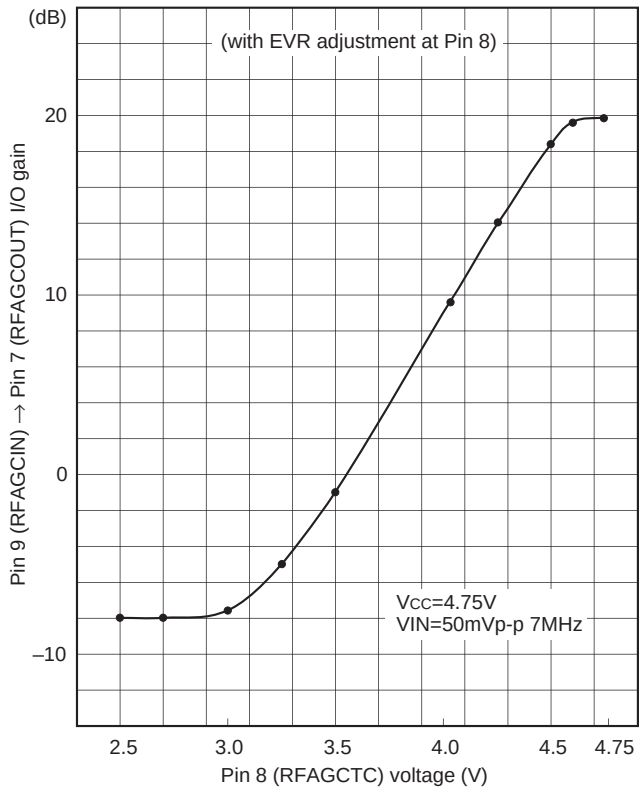
Y signal GCA gain control



C signal GCA gain control

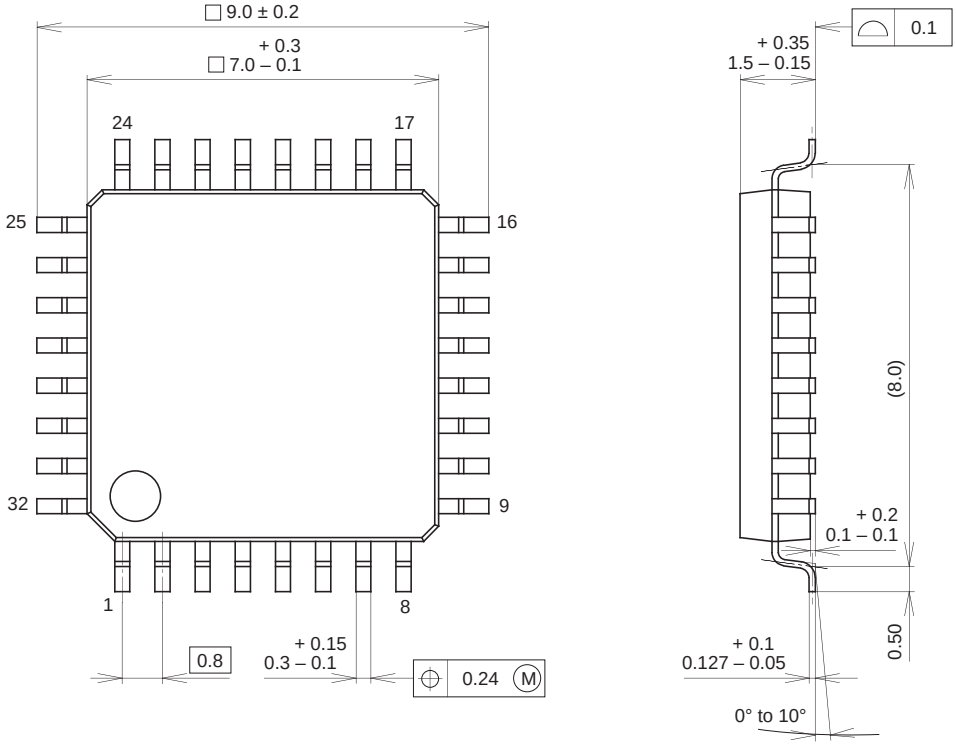


RFAGC gain control



Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g