

# 2SK3148

Silicon N Channel MOS FET  
High Speed Power Switching

# HITACHI

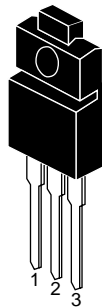
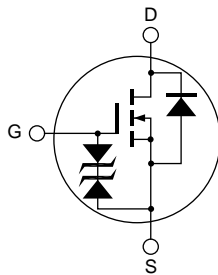
ADE-208-748A (Z)  
2nd. Edition  
February 1999

## Features

- Low on-resistance  
 $R_{DS} = 45 \text{ m}\Omega$  typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

## Outline

TO-220FM



1. Gate
2. Drain
3. Source

## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	100	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	20	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	60	A
Body-drain diode reverse drain current	$I_{DR}$	20	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	20	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	40	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	30	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

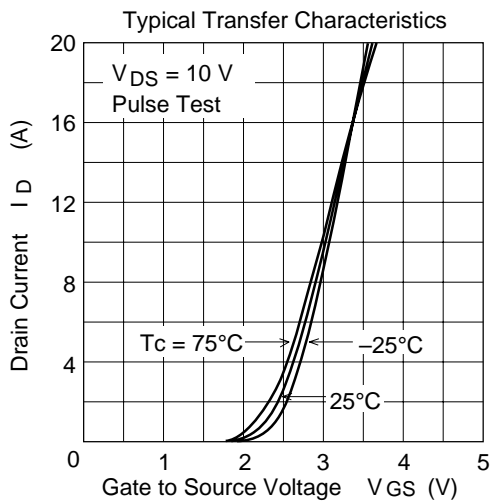
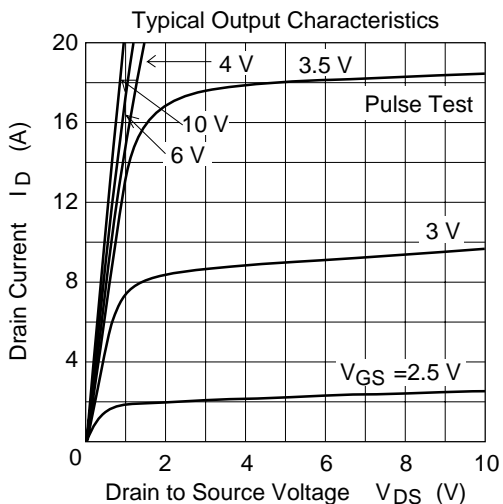
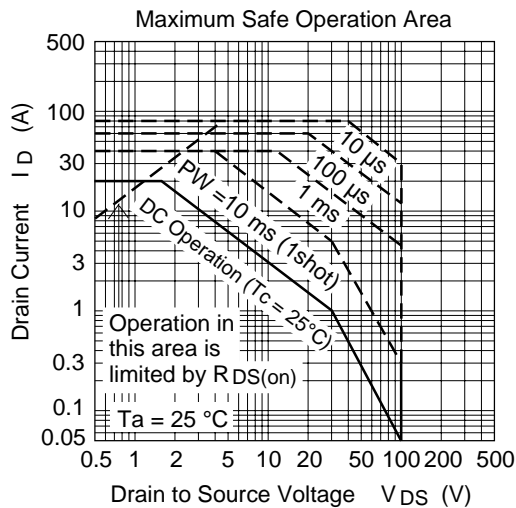
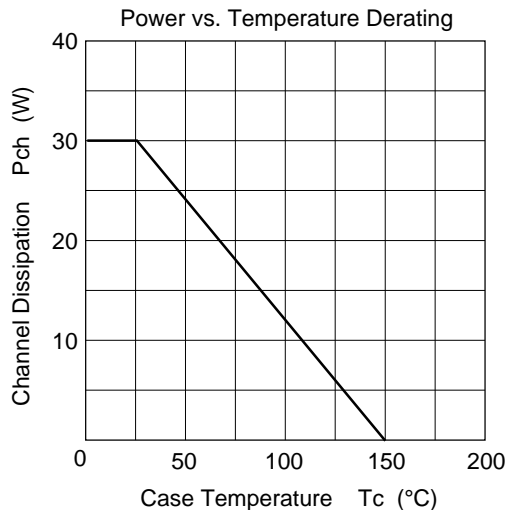
Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_c = 25^\circ C$   
 3. Value at  $T_{ch} = 25^\circ C$ ,  $R_g \geq 50 \Omega$

## Electrical Characteristics (Ta = 25°C)

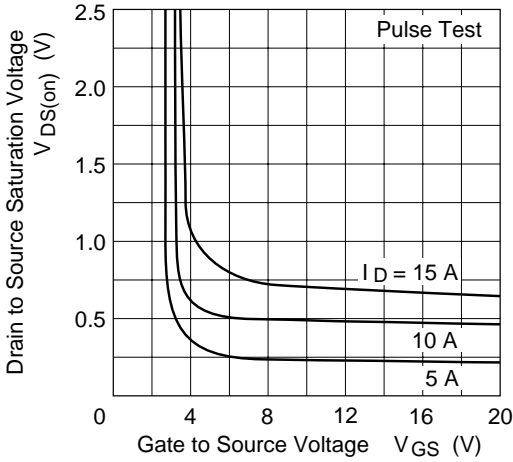
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \mu A$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu A$	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	45	60	m $\Omega$	$I_D = 10 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	65	85	m $\Omega$	$I_D = 10 \text{ A}$ , $V_{GS} = 4 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	9	15	—	S	$I_D = 10 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	840	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	350	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	180	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 10 \text{ A}$ , $V_{GS} = 10 \text{ V}$
Rise time	$t_r$	—	120	—	ns	$R_L = 3 \Omega$
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	$t_f$	—	150	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.9	—	V	$I_F = 20 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	90	—	ns	$I_F = 20 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu s$

Note: 4. Pulse test

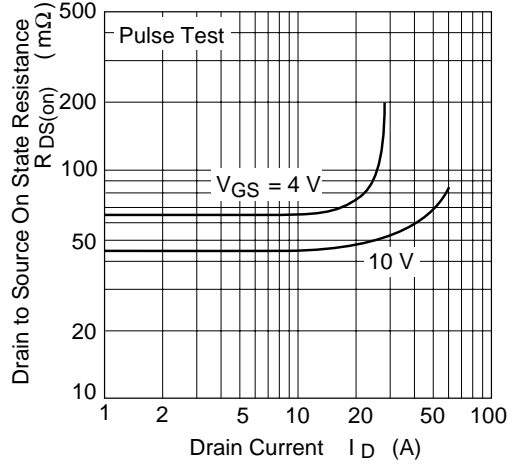
### Main Characteristics



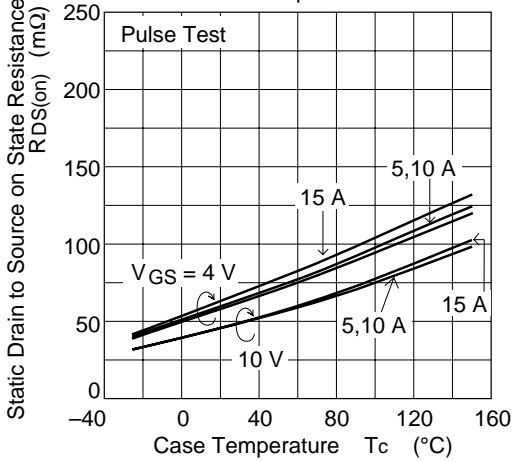
Drain to Source Saturation Voltage vs. Gate to Source Voltage



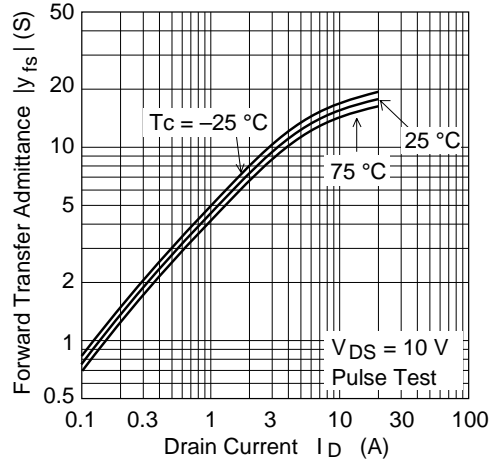
Static Drain to Source on State Resistance vs. Drain Current



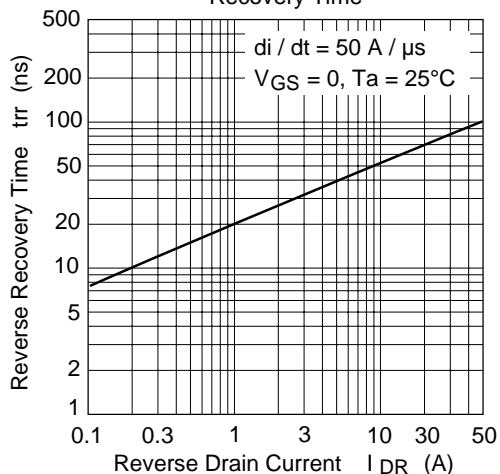
Static Drain to Source on State Resistance vs. Temperature



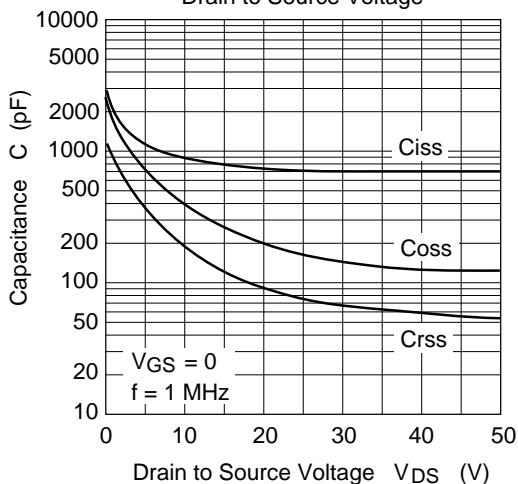
Forward Transfer Admittance vs. Drain Current



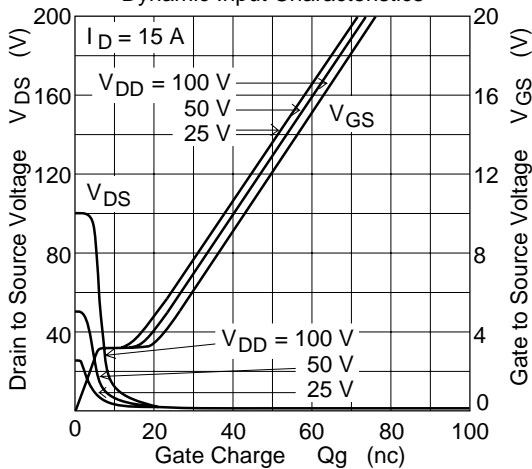
Body-Drain Diode Reverse Recovery Time



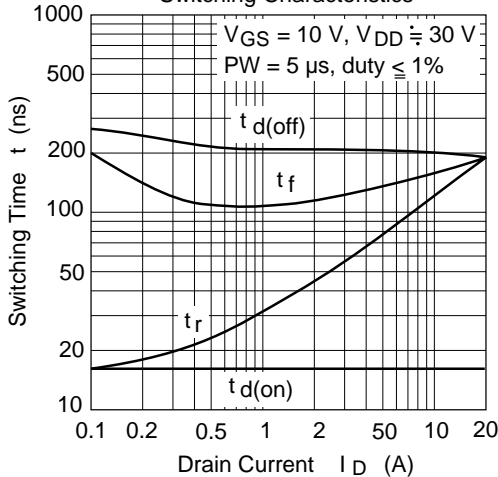
Typical Capacitance vs. Drain to Source Voltage

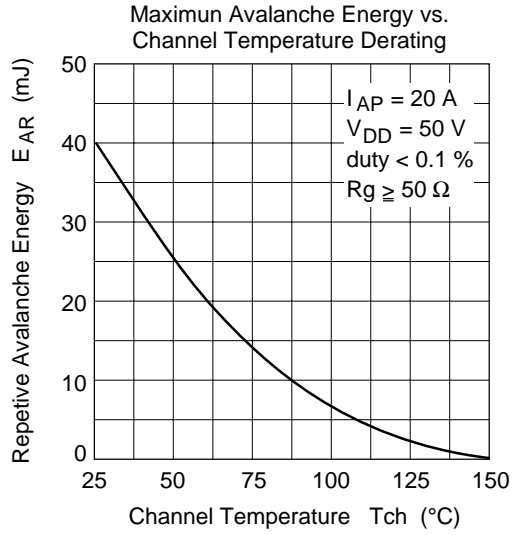
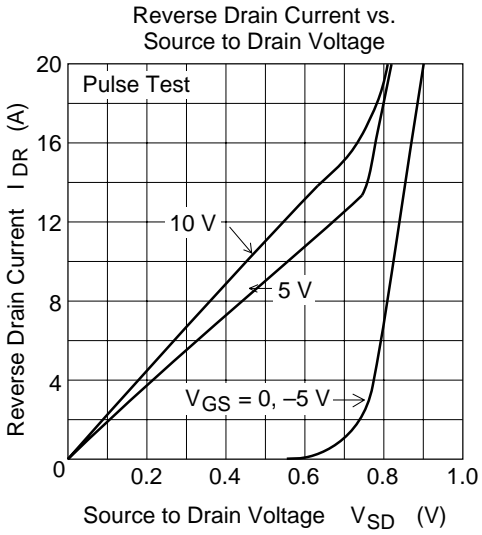


Dynamic Input Characteristics

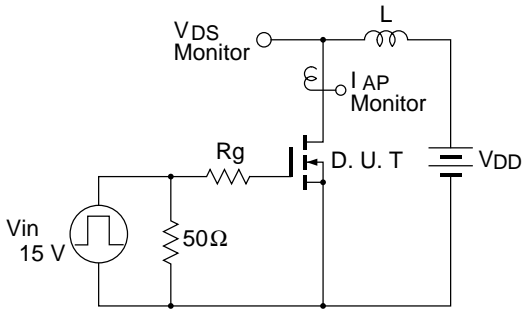


Switching Characteristics



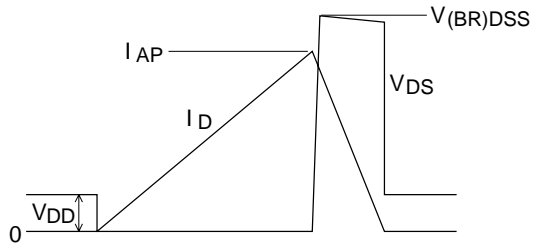


Avalanche Test Circuit

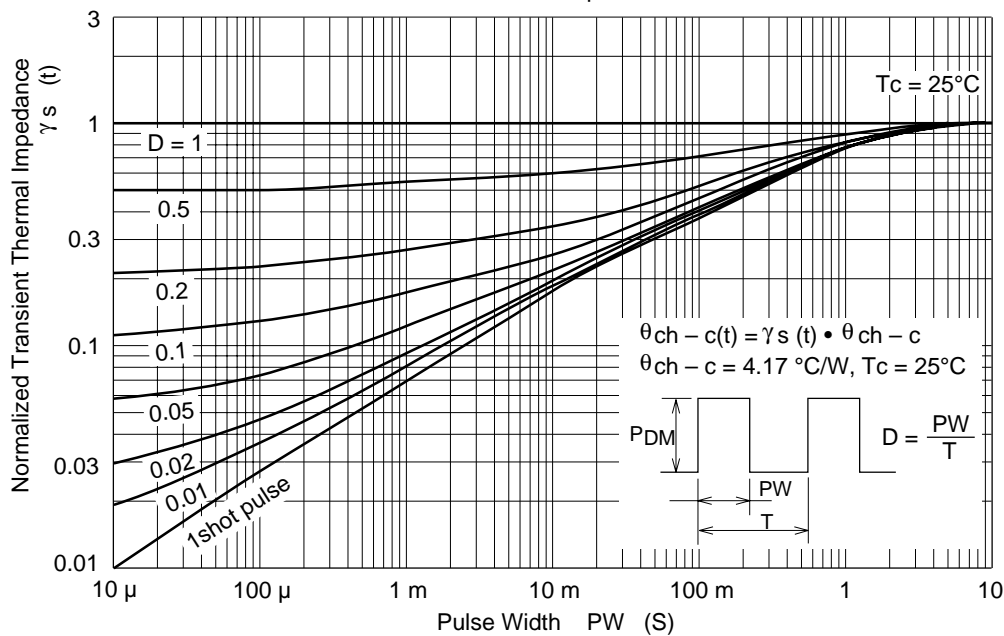


Avalanche Waveform

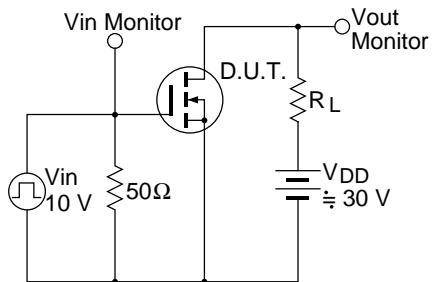
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



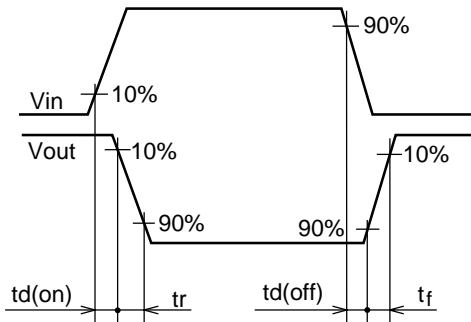
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

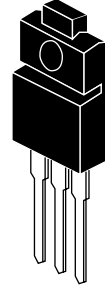
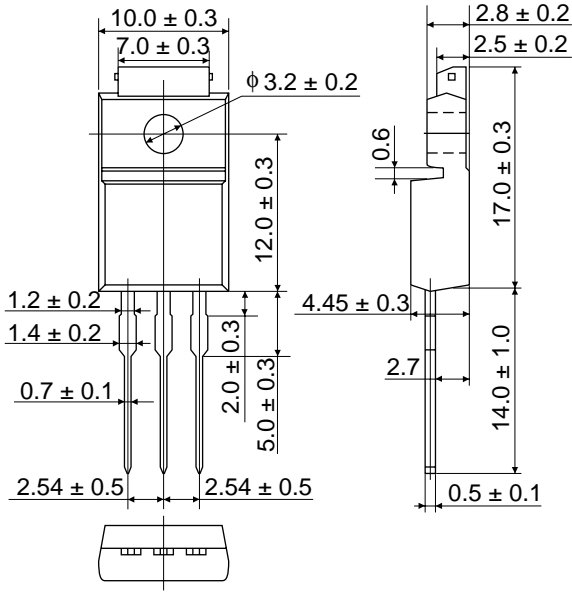


Waveform



Package Dimensions

Unit: mm



Hitachi Code	TO-220FM
EIAJ	SC-67
JEDEC	—



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