AN-6741
Flyback Power Supply Control with the SG6741

Summary

This application note describes a design strategy for a high-efficiency, compact flyback converter. Design considerations, mathematical equations, and guidelines for a printed circuit board layout are presented.

Features

- High-voltage startup
- Low operating current: 4mA
- Linearly decreasing PWM frequency to 22KHz
- Frequency hopping to reduce EMI emission
- Peak-current-mode control
- Cycle-by-cycle current limiting
- Leading-edge blanking
- Synchronized slope compensation
- Gate output maximum voltage clamp: 18V
- V_{DD} over-voltage protection (OVP)
- V_{DD} under-voltage lockout (UVLO)
- Internal open-loop protection
- Constant power limit (full AC input range)

Description

The highly integrated SG6741 series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green mode provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green mode enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, the SG6741 is manufactured using BiCMOS process, which allows an operating current of only 4mA.

The SG6741 integrates an internal frequency hopping function to reduce the EMI emission of a power supply with minimal line filtering; while the built-in synchronized slope compensation maintains a stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide AC input voltages, from $90V_{AC}$ to $264V_{AC}$.

The SG6741 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur. The PWM output is disabled until the voltage drops below the UVLO lower limit, then the controller starts again. As long as V_{DD} exceeds about 26V, the internal OVP circuit is triggered.

Pin Configuration

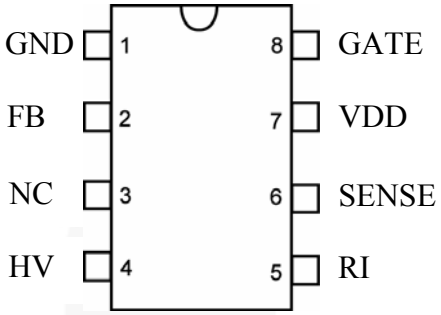

Figure 1. Pin Configuration

Block Diagram

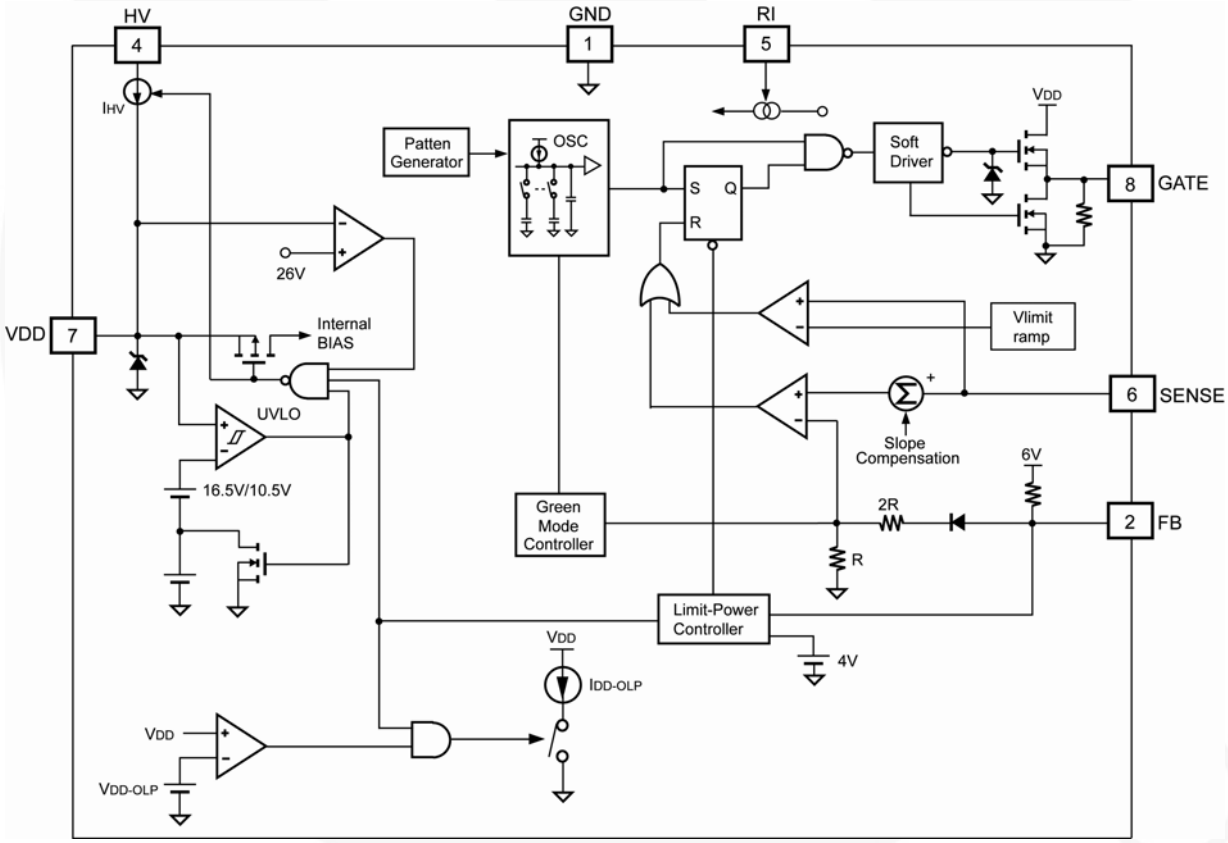

Figure 2. Block Diagram

Startup Circuitry

When the power is turned on, the internal current source (typically 8mA) charges the hold-up capacitor C_1 through a startup resistor R_{HV}. During the startup sequence, the V_{DC} from the bulk capacitor provides a startup current of about 8mA and charges the capacitor C_1. R_{HV} can be directly connected by V_{DC} to the HV pin. As the VDD pin reaches the start threshold voltage V_{DD-ON}, the SG6741 activates and signals the MOSFET. The high-voltage source current is switched off, and the supply current is drawn from the auxiliary winding of the main transformer.

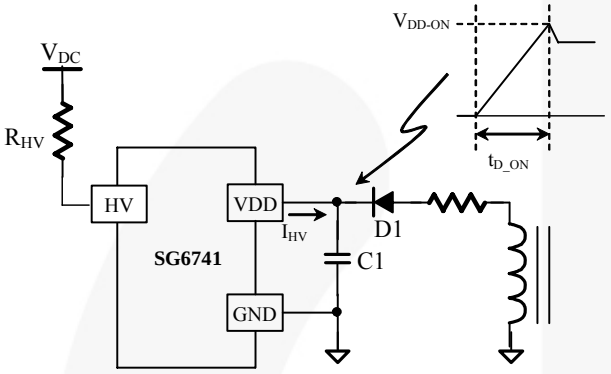

Figure 3. Startup Circuit for Power Transfer

The maximum power-on delay time is determined as:

$$t_{D\_ON} = \frac{(C1 \times V_{DD-ON})}{1.5mA} \quad (1)$$

where V_{DD-ON} is turn-on threshold voltage and t_{D_ON} is the power-on delay time of the power supply.

Due to the low startup current, a large $R_{HV,}$ such as 100KΩ, can be used. With a hold-up capacitor of 22μF, the power-on delay t_{D_ON} is less than 300ms for $90V_{AC}$ input.

When the supply current is drawn from the transformer, it draws a leakage current of about 10μA from pin HV.

The maximum power dissipation of the R_{HV} is:

$$P_{R\,HV} = I_{HV-LC(typ.)}{}^2 \times R_{HV} \quad (2)$$

where I_{Leak} is the supply current drawn from the HV pin.

$$P_{R_{HV}} = 1\mu A^2 \times 100K\Omega \cong 0.1\mu W \quad (3)$$

Under-Voltage Lockout (UVLO)

SG6741 has a voltage detector on the VDD pin to ensure that the chip has enough power to drive the MOSFET. Figure 4 shows a hysteresis of the turn-on and turn-off threshold levels and an open-loop-release voltage.

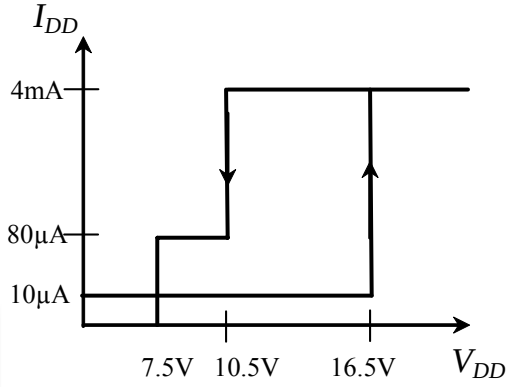

Figure 4. UVLO Specification

The turn-on and turn-off thresholds of the SG6741 are internally fixed at 16.5V and 10.5V. During startup, the V_{DD} capacitor must be charged to 16.5V to enable the IC. The capacitor continues to supply the V_{DD} until the energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 10.5V during the startup sequence.

If the secondary output short circuits or the feedback loop is open, the FB pin voltage rises rapidly toward the open-loop voltage, $V_{FB-OPEN}$. Once the FB voltage remains above V_{FB-OLP} for t_{D-OLP}, the SG6741 stops emitting output pulses. To further limit the input power under a short circuit or open-loop condition, a special two-step UVLO mechanism prolongs the discharge time of the VDD capacitor. Figure 5 shows the traditional UVLO method with the special two-step UVLO method. In the two-step UVLO mechanism, an internal sinking current, I_{DD-OLP}, pulls the V_{DD} voltage toward the V_{DD-OLP}. This sinking current is disabled after the V_{DD} drops below V_{DD-OLP}; after which, the V_{DD} voltage is charged towards V_{DD-ON}. With the addition of the two-step UVLO mechanism, the average input power during short-circuit or open-loop condition is greatly reduced and overheating doesn't occur.

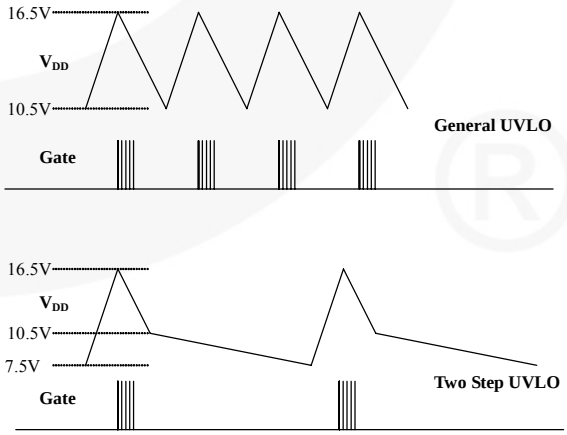

Figure 5. UVLO Effect

Oscillator and Green Mode

Resistor R_I programs the frequency of the internal oscillator of the SG6741. A 26KΩ resistor R_I generates 50μA reference current I_I and determines the PWM frequency as 65KHz:

$$I_I(mA) = \frac{1.3}{R_I(K\Omega)} \quad (4)$$

$$f_{OSC}(KHz) = \frac{1690}{R_I(K\Omega)} \quad (5)$$

The recommended range of the PWM frequency is between 50KHz~90KHz.

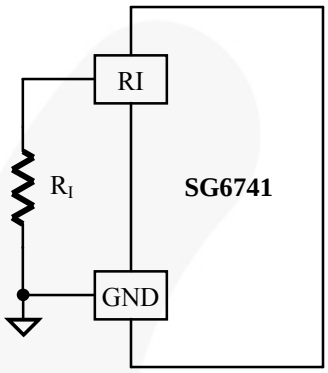

Figure 6. Setting the PWM Frequency

The proprietary green mode provides off-time modulation to reduce the PWM frequency at light-load and in no-load conditions. The feedback voltage of FB pin is taken as a reference. When the feedback voltage is lower than 2V, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the PWM frequency, the off-time modulation of the SG6741 reduces the power consumption of the power supply at light-load and in no-load conditions. For a typical case (R_I = 26KΩ), the PWM frequency is 65KHz at nominal-load and decreases to 22KHz at no-load and approximately one-third of the nominal PWM frequency.

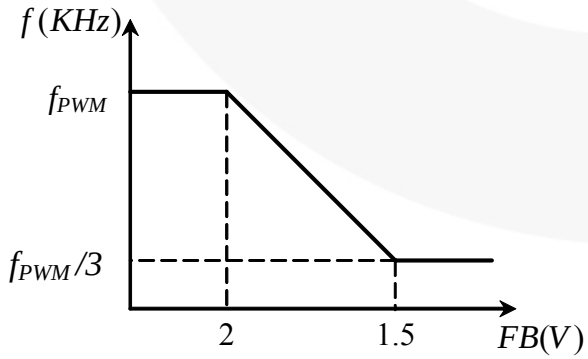

Figure 7. PWM Frequency vs. FB Voltage

FB Input

The SG6741 is designed for peak-current-mode control. A current-to-voltage conversion is done externally with a current-sense resistor R_S. Under normal operations, the peak inductor is controlled by an FB level as:

$$Ipk = \frac{V_{FB} - 1.2}{3.2 \times R_S} \quad (6)$$

where V_{FB} is the voltage of FB pin.

When V_{FB} is less than 1.2V, the SG6741 terminates the output pulses.

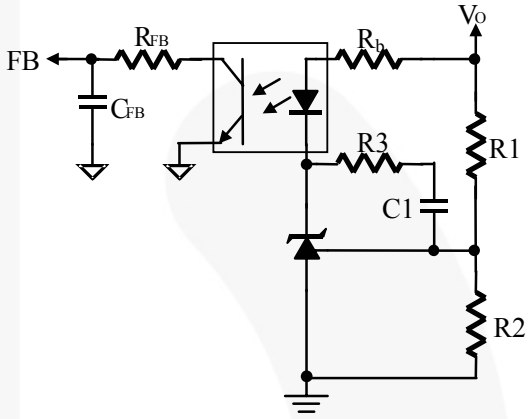

Figure 8. Feedback Circuit

Figure 8 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. RFB = 47Ω, CFB = 1nF) placed on the FB pin to the GND can further increase the stability. The maximum sourcing current of the FB pin is 1.5mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. The value of the biasing resistor R_b is determined as:

$$\frac{V_O - V_D - V_Z}{R_B} \times K \geq 1.5mA \quad (7)$$

where:

V_D is the drop voltage of photodiode, approximately 1.2V:

V_Z is the minimum operating voltage, 2.4V of the shunt regulator; and

K is the current transfer rate (CTR) of the opto-coupler.

For and output voltage V_O = 5V, with CTR = 100%, the maximum value of R_b is 860Ω.

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating the converter in CCM. With the same output power, a converter in CCM exhibits a smaller peak inductor current than in DCM; therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the RMS output current of DCM can be twice that of the CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation also results in higher output voltage spikes. A large LC filter has to be added. A flyback converter in CCM achieves better performance with a lower component cost.

Despite the above advantages of CCM operation, there is one concern—stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current remains controlled. This causes sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The SG6741 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, the SG6741 can be used to design a cost effective, highly efficient, compact flyback power supply operating in CCM without additional external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \times D \quad (8)$$

where V_{SL} = 0.33V and D = duty cycle.

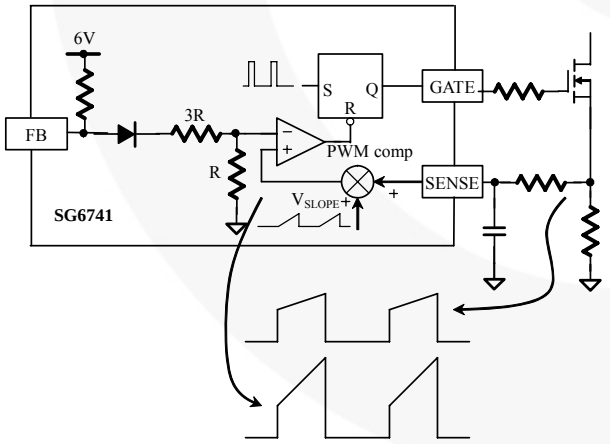

Figure 9. Synchronized Slope Compensation

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor Rs. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay t_{PD}. The delay time results in unequal power limit levels under universal input. In the SG6741, a saw-tooth power-limiter (saw limiter) is designed to solve the unequal power limit problem. As shown in Figure 10, the saw limiter is designed as a positive ramp signal ($V_{limit\ ramp}$) and is fed into the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with fixed propagation delay t_{PD}, the peak primary current would be the same for various line input voltages. Therefore, the maximum output power can remain a constant value within a wide input voltage range without adding external circuitry.

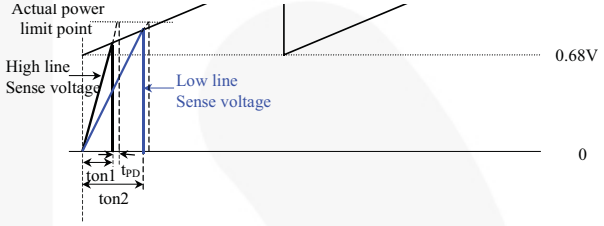

Figure 10. Constant Power Limit Compensation

Leading Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike is induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, inevitably appears on the sensed signal. Inside the SG6741, a leading-edge blanking time of about 350ns is introduced to avoid premature termination of MOSFET by the spike. Only a small-value RC filter (e.g. 100Ω+ 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the RS is recommended.

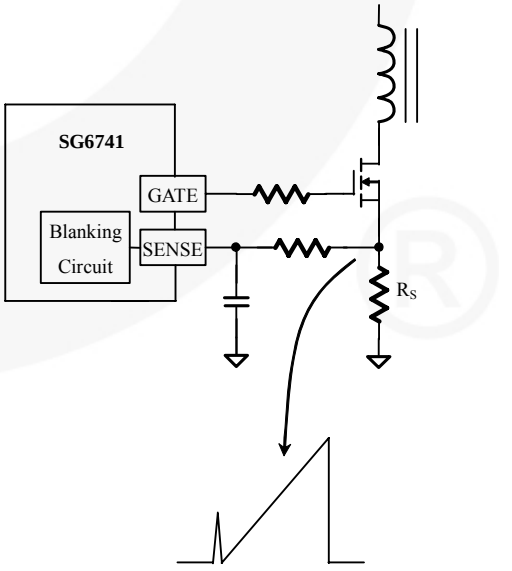

Figure 11. Turn-on Spike

Sense Pin Short-Circuit Protection

SG6741 provides a safety protection for power supply production. When a sense resistor is shorted by soldering in production, the pulse-by-pulse current limiting loses efficacy to provide an over-power protection of the unit. The unit may malfunction when the loading is larger than original maximum load. To protect against a short circuit across the current-sense resistor, the controller immediately shuts down if a continuously low voltage (around 0.15V) for 180μs on the SENSE pin is detected.

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving an external MOSFET. An internal Zener diode clamps the driver voltage under 18V to protect the MOSFET against over-voltage. By integrating circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, improving EMI performance.

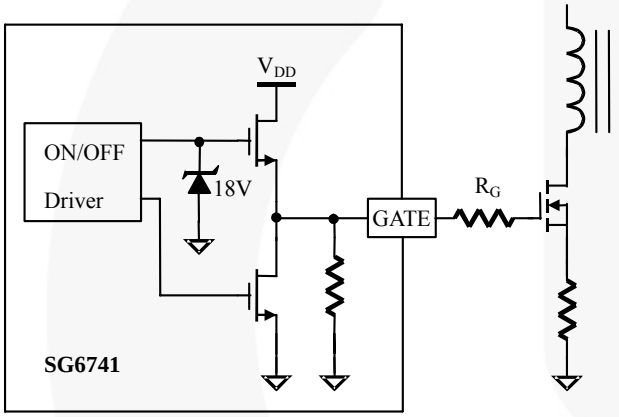

Figure 12.Gate Drive

Lab Note

Before modifying or soldering/desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during the process.

This device is sensitive to electrostatic discharge (ESD). To improve the production yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

Printed Circuit Board Layout

Current/voltage/switching frequency make printed circuit board layout and design a very important issue. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{bulk} first, then to the switching circuits.
- The high-frequency current loop is found in **C_{bulk} – Transformer – MOSFET – R_S – C_{bulk}**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage drain traces related to the MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, ground the heatsink.
- As indicated by 3, the control circuits' ground should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by the **transformer aux winding, D_1 and C_1** should also be kept small. Place C_1 close to the SG6741 for good decoupling.

Two suggestions with different pros and cons for ground connections are recommended:

- GND3→2→4→1: Possible method for circumventing the sense signals common impedance interference.
- GND3→2→1→4: Potentially better for ESD testing where a ground is not available for the power supply. The ESD discharge charges go from secondary through the transformer stray capacitance to the GND2 first. Then charges go from GND2 to GND1 and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the **positive terminal of the C_{bulk} (V_{DC})**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of the C_{bulk} (GND1)** directly. Point discharge of the Y-cap also helps with ESD. However, according to safety requirements, the creepage between the two pointed ends should be at least 5mm.

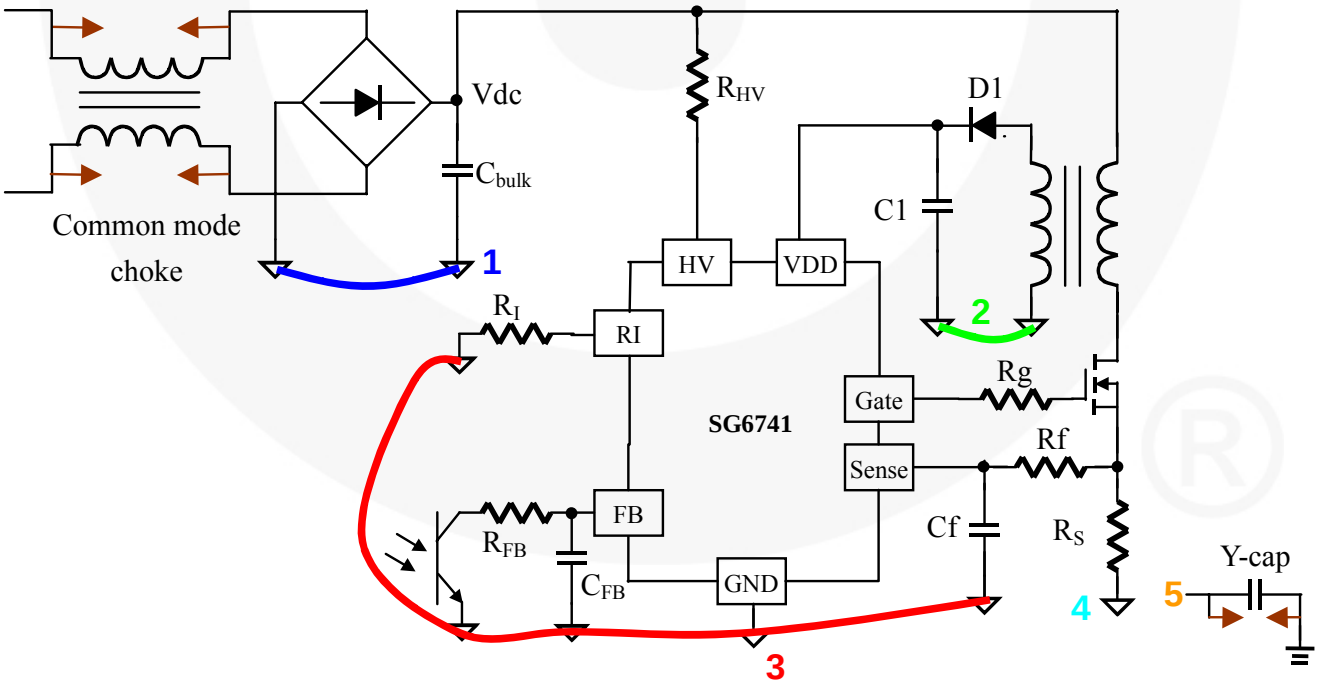

Figure 13. Layout Considerations

Related Datasheets

SG6741 — Highly Integrated Green-Mode PWM Controller