

## Very Low Output Low Dropout Regulator

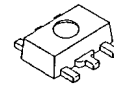
### ■ GENERAL DESCRIPTION

The NJM2842 is a very low output voltage, low drop out regulators. It delivers up to 1A output current with the output voltage of 0.8 to 1.8V. The use of an external bias voltage can improve the transient response and the ripple rejection characteristics while maintaining minimum input to output voltage.

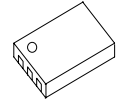
### ■ FEATURES

- Output Voltage Range 0.8V to 1.8V
- High Ripple Rejection 91 dB typ.(  $V_O=1.2V$  )
- Output Noise Voltage  $V_{NO}=44 \mu V_{rms}$
- Output Current  $I_O(max)=1.0A$
- High Precision Output  $V_O \pm 1.0\%$
- Dual Supply Voltage Type  $V_{IN}, V_{BIAS}$  (sequence free)
- High Stability for Load 0.002%/mA (max)
- Output Capacitor with 4.7 $\mu F$  ceramic capacitor ( $V_O > 1.0V$ )
- Low Dropout Voltage 0.2V typ. @  $I_O=600mA$
- ON/OFF Control
- Built-in Thermal Overload Protection and Short Circuit Current Limit Protection
- Bipolar Technology
- Package Outline SOT-89-5, ESON6-H1, TO252-5

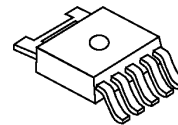
### ■ PACKAGE OUTLINE



NJM2842U2

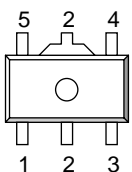


NJM2842KH1



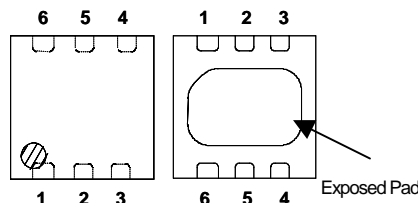
NJM2842DL3

### ■ PIN CONNECTION



1. CONTROL
2. GND
3.  $V_{OUT}$
4.  $V_{IN}$
5.  $V_{BIAS}$

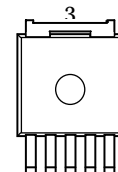
NJM2842U2



NJM2842KH1

1.  $V_{OUT}$
2.  $V_{BIAS}$
3. N.C.
4. CONTROL
5. GND
6.  $V_{IN}$

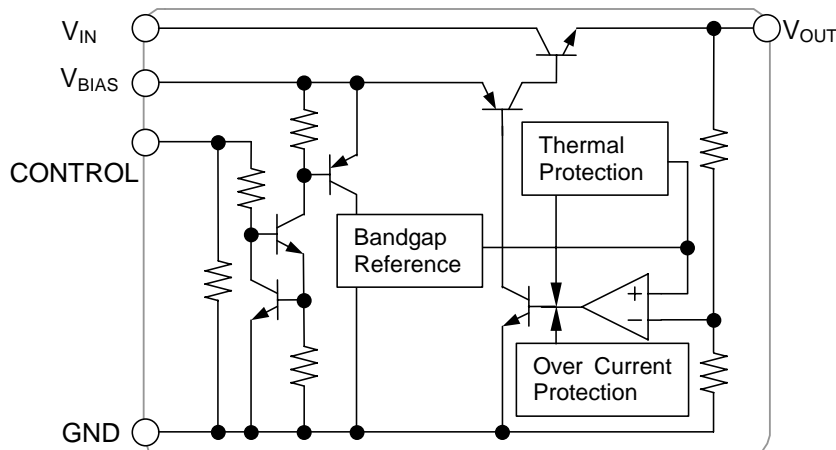
(Exposed Pad Connected to GND)



NJM2842DL3

1. CONTROL
2.  $V_{OUT}$
3. GND
4.  $V_{IN}$
5.  $V_{BIAS}$

### ■ BLOCK DIAGRAM



# NJM2842

## ■ OUTPUT VOLTAGE RANK

Device Name SOT-89-5	V <sub>out</sub>	Device Name ESON6-H1	V <sub>out</sub>	Device Name TO252-5	V <sub>out</sub>
NJM2842U2-008	0.8V	NJM2842KH1-008	0.8V	NJM2842DL3-012	1.2V
NJM2842U2-010	1.0V	NJM2842KH1-010	1.0V		
NJM2842U2-012	1.2V	NJM2842KH1-012	1.2V		
NJM2842U2-015	1.5V	NJM2842KH1-015	1.5V		
NJM2842U2-018	1.8V	NJM2842KH1-018	1.8V		

Available Fixed Output Voltage Setting Range: 0.8V to 1.8V

## ■ ABABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS		UNIT
Input Voltage	V <sub>IN</sub>	+7		V
Bias Voltage	V <sub>BIAS</sub>	+7		V
Control Voltage	V <sub>CONT</sub>	+7		V
Power Dissipation	P <sub>D</sub>	SOT-89-5	625 (*1)	mW
			2400 (*2)	
		TO252-5	1190(*1)	
			3125(*2)	
ESON6-H1	440 (*3)			
	1200 (*4)			
Operating Temperature	Topr	-40~+85		°C
Storage Temperature	Tstg	-50~+150		°C

(\*1): Mounted on glass epoxy board. (76.2x 114.3x1.6mm:EIA/JDEC standard size, 2Layers, copper area 100mm<sup>2</sup>)

(\*2): Mounted on glass epoxy board. (76.2x 114.3x1.6mm:EIA/JDEC standard size, 4Layers)

(4Layers inner foil : 74.2 x 74.2mm Applying a thermal via hall to a board based on JEDEC standard JESD51-5)

(\*3): Mounted on glass epoxy board based on EIA/JEDEC. (101.5x 114.57x1.6mm, 2Layers, Use the Exposed Pad)

(\*4): Mounted on glass epoxy board based on EIA/JEDEC. (101.5x 114.57x1.6mm, 4Layers, Use the Exposed Pad)

(4 Layers, Internal foil area: 99.5×99.5mm, Based on JEDEC Standard JESD51-5, used a Thermal Via Hole)

## ■ BIAS VOLTAGE INPUT RANGE

V<sub>BIAS</sub>= +2.5V to +5.5V (V<sub>O</sub><1.5V)

V<sub>BIAS</sub>= +V<sub>O</sub>+1V to +5.5V (V<sub>O</sub>≥1.5V)

## ■ ELECTRICAL CHARACTERISTICS

( $V_{BIAS}=2.5V(V_O \geq 1.5V)$ :  $V_{BIAS}=V_O+1V$ ,  $V_{IN}=V_O+1V$ ,  $C_{BIAS}=0.1\mu F$ ,  $C_{IN}=4.7\mu F$ ,  $C_O=4.7\mu F$ ,  $T_a=25^\circ C$ )

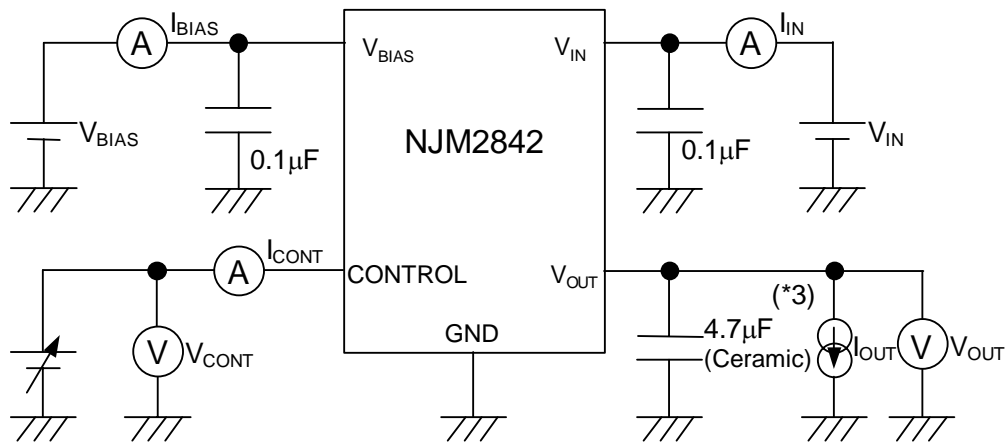
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	$V_O$	$I_O=30mA$	-1.0%	-	+1.0%	V
Unloaded Bias Current	$I_{BIAS}$	$I_O=0mA$ , except $I_{CONT}$	-	300	500	$\mu A$
Unloaded Input Current	$I_{IN}$	$I_O=0mA$ , except $I_{CONT}$	-	-	20	$\mu A$
Bias Current at Control OFF	$I_{BIAS(OFF)}$	$V_{CONT}=0V$	-	-	100	nA
Input Current at Control OFF	$I_{IN(OFF)}$	$V_{CONT}=0V$	-	-	100	nA
Output Current	$I_O$	$V_O \times 0.9V$	1000	1700	-	mA
Line Regulation 1 ( $V_{BIAS}$ )	$\Delta V_O / \Delta V_{BIAS}$	$V_{BIAS}=2.5V$ to $V_O+5.5V(V_O < 1.5V)$ $V_{BIAS}=V_O+1V$ to $V_O+5.5V(V_O \geq 1.5V)$ $I_O=30mA$	-	-	0.10	%/V
Line Regulation 2 ( $V_{IN}$ )	$\Delta V_O / \Delta V_{IN}$	$V_{IN}=V_O+1V$ to $V_O+5.5V$ , $I_O=30mA$	-	-	0.10	%/V
Load Regulation	$\Delta V_O / \Delta I_O$	$I_O=30$ to $500mA$	-	-	0.002	%/mA
Dropout Voltage	$\Delta V_{I-O}$	$I_O=600mA$	-	0.10	0.18	V
Ripple Rejection Ratio 1 ( $V_{BIAS}$ )	$RR1(V_{BIAS})$	$V_{BIAS}=3.5V$ , ebias=200mVrms, f=1kHz, $I_O=10mA$	Refer to Table 1			dB
Ripple Rejection Ratio 2 ( $V_{IN}$ )	$RR2(V_{IN})$	ebias=200mVrms, f=1kHz, $I_O=10mA$	Refer to Table 1			dB
Average Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T_a$	$T_a=0$ to $+85^\circ C$ , $I_O=10mA$	-	$\pm 50$	-	ppm/ $^\circ C$
Output Noise Voltage	$V_{NO}$	f=10Hz to 80kHz, $I_O=10mA$	Refer to Table 1			$\mu Vrms$
Control Current	$I_{CONT}$	$V_{CONT}=1.6V$	-	3	12	$\mu A$
Control Voltage for ON-state	$V_{CONT(ON)}$		1.6	-	-	V
Control Voltage for OFF-state	$V_{CONT(OFF)}$		-	-	0.6	V
Bias Voltage	$V_{BIAS}$		-	-	5.5	V
Input Voltage	$V_{IN}$		-	-	5.5	V

• Table1

Voltage Rank	RR1( $V_{BIAS}$ )				RR2( $V_{IN}$ )				$V_{NO}$			
	MIN.	TYP.	MAX.	UNIT	MIN.	TYP.	MAX.	UNIT	MIN.	TYP.	MAX.	UNIT
0.8V	-	77	-		-	93	-	dB	-	34	-	$\mu Vrms$
1.0V	-	75	-		-	92	-		-	38	-	
1.2V	-	73	-		-	91	-		-	44	-	
1.5V	-	71	-		-	90	-		-	47	-	
1.8V	-	70	-		-	89	-		-	51	-	

# NJM2842

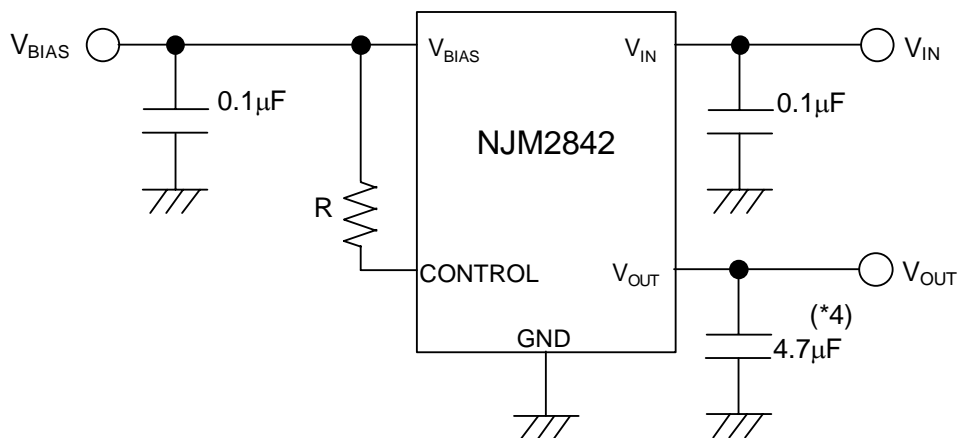
## TEST CIRCUIT



(\*3)  $V_o \leq 1.0V$  version:  $C_o = 4.7\mu F$  (Ceramic)

## TYPICAL APPLICATION

a) In case of where ON/OFF control is not required:

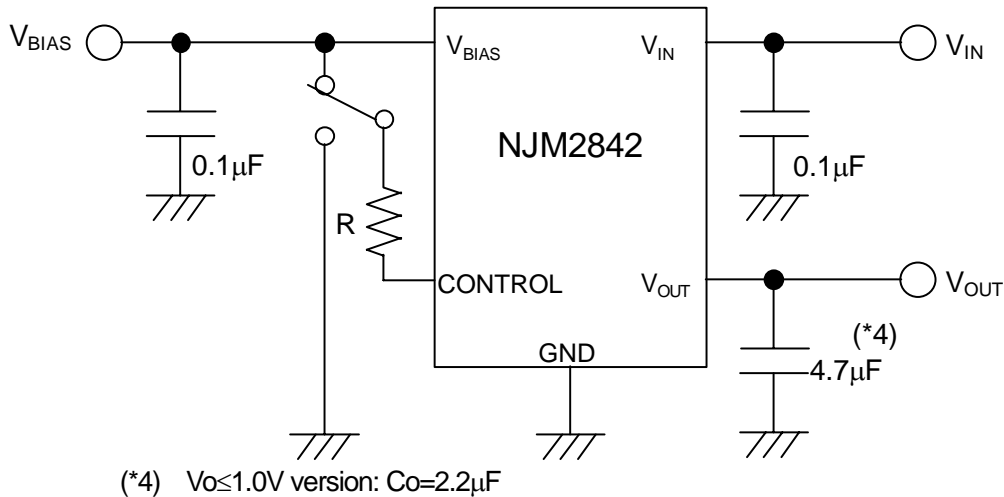


(\*4)  $V_o \leq 1.0V$  version:  $C_o = 4.7\mu F$

You shall connect control terminal to  $V_{BIAS}$  terminal.

Though the  $I_{CONT}$  decreases by inserting "R" to between Control terminal and  $V_{BIAS}$  terminal, the minimum operating voltage is increased due to the resistor "R".

b) In use of ON/OFF control:



State of control terminal:

"H" → output is enabled.

"L" or "open" → output is disabled.

\*Regarding a Bias Capacitance ( $C_{BIAS}$ ) and an Input Capacitance ( $C_{IN}$ )

$C_{BIAS}$  and  $C_{IN}$  have the effect that prevents the oscillation at the time of the following condition.

When Source impedance is high.

When  $V_{IN}$  and/or GND line is long.

Therefore, you shall connect the  $C_{BIAS}$  and  $C_{IN}$  that recommendation value or larger ( $C_{BIAS} \geq 0.1\mu F$ ,  $C_{IN} \geq 0.1\mu F$ ) so that lines that  $V_{BIAS}$ -GND and  $V_{IN}$ -GND become as short as possible.

\*Output Capacitance  $C_o$

Output capacitor ( $C_o$ ) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

This product is designed to work with a low ESR capacitor ( $C_o$ ). However use of recommended capacitance or larger value is effective for stable operation.

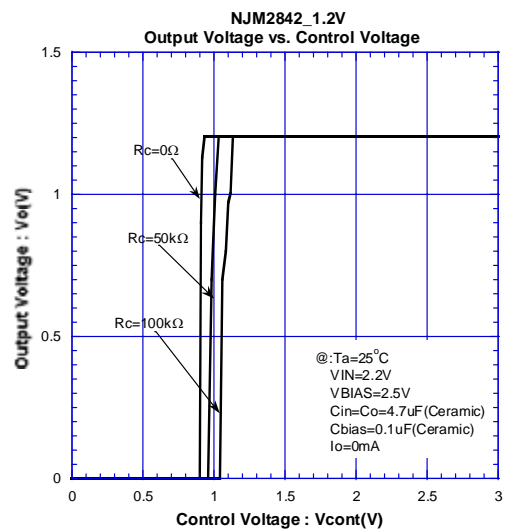
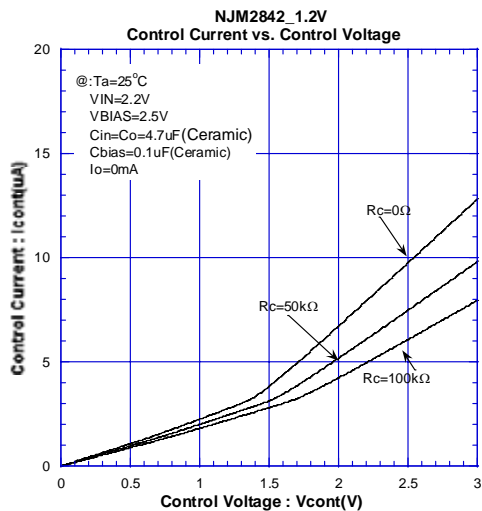
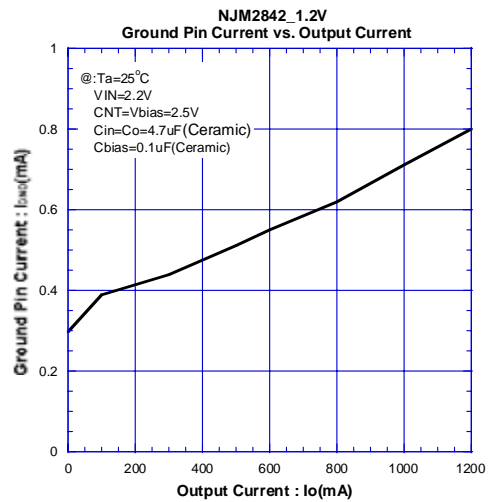
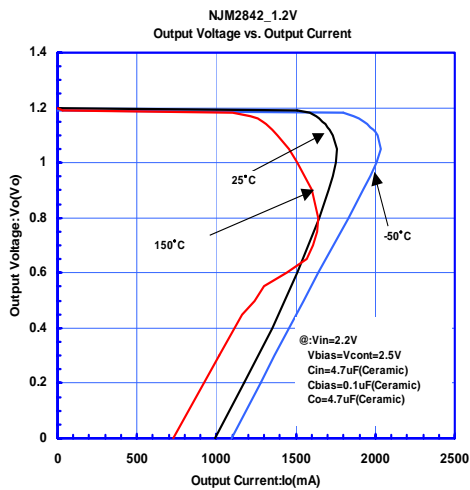
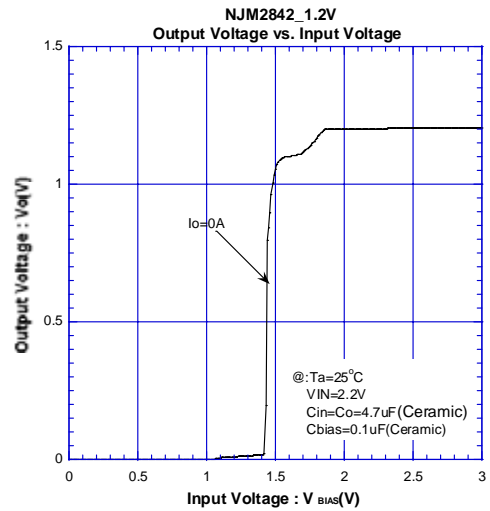
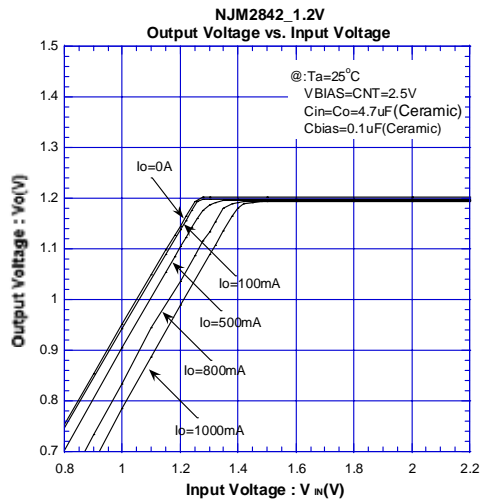
Use of a smaller  $C_o$  may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

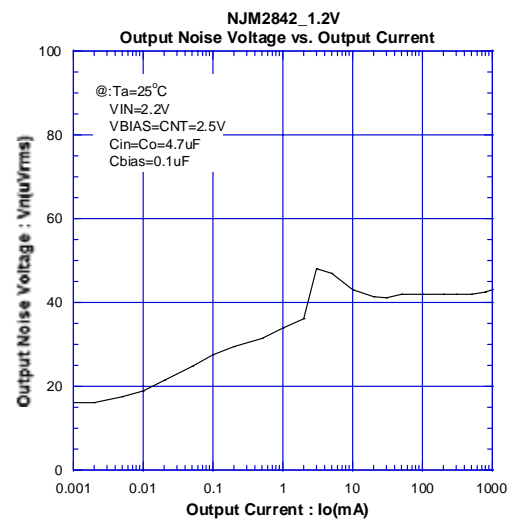
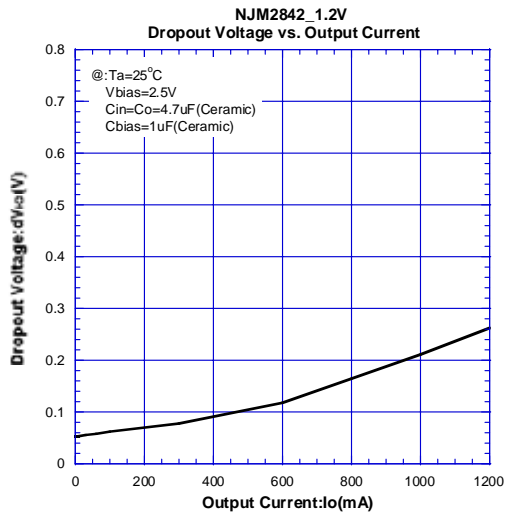
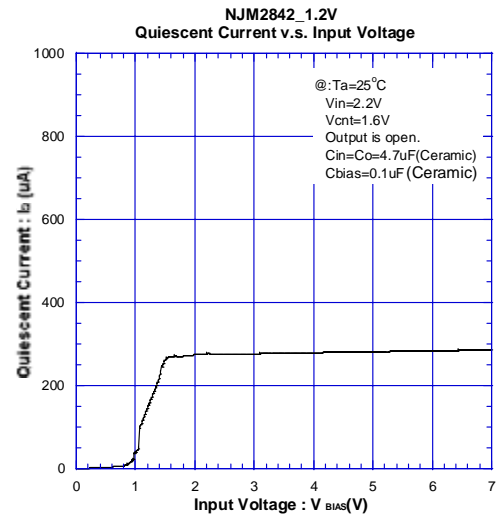
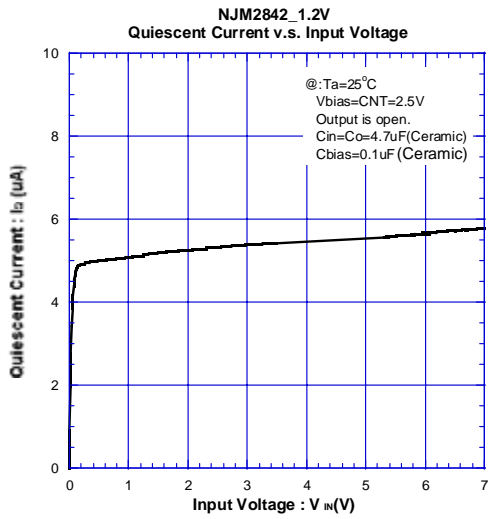
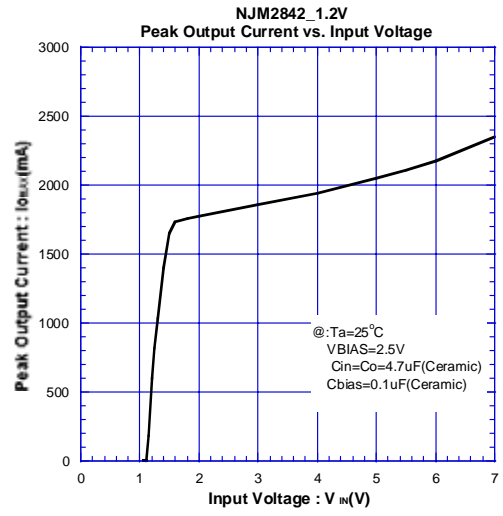
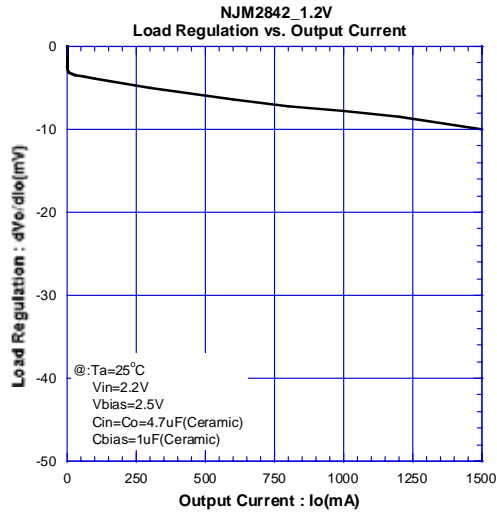
Therefore use  $C_o$  with the recommended capacitance or larger value and connect between  $V_o$  terminal and GND terminal with shortest path. The recommended capacitance depends on the output voltage rank. Low voltage regulator requires larger value  $C_o$ . Thus, check the recommended capacitance for each output voltage rank.

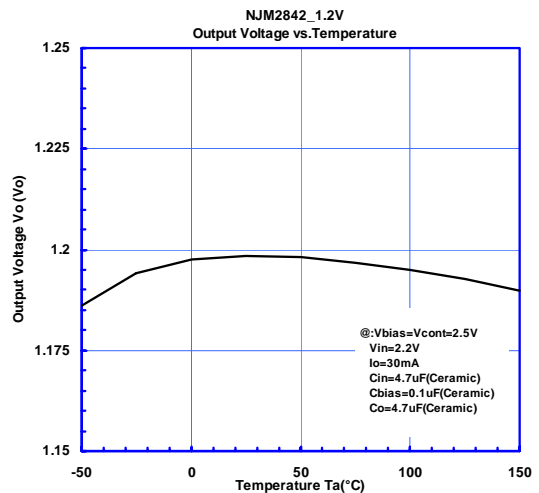
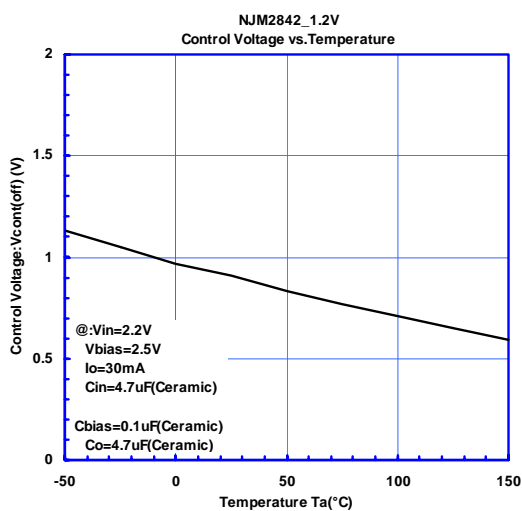
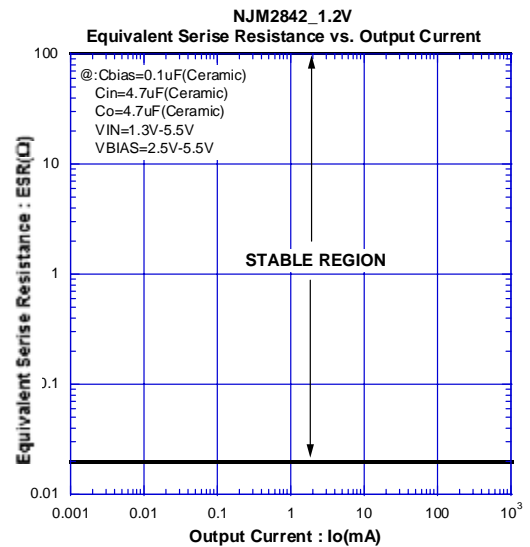
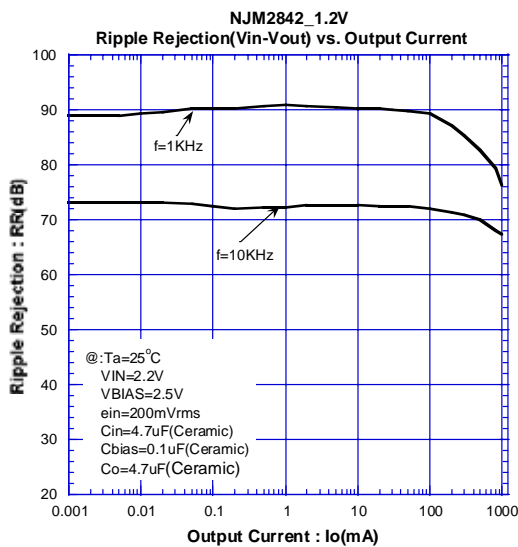
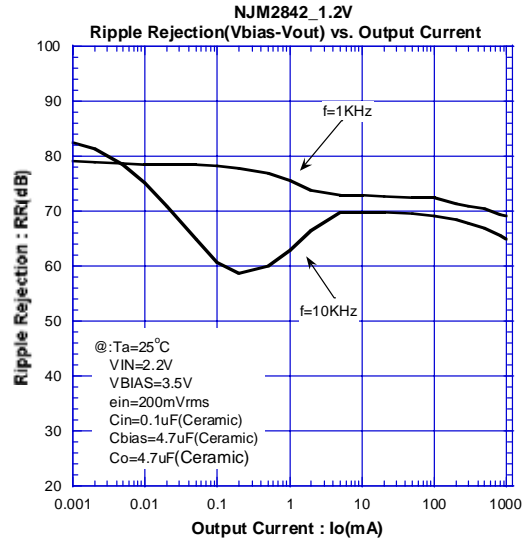
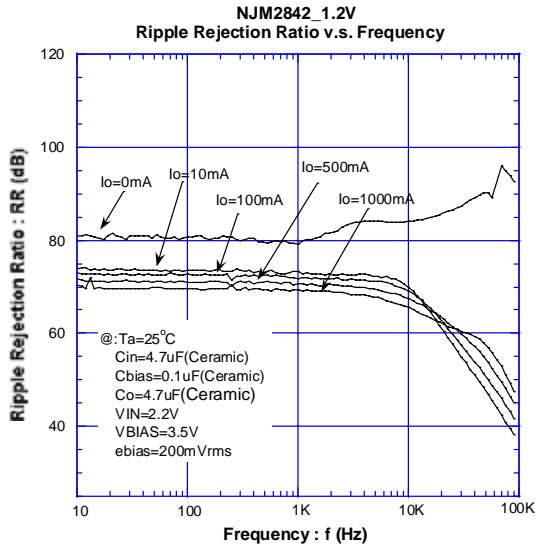
Use of a larger  $C_o$  reduces output noise and ripple output, and also improves output transient response against rapid load change.

# NJM2842

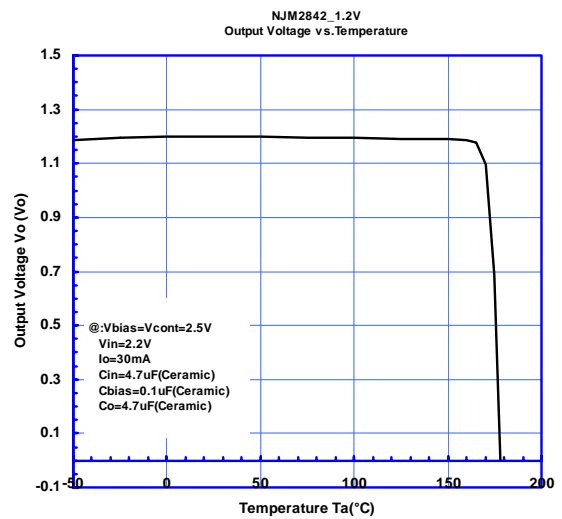
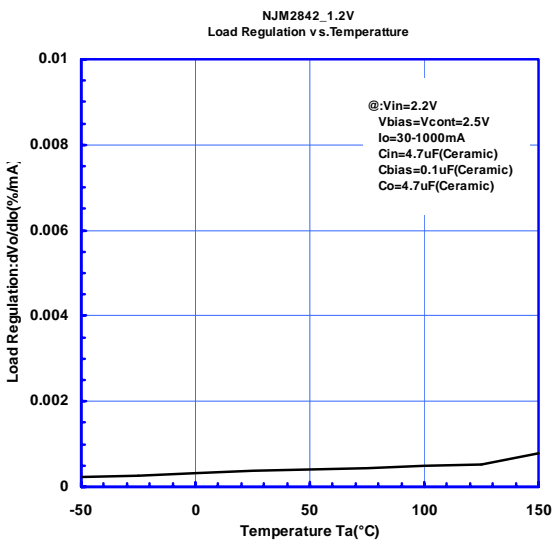
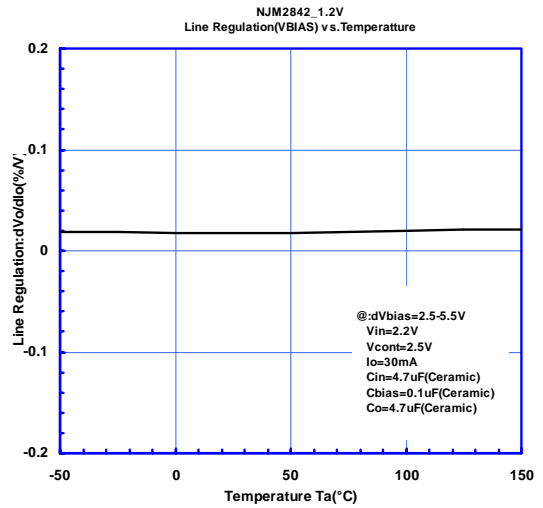
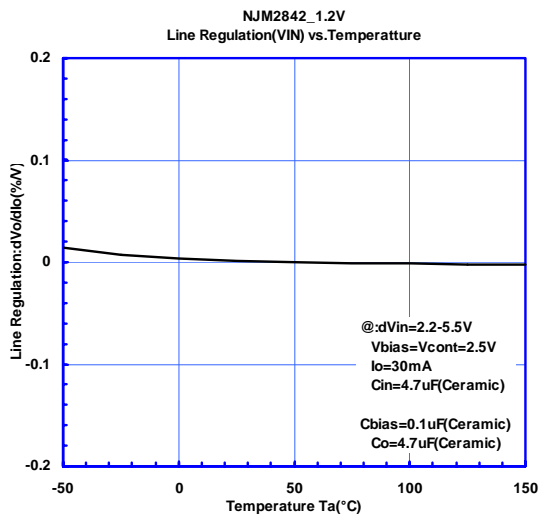
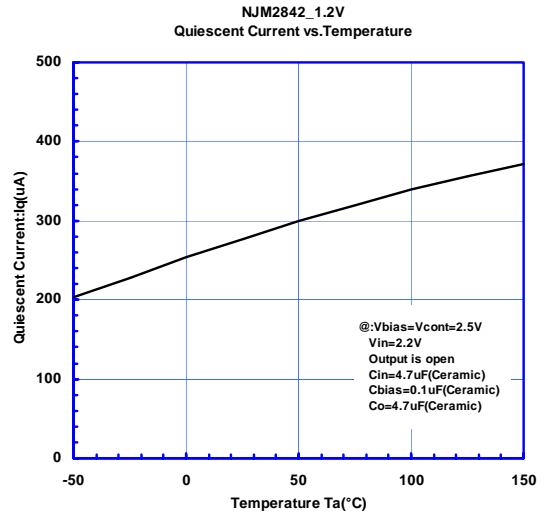
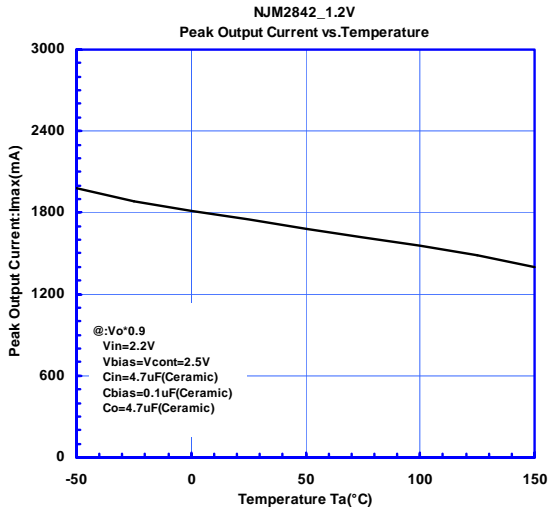
## ■ TYPICAL CHARACTERISTICS

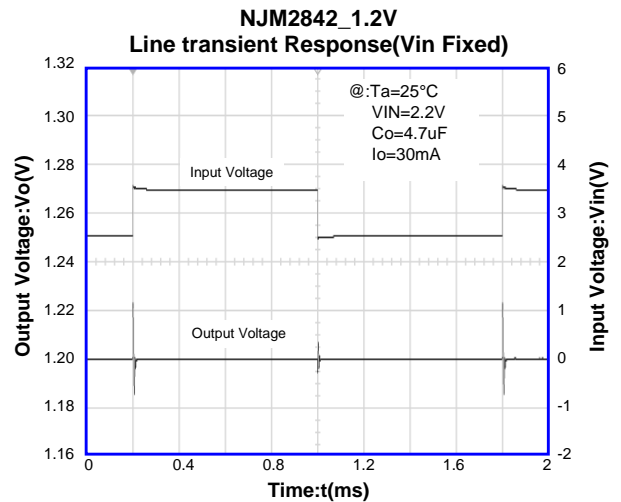
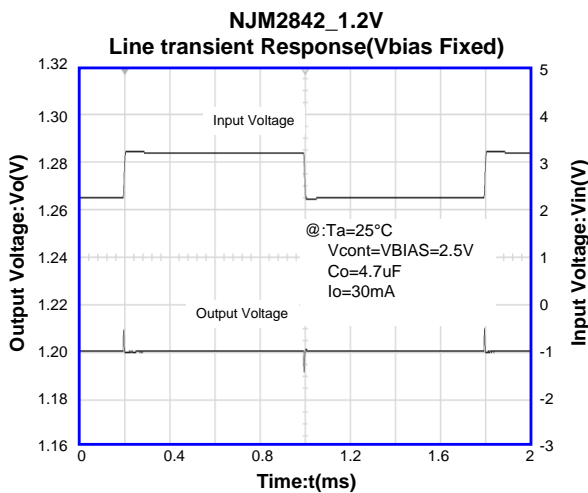
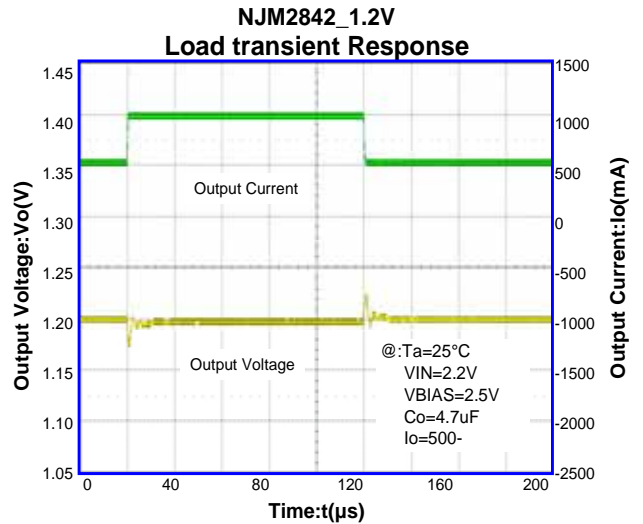
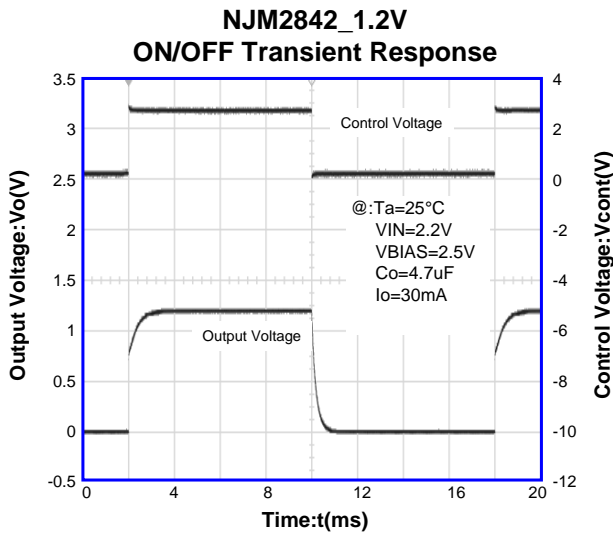
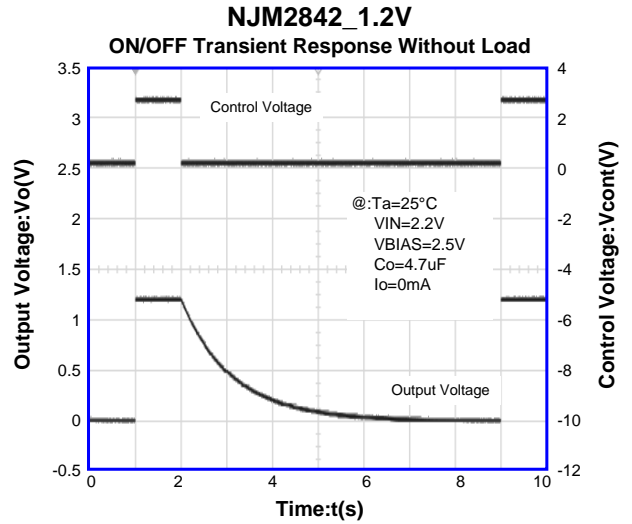
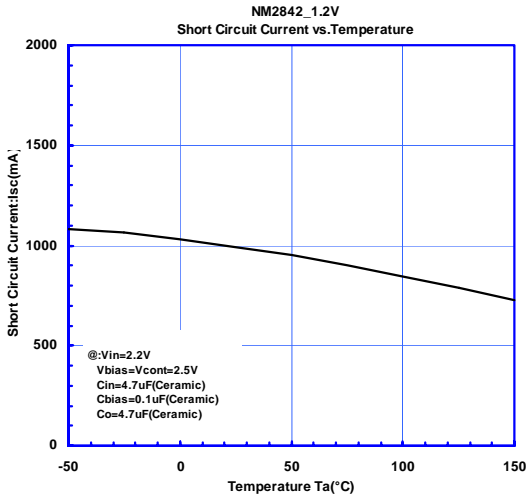












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