LSI/CSI

LS7082N1

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QUADRATURE CLOCK CONVERTER

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FEATURES:

- x1, x2 and x4 mode selection
- Up to 16MHz output clock frequency
- INDEX input and output
- UP/DOWN indicator output
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +3V to +12V operation (V_{DD} - V_{SS})
- **LS7082N1** (DIP); **LS7082N1-S** (SOIC) - **See Figure 1**

DESCRIPTION:

The **LS7082N1** is a CMOS quadrature clock converter. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B Inputs of the **LS7082N1**, are converted to strings of Up Clocks and Down Clocks. Pulses derived from the Index Track of an encoder, when applied to the INDX input, produce absolute position reference pulses which are synchronized to the Up Clocks and Down Clocks. These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

PIN ASSIGNMENT - TOP VIEW

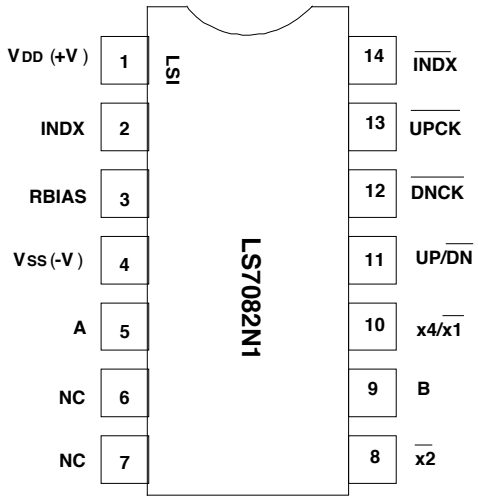

FIGURE 1

TABLE 1. MODE SELECTION TRUTH TABLE

$\overline{x2}$ Input	x4/$\overline{x1}$ Input	MODE
0	0 or 1	x2
1	0	x1
1	1	x4

INPUT/OUTPUT DESCRIPTION:

V_{DD} (Pin 1)
Supply Voltage positive terminal.

INDX (Pin 2)
Encoder Index pulses are applied to this input.

RBIAS (Pin 3)
Input for external component connection. A resistor connected between this input and V_{SS} adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A, B pulse separation ($T_{OW} \leq T_{PS}$).

V_{SS} (Pin 4)
Supply Voltage negative terminal.

A (Pin 5)
Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

$\overline{x2}$ (Pin 8)
A low level applied to this input selects x2 mode of operation. See Table 1 for Mode Selection Truth Table and Figure 2 for Input/Output timing relationship.

B (Pin 9)
Quadrature Clock Input B. This input has a filter circuit identical to input A.

x4/$\overline{x1}$ (Pin 10)
This input selects between x1 and x4 modes of operation. See Table 1 for Mode Selection Truth Table and Figure 2 for Input/Output timing relationship.

UP/$\overline{DN}$ (Pin 11)
The count direction at any instant is indicated at this output. An UP count direction is indicated by a high, and a DOWN count direction is indicated by a low (See Figure 2).

$\overline{DNCK}$ (Pin 12)
This DOWN Clock output consists of low-going pulses generated when A input lags the B input (See Figure 2).

$\overline{UPCK}$ (Pin 13)
This UP Clock output consists of low-going pulses generated when A input leads the B input (See Figure 2).

$\overline{INDX}$ (Pin 14)
This output consists of low-going pulses generated by a positive clock transition at the A input when INDX input is high and B input is low and a negative clock transition at the B input when INDX input is high and A input is high. (See Figure 2).

NOTE: All unused input pins must be tied to V_{DD} or V_{SS}.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	V_{DD} - V_{SS}	16.0	V
Voltage at any input	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operating temperature	T_A	0 to +85	°C
Storage temperature	T_{STG}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:

(All voltages referenced to V_{SS}, T_A = 0°C to 85°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	V_{DD}	3.0	12.0	V	-
Supply current	I_{DD}	-	20	µA	V_{DD} = 12V, All input frequencies = 0Hz RBIAS = 2MΩ
x4/$\overline{x1}$	V_{IL}	-	0.5	V	-
x2, INDX Logic Low	V_{IL}	-	0.3V_{DD}	V	-
A, B Logic Low	V_{IL}	-	0.7	V	V_{DD} = 3V
		-	1.0	V	V_{DD} = 5V
		-	2.8	V	V_{DD} = 12V
x4/$\overline{x1}$	V_{IH}	V_{DD} - 0.5	-	V	-
x2, INDX Logic High	V_{IH}	0.7V_{DD}	-	V	-
A, B Logic High	V_{IH}	2.0	-	V	V_{DD} = 3V
		3.0	-	V	V_{DD} = 5V
		6.6	-	V	V_{DD} = 12V
ALL OUTPUTS:					
Sink Current	I_{OL}	1.3	-	mA	V_{DD} = 3V
V_{OL} = 0.4V		1.9	-	mA	V_{DD} = 5V
		2.9	-	mA	V_{DD} = 12V
Source Current	I_{OH}	0.83	-	mA	V_{DD} = 3V
V_{OH} = V_{DD} - 0.5V		1.1	-	mA	V_{DD} = 5V
		1.6	-	mA	V_{DD} = 12V

TRANSIENT CHARACTERISTICS:

(T_A = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
A, B inputs:					
Validation Delay	T_{VD}	-	250	ns	V_{DD} = 3V
		-	170	ns	V_{DD} = 5V
		-	71	ns	V_{DD} = 12V
A, B inputs:					
Pulse Width	T_{PW}	T_{VD} + T_{OW}	Infinite	ns	-
A to B or **B to A**					
Phase Delay	T_{PS}	T_{OW}	Infinite	ns	-
A, B frequency	$f_{A, B}$	-	$\frac{1}{2T_{PW}}$	Hz	-
Input to Output Delay	T_{DS}	-	280	ns	V_{DD} = 3V
		-	220	ns	V_{DD} = 5V
		-	120	ns	V_{DD} = 12V Includes input validation delay
Output Clock Pulse Width	T_{OW}	50	-	ns	See Fig. 4 & 5

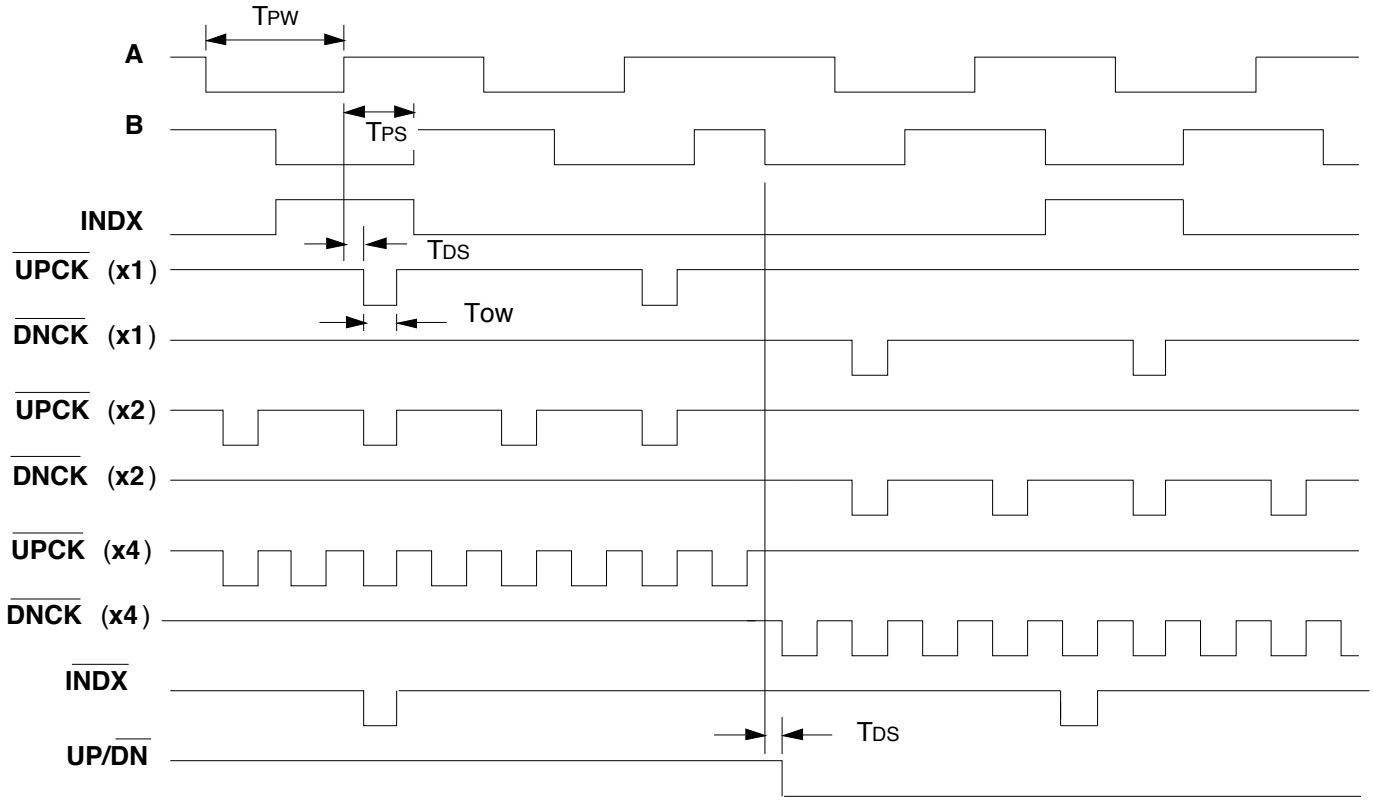

FIGURE 2. LS7082N1 INPUT/OUTPUT TIMING DIAGRAM

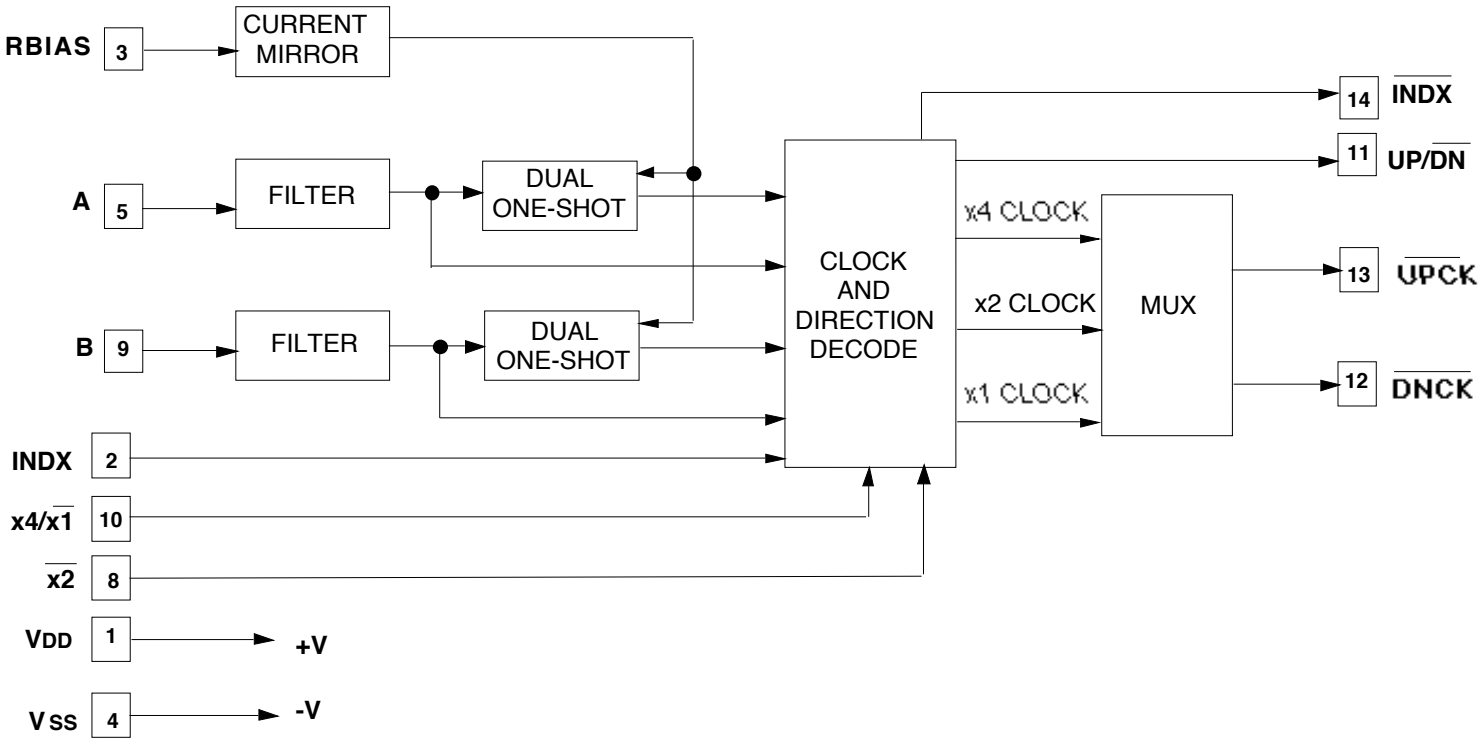

FIGURE 3. LS7082N1 BLOCK DIAGRAM

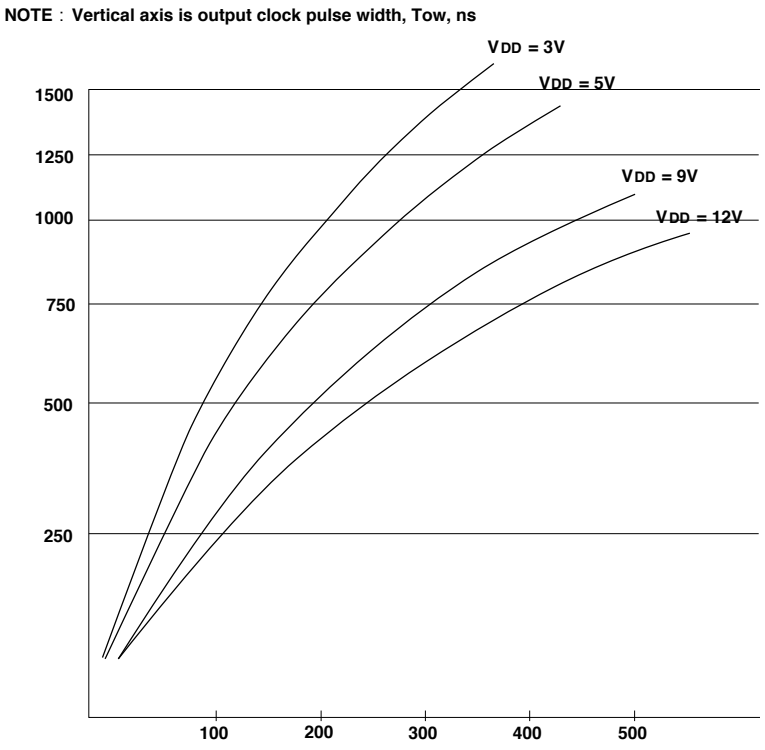

Figure 4. Tow vs R BIAS , kΩ

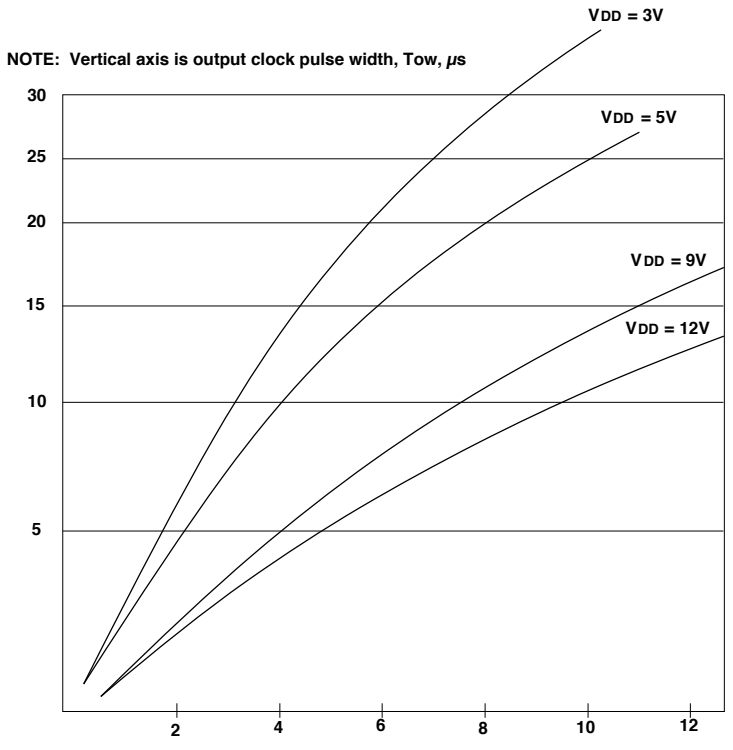

Figure 5. Tow vs R BIAS , MΩ

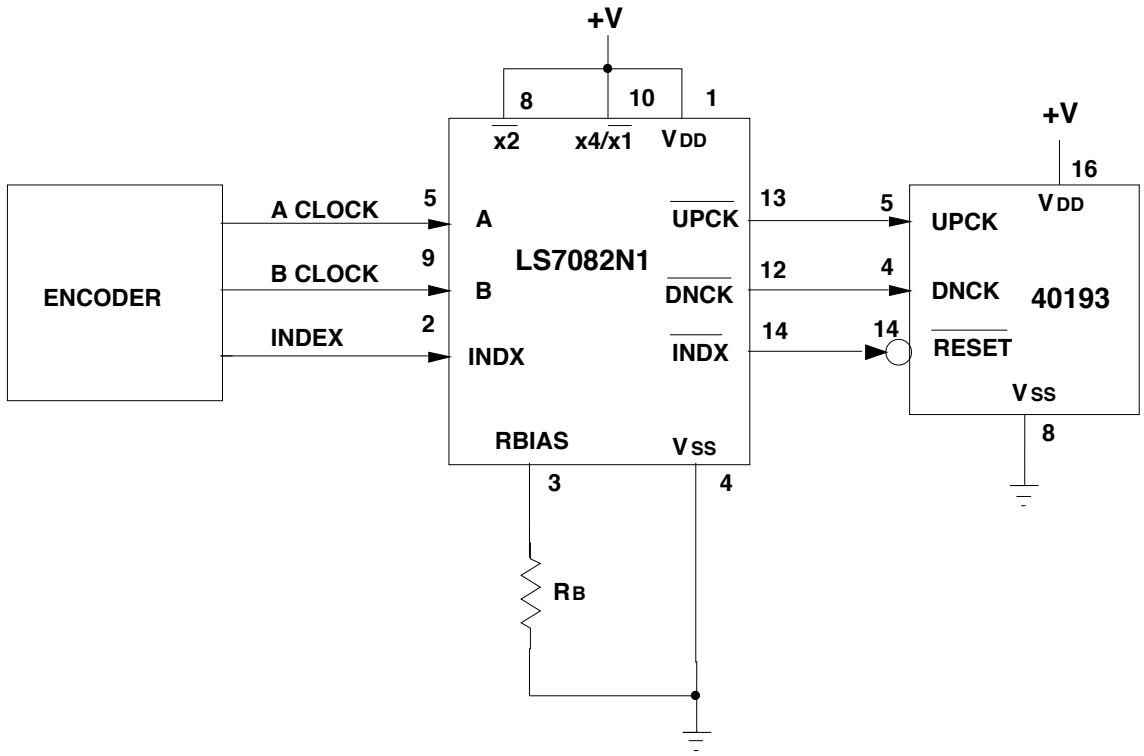

FIGURE 6. A TYPICAL APPLICATION in x4 MODE

NOTE: When driving a counter that requires $\overline{CLK}$ and Direction input, the $\overline{UPCK}$ and DNCK must be externally "Ored" together to generate one clock, $\overline{CLK}$. $\overline{CLK}$ can be applied directly to the Clock input of counters that advance on the positive edge of the clock. If the counter advances on the negative edge of the clock, an inverter must be added between $\overline{CLK}$ and the Clock input of the counter.