



# STD2NC45-1 STQ1NC45

N-CHANNEL 450V - 4.1Ω - 1.5 A IPAK / TO-92  
SuperMESH™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STD2NC45-1	450 V	< 4.5 Ω	1.5 A	30 W
STQ1NC45	450 V	< 4.5 Ω	0.5 A	3.1 W

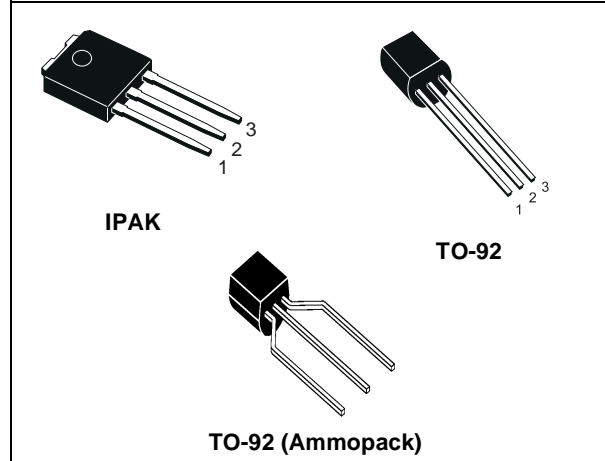
- TYPICAL R<sub>DS(on)</sub> = 4.1 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- NEW HIGH VOLTAGE BENCHMARK

## DESCRIPTION

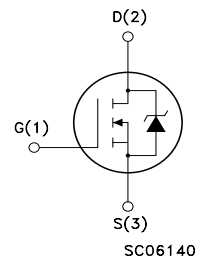
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## APPLICATIONS

- SWITCH MODE LOW POWER SUPPLIES (SMPS)
- LOW POWER, LOW COST CFL (COMPACT FLUORESCENT LAMPS)
- LOW POWER BATTERY CHARGERS



## INTERNAL SCHEMATIC DIAGRAM



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD2NC45-1	D2NC45	IPAK	TUBE
STQ1NC45	Q1NC45	TO-92	BULK
STQ1NC45-AP	Q1NC45	TO-92	AMMOPAK

**STD2NC45-1, STQ1NC45****ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value		Unit
		STD2NC45-1	STQ1NC45	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	450		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	450		V
V <sub>GS</sub>	Gate- source Voltage	± 30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	1.5	0.5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	0.95	0.315	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	6	2	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	30	3.1	W
	Derating Factor	0.24	0.025	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	3		V/ns
T <sub>j</sub>	Operating Junction Temperature	-65 to 150		°C
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 0.5A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

**THERMAL DATA**

		IPAK	TO-92	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	4.1		°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	100	120	°C/W
R <sub>thj-lead</sub>	Thermal Resistance Junction-lead Max		40	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	275	260	°C

**AVALANCHE CHARACTERISTICS**

Symbol	Parameter	Max Value		Unit
		IPAK	TO-92	
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	1.5		A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	25		mJ

**ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED)**  
ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	450			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^\circ C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30V$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.3	3	3.7	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 0.5 A$		4.1	4.5	$\Omega$

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 0.5 A$		1.1		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		160 27.5 4.7		pF pF pF

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 225 V, I_D = 0.5 A$ $R_G = 4.7\Omega, V_{GS} = 10 V$ (Resistive Load see, Figure 3)		6.7 4		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 360V, I_D = 1.5 A,$ $V_{GS} = 10V, R_G = 4.7\Omega$		7 1.3 3.2	10	nC nC nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 360V, I_D = 1.5 A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (Inductive Load see, Figure 5)		8.5 12 18		ns ns ns

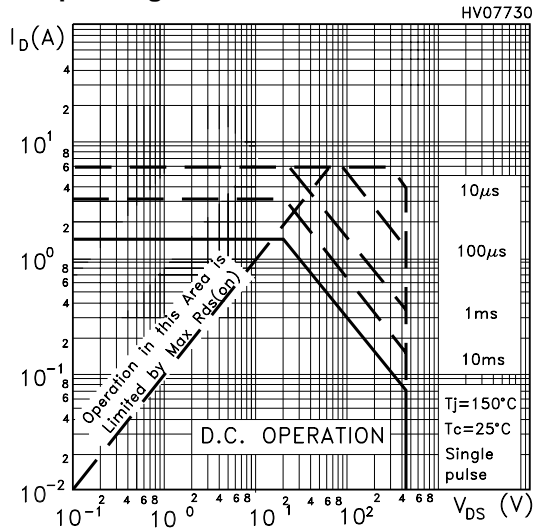
## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				1.5 6.0	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 1.5 A, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1.5 A, di/dt = 100A/\mu s$ $V_{DD} = 100V, T_j = 150^\circ C$ (see test circuit, Figure 5)		225 530 4.7		ns $\mu C$ A

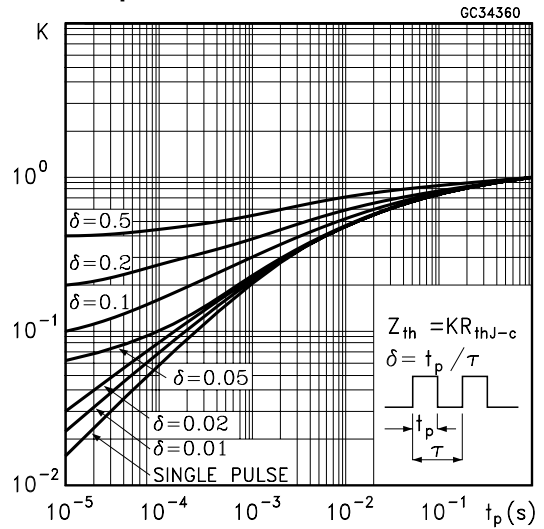
Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

# STD2NC45-1, STQ1NC45

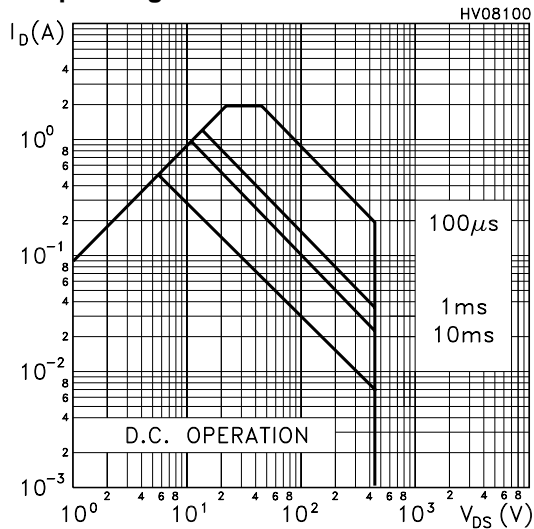
## Safe Operating Area For IPAK



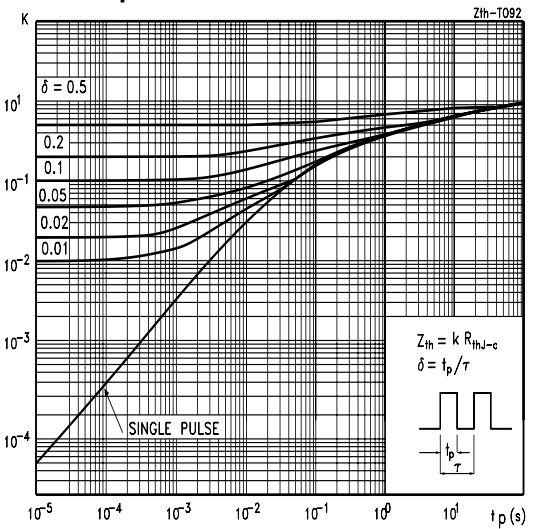
## Thermal Impedance For IPAK



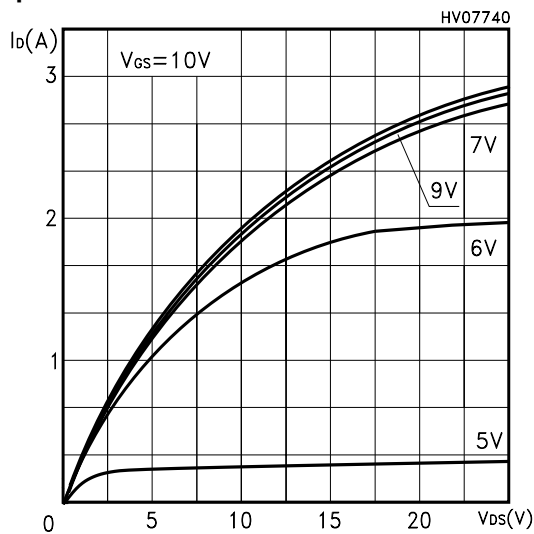
## Safe Operating Area For TO-92



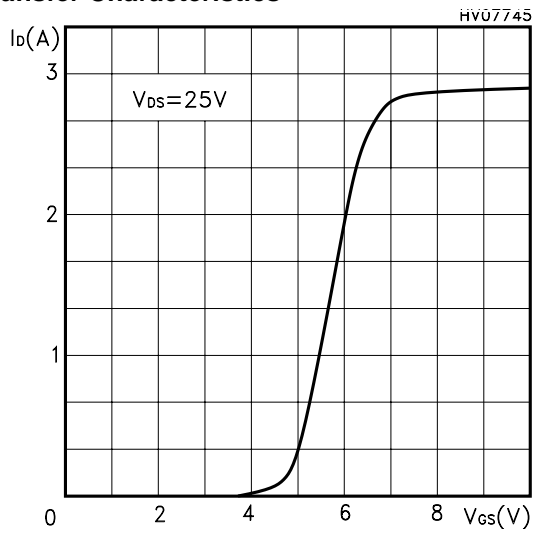
## Thermal Impedance For TO-92



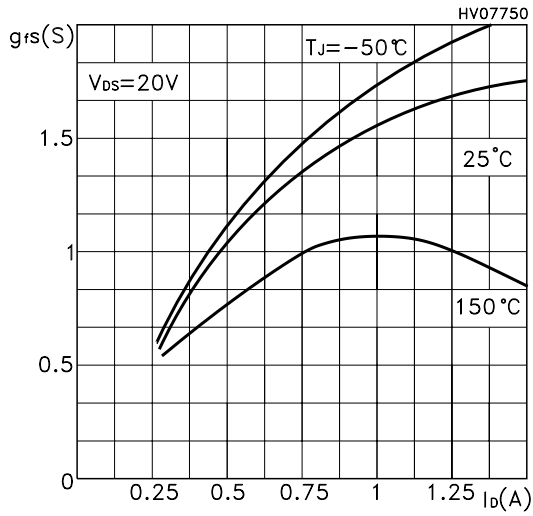
## Output Characteristics



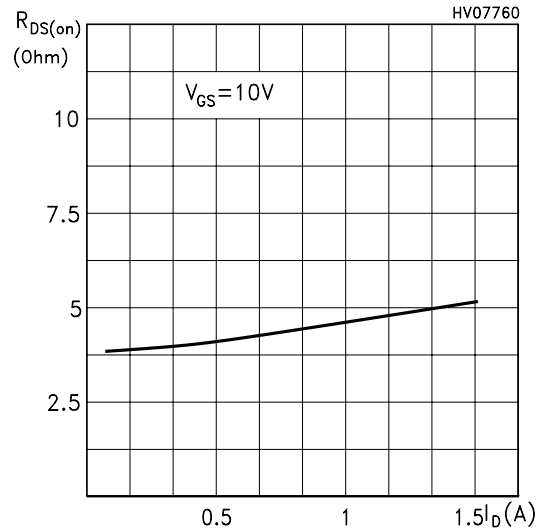
## Transfer Characteristics



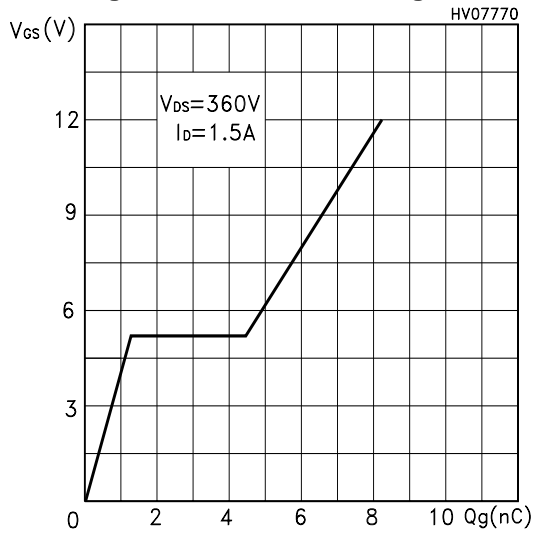
**Transconductance**



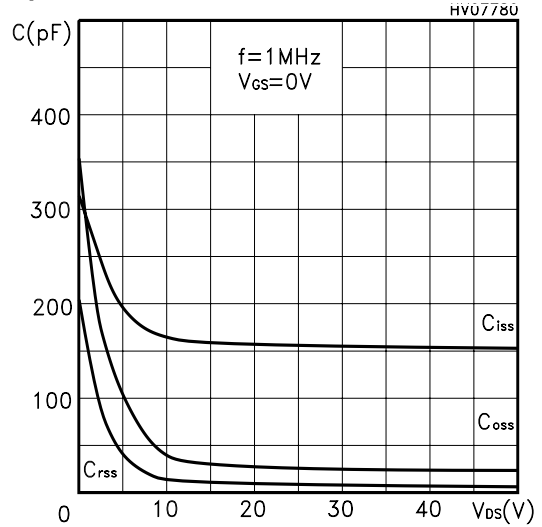
**Static Drain-source On Resistance**



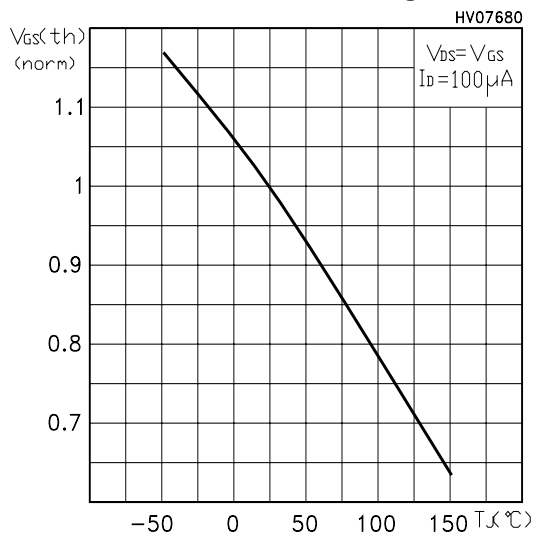
**Gate Charge vs Gate-source Voltage**



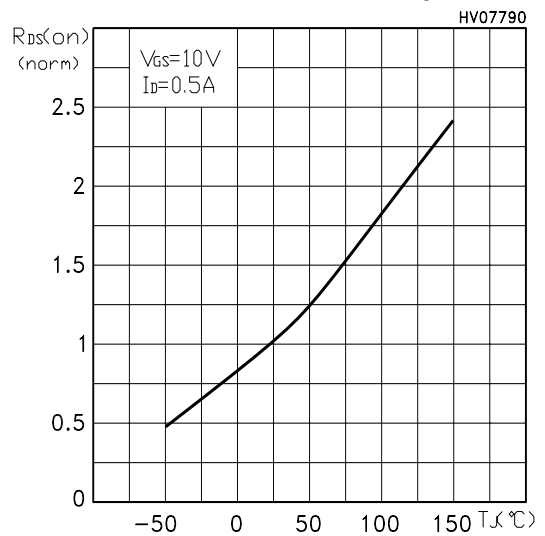
**Capacitance Variations**



**Normalized Gate Threshold Voltage vs Temp.**

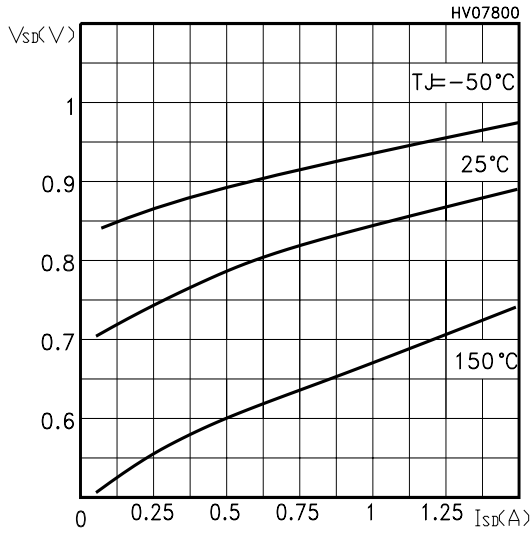


**Normalized On Resistance vs Temperature**

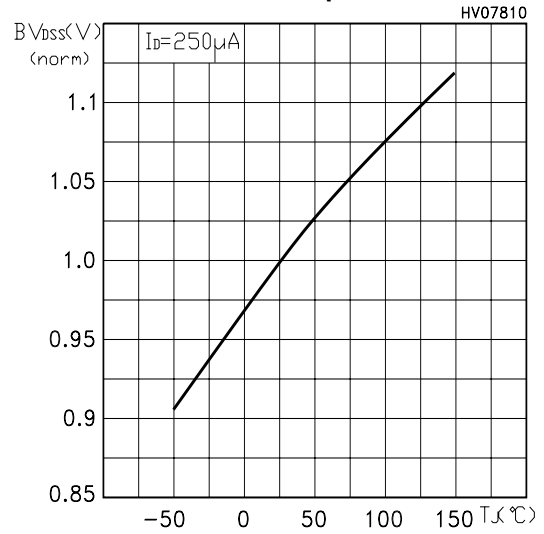


**STD2NC45-1, STQ1NC45**

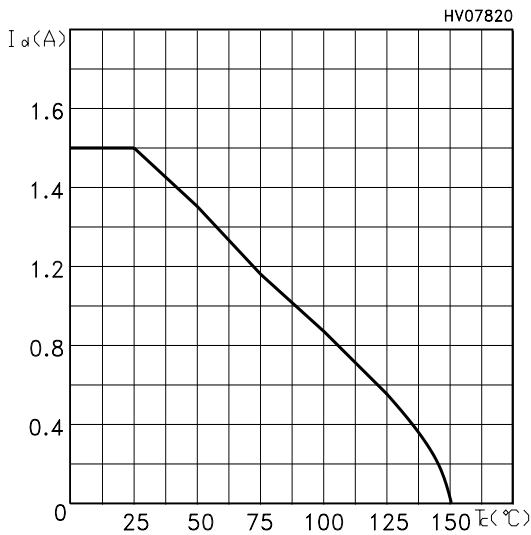
**Source-drain Diode Forward Characteristics**



**Normalized BVDSS vs Temperature**



**Max Id Current vs Tc**



**Maximum Avalanche Energy vs Temperature**

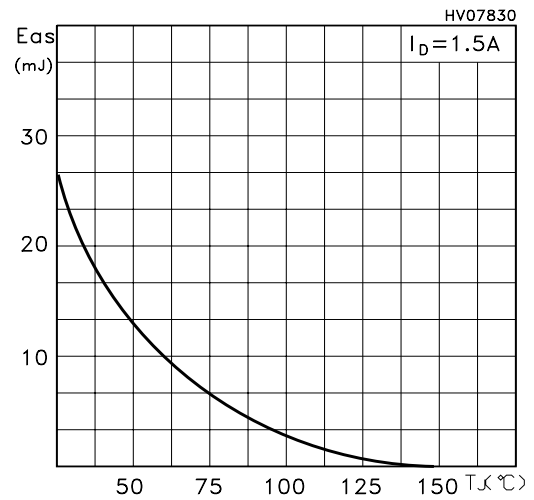


Fig. 1: Unclamped Inductive Load Test Circuit

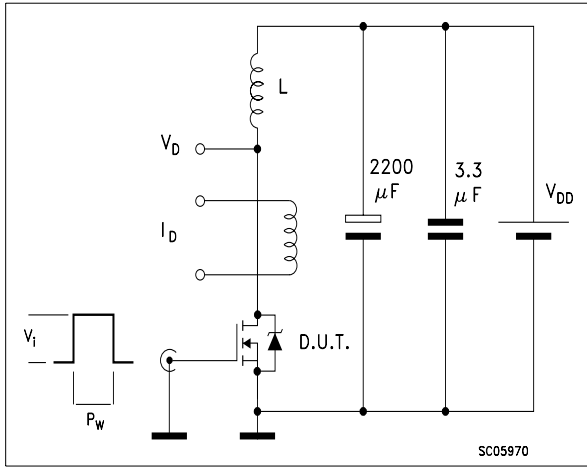


Fig. 2: Unclamped Inductive Waveform

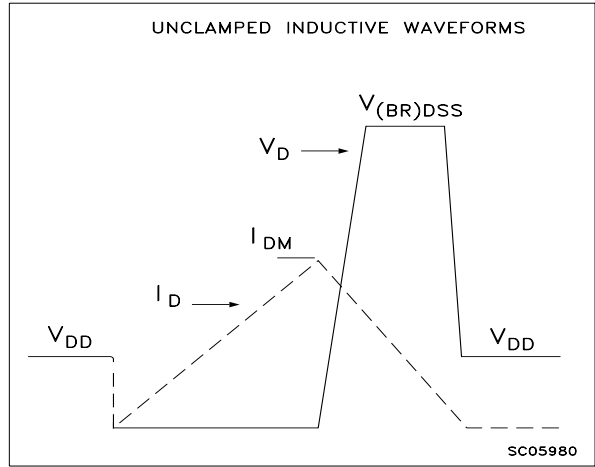


Fig. 3: Switching Times Test Circuit For Resistive Load

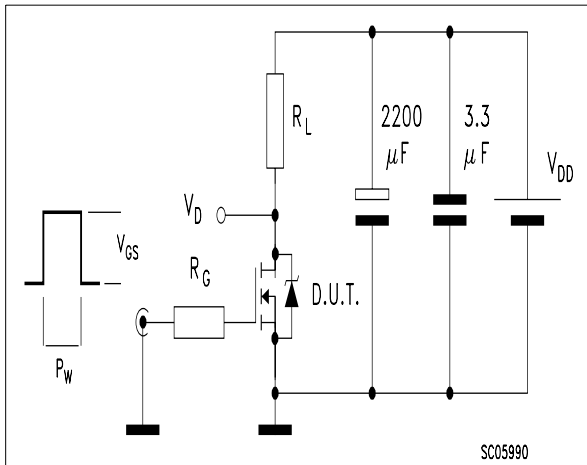


Fig. 4: Gate Charge test Circuit

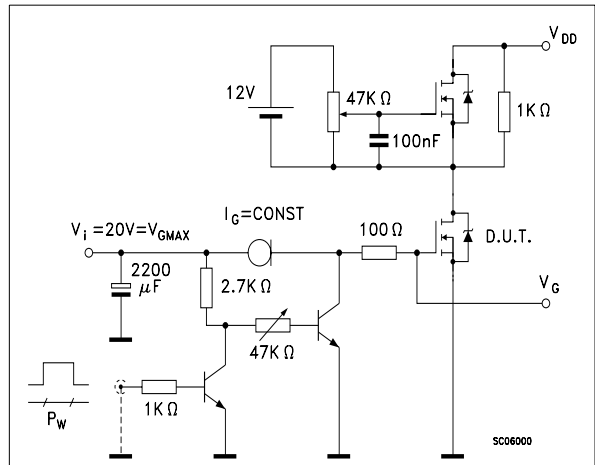
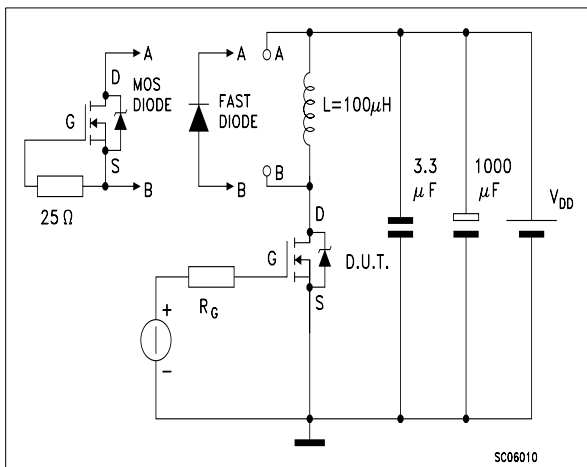


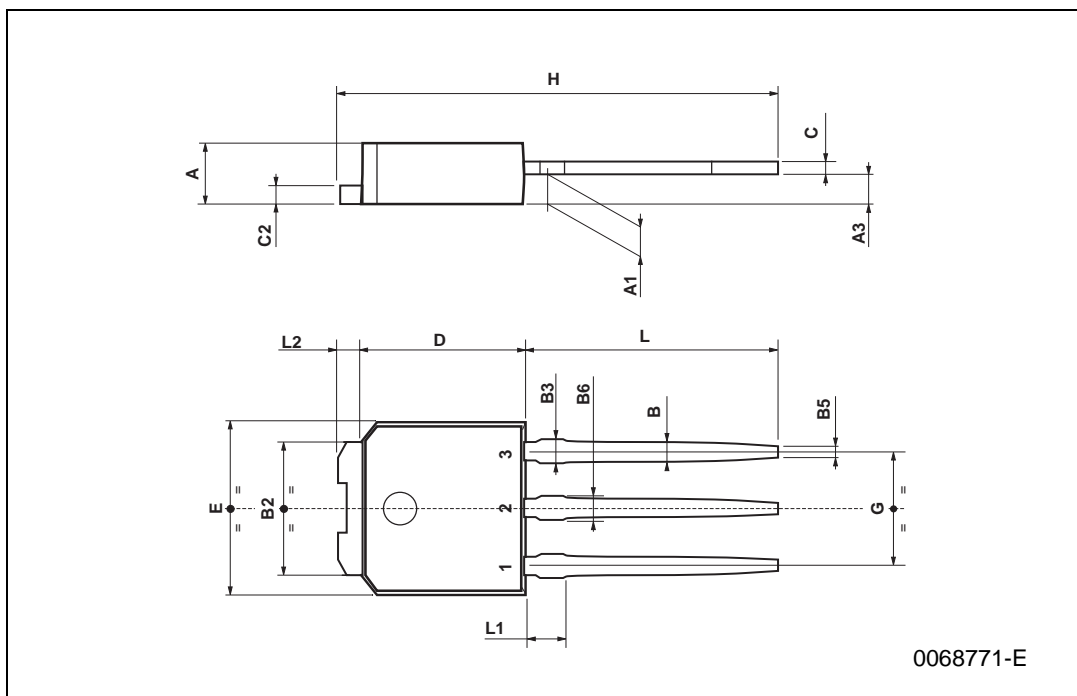
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



**STD2NC45-1, STQ1NC45**

**TO-251 (IPAK) MECHANICAL DATA**

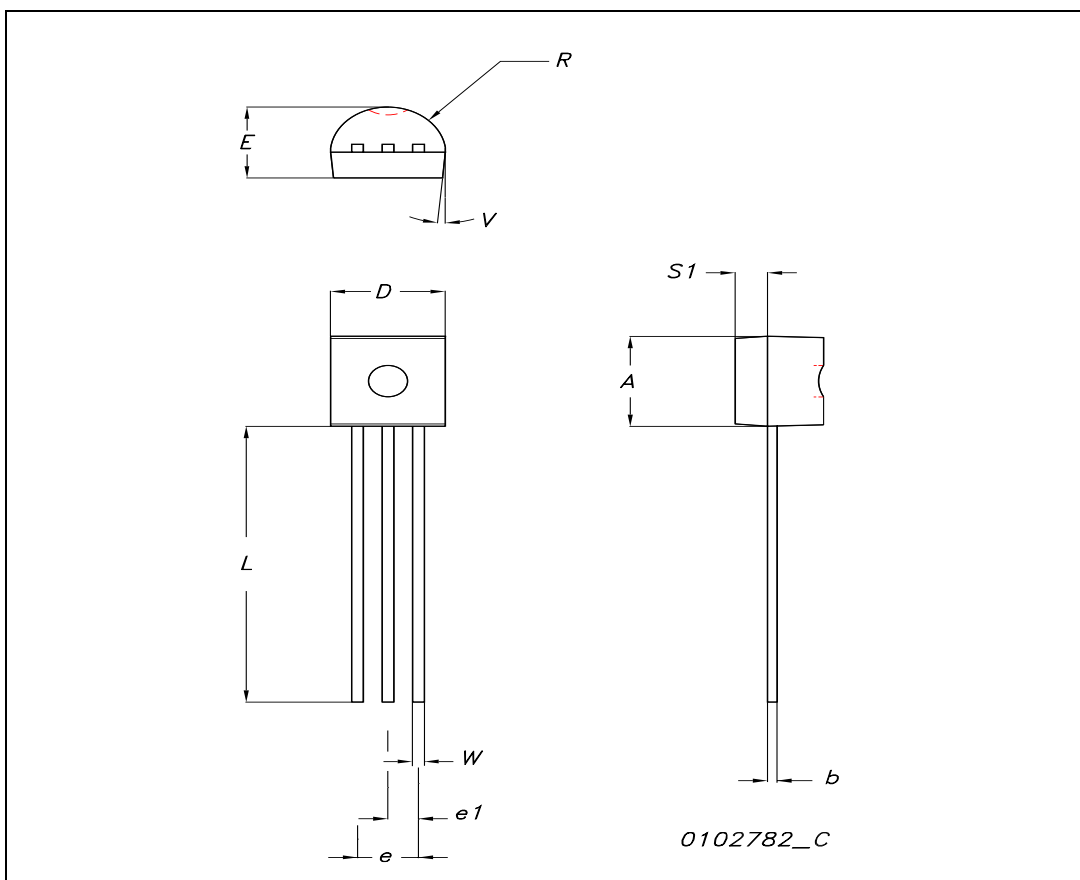
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039





**TO-92 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



**STD2NC45-1, STQ1NC45**

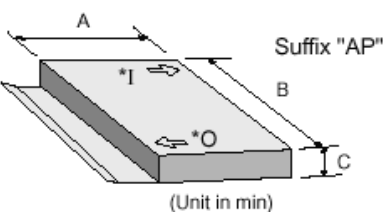
**SHIPPING METHODS**

**TO-92 AMMOPACK (suffix"-AP")**

One row consists of 25 elements



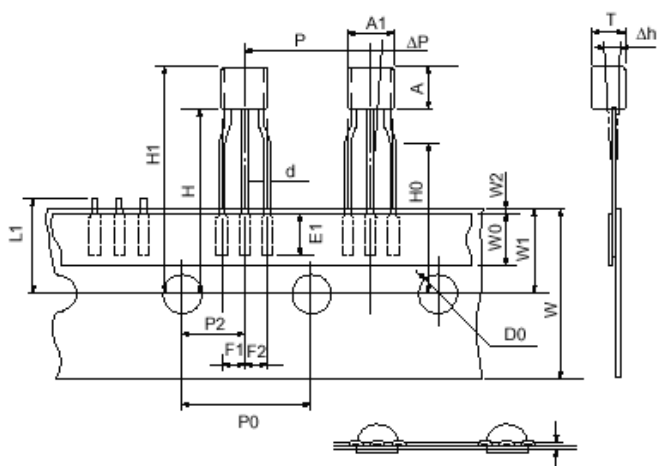
Remove more than 4 elements



(Unit in min)

\* shows a first-out electrode of a lead.  
O: Output first-out  
I: Input first-out

DIM	mm	
	Min.	Max.
A	3	250
B	3	330
C	3	45



TAPING IN FORWARD DIRECTION

BOTTOM VIEW

DIM	mm	
	Min.	Max.
A1	-	5
A	-	5
T	-	4
d	-	0.45
E1	2.5	-
P	11.7	13.7
P0	12.4	13
Hole Center to Device Center	5.95	6.75
F1/F2	2.4	2.8
Δh	-1	1
ΔP	-1	1
W	17.5	19
W0	5.7	6.3
W1	8.5	9.75
W2	-	0.5
H	-	20
H0	15.5	16.5
H1	-	25
D0	3.8	4.2
t	0.4	0.8
L1	-	11

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