

Flip-flop

54F112

DESCRIPTION

The 54F112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set (S_D) and Reset (R_D) inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A High level on the Clock (CP) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the CP is High and the flip-flop will perform according to Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of CP .

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F112/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F112/BFA	GDFP2-F16
20-Pin Ceramic LLCC	54F112/B2A	CQCC2-N20

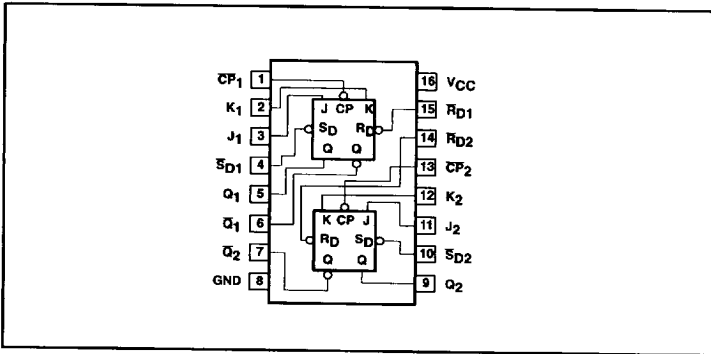
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

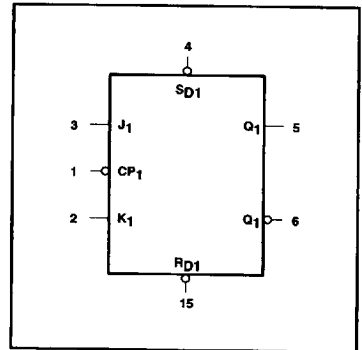
PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20 μ A/0.6mA
CP_1, CP_2	Clock pulse inputs (active falling edge)	1.0/4.0	20 μ A/2.4mA
R_{D1}, R_{D2}	Reset input (active Low)	1.0/5	20 μ A/3.0mA
S_{D1}, S_{D2}	Set input (active Low)	1.0/5	20 μ A/3.0mA
$Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as; 20 μ A in the High state and 0.6mA in the Low state.

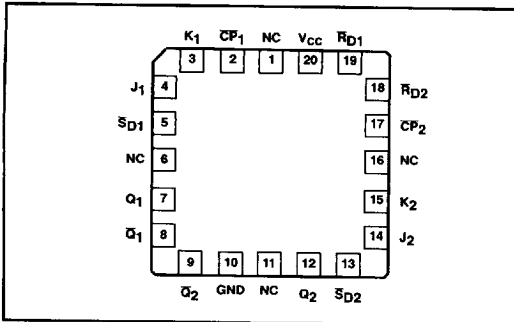
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION

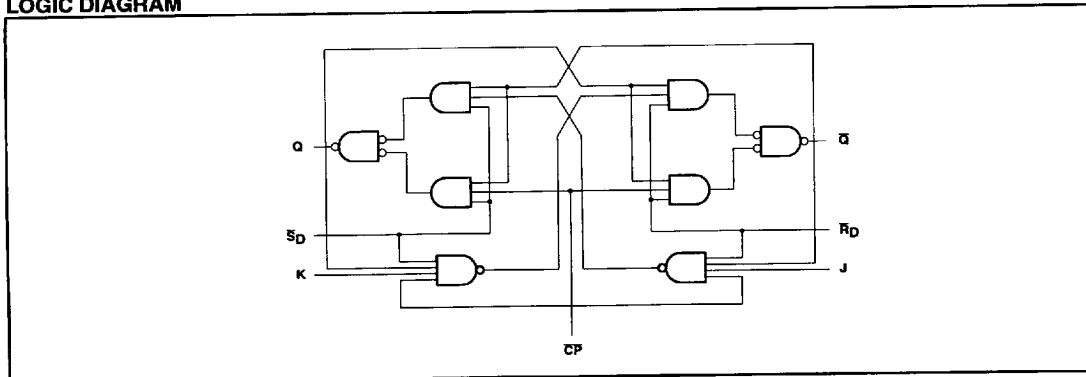


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LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\overline{S}_D	\overline{R}_D	\overline{CP}	J	K	Q	\overline{Q}
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	H	H	\overline{q}	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	\overline{q}

NOTE:

Both outputs will be High while both \overline{S}_D and \overline{R}_D are Low, but the output states are unpredictable if \overline{S}_D and \overline{R}_D go High simultaneously.

H = High voltage level steady state

h = High voltage level one setup time prior to the High-to-Low Clock transition

L = Low voltage level steady state

l = Low voltage level one setup time prior to the High-to-Low Clock transition

q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_i	Input voltage range	-0.5 to +7.0	V
I_i	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to + V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1.0	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min		0.35	0.50	V
V _{IK}	Low-level output voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max, V _I = 7.0V	J _n , K _n		100	μA
			R _{Dn} , S _{Dn}		100	μA
			CP _n		100	μA
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V	J _n , K _n		20	μA
			R _{Dn} , S _{Dn}		20	μA
			CP _n		20	μA
I _{IL}	Low-level input current	V _{CC} = Max, V _I = 0.5V	J _n , K _n		-0.6	mA
			R _{Dn} , S _{Dn}		-3.0	mA
			CP _n		-2.4	mA
I _{OS}	Short-circuit output current ³	V _{CC} = Max	-60		-150	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		12	19	mA

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _A = +25°C			T _A = -55°C to +125°C			
			Min	Typ	Max	Min	Max		
t _s (H)	Setup time, High or Low J _n or K _n to CP _n	Waveform 1	V _{CC} = +5.0V			V _{CC} = +5.0V ± 10%			ns
t _s (L)			C _L = 50pF, R _L = 500Ω			C _L = 50pF, R _L = 500Ω			
t _h (H)	Hold time, High or Low J _n or K _n to CP _n	Waveform 1	4.0			5.0			ns
t _h (L)			3.5			4.0			
t _w (H)	CP _n pulse width	Waveform 1	0.0			0.0			ns
t _w (L)			0.0			0.0			
t _w (H)	RD _n or SD _n pulse width	Waveform 1	4.5			5.0			ns
t _w (L)			4.5			5.0			
t _w (L)	Recovery time SD _n or RD _n to CP _n	Waveform 2	4.5			5.0			ns
t _{rec}			4.0			5.0			

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}, R_L = 500\Omega$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	90	130		90^5		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, \bar{Q}_n	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	ns ns
t_{PHL}	Propagation delay \bar{S}_{Dn} or \bar{R}_{Dn} to Q_n, \bar{Q}_n	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns ns

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- With the Clock input grounded and all outputs open I_{CC} is measured with the Q and \bar{Q} outputs High in turn.
- Parameter guaranteed, but not tested.

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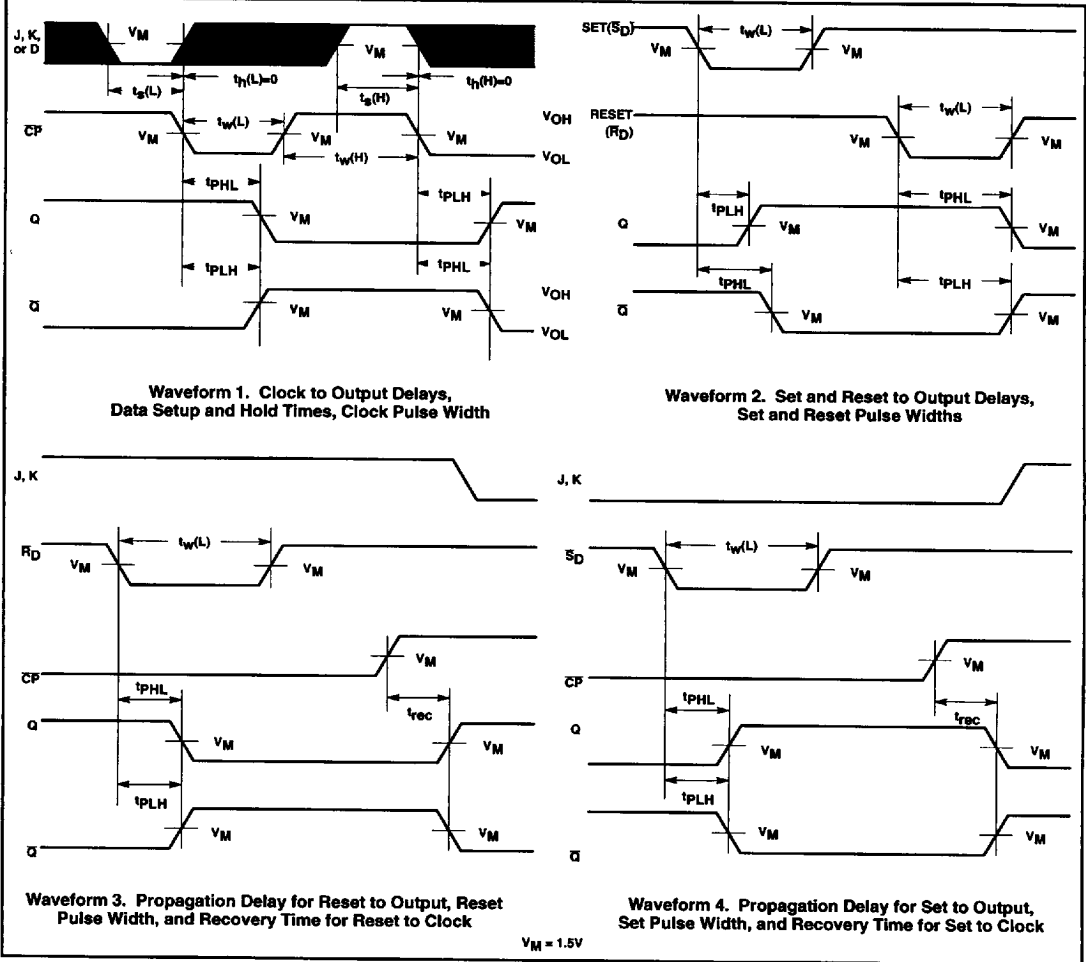
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AC WAVEFORMS



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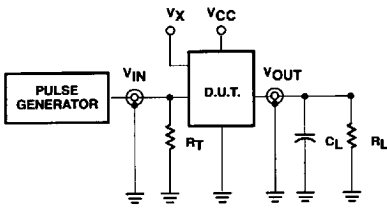
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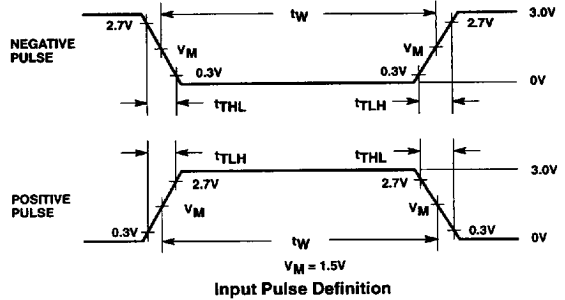
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TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unclocked pins must be held at: $\leq 0.8V$; $\geq 2.7V$ or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$

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