SG1010 Data Sheet

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Contact Information

1 Introduction

The StarGen SG1010 StarSwitch facilitates the design of high-performance and reliable StarFabric based switching systems. System designers can develop high performance systems that deliver voice, video, and data. A single-chip solution, the SG1010 offers six 2.5Gbps full duplex serial links, which deliver 30Gbps of aggregate, non-blocking, full duplex switching capacity.

Along with its high performance, the SG1010 can handle content-rich traffic through its extensive functionality and Quality of Service (QOS) support. The SG1010 supports 4 classes of service along with three routing methods providing added flexibility. The SG1010 is designed to work with other StarFabric devices and supports bridge products that employ protocols such as PCI and H.110. System designers can build system architectures that easily combine control, voice, cell and packet data.

The SG1010 allows PCI based designs to be easily migrated to StarFabric, yet maintain their investments in software and applications. The SG1010 supports two addressing models – a StarFabric address model and a PCI address model. In the StarFabric address model, the SG1010 switches path-routed and multicast frames. To support the PCI address model, the SG1010 appears as a PCI-to-PCI bridge to PCI configuration software. The SG1010 includes a PCI-compliant type1 header for 100% compatibility with existing PCI BIOS, drivers, application SW, and operating systems.

Designers don't have to deal with significant physical interface issues, which minimizes time-to-market. The SG1010 utilizes 622Mbps low voltage differential signaling (LVDS), a technology that is widely applied and thoroughly understood by industry professionals. Four transmit and receive differential pairs create a single 2.5Gbps full duplex link with 5Gbps of total bandwidth. StarFabric designs can span from chip-to-chip to room area networks. Inexpensive twisted pair copper cable can yield distances greater than 10 meters.

The SG1010 allows system designers to cost effectively engineer highly reliable and available systems. SG1010 system designs can include redundant data paths, so if a particular path fails, traffic can be rerouted over an alternate path. The SG1010 supports detection and notification of link status changes, as well as Hot-pluggable links. Path notification messages alerts operations personnel to replace faulty components and through hot swap, the offending boards can be replaced without affecting the rest of the

system. The 2.5 Gbps links also tolerate failure of up to three of the four differential pairs in a link. The re-striping of data is done automatically in silicon when differential pairs fail.

By combining the SG1010 with other StarFabric Devices, new multi-protocol, highly reliable, high performance systems can be acheived. The SG1010 offers a comprehensive solution, which includes silicon, software, and platforms to help achieve faster time-to- market.

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Features

2.1 Scalability and Performance

- 6 fabric links, 2.5 Gbps, full duplex
- 30 Gbps switching capacity
- Design limits head-of-line blocking
- Credit-based flow control

2.2 Compatibility

- Support for routing methods including PC compatible address routing
- Flexible Addressing Capability
- Physical layer interface is compliant with the IEEE 1596.3 and TIA/EIA-644 Low-Voltage Differential Signaling (LVDS) standards.

2.3 Quality of Service

- Specific credits for next-turn and class-of-service
- Separate buffering for Asynchronous, Isochronous, Multicast, and High Priority traffic classes.
- Path routing
- Multicast routing
- Dynamic bandwidth reservation protocol

2.4 Reliability, Availability, Serviceability features

- Link-by-link CRC checking on all traffic
- Redundant path routing capability
- Hot-pluggable links

2.5 Additional features

- IEEE standard 1149.1 JTAG interface

- Eight general-purpose I/O pins with accessible registers
- LED indicators for each differential pair

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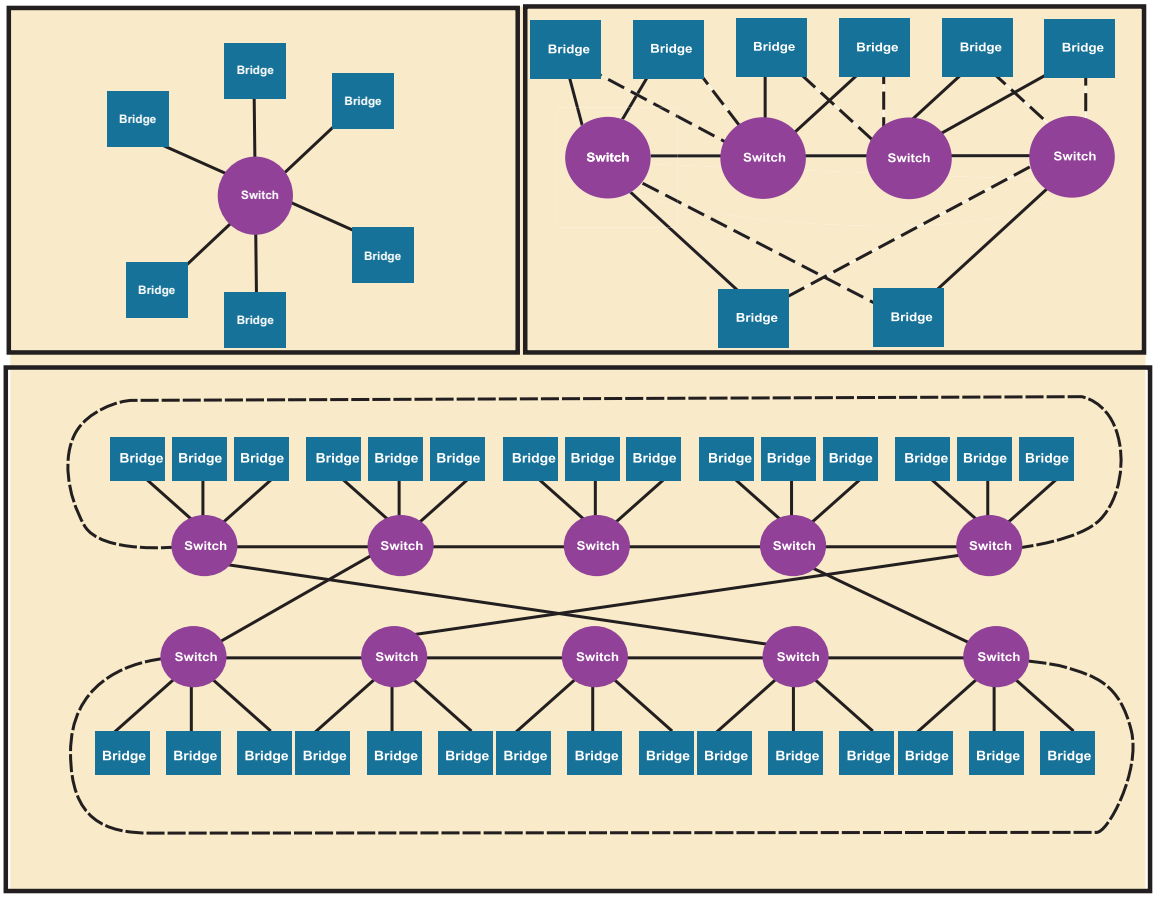
StarFabric Features

3.1 Scalability



The SG1010 switch has 30Gbps of switching capacity. When cascaded, the device enables systems to scale to gigabytes per second of capacity. The initial physical layer implemented provides 2.5 Gbps full-duplex bandwidth per link. Two links can be aggregated to create a ‘fat pipe’ with double the bandwidth. The links are well suited for chip-to-chip, backplane, and rack-to-rack interconnect. Using standard category 5 unshielded copper cables the links can extend to over 10 meters in length enabling the creation of room scale equipment.

3.2 Compenent Types

The two component types in StarFabric are edge nodes and switches. Swithes forward traffic through the StarFabric. Edge nodes provide the connection between the fabric and other protocols or devices. Bridges are edge nodes that translate other protocols (e.g., PCI, H.110) into serial StarFabric traffic. An edge node is further classified into either a root or a leaf. The root initiates fabric resets and enumeration.

3.3 Routing Methods

- Address Routing
  - Provides full compatibility with standards like PCI, Path and Multicast routing
- Path and Multicast routing
  - Provides Quality of service, reliability, and high availability

3.4 Traffic Classes

StarFabric supports 7 traffic classes. The initial parts support 4 traffic classes.

- Asynchronous / address routed class
- Isochronous Class
- Multicast Class
- High Priority Class

3.5 Fault Tolerant Strategies

- Parallel Fabrics
  - A second fabric provides redundancy. Redundant switches are used so that any switch may fail, yet end nodes remain connected. If a particular path fails, packets can be re-routed by silicon or software over the remaining functional paths.
- Fragile links
  - Automatic re stripping of data over functioning differential pairs in a link when one to three pairs fail.

3.6 Flow Control

Line credits manage flow control. Line credits are counters used to track available buffer storage between link partners. Each transmission point in the fabric has buffers for each class of traffic for each outgoing port. Traffic is sent only when the source has line credits for the output buffer on the next node for an entire frame. A switch is non-blocking because edge node congestion does not impact traffic flow to any other edge node or even to the same edge node in a different class of service. Line credits are used when a node sends a frame and restored when the node's link partner forwards the frame.

3.7 Bandwidth Reservation

Isochronous and multicast transmissions can use bandwidth reservation to allocate anticipated bandwidth requirements prior to starting data transfer. Bandwidth reservation is fully distributed and is initiated at the origin of the traffic.

3.8 Usage Models

Current StarFabric components support 3 usage models, PCI legacy, Fabric-native, and mixed legacy / Fabric-native. PCI legacy enables use of existing PCI drivers and initialization software with no modification. the interconnect looks like a collection of PCI-to-PCI bridges. This usage model amounts to a plug-and-play mode that extends the capabilities of existing systems.

The Fabric-native usage unleashes some of the StarFabric's advanced features such as path routing, class of service, bandwidth selection, redundancy for fail-over path routing, and channels. Fabric-native use also provides the isolation and mechanisms required for inter-processor communication. This enables distributed computing applications. It is possible to use a mixture of legacy and fabric-native capabilities. Developers can start with legacy and add enhanced fabric- native capability over time.

To use advanced features, some degree of software investment is necessary. StarGen provides software tools to take advantage of StarFabric's advanced features. Sample software includes enumeration and routing, bandwidth reservation, as well as routines for optimizing performance, API integration layers, BIOS/initial setup, and generating statistics. StarGen supplies tools and utilites for ROM programming, fabric access tools, and Fabric topology viewers.

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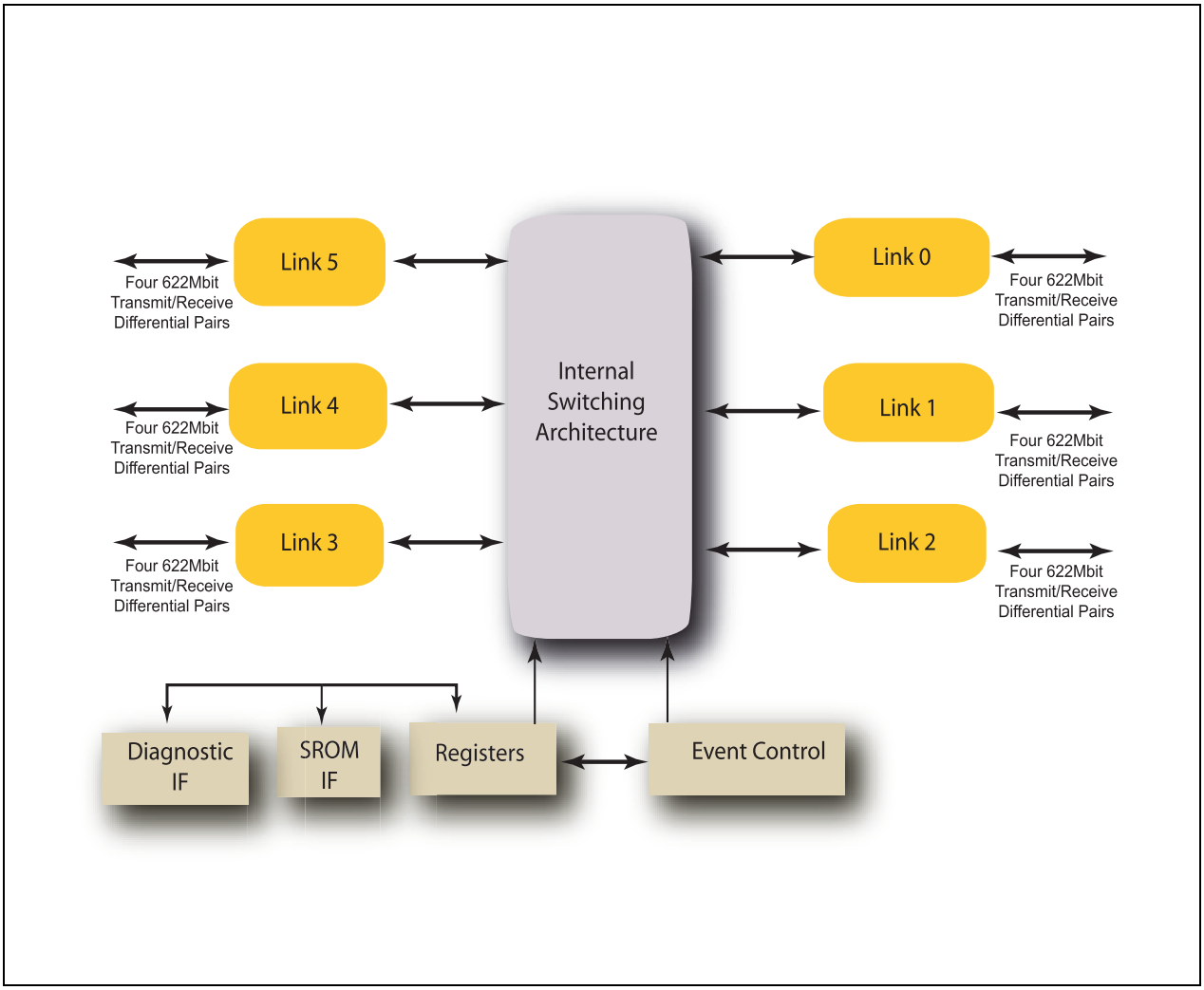
4 Specifications

4.1 Block Diagram



4.2 Package Diagram

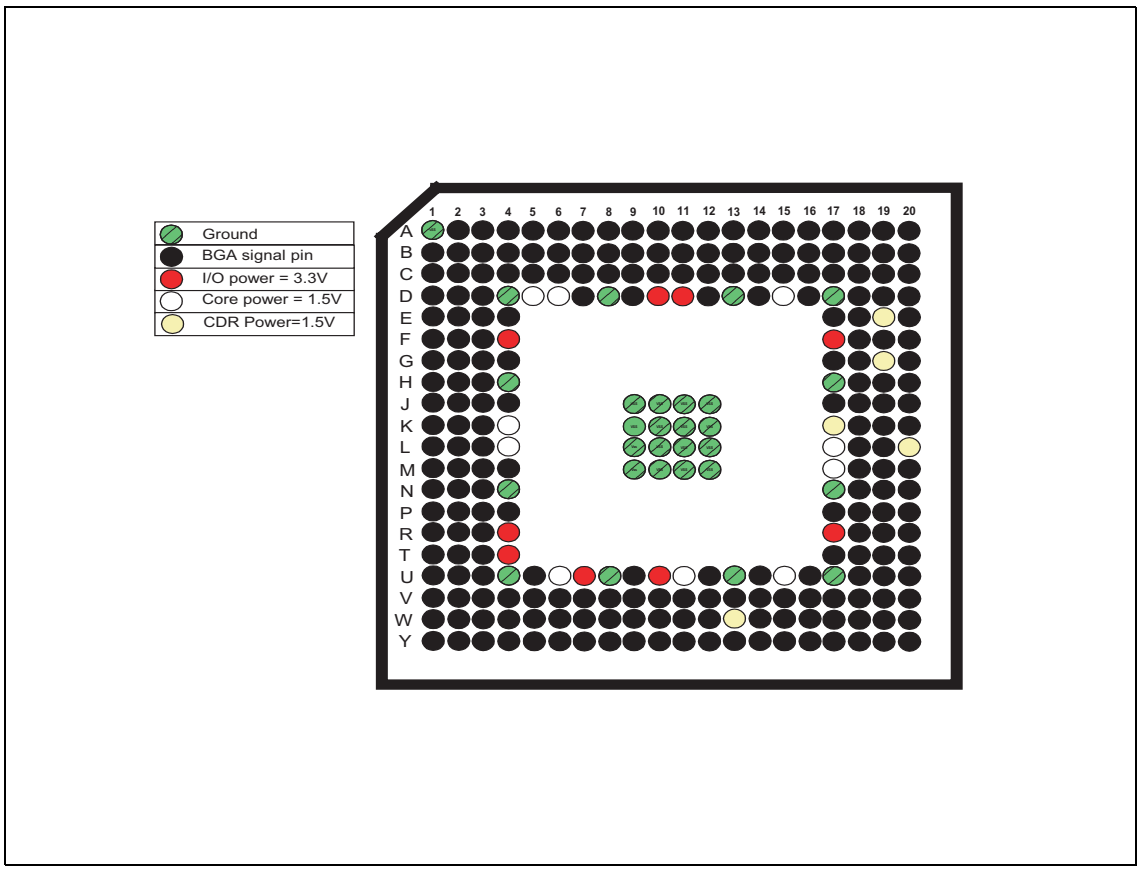
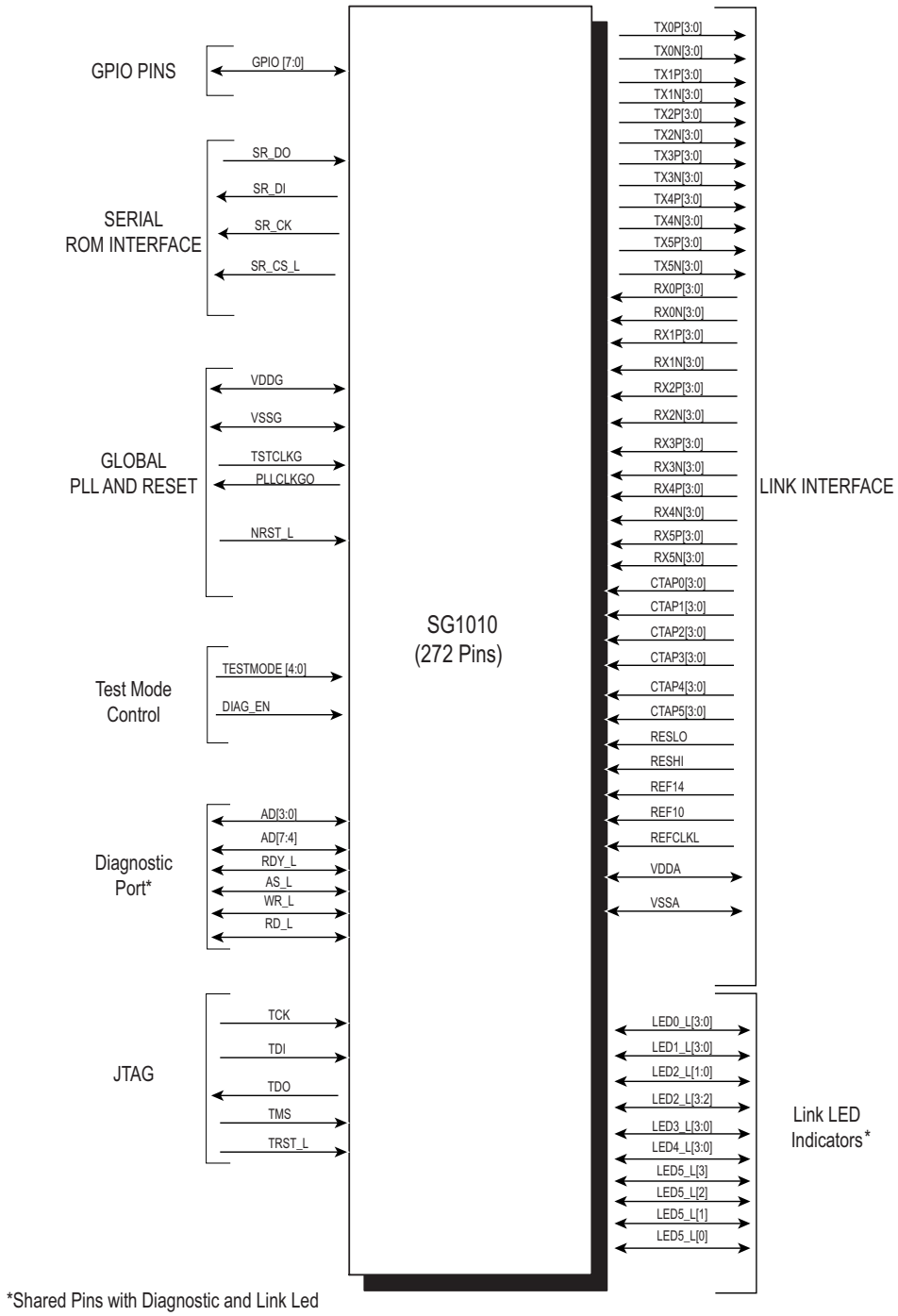


Figure 4–1 Top View Package Diagram

4.3 Pinout Diagram



*Shared Pins with Diagnostic and Link Led

4.4 Pin List By Location

Table 4–1 Pin by Location

Pin	Signal Name	Type
B1	tx1p[0]	O
C2	tx1n[0]	O
D2	tx1p[1]	O
D3	tx1n[1]	O
E4	tx1p[2]	O
E3	tx1n[2]	O
D1	tx1p[3]	O
C1	tx1n[3]	O
E2	tx0p[0]	O
E1	tx0n[0]	O
F3	tx0p[1]	O
G4	tx0n[1]	O
F2	tx0p[2]	O
F1	tx0n[2]	O
G3	tx0p[3]	O
G2	tx0n[3]	O
G1	tx5p[0]	O
H3	tx5n[0]	O
H2	tx5p[1]	O
H1	tx5n[1]	O
J4	tx5p[2]	O
J3	tx5n[2]	O
J2	tx5p[3]	O
J1	tx5n[3]	O
K2	reserved[0]	IO
K3	reserved[1]	IO
K1	reserved[2]	IO
L1	reserved[3]	IO
L2	reserved[4]	IO
L3	reserved[5]	IO
M1	reserved[6]	IO
M2	reserved[7]	IO
M3	reserved[8]	IO
M4	reserved[9]	IO
N1	reserved[10]	IO
N2	reserved[11]	IO

Table 4–1 Pin by Location

Pin	Signal Name	Type
N3	reserved[12]	IO
P1	reserved[13]	IO
P2	reserved[14]	IO
R1	reserved[15]	IO
P3	reserved[16]	IO
R2	reserved[17]	IO
T1	reserved[18]	IO
P4	diag_en	I
R3	testmode[4]	I
T2	tck	I
U1	trst_l	I
T3	tms	I
U2	tdo	O
V1	tdi	I
U3	scan_ena	I
V2	spare	I
W1	scan_out[0]	IO
V3	scan_out[1]	IO
W2	scan_out[2]	IO
Y1	scan_out[3]	IO
W3	scan_out[4]	IO
Y2	scan_out[5]	IO
W4	scan_out[6]	IO
V4	scan_out[7]	IO
U5	testmode[3]	I
Y3	testmode[2]	I
Y4	testmode[1]	I
V5	testmode[0]	I
W5	sr_cs_l	IO
Y5	sr_ck	IO
V6	sr_di	IO
W6	sr_do	I
Y6	gpio[7]	IO
V7	gpio[6]	IO
W7	gpio[5]	IO
Y7	gpio[4]	IO
V8	gpio[3]	IO
W8	gpio[2]	IO

Table 4–1 Pin by Location

Pin	Signal Name	Type
Y8	gpio[1]	IO
U9	gpio[0]	IO
V9	nrst_l	I
W9	tstclkg	I
Y9	pllclkgo	O
W10	led5_l[3]	IO
V10	led5_l[2]	IO
Y10	led5_l[1]	IO
Y11	led5_l[0]	IO
W11	led4_l[3]	IO
V11	led4_l[2]	IO
Y12	led4_l[1]	IO
W12	led4_l[0]	IO
V12	led3_l[3]	IO
U12	led3_l[2]	IO
Y13	led3_l[1]	IO
Y14	led3_l[0]	IO
W14	led2_l[3]	IO
Y15	led2_l[2]	IO
V14	led2_l[1]	IO
W15	led2_l[0]	IO
Y16	led1_l[3]	IO
U14	led1_l[2]	IO
V15	led1_l[1]	IO
W16	led1_l[0]	IO
Y17	led0_l[3]	IO
V16	led0_l[2]	IO
W17	led0_l[1]	IO
Y18	led0_l[0]	IO
U16	tstshftld	I
V17	ecsel	I
W18	etoggle	I
Y19	exdnup	I
V18	tstphase	I
W19	resettx	I
Y20	loopbken	I
W20	testrst	I
V19	bypassl	I

Table 4–1 Pin by Location

Pin	Signal Name	Type
U19	tstclkl	I
U18	refclkl	I
T17	ctap5[0]	I
V20	rx5p[0]	I
U20	rx5n[0]	I
T18	rx5p[1]	I
T19	rx5n[1]	I
T20	ctap5[1]	I
R18	rx5p[2]	I
P17	rx5n[2]	I
R19	ctap5[2]	I
R20	ctap5[3]	I
P18	rx5p[3]	I
P19	rx5n[3]	I
P20	ctap0[0]	I
N18	rx0p[0]	I
N19	rx0n[0]	I
N20	ctap0[1]	I
M18	rx0p[1]	I
M19	rx0n[1]	I
M20	rx0p[2]	I
L19	rx0n[2]	I
L18	ctap0[2]	I
K19	rx0p[3]	I
K18	rx0n[3]	I
J19	ctap0[3]	I
J18	rx1p[0]	I
J17	rx1n[0]	I
H20	ctap1[0]	I
H19	rx1p[1]	I
H18	rx1n[1]	I
G20	ctap1[1]	I
G18	rx1p[2]	I
F19	rx1n[2]	I
E20	ctap1[2]	I
G17	rx1p[3]	I
F18	rx1n[3]	I
E18	ctap1[3]	I

Table 4–1 Pin by Location

Pin	Signal Name	Type
D19	rx2p[0]	I
C20	rx2n[0]	I
E17	ctap2[0]	I
D18	rx2p[1]	I
C19	rx2n[1]	I
B20	ctap2[1]	I
C18	rx2p[2]	I
B19	rx2n[2]	I
A20	ctap2[2]	I
A19	rx2p[3]	I
B18	rx2n[3]	I
B17	ctap2[3]	I
C17	rx3p[0]	I
D16	rx3n[0]	I
A18	ctap3[0]	I
A17	rx3p[1]	I
C16	rx3n[1]	I
B16	ctap3[1]	I
A16	ctap3[2]	I
C15	rx3p[2]	I
D14	rx3n[2]	I
B15	rx3p[3]	I
A15	rx3n[3]	I
C14	ctap3[3]	I
B14	rx4p[0]	I
A14	rx4n[0]	I
C13	ctap4[0]	I
B13	rx4p[1]	I
A13	rx4n[1]	I
D12	ctap4[1]	I
C12	rx4p[2]	I
B12	rx4n[2]	I
A12	ctap4[2]	I
B11	rx4p[3]	I
C11	rx4n[3]	I
A11	ctap4[3]	I
A10	tx4p[0]	O
B10	tx4n[0]	O

Table 4–1 Pin by Location

Pin	Signal Name	Type
C10	tx4p[1]	O
C9	tx4n[1]	O
B9	tx4p[2]	O
A9	tx4n[2]	O
D9	tx4p[3]	O
C8	tx4n[3]	O
B8	tx3p[0]	O
A8	tx3n[0]	O
A7	tx3p[1]	O
B7	tx3n[1]	O
B6	tx3p[2]	O
C7	tx3n[2]	O
A6	tx3p[3]	O
A5	tx3n[3]	O
D7	tx2p[0]	O
C6	tx2n[0]	O
B5	tx2p[1]	O
A4	tx2n[1]	O
C5	tx2p[2]	O
B4	tx2n[2]	O
A3	tx2p[3]	O
B3	tx2n[3]	O
C4	reslo	I
B2	reshi	I
A2	ref14	I
C3	ref10	I

4.5 Power Pins

Table 4–2 Power Pins

Description	Pins
Ground	A1,D4,D8,D13,D17,H4,H17,J9,J10,J11,J12,K9,K10,K11,K12,L9,L11,L12 ,M9,M10,M11,M12,N4,N17,U4,U8,U13,U17
Vdd 3.3V	D11,F4,F17,R4,R17,U10,D10,T4,U7
Vdd 1.5V	D6,D15,K4,L17,U6,U15,D5,L4,M17,U11
Analog 1.5V	L20,G19,K17,E19,W13
Vssa	V13,K20,J20,D20,F20

4.6 Pin Descriptions

Table 4–3 Pin Descriptions

Pin	Description
SR_DO	SROM data out. Receives read data from the Serial Rom.
SR_DI	SROM data in. The SG1010 drives the SROM command, address, and write data on this signal
SR_CK	SROM clock input.
SR_CS_L	SROM chip select. The SG1010 drives this signal low at the beginning of an SROM operation; high at the end of the operation
VDDG	VDD for 112.5MHz phase-locked loop (PLL)
VSSG	VSS for 112.5MHz PLL
TSTCLKG	Bypass clock for 112.5 MHz PLL. Bypass mode is selected through TESTMODE [4:0] pins
PLLCLKGO	112.5MHz PLL output (used for test)
NRST_L	Chip reset pin
TX0P[3:0]	Link 0 LVDS transmit positive
TX0N[3:0]	Link 0 LVDS transmit negative
TX1P[3:0]	Link 1 LVDS transmit positive
TX1N[3:0]	Link 1 LVDS transmit negative
TX2P[3:0]	Link 2 LVDS transmit positive
TX2N[3:0]	Link 2 LVDS transmit negative
TX3P[3:0]	Link 3 LVDS transmit positive
TX3N[3:0]	Link 3 LVDS transmit negative
TX4P[3:0]	Link 4 LVDS transmit positive
TX4N[3:0]	Link 4 LVDS transmit negative
TX5P[3:0]	Link 5 LVDS transmit positive
TX5N[3:0]	Link 5 LVDS transmit negative
RX0P[3:0]	Link 0 LVDS receive positive
RX0N[3:0]	Link O LVDS receive negative
RX1P[3:0]	Link 1 LVDS receive positive
RX1N[3:0]	Link 1 LVDS receive negative
RX2P[3:0]	Link 2 LVDS receive positive
RX2N[3:0]	Link 2 LVDS receive negative
RX3P[3:0]	Link 3 LVDS receive positive
RX3N[3:0]	Link 3 LVDS receive negative
RX4P[3:0]	Link 4 LVDS receive positive
RX4N[3:0]	Link 4 LVDS receive negative
RX5P[3:0]	Link 5 LVDS receive positive
RX5N[3:0]	Link 5 LVDS receive negative
REFCLKL	Reference clock for CDR PLL

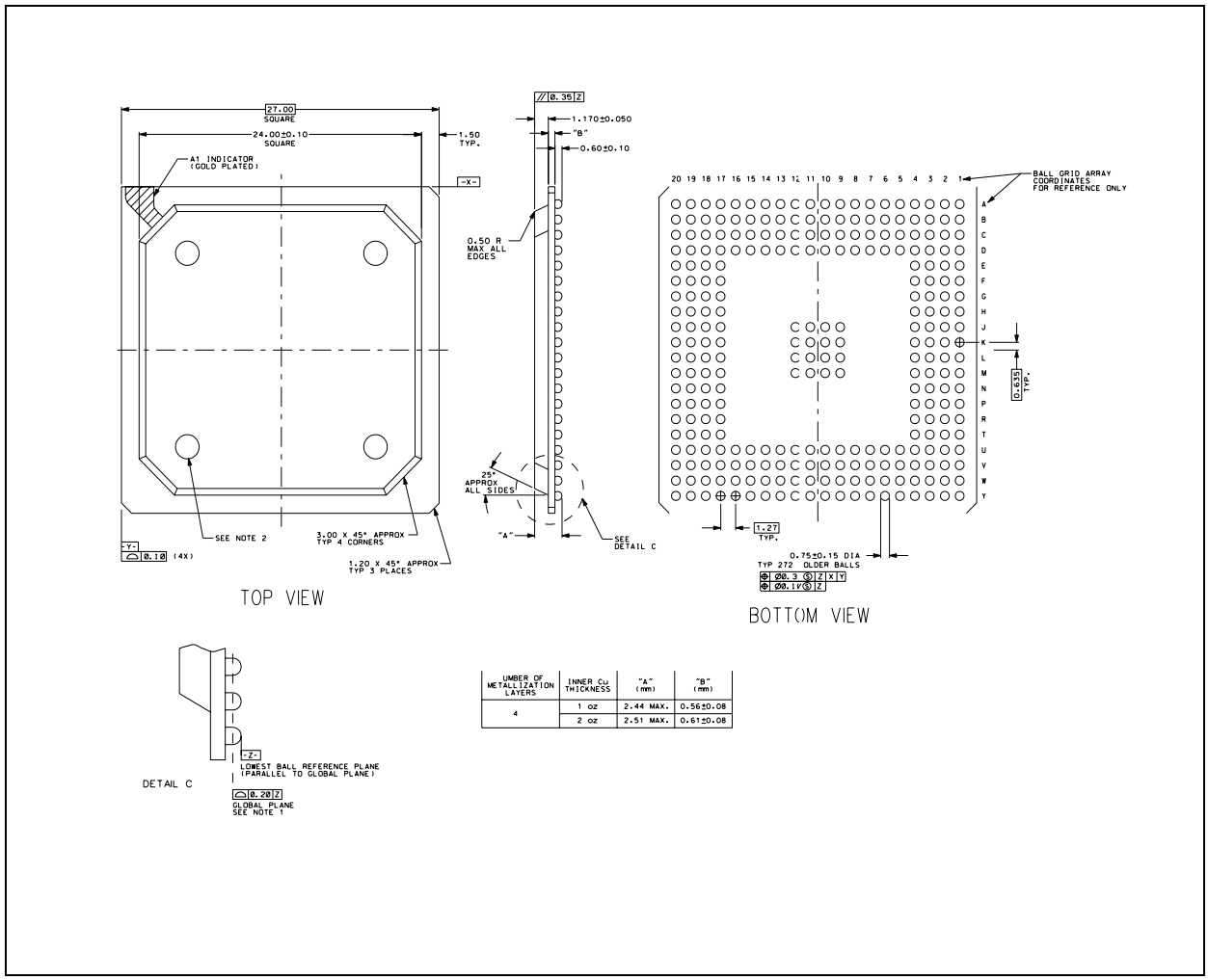
Table 4–3 Pin Descriptions

Pin	Description
CTAP0[3:0]	Link 5 LVDS center taps for external reference voltages
CTAP1[3:0]	Link 5 LVDS center taps for external reference voltages
CTAP2[3:0]	Link 5 LVDS center taps for external reference voltages
CTAP3[3:0]	Link 5 LVDS center taps for external reference voltages
CTAP4[3:0]	Link 5 LVDS center taps for external reference voltages
CTAP5[3:0]	Link 5 LVDS center taps for external reference voltages
RESLO	LVDS 100OHM reference low- connects to RESHI through 100OHM 1% resistor
RESHI	LVDS 100OHM reference high- connects to RESLO through 100 OHM 1% resistor
REF14	LVDS 1.4V reference
REF10	LVDS 1.0V reference
VDDA	Analog VDD for CDR PLL
VSSA	Analog VSS for CDR PLL
TSTCLKL	Manufacturing Test Pin
BYPASSL	Manufacturing Test Pin
RESETTX	Manufacturing Test Pin
TESTRST	Manufacturing Test Pin
TSTSHFTLD	Manufacturing Test Pin
ECSEL	Manufacturing Test Pin
ETOGGLE	Manufacturing Test Pin
EXDNUP	Manufacturing Test Pin
TSTPHASE	Manufacturing Test Pin
LOOPBKEN	Manufacturing Test Pin
TESTMODE[4:0]	Enables SG1010 functional/test
DIAG_EN	Diagnostic Port Enable
LED0_L[3:0]	Transmit state LEDs for link0
LED1_L[3:0]	Transmit state LEDs for link1
LED2_L[3:0]	Transmit state LEDs for link2
LED3_L[3:0]	Link 3 state LEDs
LED4_L[3:0]	Link 4 state LEDs
LED5_L[3:0]	Link 5 state LEDs
TCK	JTAG clock
TDI	JTAG data in
TDO	JTAG data out
TMS	JTAG mode select
TRST_L	JTAG reset
SCAN_ENA	Scan enable input
SCAN_OUT[7:0]	Scan chain outputs

Table 4–3 Pin Descriptions

Pin	Description
AD[7:0]	Diagnostic port AD[7:0]
RDY_L	Diagnostic Port Control Signal: Target Ready
AS_L	Diagnostic Port Control Signal: Address Strobe
WR_L	Diagnostic Port Control Signal: Write strobe
RD_L	Diagnostic Port Control Signal: read strobe

4.7 Package Specification



STARGEN 5

Electrical Specifications

5.1 Absolute Maximum Ratings

Table 5–1 Absolute Maximum Ratings

Junction Temperature	0 to 125 degrees C
Core Supply Voltage	1.5V +/-5%
I/O Supply Voltage	3.3V +/-5%
Storage Temperature	-55 to 125 degrees C
Operating Temperature	0 to 70 degrees C
Power dissipation	3W maximum

5.2 DC Specifications

Table 5–2 DC Specifications (non-LVDS signals)

Symbol	Parameter	Condition	Min	Max
V_{ih}	Input high voltage	–	$.5V_{cc}$	$.5V_{cc}+.5V$
V_{il}	Input low voltage	–	-0.5V	$.3V_{cc}$
V_{ipu}	Input Pull-up voltage	–	$.7V_{cc}$	–
V_{oh}	Output high voltage	I_{oh} = -500mA	$.9V_{cc}$	–
V_{ol}	Output low voltage	I_{ol} = 1500mA	–	$.1V_{cc}$
I_{in}	Input leakage current	$0 \leq V_{in} \leq V_{io}$	–	$\pm$ 10 µA
$I_{in\text{-}pme}$	PME_L input leakage	$V_o \leq 3.6V$ V_{cc} off	–	-1 mA
C_{in}	Pin capacitance	–	–	10 pF

5.3 Timing Specifications

5.3.1 Serial ROM Interface

Table 5–3 Serial ROM Interface AC Timing Specifications

Signal	Symbol	Parameter	Min	Max
SR_CLK	T_{scyc}	Cycle time	510ns	–
SR_CS_L	T_{scsl}	Minimum time low	56.5*T_{scyc}	–
SR_CS_L	T_{scssu}	Setup to SR_CLK rising	.5*T_{scyc}	–
SR_DO	T_{sdosu}	Setup to SR_CLK rising	30ns	–
SR_DO	T_{sdoh}	Hold from SR_CLK rising	30ns	–
SR_DI	$T_{sdivalb}$	Valid before SR_CLK rising	.5*T_{scyc}	–
SR_DI	$T_{sdivala}$	Valid from SR_CLK rising	.5*T_{scyc}	–

5.3.2 Global PLL Timing

Table 5–4 Global PLL and Reset AC Timing Specifications

Signal	Symbol	Parameter	Min	Max
REFCLKL	F_{xtal}	Frequency	62.208MHz - 20ppm	62.208MHz + 20ppm
REFCLKL	V_{refptp}	Peak-to-peak voltage		
REFCLKL		Slew rate	X V/ns	Y V/ns
REFCLKC		Duty Cycle		
NRST_L	T_{rstv}	Minimum assertion time after power stable	10μσεχ	

5.3.3 StarFabric Interface Timing

Table 5–5 LVDS StarFabric Interface AC Timing Specifications

Signal	Symbol	Parameter	Min	Max
TXnP, TXnN	T_{tdpsk}	Differential skew		50ps
TXnP, TXnN	T_{tppsk}	Pair to pair skew		200ps
TXnP, TXnN	T_{tdpr} (2)	Low to high time	100ps	210ps
TXnP, TXnN	T_{tdpf} (2)	High to low time	100ps	210ps
RXnP, RXnN	T_{rdpsk}	Differential skew		
RXnP, RXnN	T_{rppsk}	Pair to pair skew		2ns
RXnP, RXnN	T_{rdpr}	Low to high time		
RXnP, RXnN	T_{rdpf}	High to low time		
TXnP, TXnN, RXnP, RXnN	T_{dpfreq}	Maximum frequency		

(2) Test conditions: ZL=100Ω±1%, Cpad=3.0pF, Cpadn=3.0pF

5.3.4 Diagnostic Port Timing

Table 5–6 Diagnostic Port Read Operation Timing Diagram

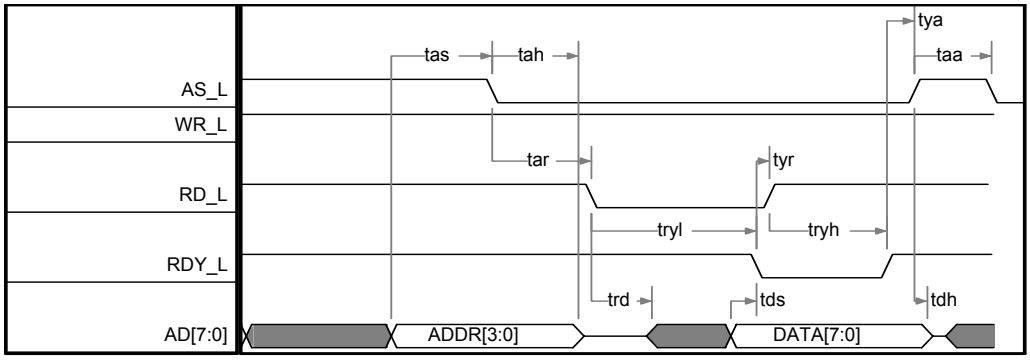


Table 5–7 Diagnostic Port Read Operation AC Timing

Signal	Symbol	Parameter	Min	Max
AD[3:0]	t_{as}	Setup time to AS_L asserted	13ns	–
AD[3:0]	t_{ah}	Hold time from AS_L asserted	23ns	–
RD_L	t_{ar}	Delay from AS_L asserted	23ns	–
AD	t_{rd}	Delay from RD_L asserted to driven	40ns	55ns
RDY_L	t_{ryl}	Delay from RD_L assertion	0ns	infinite
RD_L	t_{yr}	Delay from RDY_L assertion	0ns	–
AS_L	t_{ya}	Delay from RDY_L assertion	40ns	–
AD[7:0]	t_{ds}	Setup time to RDY_L assertion	0ns	–
AD[7:0]	t_{dh}	Hold time from AS_L deassertion	40ns	55ns
AS_L	t_{aa}	Minimu deassertion time	23ns	–
RDY_L	t_{ryh}	Delay from RD_L deassertion	40ns	55ns

Table 5–8 Diagnostic Port Write Operation Timing Diagram

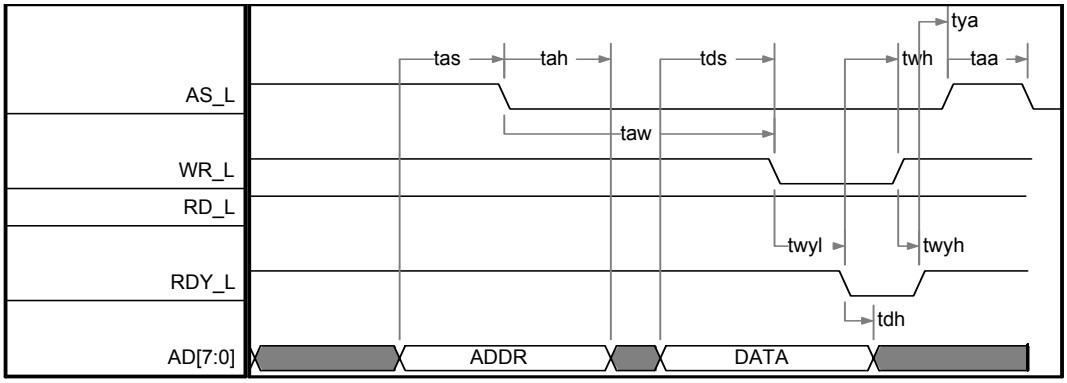


Table 5–9 Diagnostic Port Write Operation AC Timing

Signal	Symbol	Parameter	Min	Max
AD[3:0]	t_{as}	Setup time to AS_L asserted	13ns	–
AD[3:0]	t_{ah}	Hold time from AS_L asserted	23ns	–
AD[7:0]	t_{ds}	Setup time to WR_L asserted	13ns	–
AD[7:0]	t_{dh}	Hold time from RDY_L asserted	0ns	–
WR_L	t_{wh}	Hold time from RDY_L assertion	0ns	–
RDY_L	t_{wyl}	Delay from WR_L assertion	40ns	55ns
RDY_L	t_{wyh}	Delay from WR_L deassertion	40ns	55ns
WR_L	t_{aw}	Delay from AS_L assertion	36ns	–
AS_L	t_{aa}	Minimum deassertion time	23ns	–
AS_L	t_{ya}	Delay from RDY_L deassertion	0ns	–

5.3.5 JTAG Timing

Table 5–10 JTAG Signal AC TIming Specifications

Signal	Symbol	Parameter	Min	Max
TCK	F_{ftck}	Frequency	–	10MHz
TCK	T_{tckl}	Time low	50ns	–
TCK	T_{tckh}	Time high	50ns	–
TDI, TMS	T_{tsu}	Setup to TCK	40ns	–
TDI, TMS	T_{th}	Hold from TCK	40ns	–
TDO	T_{tval}	Valid from TCK	–	30ns
TDO	T_{tz}	Hi-Z from TCK	5ns	40ns

5.3.6 Asynchronous and Static Signals

Table 5–11 Asynchronous and Static Signals

Signal	Note
GPIO[7:0]	Under software control
CTAP0[3:0], CTAP1[3:0], RESLO, RESHI	LVDS control. Static.
BYPASSL, RESETTX, RESETRX, TSTSHFTLD, ECSEL, ETOGGLE, EXDNUP, TSTPHASE, LOOPBKEN	Asynchronous
TESTMODE[4:0]	Static

6

Contact Information

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