PM7375

LASAR-155™

LOCAL ATM SEGMENTATION AND REASSEMBLY & PHYSICAL LAYER INTERFACE

DATA SHEET

ISSUE 6: JUNE 1998

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
6	June 1998	Data Sheet Reformatted — No Change in Technical Content. Generated R6 data sheet from PMC-931123, P8
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CONTENTS

1 FEATURES

- Single-chip Peripheral Component Interface (PCI) Bus Local ATM Network Interface using SONET/SDH framing at 155.52 or 51.84 Mbit/s and ATM Adaptation Layer 5 (AAL-5).
- Implements the ATM Physical Layer according to the ATM Forum User Network Interface Specification and ITU-TS Recommendation I.432, and the ATM Adaptation Layer Type 5 (AAL-5) for Broadband ISDN according to ITU-TS Recommendation I.363.
- Provides a direct interface to multimode or single mode optical modules or twisted pair wiring (UTP-5) modules, with on-chip clock recovery and clock synthesis.
- Directly supports a 32-bit PCI bus interface for configuration, monitoring and transfer of packet data, with an on-chip DMA controller with scatter/gather capabilities. Other 32 bit system buses can be accommodated using external glue logic.
- Provides an on-chip 96 cell receive buffer to accommodate up to 270 µs of PCI Bus latency.
- Provides a optional microprocessor port with master and slave capabilities.
- Provides a SCI-PHY and Utopia compliant interface for connection to external PHY layer devices.
- Supports simultaneous segmentation and reassembly of 128 virtual circuits (VCs) in both transmit and receive directions.
- Provides leaky bucket peak cell rate enforcement using 8 programmable peak queues coupled with sub peak control on a per VC basis; provides sustainable cell rate enforcement using the programmable peak cell rate queues and per VC token bucket averaging; and provides aggregate peak cell rate enforcement.
- Provides a generic constant bit-rate (CBR) port.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power, 0.6 micron, +5 Volt CMOS technology.
- 208 copper slugged plastic quad flat pack (PQFP) package.

2 APPLICATIONS

- ATM Workstations and Servers
- ATM Bridges, Switches and Hubs
- Multimedia Terminals

3 REFERENCES

- ATM Forum - ATM User-Network Interface Specification, V3.1, September, 1994.
- ATM Forum - "An ATM PHY Data path Interface - Level 1", V2.0, February 1994
- ITU-TS Recommendation G.709 - "Synchronous Multiplexing Structure", Helsinki, March 1993.
- ITU-TS Recommendation I.363 - "B-ISDN ATM Adaptation Layer (AAL) Specification", Helsinki, March 1993.
- ITU-TS Recommendation I.432 DRAFT - "B-ISDN User-Network Interface-Physical Interface Specification", Helsinki, March 1993.
- ITU-TS Recommendation I.610 - "B-ISDN Operation and Maintenance Principles and Functions", Helsinki, March 1993.
- Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 1, December 1994.

  Bell Communications Research - Broadband-ISDN User to Network Interface and Network Node Interface Physical Layer Generic Criteria, TR-NWT-001112, Issue 1, June 1993.
- Bell Communications Research - Asynchronous Transfer Mode (ATM) and ATM Adaptation Layer (AAL) Protocols Generic Requirements, TA-NWT-001113, Issue 2, July 1993.
- Bell Communications Research - Generic Requirements for Operations of Broadband Switching Systems, TA-NWT-001248, Issue 2, October 1993.
- American National Standard for Telecommunications - B-ISDN ATM Adaptation Layer Type 5, ANSI T1.635-1993.

- T1X1.3/93-006R3, Draft American National Standard for Telecommunications, Synchronous Optical Network (SONET): Jitter at Network Interfaces
- IEEE 1149.1 - Standard Test Access Port and Boundary Scan Architecture, May 21, 1990.
- PCI Special Interest Group, PCI Local Bus Specification, June 1995, Version 2.1.
- PMC-940212, ATM_SCI_PHY, "SATURN Compliant Interface For ATM Devices", February 1994, Issue 1.

4 APPLICATION EXAMPLES

The LASAR-155™ is typically used to implement the core of a SONET or SDH STS-3c/STM-1 or SONET STS-1 ATM User Network Interface by which an ATM terminal is linked to an ATM switching system. The LASAR-155 can be used in a network interface card (NIC) or directly on a mother board. Though targeted for a PCI bus based system, the LASAR-155 can also be used with other host buses using external glue logic.

On the line side, the LASAR-155 is typically interfaced to UTP-5 twisted pair wiring via a line receiver, a line driver and transformers. The line receiver should perform fixed equalization and DC restoration for good bit error rate performance. Alternatively, the LASAR-155 can be directly connected to an optical datalink. If required, the LASAR-155 can be loop-timed where the recovered clock is used as the transmit clock.

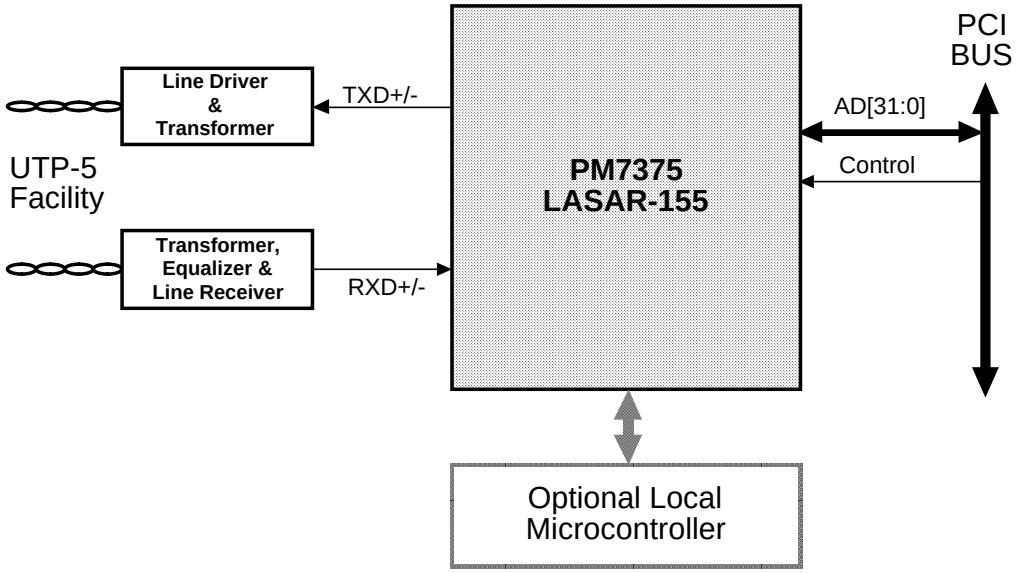
On the system side, the LASAR-155 can be directly attached to a PCI bus via the packet port. An internal DMA controller is provided to support packet segmentation from packet memory and reassembly to packet memory totally independent of the PCI Host. PCI Host notification of segmentation and/or reassembly completion can be on a per packet basis or on a multi packet basis.

The initial configuration and ongoing control and monitoring of the LASAR-155 can be provided either via the generic microprocessor interface when in slave mode, the PCI bus packet port when in master mode, or through a combination of both.

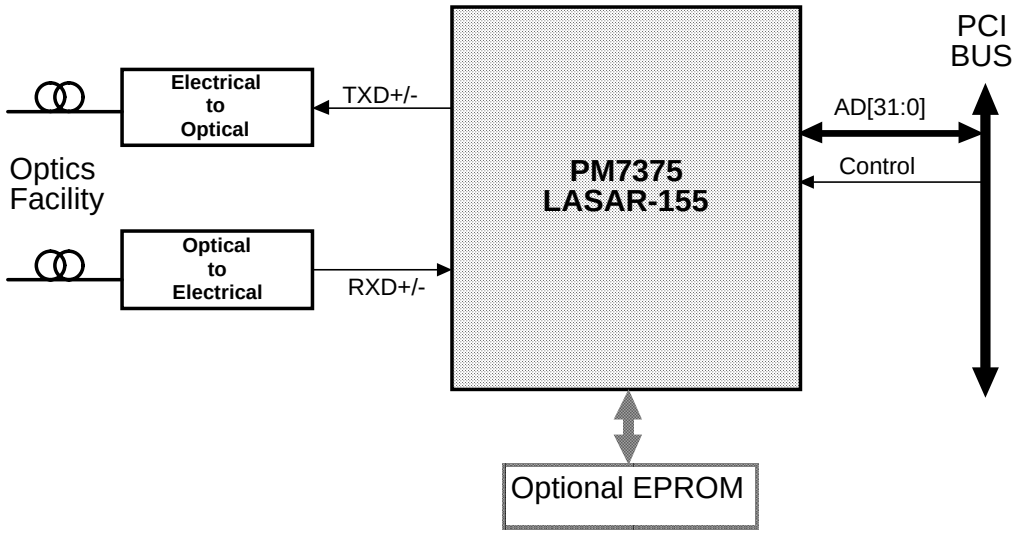
In addition, the LASAR-155 can interface to an external PHY device using the SCI-PHY/Utopia port. The generic microprocessor interface can be configured in master mode for configuration and ongoing control and monitoring. When this mode of operation is selected an optional EPROM can also be supported by the generic microprocessor interface.

4.1.1.1 Fig. 4.1 Typical Applications

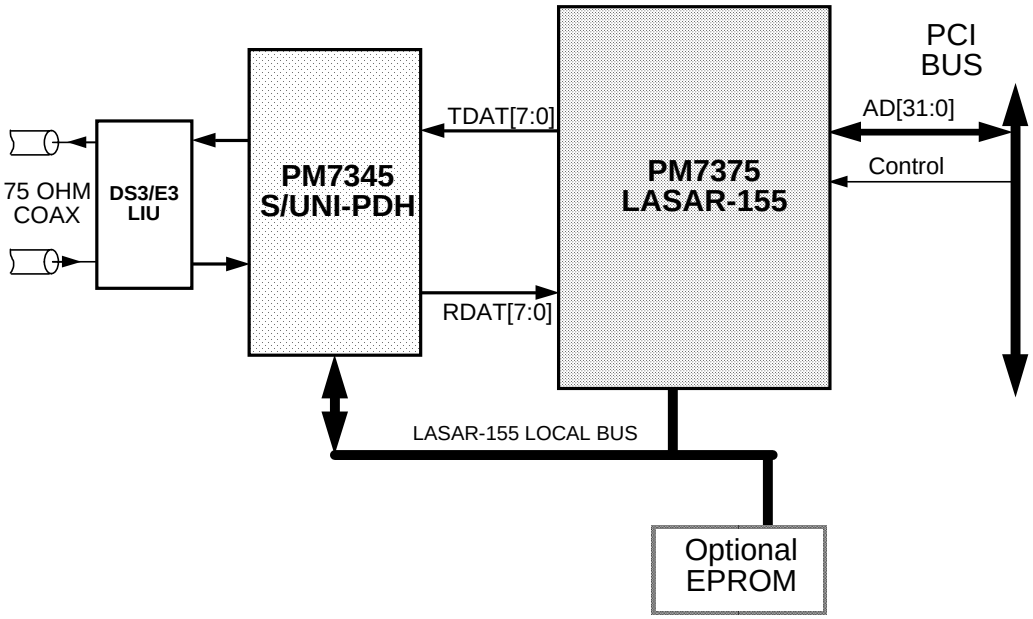
4.1.2 STS-3c UTP-5 ATM Operation



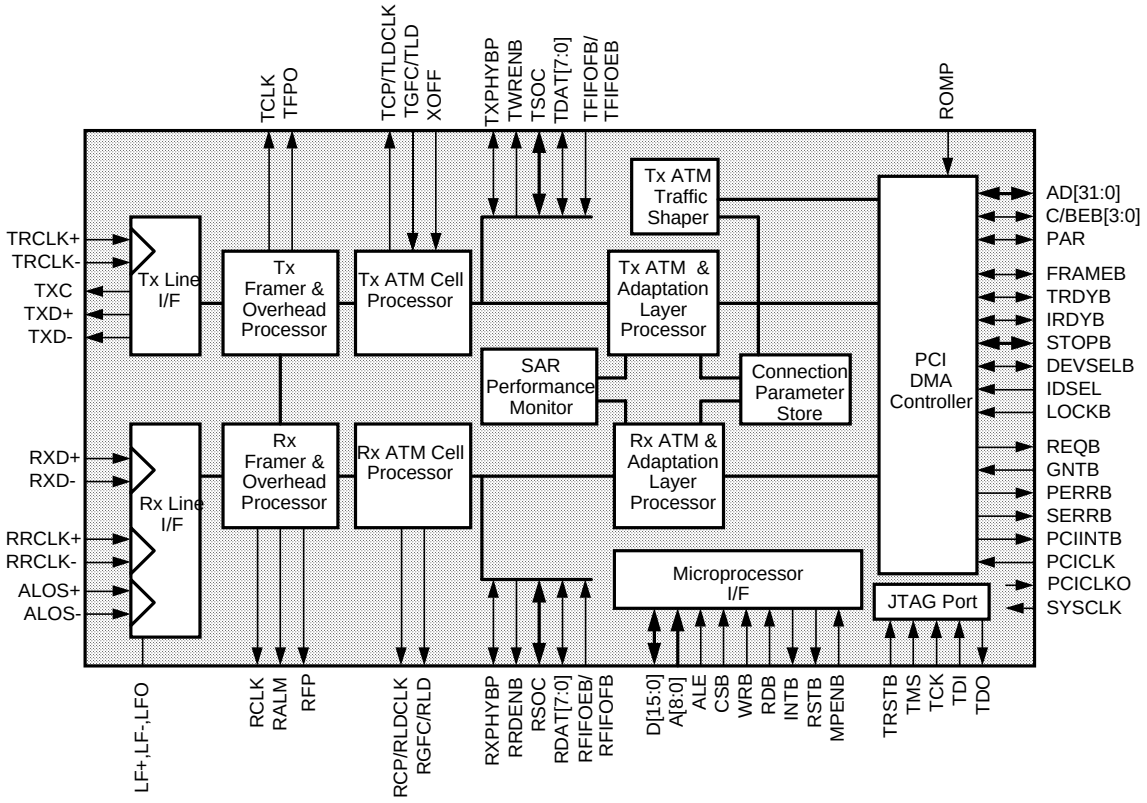
4.1.3 STS-3c/1 Optical ATM Operation



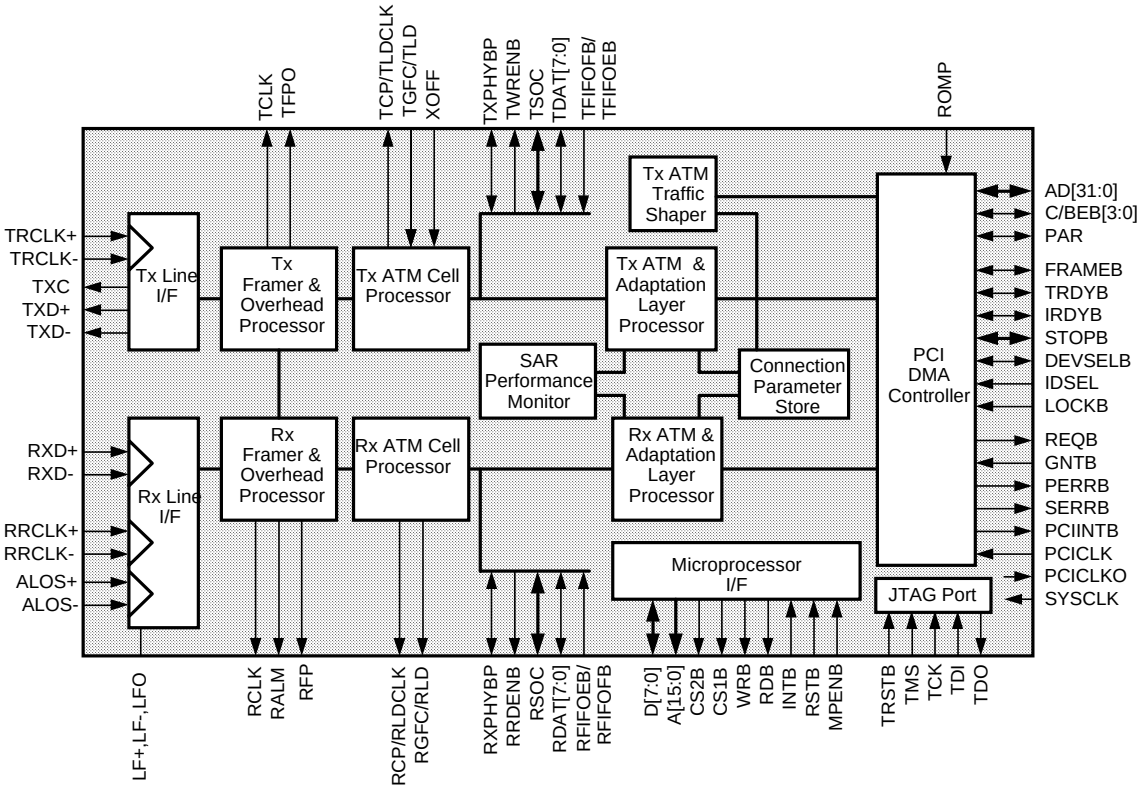
4.1.4 DS3/E3 ATM Operation



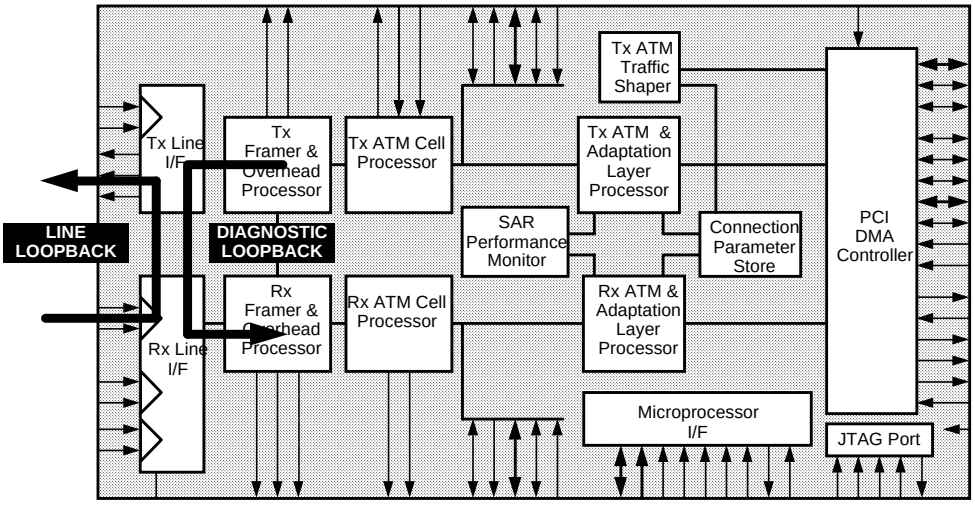
5 BLOCK DIAGRAM



Normal Operating Mode (Slave Operation)



Normal Operating Mode (Master Operation)



Loopback Modes

6 DESCRIPTION

The PM7375 LASAR-155 Local ATM Segmentation and Reassembly & Physical Layer device is a monolithic integrated circuit that implements SONET/SDH transmission convergence, ATM cell mapping, ATM Adaptation Layer, and PCI Bus memory management functions for a 155.52 or 51.84 Mbit/s ATM User Network Interface.

The LASAR-155 receives SONET/SDH frames via a bit serial interface, recovers clock and data, and processes section, line, and path overheads. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2, G1) are also accumulated. The LASAR-155 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

The LASAR-155 frames to the ATM payload using cell delineation. Payload descrambling, HEC single bit error correction, cell filtering based on HEC errors and idle/unassigned cell filtering is provided. The Generic Flow Control (GFC) field is extracted from all received cell headers and serialized out a dedicated port. Counts of received ATM cell headers that are in error and uncorrectable, cell headers that are errored and correctable and all passed cells are accumulated independently for performance monitoring purposes.

The LASAR-155 supports the simultaneous reassembly and Common Part Convergence Sublayer (CPCS) processing for 128 open Virtual Circuits (VCs). All receive VC parameters are stored locally in the LASAR-155 device to reduce overhead traffic on the PCI Host bus. The LASAR-155 takes all received error free cells and passes or blocks the cell based on an open VC. Passed cells are treated as management, control or user cells. Management and control cell payloads are optionally checked with a CRC-10 polynomial and are optionally DMA'd to receive ready queues in packet memory.

User cells are associated with an open VC and DMA'd to reassembly queues in packet memory. Once a packet is reassembled and verified using a CRC-32 polynomial, the entire packet is linked into a receive ready queue. The LASAR-155 alerts the PCI Host that there are reassembled packets or cells in a receive ready queue by asserting an interrupt on the PCI bus.

All transmit VC parameters are stored in an internal transmit parameter table to reduce overhead traffic on the PCI bus. After a PCI Host sets up a connection using the transmit parameter table, the PCI Host can provide packets to transmit using a

high or low priority ready queue. The LASAR-155 automatically appends the AAL-5 trailer, segments the packet and subjects the cells to either peak cell rate or sustainable cell rate enforcement.

The LASAR-155 generates most of a cell's header using the transmit parameter table. The generic flow control (GFC) bits may optionally be inserted using a dedicated serial port. The header error code (HEC) is automatically calculated and inserted. The cell payload is optionally scrambled. Generated transmit cells are automatically inserted into a STS-3c (STM-1) or STS-1 SONET/SDH Synchronous Payload Envelope (SPE). In the absence of transmit cells, the LASAR-155 automatically inserts Idle/unassigned cells into the SPE.

The LASAR-155 transmits SONET/SDH frames, via a bit serial interface, and formats SONET section, line, and path overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (Z2, G1) are also inserted. The LASAR-155 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload.

For system diagnostics, the LASAR-155 supports the insertion of a variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors and illegal pointers.

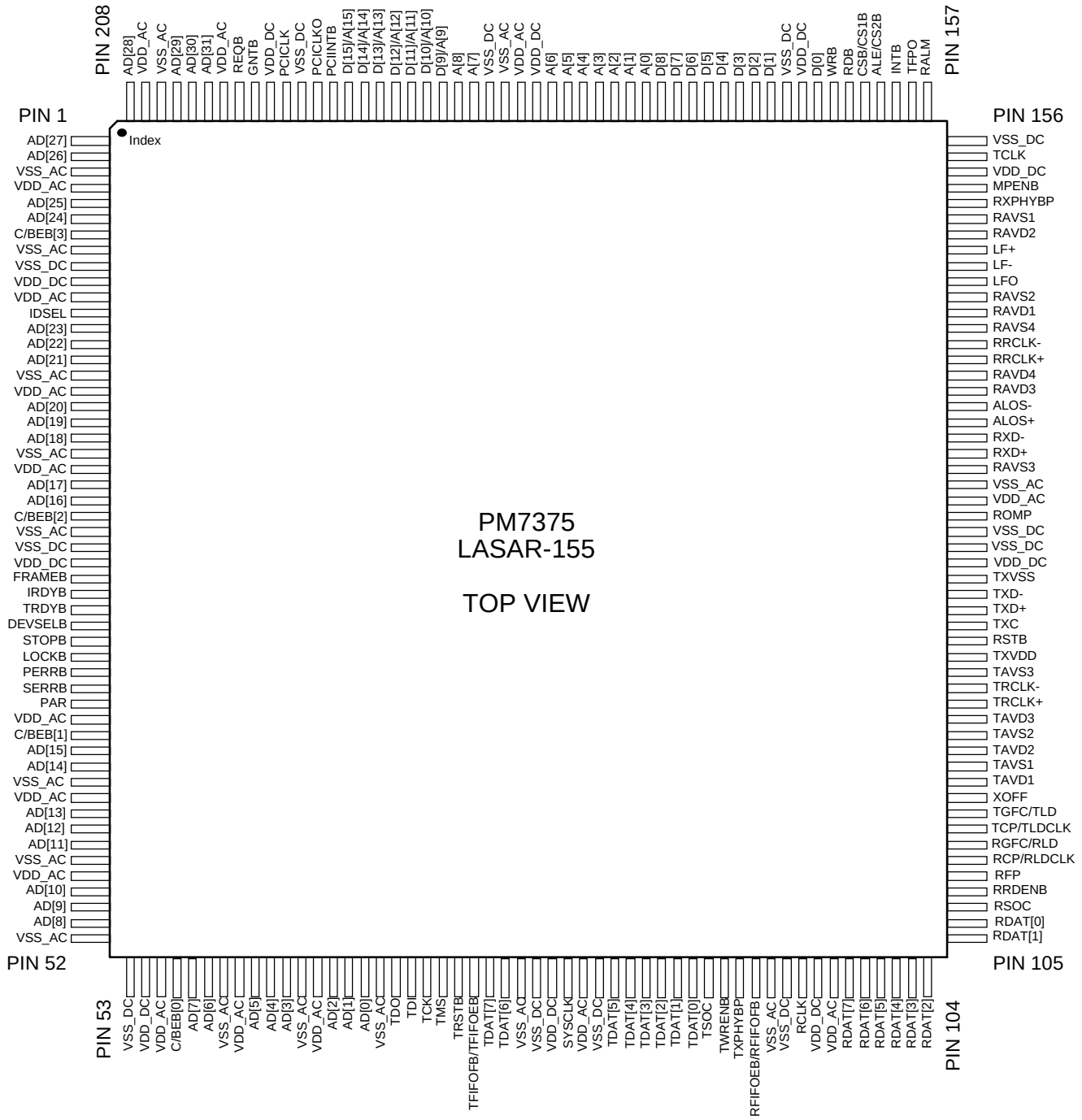
No auxiliary line clocks are required directly by the LASAR-155 as it is capable of synthesizing the line rate transmit clock and recovering the receive clock using either a 19.44 MHz or 6.48 MHz reference clock. The LASAR-155 is configured, controlled and monitored via either the generic microprocessor port interface in slave mode or the PCI bus interface in master mode. In slave mode, a mailbox scheme with shared buffers is provided for communication between the microprocessor and PCI Host.

The LASAR-155 can interface with external devices when the generic microprocessor port interface is configured for master mode operation. In this mode the PCI Host configures, controls and monitors the LASAR-155 and the external devices.

The LASAR-155 is implemented in low power, 0.6 micron, +5 Volt CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 208 pin copper slugged plastic QFP package.

7 PIN DIAGRAM

The LASAR-155 is packaged in a 208 pin slugged plastic QFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.5 mm.



8 PIN DESCRIPTION (TOTAL 208)

8.1 Line Side Interface Signals (24)

Pin Name	Type	Pin No.	Feature
RXD+ RXD-	PECL Input	136 137	The receive differential data inputs (RXD+, RXD-) contain the 155.52 Mbit/s receive STS-3c (STM-1) stream or the 51.84 Mbit/s receive STS-1 stream. RXD+/- are sampled on the rising edge of RRCLK+/- when clock recovery is disabled (the falling edge may be used by reversing RRCLK+/-), otherwise the receive clocks are recovered from the RXD+/- bit stream. RXD+/- is expected to be NRZ encoded.
RRCLK+ RRCLK-	PECL Input	142 143	The receive differential reference clock inputs (RRCLK+, RRCLK-) contain a jitter-free 19.44 MHz or 6.48 MHz reference clock when clock recovery is enabled. When clock recovery is bypassed, RRCLK+/- is nominally a 155.52 MHz or 51.84 MHz, 50% duty cycle clock and provide timing for the LASAR-155 receive functions. In this case, RXD+/- is sampled on the rising edge of RRCLK+/-. Clock recovery bypass is selectable using the RBYP bit in the LASAR-155 Master Configuration register.
ALOS+ ALOS-	PECL Input	138 139	The analog loss of signal (ALOS+/-) differential inputs are used to indicate a loss of receive signal power. When ALOS+/- is asserted, the data on the receive data (RXD+/-) pin will be squelched and the phase locked loop shall switch to the reference clock (RRCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled.
LF+, LF-, LFO	Analog	149 148 147	Passive components connected to the recovery loop filter (LF+, LF- and LFO) pins determine the dynamics of the clock recovery unit. Refer to the Operation section for details.

RCLK	Output	96	The receive clock (RCLK) output provides a timing reference for the LASAR-155 receive line interface outputs. RCLK is a 19.44 MHz or 6.48 MHz, nominally 50% duty cycle clock. RCLK is a divide by eight of the recovered clock or the RRCLK+/- inputs as determined using the RBYP bit in the LASAR-155 Master Configuration register.
RALM	Output	157	The receive alarm (RALM) output indicates the state of the receive framing. RALM is low if no receive alarms are active. RALM is high if loss of signal (LOS), line AIS, path AIS, loss of frame (LOF), loss of pointer (LOP) or loss of cell delineation (LCD) is detected. RALM is updated on the falling edge of RCLK.
RFP	Output	109	The receive frame pulse (RFP) output is an 8 kHz signal derived from the receive line clock. RFP is pulsed high for one RCLK cycle every 2430 RCLK cycles for STS-3c (STM-1) or every 810 RCLK cycles for STS-1. A single discontinuity in RFP position occurs if a change of frame alignment occurs.
TRCLK+ TRCLK-	PECL Input	120 121	The transmit differential reference clock inputs (TRCLK+, TRCLK-) are a jitter-free 19.44 MHz or 6.48 MHz reference clock when clock synthesis is enabled. When clock synthesis is bypassed, TRCLK+/- is nominally a 155.52 MHz or 51.84 MHz, 50% duty cycle clock. This clock provides timing for the LASAR-155 transmit functions. TRCLK+/- may be left unconnected when LASAR-155 loop timing is enabled using the LASAR-155 Master Control Register.
TXC	Output	125	The transmit clock (TXC) output is available when STS-1 (51.84 Mbits/s) mode of operation is selected using the LASAR-155 Master Configuration register. When STS-3c (STM-1) mode of operation is selected, TXC is held low. TXD+/- are updated on the falling edge of TXC.

TXD+ TXD-	Output	126 127	The transmit differential data outputs (TXD+, TXD-) contain the 155.52 Mbit/s transmit STS-3c (STM-1) stream or the 51.84 Mbit/s transmit STS-1 stream. When the STS-1 stream is selected, TXD+/- are updated on the falling edge of TXC. TXD+/- is NRZ encoded.
TCLK	Output	155	The transmit byte clock (TCLK) is either a 19.44 MHz or a 6.48 MHz clock derived from the transmit line rate.
TFPO	Output	158	The active high framing position output (TFPO) signal is an 8 kHz timing marker for the transmitter. TFPO goes high for a single TCLK period once every 2430 in STS-3c (STM-1) mode or 810 in STS-1 mode TCLK cycles. TFPO is updated on the rising edge of TCLK.
RGFC/RLD	Output	111	The RGFC/RLD output is a dual function output controlled using the UNI_POTS bit in the LASAR-155 Master Configuration register. When the UNI_POTS bit is low, the receive generic flow control (RGFC) output presents the extracted GFC bits in a serial stream. The four GFC bits are presented for each received cell, with the RCP output indicating the position of the most significant bit. The updating of RGFC by particular GFC bits may be disabled through the RACP Configuration register. The serial link is forced low if cell delineation is lost. RGFC is updated on the rising edge of RCLK. When the UNI_POTS bit is high, the receive line DCC (RLD) signal contains the serial line data communications channel (D4 - D12) extracted from the incoming stream. RLD is updated on the falling edge of RLDCLK.

RCP/ RLDCLK	Output	110	The RCP/RLDCLK output is a dual function output controlled using the UNI_POTS bit in the LASAR-155 Master Configuration register. When the UNI_POTS bit is low, the receive cell pulse (RCP) indicates the location of the four GFC bits in the RGFC serial stream. RCP is coincident with the most significant GFC bit. RCP is updated on the rising edge of RCLK. When the UNI_POTS bit is high, the receive line DCC clock (RLDCLK) is a 576 kHz clock used to update the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock.
TGFC/TLD	Input	113	The TGFC/TLD input is a dual function input controlled using the UNI_POTS bit in the LASAR-155 Master Configuration register. When the UNI_POTS bit is low, the transmit generic flow control (TGFC) input provides the ability to insert the GFC value. The four TCLK periods following the TCP output pulse contain the GFC value to be inserted into the current cell. The GFC enable bits of the TACP Configuration register enable the insertion of each serial bit. TGFC is sampled on the rising edge of TCLK. When the UNI_POTS bit is high, the transmit line DCC (TLD) signal contains the serial line data communications channel (D4 - D12). TLD is sampled on the rising edge of TLDCLK.

TCP/ TLDCLK	Output	112	The TGFC/TLDCLK output is a dual function output controlled using the UNI_POTS bit in the LASAR-155 Master Configuration register. When the UNI_POTS bit is low, the transmit cell pulse (TCP) indicates where the valid TGFC serial bits are expected. If TCP is asserted high, the most significant GFC bit is expected in the subsequent TCLK period. TCP pulses high for one TCLK for every transmitted cell. TCP is updated on the rising edge of TCLK. When the UNI_POTS bit is high, the transmit line DCC clock (TLDCLK) is a 576 kHz clock used to sample the TLD input. TLDCLK is generated by gapping a 2.16 MHz clock.
XOFF	Input	114	The transmit off (XOFF) signal can be used to control the transmission of user cells. When XOFF is asserted high, the LASAR-155 is prohibited from transmitting user cells. Under this operating condition, the LASAR-155 can only transmit Idle/Unassigned cells. When XOFF is low, the LASAR-155 operates normally. XOFF is sampled on the rising edge of TCLK.

8.2 Multipurpose Port Interface Signals (24)

Pin Name	Type	Pin No.	Feature
RXPHYBP	I/O	152	The receive physical layer bypass (RXPHYBP) signal selects whether or not to bypass the internal SONET PHY in the receive direction. When RXPHYBP is set high, the internal SONET PHY is bypassed and a SCI-PHY/Utopia compliant interface consisting of signals: RSOC, RRDENB, RFIFOEB and RDAT[7:0] is supported. When RXPHYBP is set low, the LASAR-155 operates normally with the internal SONET PHY. In this mode, signals RSOC, RRDENB, RFIFOFB and RDAT[7:0] can be used to interface to an external FIFO to support CBR VCs and Management cells. Under analog test mode as selected using the PMCATST bit in the LASAR-155 Master Test register, this pin is configured as an output and is used for test purposes.

RRDENB	Output	108	The active low receive read enable (RRDENB) signal's function is configured using input RXPHYBP. When RXPHYBP is set high, the LASAR-155's SONET physical layer blocks are bypassed and RRDENB is used to initiate reads from an external FIFO associated with a physical layer device (eg. the PMC SUNI-PDH device). When RRDENB is set low and RFIFOEB is sampled high on a rising edge of SYSCLK, a cell byte is sampled on the RDAT[7:0] bus on the next rising edge of SYSCLK. If RRDENB is set high on the rising edge of SYSCLK, a cell byte is not sampled on the next rising edge of SYSCLK. RRDENB is updated on the rising edge of SYSCLK. When RXPHYBP is set low, the LASAR-155 operates normally with the integrated STS-3c (STM-1) or STS-1 PHY. When RRDENB is set low on the rising edge of SYSCLK, the data on the RDAT[7:0] bus is valid. When RRDENB is set high on the rising edge of SYSCLK, the data on the RDAT[7:0] bus is not valid. RRDENB is updated on the rising edge of SYSCLK.
RSOC	I/O	107	The receive start of cell (RSOC) signal's function is configured using input RXPHYBP. When RXPHYBP is set high, RSOC becomes an input and is expected to mark the start of cell on the RDAT[7:0] bus. For this mode of operation, RSOC is sampled using the rising edge of SYSCLK. When RXPHYBP is set low, RSOC becomes an output and marks the start of cell on the RDAT[7:0] bus. For this mode of operation, RSOC is updated on the rising edge of SYSCLK.

RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7]	I/O	106 105 104 103 102 101 100 99	The receive cell data (RDAT[7:0]) bus' function is configured using input RXPHYBP. When RXPHYBP is set high, the RDAT[7:0] signals become inputs and are expected to carry the ATM cell octets that are read from an external FIFO associated with an external physical layer device. For this mode of operation, RDAT[7:0] is sampled using the rising edge of SYSCLK. When RXPHYBP is set low, the RDAT[7:0] signals become outputs and carry ATM cell octets marked for this output port. For this mode of operation, RDAT[7:0] is updated on the rising edge of SYSCLK.
RFIFOEB RFIFOFB	Input	93	When RXPHYBP is set high, the active low receive FIFO empty (RFIFOEB) signal indicates when a byte is available to be read from an external FIFO. When sampled high, RFIFOEB indicates that at least one byte can be read. When sampled low, RFIFOEB indicates that there are no bytes to be read. In this mode of operation, RFIFOEB is sampled using the rising edge of SYSCLK. When RXPHYBP is set low, the active low receive FIFO full (RFIFOFB) signal indicates when a byte can be written to an external FIFO. When sampled high, RFIFOFB indicates that at least one byte can be written. When sampled low, RFIFOFB indicates that the external FIFO is full and can accept no more writes. In this mode of operation, RFIFOFB is sampled using the rising edge of SYSCLK.

TXPHYBP	I/O	92	The transmit physical layer bypass (TXPHYBP) signal selects whether or not to bypass the internal SONET PHY in the transmit direction. When TXPHYBP is set high, the internal SONET PHY is bypassed and a SCI-PHY/Utopia compliant interface comprising of signals: TSOC, TWRENB, TFIFOFB and TDAT[7:0] is supported. When TXPHYBP is set low, the LASAR-155 operates normally with the internal SONET PHY. In this mode, signals TSOC, TWRENB, TFIFOEB and TDAT[7:0] can be used to interface to an external FIFO to support CBR VCs. Under analog test mode as selected using the PMCATST bit in the LASAR-155 Master Test register, this pin is configured as an output and is used for test purposes.
TWRENB	Output	91	The active low transmit write enable (TWRENB) signal's function is configured using input TXPHYBP. When TXPHYBP is set high, the LASAR-155's SONET physical layer blocks are bypassed and TWRENB is used to initiate writes to an external FIFO associated with a physical layer device (e.g. the PMC SUNI-PDH). When TWRENB is low and TFIFOFB is high during a SYSCLK cycle, the current cell byte on bus TDAT[7:0] is written into the external FIFO. When TWRENB is high during a SYSCLK cycle, no write is performed. In this mode of operation, TWRENB is generated using the rising edge of SYSCLK. When TXPHYBP is set low, the LASAR-155 operates normally with the integrated STS-3c (STM-1) or STS-1 PHY. When TWRENB is low on the rising edge of a SYSCLK cycle and TFIFOEB is high, a cell byte is expected on the TDAT[7:0] bus on the next rising edge of SYSCLK. When TWRENB is set high on the rising edge of a SYSCLK cycle, data is not expected on the TDAT[7:0] bus on the next rising edge of SYSCLK. Once a full cell is sampled, it is automatically inserted into the cell stream. In this mode of operation, TWRENB is generated using the rising edge of SYSCLK.

TSOC	I/O	90	The transmit start of cell (TSOC) signal's function is configured using input TXPHYBP. When TXPHYBP is set high, TSOC becomes an output and is expected to mark the start of cell on the TDAT[7:0] bus. For this mode of operation, TSOC is updated on the rising edge of SYSCLK. When TXPHYBP is set low, TSOC becomes an input and marks the start of cell on the TDAT[7:0] bus. When TSOC is high, the first octet of the cell is present on the TDAT[7:0] bus. It is not necessary for TSOC to be present at each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the selected data structure. For this mode of operation, TSOC is sampled using the rising edge of SYSCLK.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7]	I/O	89 88 87 86 85 84 77 76	The transmit cell data (TDAT[7:0]) bus' function is configured using input TXPHYBP. When TXPHYBP is set high, the TDAT[7:0] signals become outputs and carry the ATM cell octets that are written to a FIFO associated with an external physical layer device. For this mode of operation, TDAT[7:0] is updated on the rising edge of SYSCLK. When TXPHYBP is set low, the TDAT[7:0] signals become inputs and carry the ATM cell octets that are read from an external FIFO. For this mode of operation, TDAT[7:0] is sampled using the rising edge of SYSCLK.

TFIFOFB TFIFOEB	Input	75	When TXPHYBP is set high, the active low transmit FIFO full (TFIFOFB) signal indicates when a byte can be written to an external FIFO. When sampled low, TFIFOFB indicates that the external FIFO is full and can accept four more writes. When sampled high, TFIFOFB indicates that at least one byte can be written. In this mode of operation, TFIFOFB is sampled using the rising edge of SYSCLK. When TXPHYBP is set low, the active low transmit FIFO empty (TFIFOEB) signal indicates when a byte is available to be read from an external FIFO. When sampled low, TFIFOEB indicates that there are no bytes to be read. When sampled high, TFIFOEB indicates that at least one byte can be read. In this mode of operation, TFIFOEB is sampled using the rising edge of SYSCLK.

8.3 PCI Host Interface Signals (52)

Pin Name	Type	Pin No.	Feature
PCICLK	Input	198	The PCI clock (PCICLK) provides timing for PCI bus accesses. PCICLK should be nominally a 50% duty cycle 0 to 33 MHz clock.
PCICLKO	Output	196	The PCI clock output (PCICLKO) is a buffered version of the PCI clock input, PCICLK. PCICLKO can be used to drive the SYSCLK input.
ROMP	Input	132	The ROMP input can be used to indicate whether an Expansion ROM is present or not. If ROMP is logic one, an expansion ROM is assumed to be present on the LASAR-155 local bus and the Expansion ROM Base Address register operates normally. If ROMP is logic zero, the XRBS bits in the Expansion ROM Base Address register is zeroed out indicating there is no expansion ROM. ROMP must be used to allow Interoperability with some BIOs implementations. ROMP has an integral pull up resistor.

AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7] AD[8] AD[9] AD[10] AD[11] AD[12] AD[13] AD[14] AD[15] AD[16] AD[17] AD[18] AD[19] AD[20] AD[21] AD[22] AD[23] AD[24] AD[25] AD[26] AD[27] AD[28] AD[29] AD[30] AD[31]	I/O	68 67 66 63 62 61 58 57 51 50 49 46 45 44 41 40 24 23 20 19 18 15 14 13 6 5 2 1 208 205 204 203	The PCI address and data (AD[31:0]) bus is used to carry multiplexed address and data. During the first clock cycle of a transaction, AD[31:0] contains a physical byte address. Subsequent clock cycles of a transaction should contain data. A transaction is defined as an address phase followed by one or more data phases. When Little-Endian byte formatting is used. AD[31:24] should contain the most significant byte of a DWORD while AD[7:0] should contain the least significant byte of a DWORD. When Big-Endian byte formatting is used. AD[7:0] should contain the most significant byte of a DWORD while AD[31:24] should contain the least significant byte of a DWORD. When the LASAR-155 is the initiator, AD[31:0] are outputs during the first (address) phase of a transaction. For write transactions, AD[31:0] remain outputs for the data phases of the transaction. For read transactions, AD[31:0] become inputs. When the LASAR-155 is the target, AD[31:0] are inputs during the first (address) phase of a transaction. For write transactions, AD[31:0] become inputs for the data phases of the transaction. For read transactions, AD[31:0] remain outputs for the transaction. When the LASAR-155 is not involved in the current transaction, AD[31:0] are tri-stated. Signals, AD[31:0] are updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether they are outputs or inputs.

C/BEB[0] C/BEB[1] C/BEB[2] C/BEB[3]	I/O	56 39 25 7	The PCI bus command and byte enable (C/BEB[3:0]) bus contains the bus command or the byte valid indications. During the first clock cycle of a transaction, C/BEB[3:0] contains the bus command code. For subsequent clock cycles, C/BEB[3:0] identifies which bytes on the AD[31:0] bus carry meaningful data. C/BEB[3] is associated with byte 3 (AD[31:24]) while C/BEB[0] is associated with byte 0 (AD[7:0]). When C/BEB[n] is high, the associated byte is meaningless. When C/BEB[n] is low, the associated byte is valid. When the LASAR-155 is the initiator, C/BEB[3:0] are outputs. When the LASAR-155 is the target, C/BEB[3:0] are inputs. When the LASAR-155 is not involved in the current transaction, C/BEB[3:0] are tri-stated. C/BEB[3:0] are updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether they are outputs or inputs.
PAR	I/O	37	The parity (PAR) signal is the even parity calculated over the 36 signals, AD[31:0] and C/BEB[3:0] regardless of whether all the bytes of the AD bus are meaningful. PAR always is the calculated parity for the previous PCICLK cycle. Parity errors detected by the LASAR-155 are indicated on output PERRB and in the PCID Interrupt Status register. When the LASAR-155 is the initiator, PAR is an output for writes and an input for reads. When the LASAR-155 is the target, PAR is an input for writes and an output for reads. When the LASAR-155 is not involved in the current transaction, PAR is tri-stated. PAR is updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether it is an output or an input.

FRAMEB	I/O	29	The active low cycle frame (FRAMEB) is used to identify a transaction cycle. When FRAMEB transitions low, the start of a bus transaction is indicated. FRAMEB remains low to define the duration of the cycle. When FRAMEB transitions high, the last data phase of the current transaction is indicated. When the LASAR-155 is the initiator, FRAMEB is an output. When the LASAR-155 is the target, FRAMEB is an input. When the LASAR-155 is not involved in the current transaction, FRAMEB is tri-stated. FRAMEB is updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether it is an output or an input.
TRDYB	I/O	31	The active low target ready (TRDYB) signal is used to indicate whether the target is ready to start or continue a transaction. TRDYB works in conjunction with IRDYB to complete transaction data phases. When TRDYB is high and a transaction is in progress, the target could not complete the current data phase and is forcing a wait state. When TRDYB is low and a transaction is in progress, the target has completed the current data phase. Note, whether the data phase is completed or not depends on the initiator's ready signal IRDYB. When the LASAR-155 is the initiator, TRDYB is an input. When the LASAR-155 is the target, TRDYB is an output. It is expected that for LASAR-155 register accesses, TRDYB will be used to extend data phases to multiple PCICLK cycles. When the LASAR-155 is not involved in the current transaction, TRDYB is tri-stated. TRDYB is updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether it is an output or an input.

IRDYB	I/O	30	The active low initiator ready (IRDYB) signal is used to indicate whether the initiator is ready to start or continue a transaction. IRDYB works in conjunction with TRDYB to complete transaction data phases. When IRDYB is high and a transaction is in progress, the initiator could not complete the current data phase and is forcing a wait state. When IRDYB is low and a transaction is in progress, the initiator has completed the current data phase. Note, whether the data phase is completed or not depends on the target's ready signal TRDYB. When the LASAR-155 is the initiator, IRDYB is an output. When the LASAR-155 is the target, IRDYB is an input. When the LASAR-155 is not involved in the current transaction, IRDYB is tri-stated. IRDYB is updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether it is an output or an input.
STOPB	I/O	33	The active low stop (STOPB) signal is used by a target to request the initiator to stop the current bus transaction. When STOPB is high, the initiator continues with the transaction. When STOPB is low, the initiator should stop the current transaction. When the LASAR-155 is the initiator, STOPB is an input. If STOPB is sampled low, the LASAR-155 terminates the current transaction in the next PCICLK cycle. When the LASAR-155 is the target, STOPB is an output. As a target, the LASAR-155 only issues transaction stop requests when its internal bus latency buffers are in a near overflow state. When the LASAR-155 is not involved in the current transaction, STOPB is tri-stated. STOPB is updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether it is an output or an input.

IDSEL	Input	12	The initialization device select (IDSEL) signal is used as the chip select during PCI configuration register reads and writes. When high during the address phase of a transaction with the C/BEB[3:0] code indicating a register read or write, the LASAR-155 assumes a PCI configuration register transaction. In response, the LASAR-155 asserts the DEVSELB signal in the subsequent PCICLK period. IDSEL is sampled using the rising edge of PCICLK.
DEVSELB	I/O	32	The device select (DEVSELB) signal is forced low by a target to claim the current bus transaction. During the address phase of a transaction, all targets decode the address on the AD[31:0] bus. If a target recognizes the address as its own, it forces DEVSELB low to indicate to the initiator that the address is valid. If no target claims the address in six bus clock cycles, the initiator must assume that the target does not exist or cannot respond and must abort the transaction. When the LASAR-155 is the initiator, DEVSELB is an input. If no target responds to an address in six PCICLK cycles, the LASAR-155 aborts the current transaction and alerts the PCI Host via an interrupt. When the LASAR-155 is the target, DEVSELB is an output. DEVSELB is updated on the rising edge of PCICLK or sampled using the rising edge of PCICLK depending on whether it is an output or an input. When the LASAR-155 is not involved in the current transaction, DEVSELB is tri-stated.
LOCKB	Input	34	The active low bus lock (LOCKB) signal is used to lock a target device. When LOCKB is low, FRAMEB is low and the LASAR-155 is the target, an initiator is locking the LASAR-155 as an "owned" target. Under these circumstances, the LASAR-155 will reject all transaction with other initiators. The LASAR-155 will continue to reject other initiators until its owner releases the lock by forcing both FRAMEB and LOCKB high. As an initiator, the LASAR-155 never locks a target. LOCKB is sampled using the rising edge of PCICLK.

REQB	Output	201	The active low PCI bus request (REQB) signal is used by the LASAR-155 to request an external arbiter for control of the PCI bus. REQB is forced low when the internal PCI DMA controller requires access to the packet memory. Otherwise, REQB is forced high. REQB is updated on the rising edge of PCICLK.
GNTB	Input	200	The active low PCI bus grant (GNTB) signal is used to grant control of the PCI to the LASAR-155 in response to a bus request via the REQB output. When GNTB is high, the LASAR-155 does not control the PCI bus and thus must wait. When GNTB is low, the external arbiter has granted the LASAR-155 control of the PCI bus. However, the LASAR-155 does not proceed until the FRAMEB signal is high indicating no current transactions. GNTB is sampled using the rising edge of PCICLK.
PERRB	Output	35	The active low parity error (PERRB) signal indicates when the LASAR-155 detects a parity error over the AD[31:0] and C/BEB[3:0] signals when compared to the PAR input. PERRB is high when no parity error is detected. PERRB is forced low for the cycle immediately following the offending PAR cycle. PERRB is enabled using a bit in the Control register in the PCI Configuration registers space. In addition, regardless of whether output, PERRB is enabled or not, parity errors are indicated in the Status register in the PCI Configuration registers space. PERRB is updated on the rising edge of PCICLK.

SERRB	OD Output	36	The active low system error (SERRB) signal indicates when the LASAR-155 detects an address parity error or when configured as an initiator, it generates a master abort or receives a target abort. Address parity errors are indicated when the even parity calculation during an address phase does not match the PAR input. When the LASAR-155 detects a system error, SERRB is forced low for one PCICLK period. SERRB is enabled using a bit in the Control register in the PCI Configuration registers space. In addition, regardless of whether output, SERRB is enabled or not, system errors are indicated in the Status register in the PCI Configuration registers space. SERRB is asserted on the rising edge of PCICLK. SERRB is an open drain output and relies on an external pull up resister to return to the logic one state.
PCIINTB	OD Output	195	The active low PCI interrupt (PCIINTB) signal goes low when a LASAR-155 interrupt source is active, and that source is unmasked. The LASAR-155 may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line far end receive failure (FERF), loss of pointer (LOP), path AIS, path RDI, and many others. PCIINTB returns high when the interrupt is acknowledged via an appropriate register access. PCIINTB is an open drain output. When the PCIINTB signal asserts, the PCID Interrupt Status and the PCID Mailbox/Microprocessor Interrupt Status/Enable registers should be read to determine the source of the interrupt. PCIINTB is updated on the rising edge of PCICLK.

8.4 Microprocessor Interface Signals (31)

Pin Name	Type	Pin No.	Feature
MPENB	Input	153	The active low microprocessor port enable (MPENB) signal is used to configure the Microprocessor Interface Port for master or slave mode operation. If MPENB is low, the port is configured for slave mode operation and an external microprocessor is permitted to access LASAR-155 registers using signals, CSB, RDB, WRB, D[15:0] and A[8:0]. Please refer to the Normal Mode Register Description Section for register details. If MPENB is high, LASAR-155 register accesses using the Microprocessor Interface Port is disabled. The Microprocessor Interface Port is configured as a master and the PCI Host has control of all internal LASAR-155 registers and the LASAR-155 Local Bus.
CSB/CS1B	I/O	161	For slave mode operation the active low chip select (CSB) signal is configured as an input. CSB is low during LASAR-155 Microprocessor Interface Port register accesses. If CSB is not used and Microprocessor Interface Port register accesses are controlled using only the RDB and the WRB signals, CSB should be connected to an inverted version of RSTB. For master mode operation the active low chip select one (CS1B) signal is configured as an output. CS1B is set low during LASAR-155 Local Bus accesses to the External Devices address space as defined using the External Device Memory Base Address register. For this mode of operation CS1B is generated on the rising edge of PCICLK.

RDB	I/O	162	For slave mode operation the active low read enable (RDB) signal is configured as an input. RDB is low during LASAR-155 Microprocessor Interface Port register read accesses. The LASAR-155 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low. For master mode operation the active low read enable (RDB) signal is configured as an output. RDB is low during LASAR-155 Local Bus read accesses. The device being read should drive the D[7:0] bus with the contents of the addressed memory location while RDB and either CS1B or CS2B is low. For this mode of operation RDB is generated on the rising edge of PCICLK.
WRB	I/O	163	For slave mode operation the active low write strobe (WRB) signal is configured as an input. WRB is low during a LASAR-155 Microprocessor Interface Port register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. For master mode operation the active low write strobe (WRB) signal is configured as an output. WRB is low during a LASAR-155 Local Bus write accesses. D[7:0] bus contents are clocked into the addressed memory location of the device being written to on the rising WRB edge while either CS1B or CS2B is low. For this mode of operation WRB is generated on the rising edge of PCICLK.

D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9]/A[9] D[10]/A[10] D[11]/A[11] D[12]/A[12] D[13]/A[13] D[14]/A[14] D[15]/A[15]	I/O	164 167 168 169 170 171 172 173 174 188 189 190 191 192 193 194	For slave mode operation the bi-directional data bus D[15:0] is used during LASAR-155 Microprocessor Interface Port register read and write accesses. Little-endian byte formatting is used. D[15:8] should contain the most significant byte of a word while D[7:0] should contain the least significant byte of a word. For master mode operation, only D[7:0] is used for LASAR-155 Local Bus accesses data transfers. A[15:9] are configured as outputs and supply the most significant seven bits of the address on the LASAR-155 Local Bus. For this mode of operation A[15:9] are updated on the rising edge of PCICLK. Note, D[8] is not used and should be pulled high.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8]	I/O	175 176 177 178 179 180 181 186 187	For slave mode operation the address bus A[8:0] is configured as inputs. A[8:0] selects specific Microprocessor Interface Port registers during LASAR-155 register accesses. A[8] is the Test Register Select (TRS) address pin. TRS selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. For master mode operation the A[8:0] bus is configured as an output. A[8:0] supplies the least significant nine bits of the address on the LASAR-155 Local Bus. For this mode of operation A[8:0] are updated on the rising edge of PCICLK.

ALE/CS2B	I/O	160	For slave mode operation the address latch enable (ALE) is configured as an input. ALE is active high and latches the address bus A[8:0] when low. When ALE is high, the internal address latches are transparent. It allows the LASAR-155 to interface to a multiplexed address/data bus. For master mode operation the active low chip select two (CS2B) signal is configured as an output. CS2B is set low during LASAR-155 Local Bus accesses to the expansion ROM address space as defined using the Expansion ROM Base Address register. CS2B is generated on the rising edge of PCICLK for this mode of operation.
INTB	OD I/O	159	For slave mode operation (MPENB=0), the active low interrupt (INTB) signal is configured as an output. INTB goes low when a LASAR-155 interrupt source is active, and that source is unmasked. The LASAR-155 may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line far end receive failure (FERF), loss of pointer (LOP), path AIS, remote defect indication (RDI), and many others. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output. For slave mode operation, the LASAR-155 Master Interrupt Status register should be read to determine the source of the interrupt. For master mode operation (MPENB=1), the active low interrupt (INTB) signal is configured as an input. When INTB is low and enabled using the EXTINTBE bit in the LASAR-155 Master Interrupt Enable register and the EXTIE bit in the PCID Mailbox/Microprocessor Interrupt Status/Enable register, it is assumed that a device on the LASAR-155 Local Bus is requesting interrupt servicing. Servicing is indicated by asserting an interrupt using the PCI interrupt output, PCIINTB.

8.5 Miscellaneous Interface Signals (77)

Pin Name	Type	Pin No.	Feature
SYSCLK	Input	81	The system clock (SYSCLK) provides timing for the LASAR-155's Adaptation Layer hardware. SYSCLK should be nominally a 50% duty cycle 25 MHz to 33 MHz clock.
RSTB	Input	124	The active low reset (RSTB) signal provides an asynchronous LASAR-155 reset. RSTB is a Schmitt triggered input with an integral pull up resistor. When RSTB is forced low, all LASAR-155 registers are forced to their default states. In addition, all digital output pins with the exception of TDO are forced tri-state. Digital outputs remain tri-stated until RSTB is forced high.
TCK	Input	72	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	73	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	71	When the LASAR-155 is configured for JTAG operation, the test data input (TDI) signal carries test data into the LASAR-155 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	70	The test data output (TDO) signal carries test data out of the LASAR-155 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.

TRSTB	Input	74	The active low test reset (TRSTB) signal provides an asynchronous LASAR-155 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.
VDD_DC1 VDD_DC2 VDD_DC3 VDD_DC4 VDD_DC5 VDD_DC6 VDD_DC7 VDD_DC8 VDD_DC9 VDD_DC10	Power	10 28 54 80 97 129 154 165 182 199	The DC power pins should be connected to a well decoupled +5 V DC in common with VDD_AC.
VSS_DC1 VSS_DC2 VSS_DC3 VSS_DC4 VSS_DC5 VSS_DC6 VSS_DC7 VSS_DC8 VSS_DC9 VSS_DC10 VSS_DC11 VSS_DC12	Ground	9 27 53 79 83 95 130 131 156 166 185 197	The DC ground pins should be connected to GND in common with VSS_AC.

VDD_AC1 VDD_AC2 VDD_AC3 VDD_AC4 VDD_AC5 VDD_AC6 VDD_AC7 VDD_AC8 VDD_AC9 VDD_AC10 VDD_AC11 VDD_AC12 VDD_AC13 VDD_AC14 VDD_AC15 VDD_AC16	Power	4 11 17 22 38 43 48 55 60 65 82 98 133 183 202 207	The pad ring power pins should be connected to a well decoupled +5 V DC in common with VDD_DC
VSS_AC1 VSS_AC2 VSS_AC3 VSS_AC4 VSS_AC5 VSS_AC6 VSS_AC7 VSS_AC8 VSS_AC9 VSS_AC10 VSS_AC11 VSS_AC12 VSS_AC13 VSS_AC14 VSS_AC15 VSS_AC16	Ground	3 8 16 21 26 42 47 52 59 64 69 78 94 134 184 206	The pad ring ground pins should be connected to GND in common with VSS_DC.
TXVDD	Power	123	The transmit pad power (TXVDD) supplies the TXC and TXD+/- outputs. TXVDD is physically isolated from the other device power pins and should be a clean, well decoupled +5 V supply to minimize the noise coupled into the transmit stream.

TXVSS	Ground	128	The transmit pad ground (TXVSS) is the return path for the TXC and TXD+/- outputs. TXVSS is physically isolated from the other device ground pins and should be clean to minimize the noise coupled into the transmit stream.
TAVD1	Power	115	The power (TAVD1) pin for the transmit clock synthesizer reference circuitry. TAVD1 should be connected to a clean, well decoupled, +5V supply.
TAVS1	Ground	116	The ground (TAVS1) pin for the transmit clock synthesizer reference circuitry. TAVS1 should be connected to a clean ground reference.
TAVD2	Power	117	The power (TAVD2) pin for the transmit clock synthesizer oscillator. TAVD2 should be connected to a clean, well decoupled, +5V supply.
TAVS2	Ground	118	The ground (TAVS2) pin for the transmit clock synthesizer oscillator. TAVS2 should be connected to a clean ground reference.
TAVD3	Power	119	The power (TAVD3) pin for the transmit reference clock (TRCLK+/-) inputs. TAVD3 should be connected to a clean, well decoupled, +5V supply.
TAVS3	Ground	122	The ground (TAVS3) pin for the transmit reference clock (TRCLK+/-) inputs. TAVS3 should be connected to a clean ground reference.
RAVD1	Power	145	The power (RAVD1) pin for receive clock and data recovery block reference circuitry. RAVD1 should be connected to a clean, well decoupled, +5V supply.
RAVS1	Ground	151	The ground (RAVS1) pin for receive clock and data recovery block reference circuitry. RAVS1 should be connected to a clean ground reference.
RAVD2	Power	150	The power (RAVD2) pin for receive clock and data recovery block active loop filter and oscillator. RAVD2 should be connected to a clean, well decoupled, +5V supply.
RAVS2	Ground	146	The ground (RAVS2) pin for receive clock and data recovery block active loop filter and oscillator. RAVS2 should be connected to a clean ground reference.

RAVD3	Power	140	The power (RAVD3) pin for the RXD+/- and ALOS+/- PECL inputs. RAVD3 should be connected to a clean, well decoupled, +5V supply.
RAVS3	Ground	135	The ground (RAVS3) pin for the RXD+/- and ALOS+/- PECL inputs. RAVS3 should be connected to a clean ground reference.
RAVD4	Power	141	The power (RAVD4) pin for the RRCLK+/- PECL inputs. RAVD4 should be connected to a clean, well decoupled, +5V supply.
RAVS4	Ground	144	The ground (RAVS4) pin for the RRCLK+/- PECL inputs. RAVS4 should be connected to a clean ground reference.

Notes on Pin Description:

1. All LASAR-155 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels, with the exception of RXPHYBP and TXPHYBP I/O which are CMOS.

2. Most LASAR-155 digital outputs and bidirectionals have 4 mA drive capability, except the PCICLKO, TXD+ and TXD- outputs which have 8 mA drive capability; and the PCI outputs which have standard PCI drive capability.

3. Inputs RSTB, ROMP, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VSS_DC, VSS_AC, TXVSS, TAVS and RAVS ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage to the LASAR-155.

5. The VDD_DC , VDD_AC, TXVDD, TAVD and RAVD power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage to the LASAR-155.

6. The TAVD[3:1] and RAVD[4:1] pins provide power to sensitive analog circuitry in the LASAR-155. These signals should be connected to the PCB VDD power plane at a point where the supply is clean and as free as possible of digitally induced switching noise. In a typical system, TAVD and RAVD should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system VDD enters the PCB. In some systems a clean VDD supply cannot be readily obtained, and RAVD and TAVD may require separate regulation.

7. Each TAVD and RAVD pin should be separately decoupled using ceramic decoupling capacitors located as close as possible to the LASAR-155.

8. The TAVS[3:1] and RAVS[4:1] pins provide the ground return path for sensitive analog circuitry in the LASAR-155. These signals should be connected to the PCB ground plane at a point where the ground is clean and as free as possible of digital return currents. In a typical system, TAVS and RAVS should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system ground reference enters the PCB.

9. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.

10. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

11. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

12. Ensure that all digital power is applied simultaneously, and it is applied before the analog power is applied. Refer to the Power Sequencing description in the Operations section.

9 FUNCTIONAL DESCRIPTION

9.1 Receive Line Interface

The Receive Line Interface block performs clock and data recovery and performs serial to parallel conversion. The clock and data recovery unit can be bypassed using primary inputs to allow interworking the LASAR-155 with an external CRU.

9.1.1 Clock Recovery Unit

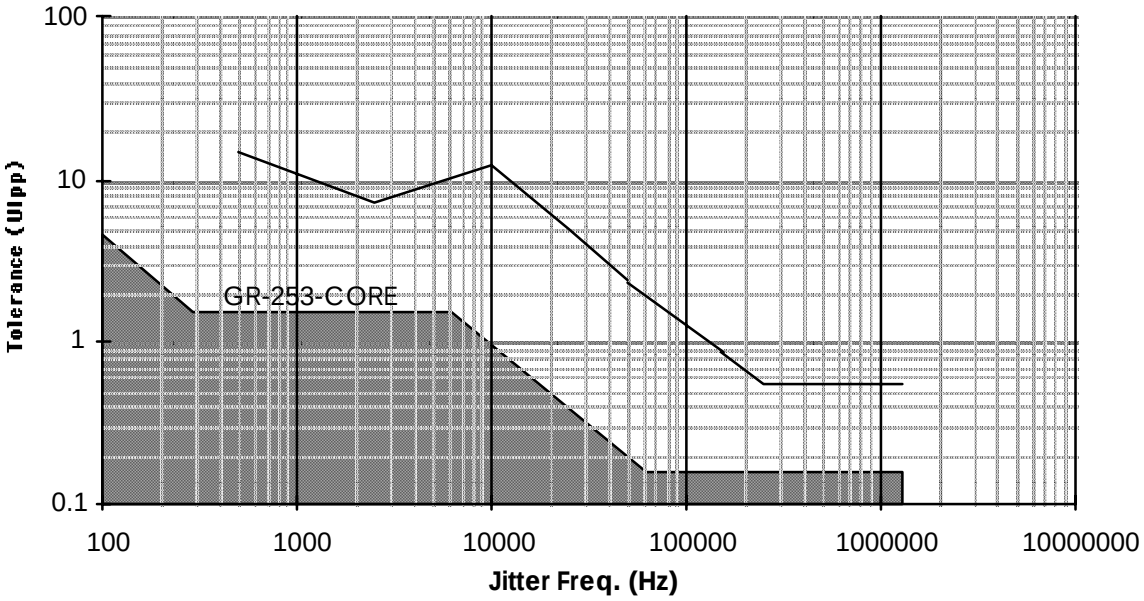
The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit will continue to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit can be configured to utilize reference clocks at 6.48 or 19.44 MHz. The clock recovery unit also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, RRCLK+/-. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the RRCLK+/- reference accuracy in the case of a loss of signal condition. In applications that are required to meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20 ppm. When not loop timed, the RRCLK+/- accuracy may be relaxed to +/-50 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by GR-253-CORE (Figure 9.1). The jitter tolerance illustrated is associated with the external loop filter components recommended in the Operation section.

9.1.1.1 Fig. 9.1 Jitter Tolerance Mask



Note that for frequencies below 300 Hz the jitter tolerance is greater than 15 UIpp; 15 UIpp is the maximum jitter tolerance of the test equipment. Also note that the dip in the tolerance curve between 300 Hz and 10 kHz is due to the LASAR-155's internal clock difference detector: if the recovered clock drifts beyond 488 ppm of the reference, the PLL locks to the reference clock.

9.1.2 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial SONET stream to a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

9.2 Receive Framer and Overhead Processor

The Receive Framer and Overhead Processor block frames to an incoming STS-3c (STM-1) or STS-1 SONET/SDH stream and performs all the SONET section, line and path overhead processing. Section, line and path processing are performed using the Receive Section Overhead, Receive Line Overhead and the Receive Path Overhead Processors as described below.

9.2.1 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm detection (LOS, OOF,LOF) and performance monitoring.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received. While out-of-frame, the RSOP depends on the SIPO block to monitor the bit serial data stream for an occurrence of the framing pattern. When a framing pattern has been recognized, the RSOP verifies that an error free framing pattern is present in the next frame before declaring in-frame.

When in-frame, descrambling is performed using the standard generating polynomial $1 + x^6 + x^7$. Section BIP-8 calculation and verification is automatically performed with errors accumulated into an internal saturating one second counter. A loss of signal (LOS) condition is declared when 20 ± 3 µs of all zeros pattern is detected. LOS is cleared when two valid framing words are detected and during the intervening time, no LOS condition is detected. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. LOF is cleared when an in-frame condition persists for a period of 3 ms.

9.2.2 Receive Line Overhead Processor

The Receive Line Overhead Processor (RLOP) provides line level alarm detection (line FERF, line AIS) and performance monitoring.

Line Far End Receive Failure (FERF) is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for five consecutive frames. FERF is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. Line Alarm Indication Signal (AIS) is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte, for five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

Line BIP-24/8 calculation and verification is automatically performed with errors accumulated into an internal saturating one second (STS-3c (STM-1) rate) counter. Accumulation of line far end block error (FEBE) indications into an internal saturating one second (STS-3c (STM-1) rate) counter is also provided.

9.2.3 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, path level alarm detection (LOP, path AIS, RDI) and performance monitoring. Pointer interpretation conforms to both Bellcore and ETSI standards.

The RPOP interprets the incoming pointer (H1, H2) as specified in the references. Loss of pointer (LOP) in the incoming STS-3c (STM-1) or STS-1 is declared as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. LOP is removed when the same valid pointer with normal NDF is detected for three consecutive frames. Path Alarm Indication Signal (PAIS) in the incoming STS-1/3c stream is declared after three consecutive AIS indications. PAIS is removed when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid pointer with NDF enabled is detected. Path Remote Defect Indication (RDI) is raise when bit 5 of the path G1 byte is set high for five consecutive frames. Path RDI is cleared when bit 5 is low for five consecutive frames.

Path BIP-8 calculation and verification is automatically performed with errors accumulated into an internal saturating one second (STS-3c (STM-1) rate) counter. Accumulation of path far end block error (FEBE) indications into an internal saturating one second (STS-3c rate) counter is also provided.

9.3 Receive ATM Cell Processor

The Receive ATM Cell Processor (RACP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection, cell filtering based on HEC error detection, Generic Flow Control (GFC) field extraction, ATM layer alarm detection (OCD, LCD) and performs ATM cell payload descrambling.

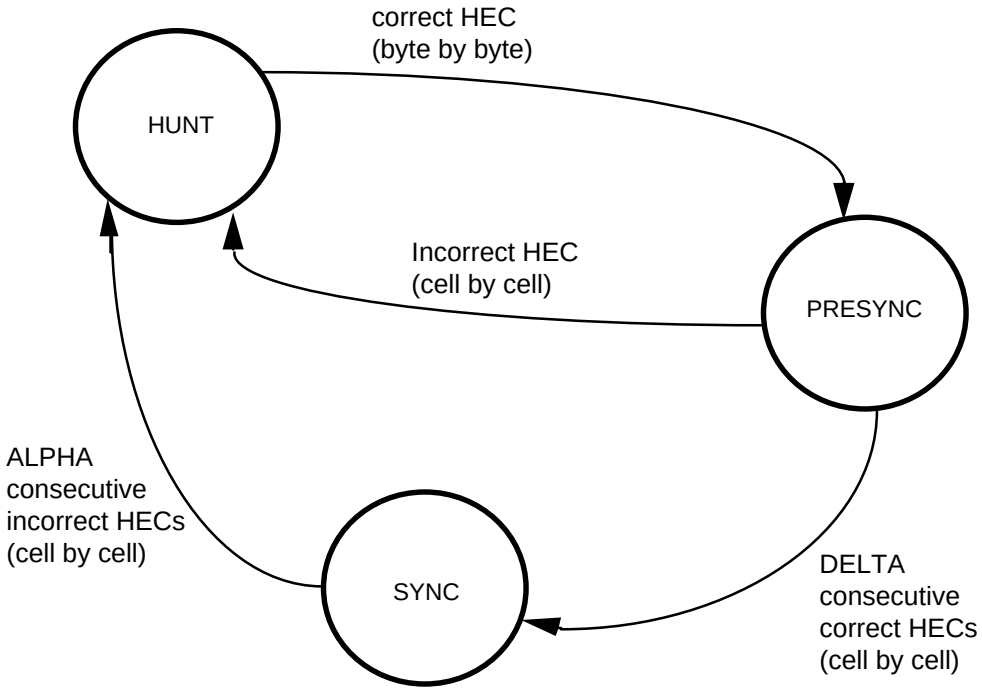
In addition, the number of received assigned cells is accumulated in a one second (STS-3c/STM-1 rate) saturating counter.

9.3.1 Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header error code (HEC) field found in the cell header. The HEC is a CRC-8 calculation over the first 4 octets of the ATM cell header. Cell delineation is performed using the Cell Delineation State Diagram as illustrated below. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in a maximum average time to delineate of 31 µs for STS-3c (STM-1) and 93 µs for STS-1. When in the HUNT state, the RACP block asserts the out of cell delineation (OCD) alarm. If OCD

persists for 4 ms, loss of cell delineation is asserted (LCD). LCD is removed when no OCD condition has been detected for 4 ms.

9.3.1.1 Fig. 9.2 Cell Delineation State Diagram

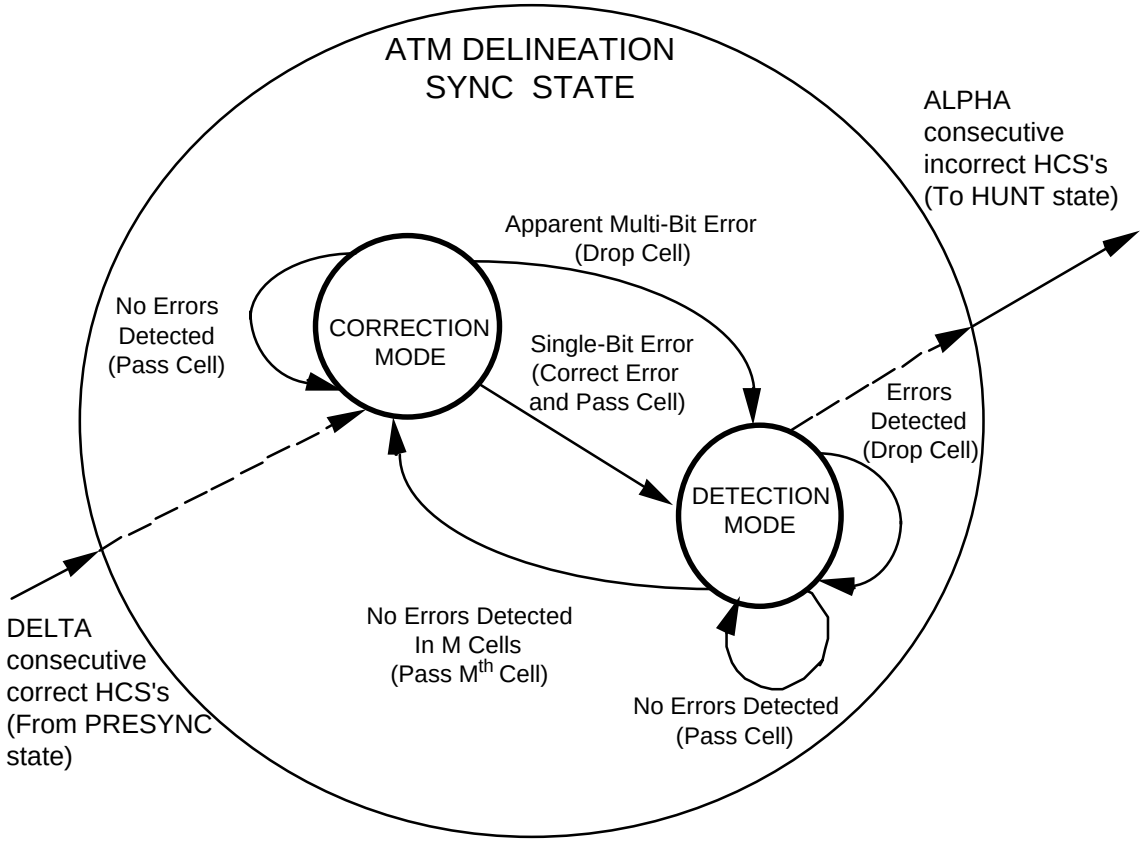


9.3.2 Cell Filter and HEC Verification

Cells are filtered (or dropped) based on HEC errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RACP registers. When both filtering and HEC checking are enabled, cells are dropped if uncorrectable HEC errors are detected, or if the corrected header contents match the pattern contained in the RACP Match Header Pattern and RACP Match Header Mask registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the RACP Match Header Pattern and RACP Match Header Mask registers.

The HEC is a CRC-8 calculation over the first 4 octets of the ATM cell header using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$ is optionally added (modulo 2) to the received HEC octet before comparison with the calculated result. While the Cell Delineation State Machine (described above) is in the SYNC state, the HEC verification circuit implements the state machine shown below.

9.3.2.1 Fig. 9.3 HEC Verification State Diagram



In normal operation, the HEC verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HEC errors are passed for further ATM/AAL layer processing. In addition, incoming cells with single-bit errors are corrected and the resulting cells are passed for further ATM/AAL layer processing. Upon detection of a single- bit error or a multi-bit error, the state machine transitions to the 'Detection Mode' state. In this state, programmable HEC error filtering is provided. The detection of any HEC error causes the corresponding cell to be dropped. The state machine transitions back to the 'Correction Mode' state when M (where M = 1, 2, 4, 8) cells are received with correct HCSs. The M^{th} cell is not discarded.

Two 8-bit saturating one second HEC error event counters are provided to accumulate correctable HEC errors and uncorrectable HEC errors. Counters are enabled only when the RACP is in the SYNC state.

9.3.3 GFC Extraction

The four GFC bits are extracted and serialized out via output RGFC/RLD if enabled using the UNI_POTS bit in the LASAR-155 Master Configuration register. The updating of RGFC by particular GFC bits may be disabled through an internal register. By default, RGFC only outputs the state of the most significant GFC bit, thus allowing this output to be used as a XON/XOFF indication for controlled data terminal applications. The serial link is forced low if cell delineation is lost.

9.3.4 Payload Descrambling

The self synchronous descrambler operates on the 48 byte cell payload using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HEC fields, and may optionally be disabled.

9.4 Receive ATM and Adaptation Layer Cell Processor

The Receive ATM and Adaptation Layer Cell Processor (RALP) performs ATM layer and AAL Type 5 (AAL-5) layer processing. In addition, if enabled, the RALP also performs VC aging and non-activity termination. Please refer to the Operations section for the ATM header fields and the AAL-5 protocol data unit structures.

9.4.1 ATM Layer Processing

ATM Layer processing includes open VC verification, cell filtering, cell copying and CRC-10 verification. Cell filtering is the action of not passing cells to the PCI Host. Cell copying is the action of copying cells to the Multipurpose Port. Cell filtering and cell copying are mutually exclusive.

For every incoming cell, the RALP must verify that the VPI and VCI header fields correspond to an open VC. Since only 128 VCs are allowed, a subset of the VPI and VCI field bits are required to identify the VC. Selection of which VPI and VCI bits contribute to the formation of the VPI/VCI code is programmable. If a cell arrives and its VPI /VCI code does not identify an open VC, the cell is filtered.

Given that the incoming cell can be associated with an open VC, the RALP block interprets the PTI fields to identify what payload is being carried. For F4 and F5 OAM cells, the CRC-10 is optionally verified using the polynomial, $x^{10}+x^9+x^5+x^4+1$. If configured, cells can be filtered based on illegal PTI codepoints (110, 111), F5 OAM flows (100, 101), specific VPI/VCI codes (i.e. F4 OAM cells) or cells with CRC-10 errors. Filtered cells are not passed onto the PCI Host and are accumulated in the SAR PMON block.

Cell copying is only supported if the LASAR-155's receive Multipurpose Port is enabled to source cells using input RXPHYBP. If enabled as a cell source, cell copying to the Multipurpose Port can be based on the VPI/VCI code and/or PTI codepoints.

9.4.2 AAL Layer Processing

AAL Layer processing includes Common Part Convergence Sublayer AAL Type 5 Protocol Data Unit (CPAAL5_PDU) reassembly and verification. In addition, a mechanism for smooth reassembly startup and smooth reassembly shutdown is provided.

The RALP performs CPAAL5_PDU reassembly by associating cells with the same VPI/VCI code with a CPAAL5_PDU. The normal indication of the end of a CPAAL5_PDU is provided using a PTI codepoint while the start of a CPAAL5_PDU is implicit based on the previous CPAAL5_PDU end indication. When a VC is first provisioned for reception and a cell for the VC arrives, the RALP starts to reassemble a CPAAL5_PDU. As additional cells of a CPAAL5_PDU are received, the RALP continues to accumulate cells for a given CPAAL5_PDU until the CPAAL5_PDU is terminated either normally or abnormally through an exception. Reassembly is facilitated using the PCI DMA Controller (PCID) block.

Normal termination of a CPAAL5_PDU results from the reception of a cell with the appropriate PTI codepoint and valid CPAAL5_PDU Length, Control and CRC-32 fields. The CRC-32 polynomial used is:

$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$.

Abnormal termination of a CPAAL5_PDU can result from either CPAAL5_PDU length exceptions, Control field exceptions or CRC-32 exceptions. Length exceptions can result from either the receive CPAAL5_PDU LENGTH field not matching the received number of CPAAL5_SDU octets, the receive CPAAL5_PDU LENGTH field equal to zero (indicating a forward abort) or the received CPAAL5_PDU exceeding the maximum CPAAL5_PDU size. If the current CPAAL5_PDU under reassembly exceeds the maximum CPAAL5_PDU size, the CPAAL5_PDU is terminated and all additional cells received are dropped until the last cell of the CPAAL5_PDU is received. The maximum CPAAL5_PDU size can be user programmed. Control field exceptions result when the received CPAAL5_PDU CPI field is non zero. A CRC-32 exception results when the calculated CRC-32 over the received CPAAL5_PDU does not produce the expected residue.

The RALP block also provides smooth reassembly shut down. Through user control, the RALP can be configured to either stop reassembly on all VCs immediately or after the active CPAAL5_PDU has been reassembled.

9.5 Connection Parameter Store

The Connection Parameter Store (COPS) block provides the internal VC parameter storage for both the 128 receive VCs and 128 transmit VCs. The COPS block provides VC parameter access to the RALP, TATS and TALP blocks. In addition, indirect access to the parameter memory space is also provided to the microprocessor and PCI Host.

9.6 SAR Performance Monitor

The SAR Performance Monitor (SAR PMON) block interfaces directly to the RALP and PCID blocks and accumulates the following statistics:

- ATM Cell unprovisioned VPI/VCI errors
- ATM Cell CRC-10 errors
- Receive CPAAL5_PDU Invalid Common Part Indicator errors
- Receive CPAAL5_PDU Invalid SDU Length errors
- Receive CPAAL5_PDU CRC-32 errors
- Receive CPAAL5_PDU Oversize PDU errors
- Receive CPAAL5_PDU Abort errors
- Receive CPAAL5_PDU Count
- Receive Buffer errors
- Transmit CPAAL5_PDU Oversize SDU errors
- Transmit CPAAL5_PDU Count

Counts are accumulated in saturating counters. ATM Cell counters are sized such that they can be polled once per second. Packet registers are sized such that they can be polled once per second given that every CPAAL5_PDU is in error and the average packet size is 8 cells. If CPAAL5_PDU characteristics are different and exact CPAAL5_PDU counts must be maintained, the user must poll every 125 ms. When the RACP block declared loss of cell delineation (LCD), no receive statistics are accumulated.

The user can indicate the end of an accumulation interval by writing to the LASAR-155 Master Reset / Load Meters register. The write will transfer the current counter values into visible registers and will reset the counters to begin accumulating error events for the next interval. Writing to the LASAR-155 Master Reset / Load Meters register initiates transfers for all counters in all blocks (i.e. RSOP, RLOP, RPOP, RACP, TACP and SAR PMON).

9.7 Transmit ATM Traffic Shaper

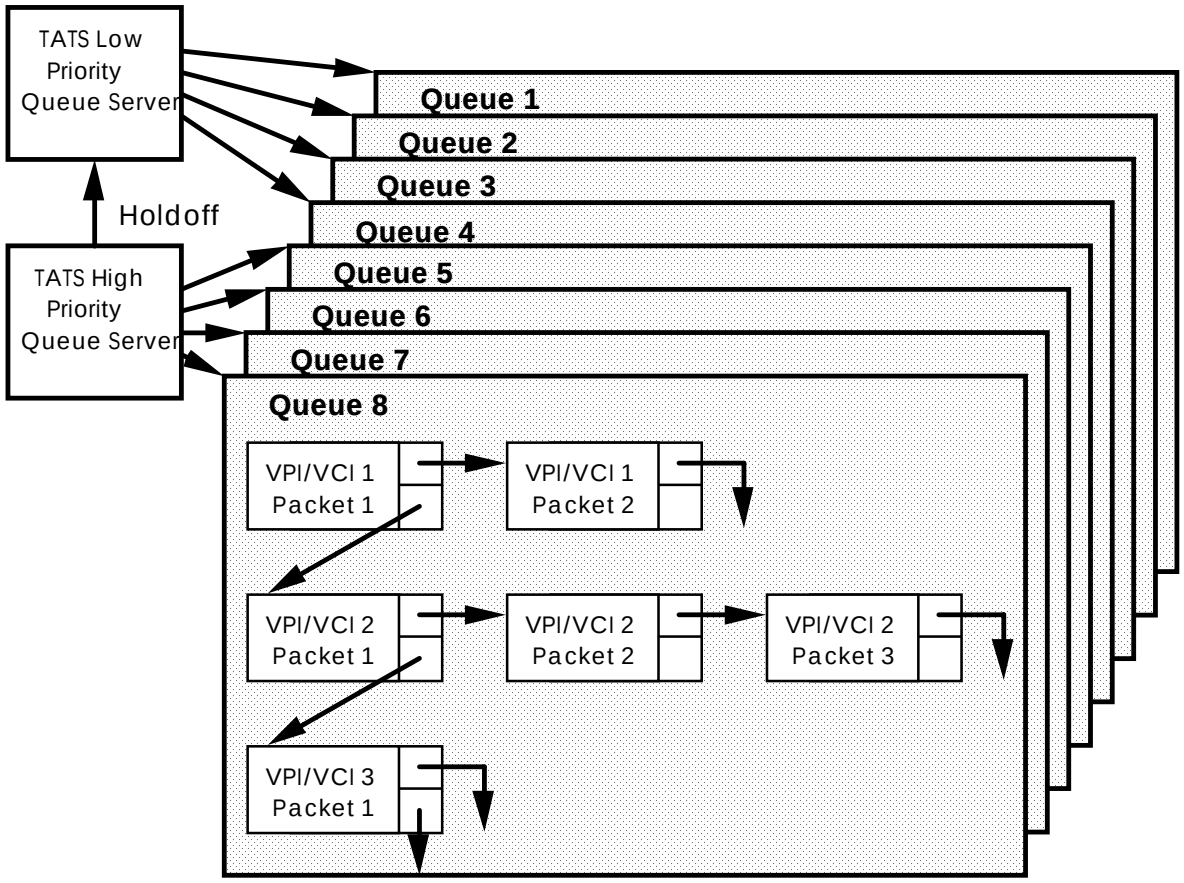
The Transmit ATM Traffic Shaper (TATS) block provides for Variable Bit Rate (VBR) traffic shaping. VBR traffic shaping requires each VC to conform to peak cell rate enforcement, using peak cell rate queues, and sustainable cell rate enforcement, using peak cell rate queues coupled with token bucket averaging. In addition a proprietary Credit Based Rate Control (CBRC) algorithm can be applied to the Variable Bit Rate (VBR) VCs.

9.7.1 Rate Queue Structures

The TATS block provides for eight peak cell rate queues arranged as a group of four high priority queues and a group of four low priority queues. As part of the provisioning process, a VC must be associated with one of the eight rate queues. Once a VC is provisioned, packets supplied by the PCI Host are attached to the associated rate queue as conceptually shown below. Successive packets of an existing VC are linked to the existing packets waiting to be transmitted over the VC in question.

To enforce fairness, rate queues are serviced in a round-robin fashion on a per queue group basis. High priority queues are serviced in a round-robin manner before the low priority queues. If the high priority queues consume all the available link bandwidth, the low priority queues are allowed to starve. An indication is provided to indicate if any queue has experienced a starvation condition. Servicing of low priority queues is allowed to be pre-empted by high priority queues. Once the TATS begins to service a high priority queue , the queue will be completely serviced before another queue is serviced. For both low and high priority queues, VCs on the same queue are serviced on a round-robin fashion.

9.7.1.1 Fig. 9.4 Peak Cell Rate Queues Diagram



9.7.2 Peak Cell Rate (PCR) and Sustainable Cell Rate (SCR) Transmission

The TATS allows packet transmission at either the PCR or the SCR based on the generation of tokens. PCR transmission is defined on a per VC basis by associating a VC with one of the eight rate queues and by selecting whether to use 100%, 50% or 25% of the peak cell rate provided by the queue. SCR transmission is defined on a per VC basis by allowing generation of tokens at the PCR or at some fraction (1/n where n = 1 to 8) of the PCR.

The TATS provides each VC with a programmable size token bucket. Transmission over a VC is only permitted if the VC's bucket is not empty. Given that the link is idle, the TATS will fill a VC's token bucket at the SCR until either the bucket is full or until a packet needs to be transmitted. If the bucket becomes full, additional generated tokens are discarded. If a packet needs to be segmented and transmitted over a VC, the TATS transmits cells at the PCR consuming one token for every cell transmitted. Transmission at the PCR is maintained until the bucket is

empty. In this way, the maximum burst is defined by the selectable bucket capacity. When the bucket is empty, transmission continues at the SCR or the rate of token generation.

9.7.3 CBRC Support

VBR VCs are subject to both PCR and SCR traffic shaping as described above. However in addition to PCR and SCR shaping, for VCs that are subjected to CBRC, the TATS maintains an aggregate credit count to allow the network to back pressure transmission.

A user programmable number of credits are issues by the network using the second most significant bit of the GFC field in the cell flow from the network to the LASAR-155 device. After each cell transmission for a CBRC VC, the TATS decrements the credit count. Cell transmission for all CBRC VCs continues until the credit supply is exhausted at which point the TATS suspends transmission of all VCs subjected to CBRC until the network issues more credits.

9.8 Transmit ATM and Adaptation Layer Cell Processor

The Transmit ATM and Adaptation Layer Cell Processor (TALP) performs ATM layer and AAL (Type 5) layer processing. Please refer to the Operations Section for the ATM header fields and the AAL-5 protocol data unit structures.

9.8.1 AAL Layer Processing

The TALP block performs packet segmentation with the help of the TATS and PCID blocks. As described above, the TATS block schedules when cells from a CPAAL5_PDU under segmentation should be sent. The PCID block actually performs the segmentation and retrieves the packet's bytes from the host packet memory. The TALP block aids in segmentation by calculating the CPAAL5_PDU's CRC-32 field and adding the CPAAL5_PDU CRC-32 field to form the entire CPAAL5_PDU. The CRC-32 polynomial used is:

$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$.

9.8.2 ATM Layer Processing

ATM Layer processing includes generating the GFC, VPI, VCI, PTI, CLP fields and optionally generating the CRC-10 field for each cell transmitted. In addition, the TALP provides the ability to multiplex cells in from the Multipurpose Port and to enforce an aggregate peak cell rate (APCR).

For each cell, the TALP block generates the GFC, VPI, VCI, PTI and CLP cell header fields. The GFC, VPI and VCI fields are inserted from the values programmed when the VC was initially provisioned. The PTI and CLP fields are inserted from the default values from when the VC was initially provisioned or as specified by the PCI Host on a per packet basis.

CRC-10 field generation and inclusion is provided to support F4 and F5 OAM cell generation. For F4 and F5 OAM cells, the CRC-10 is generated using the polynomial, $x^{10}+x^9+x^5+x^4+1$. The OAM cell flow is expected to be either from the PCI Host or through the Multipurpose Port. When the flow is through the Multipurpose Port, the ATM header bytes GFC, VPI, VCI, PTI and CLP must be pre-pended by the external cell source.

The Multipurpose Port is provided to allow either insertion of CBR cells and/or OAM cells into the cell stream. When the port indicates that a cell is ready to be transmitted, the TALP block either inserts the cell into the aggregate cell stream at the earliest opportunity or waits until no cells are being sourced from the PCI Host before inserting the cell into the aggregate cell stream. The selection of the insertion mode is made using the CINPORT_PR bit in the TALP Control register.

No per VC traffic shaping is applied to this stream. Only traffic shaping of the aggregate cell stream sourced from the Multipurpose Port is provided.

The TALP block enforces an APCR on the aggregate cell stream using a peak cell rate counter. The APCR can be selectable from 32 Kbps to the full rate of 149 Mbit/s for STS-3c (STM-1).

9.9 Transmit ATM Cell Processor

The Transmit ATM Cell Processor (TACP) provides rate adaptation via idle/unassigned cell insertion, provides HEC generation and insertion, provides GFC insertion and performs ATM cell scrambling.

Idle/Unassigned Cell are transmitted in the absence of assigned cells. Registers are provided to program the GFC, PTI, and CLP fields of the Idle/Unassigned cell header and the cell payload. The HEC is automatically calculated and inserted.

The HEC calculation over the first four header octets is performed using the polynomial, x^8+x^2+x+1. The coset polynomial, $x^6+x^4+x^2+1$ is optionally added (modulo 2) to the residue.

Scrambling is performed using the self synchronous scrambler, $x^{43}+1$. Scrambling is performed only over cell payloads; cell headers are not scrambled.

9.10 Transmit Transmitter and Overhead Processor

The Transmit Transmitter and Overhead Processor block inserts all path, line and section overhead bytes in the outgoing STS-3c (STM-1) or STS-1 SONET/SDH stream. Section, line and path overhead processing is performed using the Transmit Section Overhead, Transmit Line Overhead and the Transmit Path Overhead Processors as described below.

9.10.1 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), section BIP-8 (B1) insertion, scrambling and section level alarm signal insertion. The default section overhead bytes inserted by the TSOP are shown in the STS-3c (STM-1) Default Transport Overhead Values figure below.

The section BIP-8 code is based on a bit interleaved parity calculation using even parity calculated over all SONET frame bytes. The calculated BIP-8 code is inserted into the B1 byte of the following frame before scrambling.

Scrambling is performed using the generating polynomial $1 + x^6 + x^7$. All bytes of the SONET frame are scrambled except the framing bytes (A1, A2) and the identity bytes (C1).

For alarm assertion and diagnostics, line AIS can be forced, all zeros may be continuously inserted after scrambling (LOS) and BIP-8 errors may be continuously inserted.

9.10.2 Transmit Line Overhead Processor

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion and line BIP-8/24 insertion (B2). The default line overhead bytes inserted by the TLOP are shown in the STS-3c (STM-1) Default Transport Overhead Values figure below.

The line BIP-8/24 code is based on a bit interleaved parity calculation using even parity calculated over all SONET frame bytes except the section overhead bytes. The calculated BIP-8/24 code is inserted into the B2 byte(s) of the following frame.

For alarm assertion and diagnostics, line FERF can be forced (K2), line FEBE can be automatically accumulated and inserted (Z2) and BIP-8/24 errors may be continuously inserted.

9.10.2.1 Fig. 9.5 STS-3c (STM-1) Default Transport Overhead Values

A1 (0xF6)	A1 (0xF6)	A1 (0xF6)	A2 (0x28)	A2 (0x28)	A2 (0x28)	C1 (0x01)	C1 (0x02)	C1 (0x03)
B1 (*)	(0x00)	(0x00)	E1 (0x00)	(0x00)	(0x00)	F1 (0x00)	(0x00)	(0x00)
D1 (0x00)	(0x00)	(0x00)	D2 (0x00)	(0x00)	(0x00)	D3 (0x00)	(0x00)	(0x00)
H1 (0x6A)	H1 (0x93)	H1 (0x93)	H2 (0x0A)	H2 (0xFF)	H2 (0xFF)	H3 (0x00)	H3 (0x00)	H3 (0x00)
B2 (*)	B2 (*)	B2 (*)	K1 (0x00)	(0x00)	(0x00)	K2 (0x00)	(0x00)	(0x00)
D4 (0x00)	(0x00)	(0x00)	D5 (0x00)	(0x00)	(0x00)	D6 (0x00)	(0x00)	(0x00)
D7 (0x00)	(0x00)	(0x00)	D8 (0x00)	(0x00)	(0x00)	D9 (0x00)	(0x00)	(0x00)
D10 (0x00)	(0x00)	(0x00)	D11 (0x00)	(0x00)	(0x00)	D12 (0x00)	(0x00)	(0x00)
Z1 (0x00)	Z1 (0x00)	Z1 (0x00)	Z2 (0x00)	Z2 (0x00)	Z2 (*)	E2 (0x00)	(0x00)	(0x00)

* : B1, B2 values depend on payload contents
Z2 value depends on incoming line bit errors

9.10.2.2 Fig. 9.6 STS-1 Default Transport Overhead Values

A1 (0xF6)	A2 (0x28)	C1 (0x01)
B1 (*)	E1 (0x00)	F1 (0x00)
D1 (0x00)	D2 (0x00)	D3 (0x00)
H1 (0x6A)	H2 (0x0A)	H3 (0x00)
B2 (*)	K1 (0x00)	K2 (0x00)
D4 (0x00)	D5 (0x00)	D6 (0x00)
D7 (0x00)	D8 (0x00)	D9 (0x00)
D10 (0x00)	D11 (0x00)	D12 (0x00)
Z1 (0x00)	Z2 (*)	E2 (0x00)

* : B1, B2 values depend on payload contents
Z2 value depends on incoming line bit errors

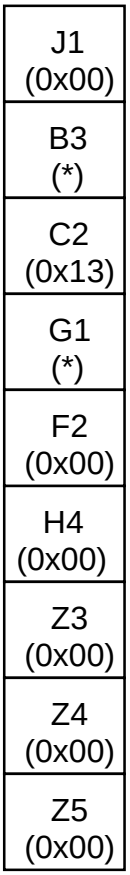
9.11 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion, insertion of the synchronous payload envelope, path BIP-8 (B3) insertion and the insertion of path level alarm signals. The default line overhead bytes inserted by the TPOP are shown in the Default Path Overhead Values figure below.

The TPOP generates the outgoing pointer as specified in the references. On startup, the pointer value defaults to 522, the byte after the C1 byte.The path BIP-8 code is based on a bit interleaved parity calculation using even parity calculated over all SONET synchronous payload envelope (SPE) bytes. The calculated BIP-8 code is inserted into the B3 byte of the following frame.

For alarm assertion and diagnostics, path Remote Defect Indication (RDI) can be forced, path FEBE can be automatically accumulated and inserted (G1), BIP-8 errors may be continuously inserted and pointers can be incremented, decremented or arbitrarily forced.

9.11.1.1 Fig. 9.7 Default Path Overhead Values



* : B3 value depend on payload contents
G1 value depends on incoming path bit errors

9.12 Transmit Line Interface

The Transmit Line Interface block performs clock synthesis and performs parallel to serial conversion. The clock synthesis unit can be bypassed using primary inputs to allow operation with an external line rate clock source.

9.12.1 Clock Synthesis

The transmit clock may be synthesized from a 19.44 MHz or 6.48 MHz reference. The phase lock loop filter transfer function is optimized to enable the PLL to track the reference, yet attenuate high frequency jitter on the reference signal. This transfer function yields a typical low pass corner of 1 MHz, above which reference jitter is attenuated at 3 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference, the intrinsic jitter is typically less than 0.01 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency.

9.12.2 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the internal byte serial stream to a bit serial stream.

9.13 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The LASAR-155 identification code is 073750CD hexadecimal.

9.14 PCI DMA Controller Interface

The PCI DMA Controller (PCID) block provides an interface to the PCI Local Bus to facilitate data transfer to and from the LASAR-155. When the LASAR-155 is the initiator, the PCID uses burst DMA cycles to read or write data on the PCI Bus which minimizes PCI Host bus traffic. When the LASAR-155 is the target, the PCID allows the PCI Host to access the LASAR-155's internal registers, to communicate with the microprocessor or to access external devices when the microprocessor is not present. Communication with an optional microprocessor is facilitated using a mailbox scheme.

The PCID block provides two transmit and two receive DMA channels to move packets to and from the LASAR-155. The receive DMA channels are divided into management data and packet data channels. The transmit DMA channels are divided into high priority and low priority channels. The DMA channels support scatter/gather buffer manipulation to allow for flexible and independent operation with the PCI Host.

The PCID services the four DMA channels using either a round-robin scheme or a receive priority scheme. For the round-robin scheme, simultaneous DMA requests are serviced in a fair rotational manner. For the receive priority scheme, receive

DMA requests are always serviced before transmit DMA requests. Selection can be made by the user.

In the transmit direction, an eight cell queue is provided to allow prefetching of transmit cells to account for PCI bus latency. In the receive direction, a 96 cell queue is provided to allow for a 270 µs PCI bus latency.

9.14.1 PCI Interface and Mailbox

The LASAR-155 provides a PCI Local Bus Specifications Version 2.1 (PCID) interface. When operating as the target, the PCI Interface provides access to the LASAR-155 registers to configure the LASAR-155, monitor the LASAR-155 and to control the DMA queues. Register access is described in the microprocessor and PCI Host Register Memory Map Section below.

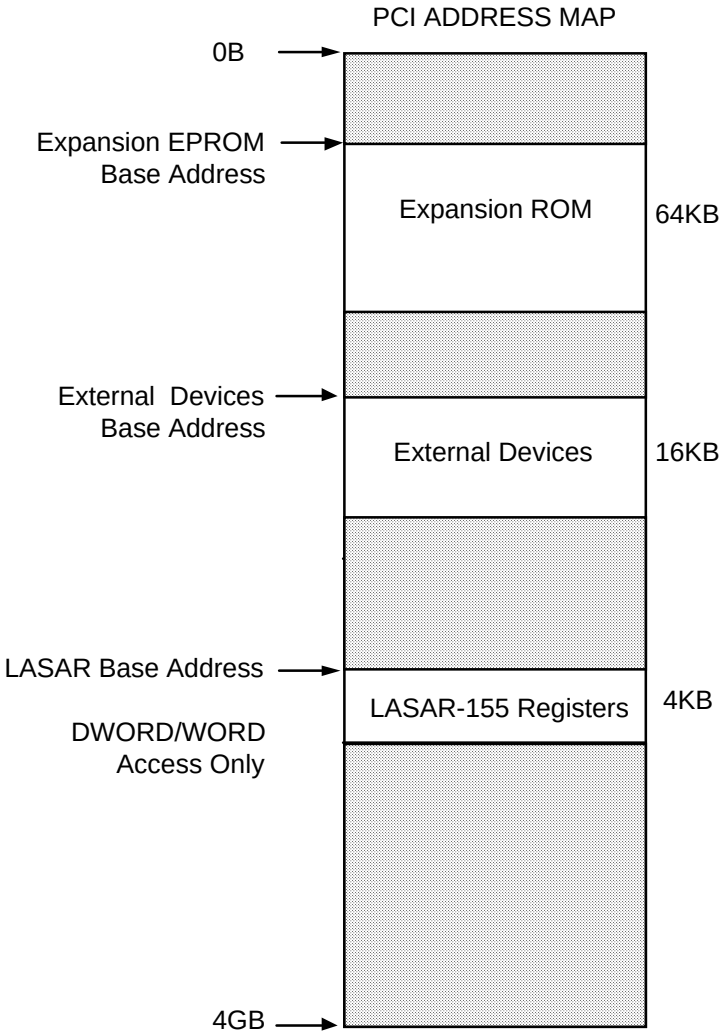
A mailbox scheme is provided to allow the PCI Host to communicate with an external microprocessor. Two 64 word buffers with associated semaphores are provided. One buffer is used for PCI Host to microprocessor communication while the other buffer is used for microprocessor to PCI Host communication. The data transfer format is implementation specific.

When the local microprocessor is present in the system, as indicated when the MPENB pin is sampled low, the PCI Host can only access dedicated registers. The base of the LASAR-155's internal address space is set via the LASAR-155 Memory Base Address register in the PCI Configuration memory space. The maximum size of the memory space is 4K Bytes. If the PCI Host wishes to access any registers controlled by the local microprocessor it must do so via the mailbox.

When the local microprocessor is not present, the PCI Host has direct access to all registers in the LASAR-155. In addition the PCI Host can access an Expansion EPROM and external devices via the LASAR-155 Local Bus. The base of the LASAR-155's internal address space is set via the LASAR-155 Memory Base Address register in the PCI Configuration memory space. The maximum size of the memory space is 4K Bytes. The Expansion EPROM space is set by the Expansion ROM Base Address Register in the PCI Configuration memory space. The maximum size of the memory space is 64K Bytes. The External device space is 16K Bytes maximum and is located using the External Device Memory Base Address register in the PCI Configuration memory space. The LASAR-155's PCI address map is shown below.

Note, both the LASAR-155 Memory and External Device Memory is DWORD and Word accessible only.

9.14.1.1 Fig. 9.8 LASAR-155 Address Map



9.14.2 Transmit Request Machine

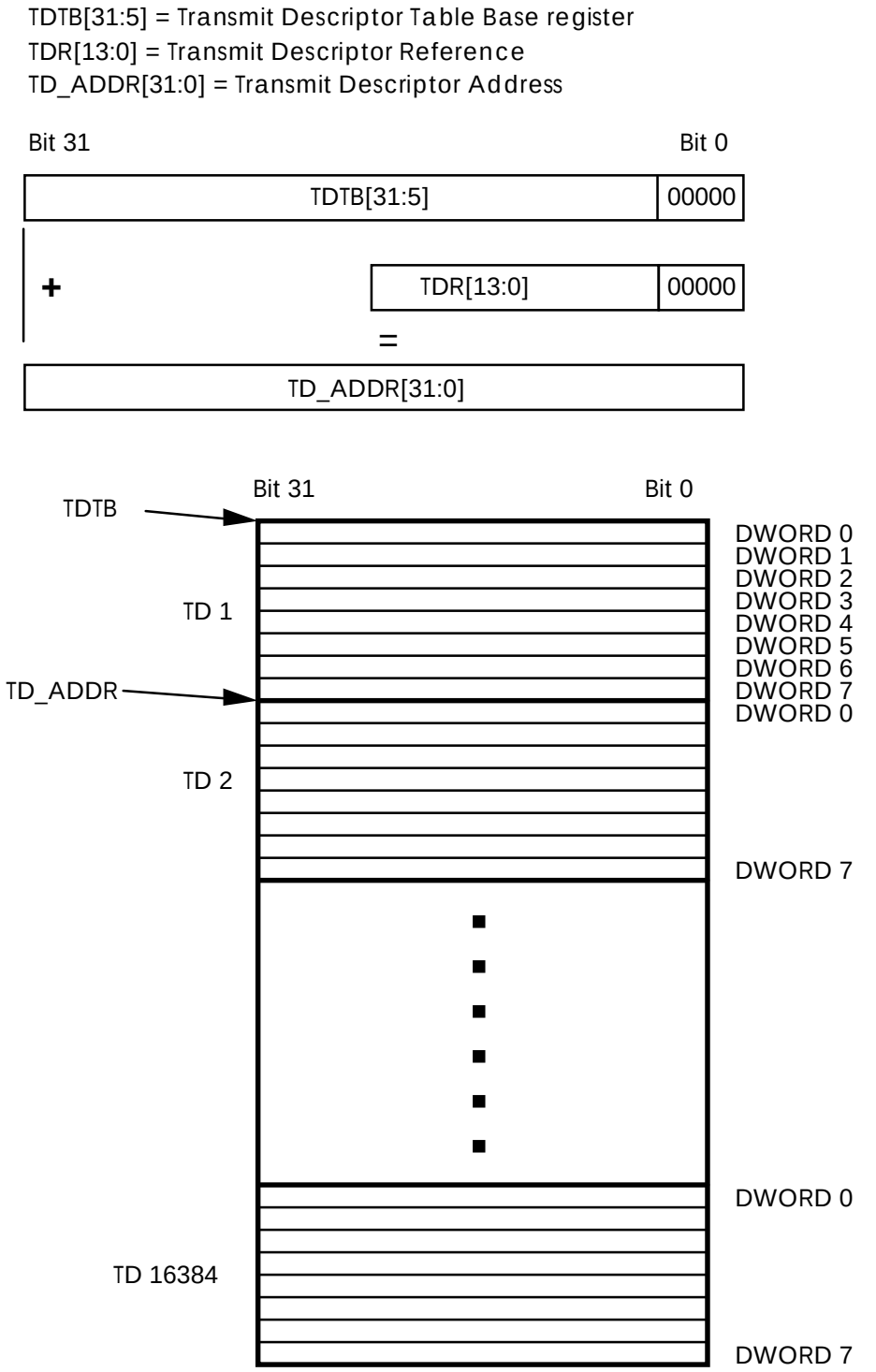
The transmit DMA channels are controlled using the Transmit Request Machine (TRM). The TRM receives segmentation requests from the TATS block, retrieves packet bytes using the PCI Interface and provides the bytes to the TALP block for inclusion into cells. All transmit DMA data transfer actions are performed with minimum PCI Host interaction with the aid of internal per VC storage.

PCI Host communication is provided using Transmit Descriptors (TD), a Transmit Descriptor Reference Free (TDRF) Queue and a Transmit Descriptor Reference Ready (TDRR) High and Low priority Queues. All four data structures are found in the PCI Host memory space and are referenced using LASAR-155 registers. A TD is a thirty-two byte data structure which can be used by the PCI Host to describe a packet or a portion of a packet. The TD data structure is fully described below in the Transmit Descriptor Section.

9.14.3 Transmit Descriptor Table

Each TD resides in the Transmit Descriptor Table in the PCI Host memory. The Transmit Descriptor Table can contain a maximum of 16384 TDs. The based of the Transmit Descriptor Table is user programmable using the PCID Transmit Descriptor Table Base (TDTB) register. As shown below, each TD can be located using a Transmit Descriptor Reference (TDR) combined with the TDTB register.

9.14.3.1 Fig. 9.9 Transmit Descriptor Table



9.14.4 Transmit Queues and Operation

TDRs describing TD of packet(s) are passed from the PCI Host to the TRM using the Transmit Descriptor Reference Ready (TDRR) Queues found in the PCI Host memory. Two ready queues are provided, a high priority and a low priority queue. TDs in the high priority queue get queued for transmission before TDs in the low priority queue. When packets associated with descriptors are transmitted is determined by the Transmit ATM Traffic Shaper (TATS) block.

TDRs describing TD of packet(s) that have been segmented and transmitted are passed from the TRM to the PCI Host using the Transmit Descriptor Reference Free (TDRF) Queue found in the PCI Host memory. Some buffering of TDs being returned to the TDRF Queue is optionally provided to decrease PCI bus accesses.

All three queues are defined using a common base pointer residing in the PCID Transmit Queue Base register and twelve offset pointers, four per queue. For each queue, two pointers are required to define the start and the end of a queue while two pointers are required for the current write and read locations within the queue. The read pointer always points to the last location read while the write pointer always points to the next location to be written.

A full condition for the queues is defined as the read and the write pointers being equal. An empty condition is defined as the read pointer one less then the write pointer. The last location in a queue is not considered as part of the queue and thus is not a valid entry.

Packets are assembled in PCI Host memory using TDs. Each TD contains control fields, a TD pointer reference field and a buffer pointer field. The control fields can be used by the PCI Host to associate a packet with an open VC and to inform the LASAR-155 how to segment the packet. If a packet requires more memory then available in the buffer referenced by the current TD, the PCI Host can link a new TD to the current TD using the current TD's TD pointer reference. When the PCI Host needs to transmit a packet, it formats a TD and adds the TD's TDR to the high or low priority TDRR Queue as shown below.

Once the TRM is notified that a packet has been added onto the TDRR Queue, it removes the TDR from the TDRR Queues, verifies that the VC the current packet is associated with is in fact open and adds the TDR to its internal transmit VC queues. Segmentation of the packet then proceeds at the negotiated VC traffic parameters as controlled by the TATS block. As TD buffers are consumed and become empty, the TRM attaches the TD's TDR to the TDRF Queue and indicates the success of the packet transmission in the TDR. In order to take advantage of burst PCI transfers, the TRM optionally buffers up to six TDs before attaching them to the TDRF Queue. If TD buffering is enabled, the TDs are flushed to the TDRF Queue

when six buffers have been accumulated or when a TD has been processed with its IOC bit set. Please refer to the Transmit Descriptor Data Structure Section for IOC bit details.

9.14.4.1 Fig. 9.10 TDRF and TDRR Queues

Transmit Descriptor Referance Queues

Base Address:

TQB[31:2] = Tx Queue Base register

Index Registers:

High Priority Ready:

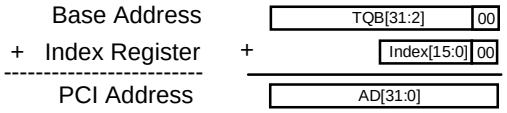
TDRHRQS[15:0] = TDR Ready High Queue Start register
TDRHRQW[15:0] = TDR Ready High Queue Write register
TDRHRQR[15:0] = TDR Ready High Queue Read register
TDRHRQE[15:0] = TDR Ready High Queue End register

Low Priority Ready:

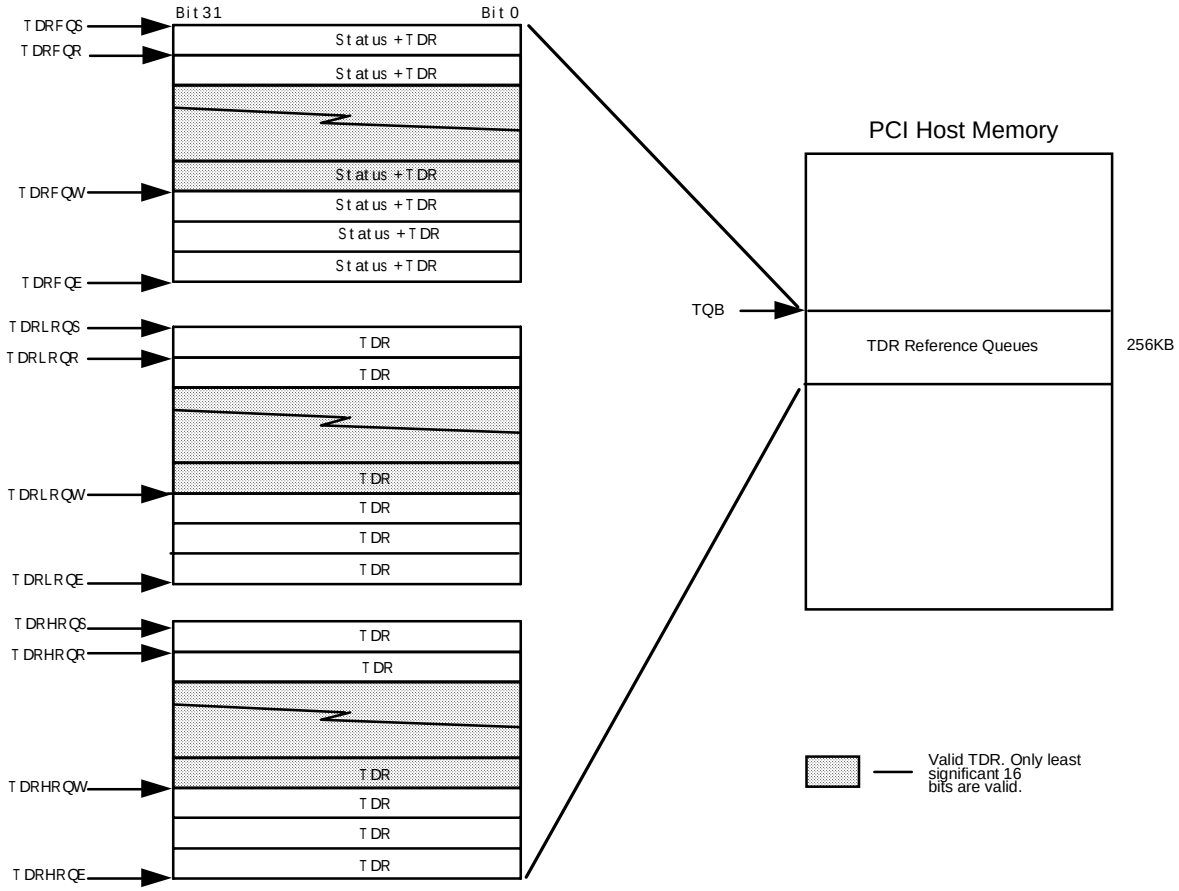
TDRLRQS[15:0] = TDR Ready Low Queue Start register
TDRLRQW[15:0] = TDR Ready Low Queue Write register
TDRLRQR[15:0] = TDR Ready Low Queue Read register
TDRLRQE[15:0] = TDR Ready Low Queue End register

Free:

TDRFQS[15:0] = TDR Free Queue Start register
TDRFQW[15:0] = TDR Free Queue Write register
TDRFQR[15:0] = TDR Free Queue Read register
TDRFQE[15:0] = TDR Free Queue End register

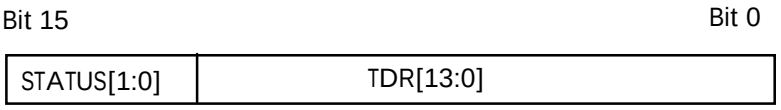


Tx Descriptor Reference Queue Memory Map



Each queue element is a sixteen bit structure consisting of a TDR and several Status bits. Status bits are used by the TRM to inform the PCI Host on the success of packet segmentation. Please refer below.

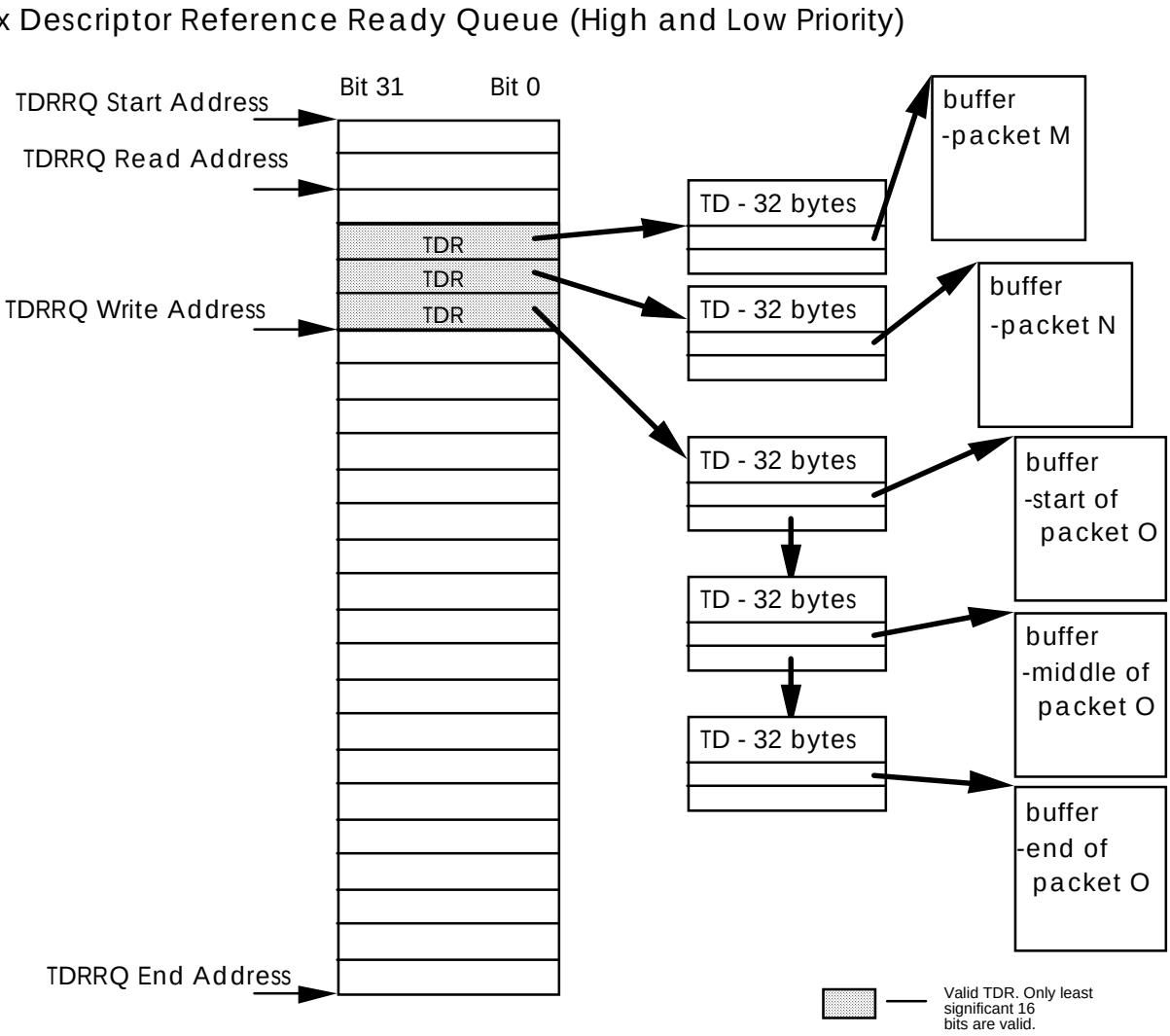
9.14.4.2 Fig. 9.11 TDRF Queue Elements



Status	Descriptor
00	Segmentation successful, last/only buffer of packet.
01	Segmentation successful, buffer of partial packet.
1x	Segmentation failed due to unprovisioned VC or Max SDU error.

If transmission of a packet over an unprovisioned VC or transmission of an oversized SDU packet is attempted, the TRM will abort transmission before the first cells has been transmitted and will attach the packet's TDR to the TDRF Queue with the segmentation failed status. In addition if a VC is unprovisioned and it is currently segmenting a packet, the current TDR of the packet will be returned with a segmentation failed status. Note, only the first TDR of the linked list of TDRs is attached to the TDRF Queue. The PCI Host can follow the Host Next TD Pointer and the PCID Next TD Pointer in the TD to recover all the buffers associated with the packet. Please refer to the Transmit Descriptor section for a detailed description of these pointers.

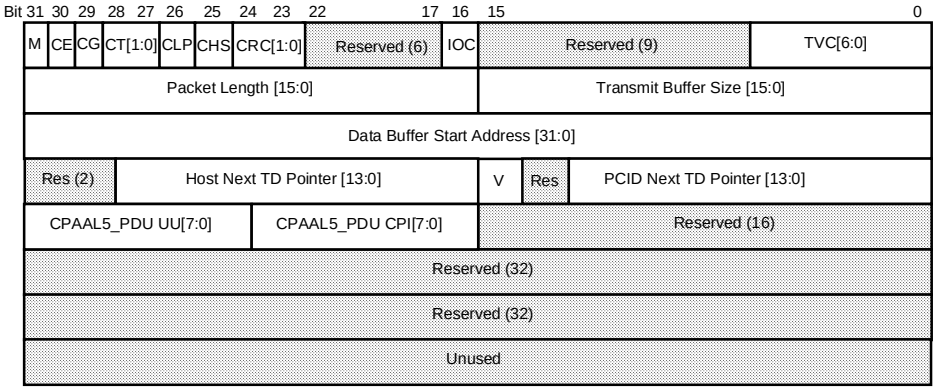
9.14.4.3 Fig. 9.12 TDRR Queue Operation



9.14.5 Transmit Descriptor Data Structure

The thirty-two byte Transmit Descriptor Data Structure is used by the PCI Host to describe a packet or portion of a packet to the PCID's TRM. The data structure and the fields are described below:

9.14.5.1 Fig. 9.13 Transmit Descriptor



Field	Description
M	The More (M) bit is used by the PCI Host to support packets that require multiple Transmit Descriptors (TDs). If M is set to logic one, the LASAR-155 assumes that the current TD is just one of several TDs for the current packet. If M is set to logic zero, the LASAR-155 assumes that this TD describes the entire packet for the single TD packet case or describes the end of a packet for the multiple TD packet case. Note, the More bit cannot be set to logic one when the Chain End bit is set to logic one.

CE	The Chain End (CE) bit is used by the PCI Host to indicate the end of a linked list of TDs presented to the LASAR-155. The linked list can contain one or more packets as delineated using the M bit. When CE is set to logic one, the current TD is the last TD of a linked list of TDs. When CE is set to logic zero, the current TD is not the last TD of a linked list. When the current TD is not the last of the linked list, the Host Next TD Pointer[13:0] field is valid; otherwise the field is not valid. Note, the Chain End bit cannot be set to logic one when the More bit is set to logic one.
CG	The Congestion (CG) bit is used by the PCI Host to indicate whether the cells used to transmit the buffer data described by the current TD should be used to indicate congestion using their Payload Type Indicators (PTIs). Note, this bit is not considered unless the CHS bit is set to logic one. When CG is set to logic one, all cells involved in the transport of the current buffer will contain a PTI field which indicates congestion. If CG is set to logic zero, congestion is not indicated. The CG bit cannot be set to logic one at the same time the CT[1:0] bits are set to 10 or 11. For multiple TD packets, for all TDs of the packet, the CG bit must be consistent.
CT[1:0]	The Cell Type (CT[1:0]) bits are used by the PCI Host to determine the cell type as defined below. 00 - AAL5 user cell 01 - Raw user cell 10 - segment OAM F5 flow cell 11 - End to end OAM F5 flow cell When CT specifies non AAL5 user cells (i.e. 01, 10 or 11), the current TD's Packet Length must be less than or equal to forty eight octets. The exact number depends on the CRC type indicated.

CLP	The Cell Loss Priority (CLP) bit is used by the PCI Host to control the CLP field in the cell headers used to transport the current TD's buffer data. Note, this bit is not considered unless the CHS bit is set to logic one. When CLP is set to logic one, all cells involved in the transport of the current buffer will contain a CLP field set to logic one. If CLP is set to logic zero, all cells involved in the transmit of the current TD's buffer data will contain a CLP field set to logic zero. For multiple TD packets, for all TDs of the packet, the CLP bit must be consistent.
CHS	The Cell Header Select (CHS) bit is used by the PCI Host to select the source of the cell header fields used to transport the current TD's buffer data. When CHS is logic one, the CG, CT[1:0] and CLP bits in the current TD are used to form the Payload Type Indicator (PTI) field and the Cell Loss Priority (CLP) field in the cell headers. When the CHS is logic zero, the default PTI and CLP fields programmed into the Connection Parameter Store (COPS) are used. Note, if CT[1:0] selects AAL5 user cells (00), then CHS must be set to logic one.
CRC[1:0]	The CRC select (CRC[1:0]) bits select whether the CRC-32 polynomial, CRC-10 polynomial or no CRC should be applied to the packet/cell described in the current TD. 00 - CRC-32 01 - CRC-10 10 - No CRC 11 - No CRC For multiple TD packets, for all TDs of the packet, the CRC bits must be consistent.

IOC	The Interrupt On Complete (IOC) bit is used by the PCI Host to instruct the LASAR-155 to interrupt it when it has completed transmission of the current TD's buffer. When IOC is logic one, the LASAR-155 will interrupt the PCI Host using the PCIINTB output if it is enabled using a register bit. In addition, it will flush the LASAR-155's internal six deep TD buffer and place all the TDs onto the Tx Descriptor Reference Free Queue. If IOC is logic zero, the LASAR-155 will not interrupt the PCI Host. The TD will be place in the internal six deep TD buffer (if enabled).
TVC[6:0]	The Transmit Virtual Connection Code (TVC[6:0]) bits are used by the PCI Host to indicate which VC a TD should be associated with. The TVC bits are constructed from N (where N=0,1,2) bits of the Virtual Path Identifier (VPI) and M (where M=7,6,5) bits of the Virtual Channel Identifier. Selection of M and N are made using a COPS register. In addition, for all TDs of the same link list structure the PCI Host adds to the Tx Descriptor Reference Ready Queue, the TVC fields must be the same.
Packet Length [15:0]	The Packet Length bits are used by the PCI Host to indicate the total number of bytes in the packet to be transmitted. For multiple TD packets, the Packet Length fields of each TD must be the same. In all but the last TD, all bytes of each TD's buffer are expected to contain packet data. The Packet Length[15:0] field can be modified by the LASAR-155. The original value set by the PCI Host may not be present when the TDR is returned to the PCI Host via the TDRF Queue.
Transmit Buffer Size [15:0]	The Transmit Buffer Size bits are used to indicate the size in octets of the current TD's data buffer. This field must be configured by the PCI Host. The minimum size supported is 4 bytes.

Data Buffer Start Address[31:0]	The Data Buffer Start Address bits are used as a pointer to the packet buffer of the current TD in PCI Host memory. No DWORD alignment is assumed.
Host Next TD Pointer [13:0]	The Host Next TD Pointer is used to store TDRs which permits the PCI Host to support linked lists of TDs. As mentioned above, linked lists are terminated using the CE bit. Linked lists of TDs are used by the PCI Host to pass the LASAR-155 multiple TD packets or to pass the LASAR-155 multiple packets associated with the same VC.
V	The V bit is used to indicate that the PCID Next TD Pointer field is valid. When V is set to logic one the PCID Next TD Pointer[13:0] field is valid. When V is set to logic zero, the PCID Next TD Pointer[13:0] field is invalid. This field is used by the host to rebuild the PCID packet links in the event of a segmentation failure condition. This field must be initialized to zero by the PCI Host.
PCID Next TD Pointer [13:0]	The PCID Next TD Pointer bits are used to store TDRs which permits the TRM to create linked lists, of TDs passed to it via the TDRR Queues. The TDs are linked with other TDs with the same VC. In the case that the TRM aborts a packet, the TRM will only place the first TD of a VC on the TDRF Queue. It is the responsibility of the PCI Host to follow the PCID and Host links in order to recover all the buffers.
CPAAL5_PDU UU[7:0]	The Common Part Convergence Sublayer AAL Type 5 Protocol Data Unit User to User (CPAAL5_PDU UU) octet is used by the LASAR-155 to insert into the UU field of the associated CPAAL5_PDU. Insertion can be enabled or disabled using a register bit. If disabled, the LASAR-155 inserts 00H into the UU field of the associated CPAAL5_PDU. For multiple TD packets, for all TDs of the packet, the CPAAL5_PDU UU field must be consistent. Note, the CPAAL5_PDU UU field is only used when CT[1:0] selects AAL5 user cells (00).

CPAAL5_PDU CPI[7:0]	The Common Part Convergence Sublayer AAL Type 5 Protocol Data Unit Common Part Indicator (CPAAL5_PDU CPI) octet is used by the LASAR-155 to insert into the CPI field of the associated CPAAL5_PDU. Insertion can be enabled or disabled using a register bit. If disabled, the LASAR-155 inserts 00H into the CPI field of the associated CPAAL5_PDU. For multiple TD packets, for all TDs of the packet, the CPAAL5_PDU CPI field must be consistent. Note, the CPAAL5_PDU CPI field is only used when CT[1:0] selects AAL5 user cells (00).

9.14.6 Receive Request Machine

The receive DMA channel is controlled using the Receive Request Machine (RRM). The RRM receives cell payloads associated with an open VC from the RALP block. Payloads are assumed to be either management cells or part of a packet under reassembly. For management cells, the payload is burst written into PCI Host memory and the host is alerted. Some flexibility is provided to allow for the accumulation of several cells before the PCI Host is alerted. For payloads of packets under reassembly, the payload is burst written into PCI Host memory but the PCI Host is not alerted until the complete packet has been reassembled. All DMA burst data transfers are performed with minimum PCI Host interaction with the aid of internal per VC storage.

For packets, PCI Host communication is provided using Receive Packet Descriptors (RPD), a Receive Packet Descriptor Reference Small Buffer Free (RPDRSF) Queue, a Receive Packet Descriptor Reference Large Buffer Free (RPDRLF) Queue and a Receive Packet Descriptor Reference Ready (RPDRR) Queue. Two free queues are provided to allow for flexible buffer sizes. For large buffers the RPDRLF Queue and for small buffers the RPDRSF Queue. All four data structures are located in PCI Host memory. A RPD is a thirty two byte data structure set up by the PCI Host and used by the LASAR-155 to describe a packet or a portion of a packet. The RPD data structure is fully described in the Receive Packet Descriptor Section.

For management cells, PCI Host communication is provided using Receive Management Descriptors (RMD), a Receive Management Descriptor Reference Free (RMDRF) Queue and a Receive Management Descriptor Reference Ready (RMDRR) Queue. All three data structures are located in PCI Host memory. A RMD is a thirty two byte data structure set up by the PCI Host and used by the LASAR-155 to describe a management cell. The RMD data structure is fully described in the Receive Management Descriptor Section.

9.14.7 Receive Packet Descriptor Table

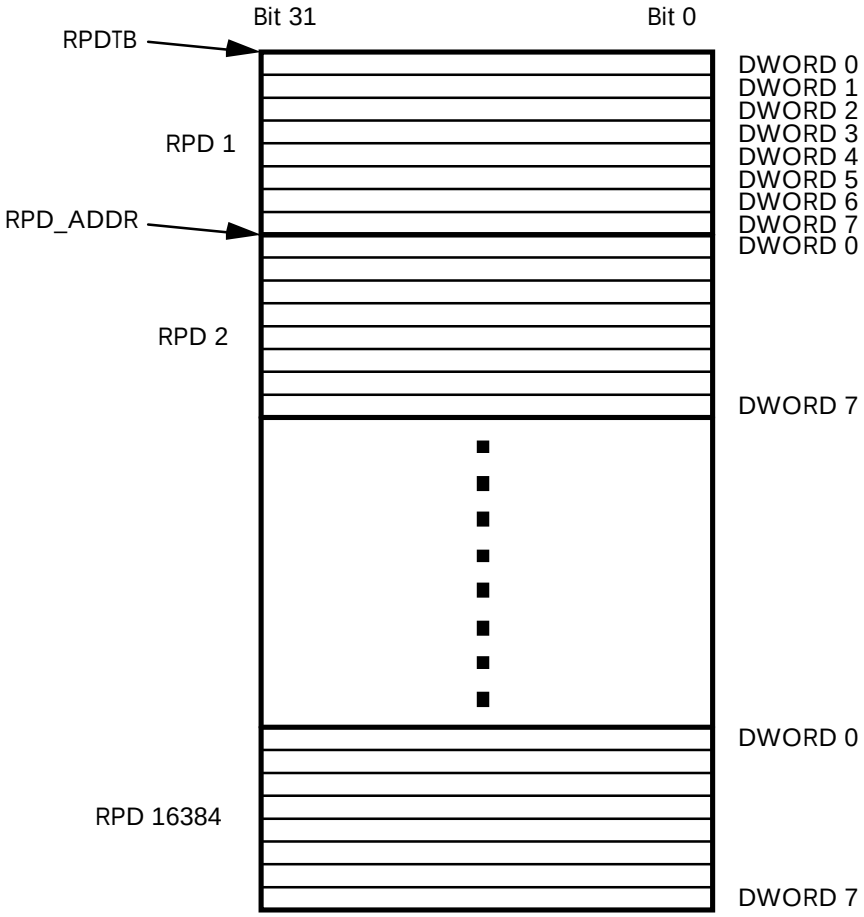
Each RPD resides in the Receive Packet Descriptor Table. The Receive Packet Descriptor table can contain a maximum of 16384 RPDs. The base of the Receive Packet Descriptor Table is user programmable via the PCID Rx Packet Descriptor Table Base register. Thus, as shown below, a RPD can be located using a Receive Packet Descriptor Reference (RPDR) combined with the PCID Rx Packet Descriptor Table Base register.

9.14.7.1 Fig. 9.14 Receive Packet Descriptor Table

RPDTB[31:5] = Rx Packet Descriptor Table Base register

RPDR[13:0] = Receive Packet Descriptor Reference

RPD_ADDR[31:0] = Receive Packet Descriptor Address



9.14.8 Receive Packet Queues and Operation

RPDRs pointing to free RPD are passed from the PCI Host to the RRM using the Receive Packet Descriptor Reference Small Free (RPDRSF) and the Receive Packet Descriptor Reference Large Free (RPDRLF) Queues. The RRM uses one or more free RPDs for packet reassembly. Two free queues are used by the RRM, the RPDRLF Queue for large buffers and the RPDRSF Queue for small buffers. At the start of packet reception the RRM will use a small buffer to store the start of a packet. If the packet exceeds the small buffer size, the RRM will use large buffers to store the remainder of the packet.

In order to take advantage of burst PCI transfers, the RRM reads up to six RPDs from each Free Queue and stores them locally. Once a packet has been reassembled, the RRM passes completed RPDs to the PCI Host using the Receive Packet Descriptor Reference Ready (RPDRR) Queue.

All three Queues reside in PCI Host memory and are defined using a common base pointer residing in the PCID Receive Queue Base register and twelve offset pointers, four per queue. For each queue, two pointers are required to define the start and the end of a queue while two pointers are required for the current write and read locations within the queue. The read pointer always points to the last location read while the write pointer always points to the next location to be written.

A full condition for the queues is defined as the read and the write pointers being equal. A empty condition is defined as the read pointer one less then the write pointer. The last location in a queue is not considered as part of the queue and thus is not a valid entry.

The LASAR-155 reassembles packets using RPDs in Host memory. Each RPD contains control fields, a RPD pointer reference field and a buffer pointer field. The control fields are used by the LASAR-155 to indicate to the PCI Host which VC a reassembled packet is associated with and the state of the reassembled packet. The buffer pointer is used to point to a buffer where the reassembled packet is stored. If the packet was too large for a single buffer, the RPD pointer reference field is provided to create a linked list of RPDs. When the LASAR-155's RRM has assembled a packet, it attaches the RPDR of the RPD describing the packet to the RPDRR Queue. For multiple RPD packets, only the first RPD's RPDR of the linked list is attached. Please refer below.

9.14.8.1 Fig. 9.15 RPDRF and RPDRR Queues

Receive Packet Descriptor (RPD) Referance Queues

Base Address:

RQB[31:2] = Rx Queue Base register

Index Registers:

Large Buffer Free Queue:

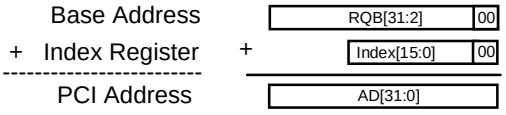
RPDRLFQS[15:0] = RPDR Large Free Queue Start register
RPDRLFQW[15:0] = RPDR Large Free Queue Write register
RPDRLFQR[15:0] = RPDR Large Free Queue Read register
RPDRLFQE[15:0] = RPDR Large Free Queue End register

Small Buffer Free Queue:

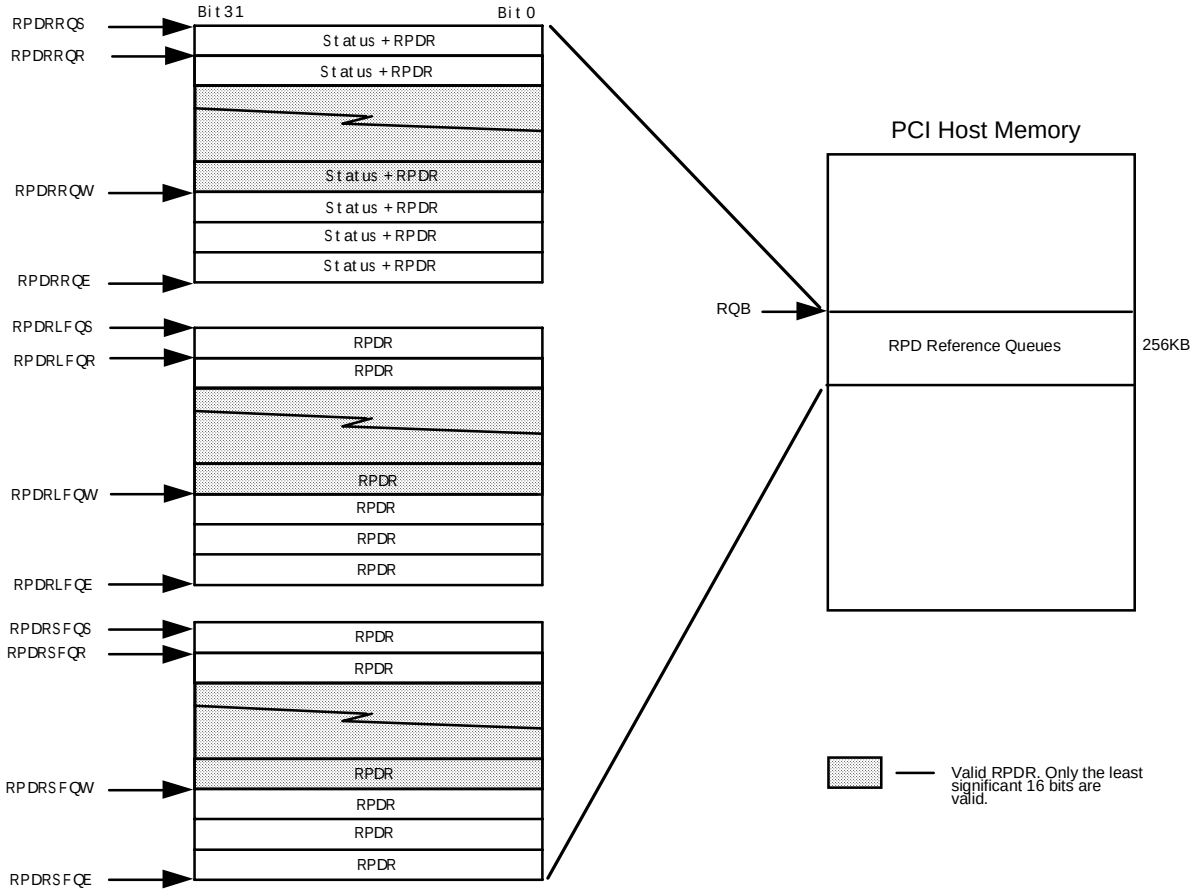
RPDRSFQS[15:0] = RPDR Small Free Queue Start register
RPDRSFQW[15:0] = RPDR Small Free Queue Write register
RPDRSFQR[15:0] = RPDR Small Free Queue Read register
RPDRSFQE[15:0] = RPDR Small Free Queue End register

Ready Queue:

RPDRRQS[15:0] = RPDR Ready Queue Start register
RPDRRQW[15:0] = RPDR Ready Queue Write register
RPDRRQR[15:0] = RPDR Ready Queue Read register
RPDRRQE[15:0] = RPDR Ready Queue End register

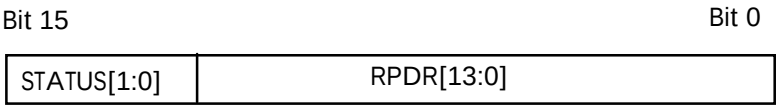


Rx Packet Descriptor Reference Queue Memory Map



Each queue element is a sixteen bit structure consisting of a RPDR and several Status bits. Status bits are used by the RRM to inform the PCI Host on the success of packet reassembly. Please refer below.

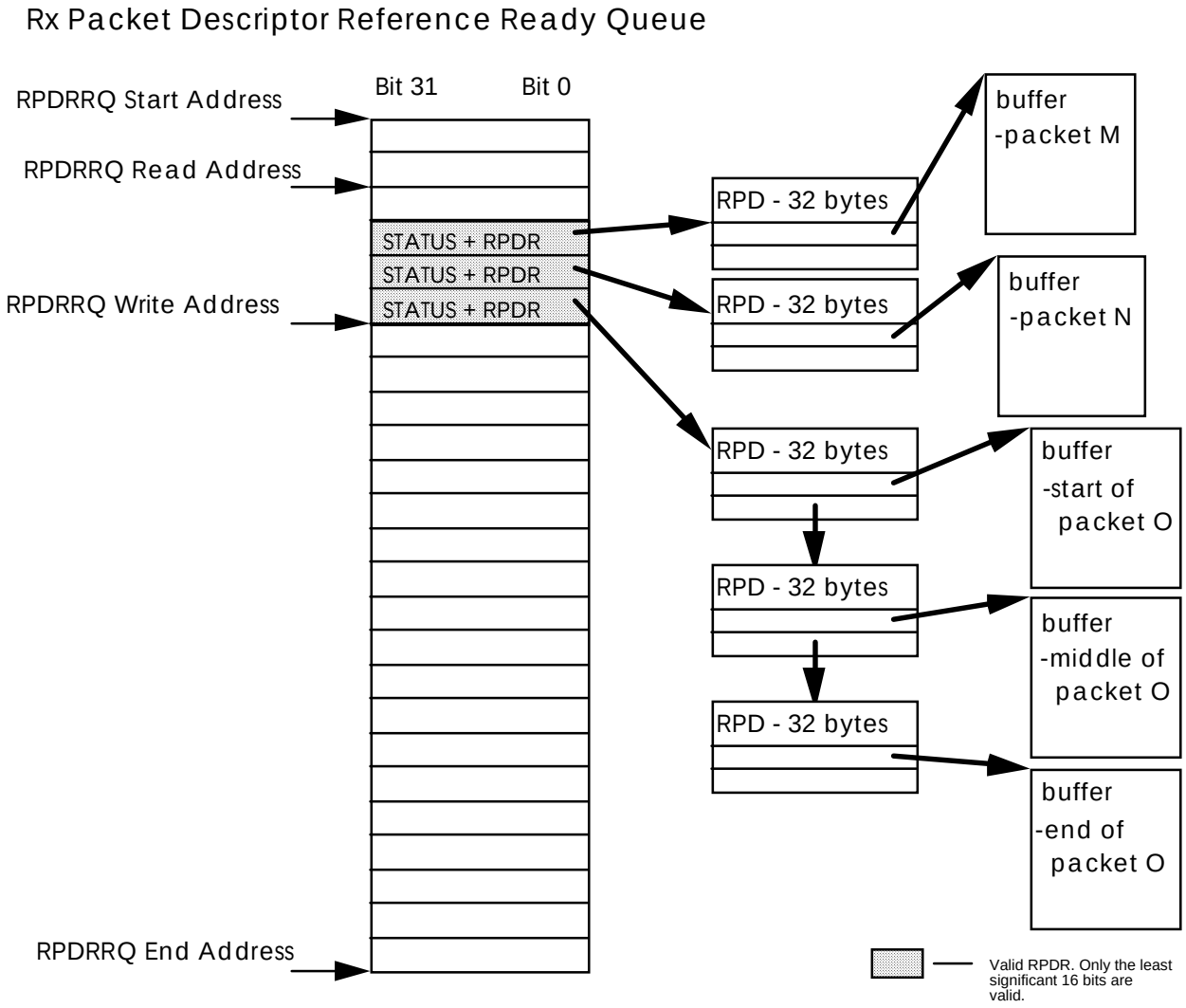
9.14.8.2 Fig. 9.16 RPDRR Queue Elements



Status	Descriptor
00	Reassembly successful.
01	Reassembly failed.
1x	Unused.

Fatal packet reassembly errors are indicated using the status field of a queue element. A status value of 00B indicates that the packet was received without errors. A status field value of 01B indicates that the packet reassembly experienced either a CPAAL5_PDU oversize, a CPAAL5_PDU LENGTH field zero, a CPAAL5_PDU CRC-32 or a CPAAL5_SDU length error. Please refer to the Receive Packet Descriptor Data Structure section for a description of the errors.

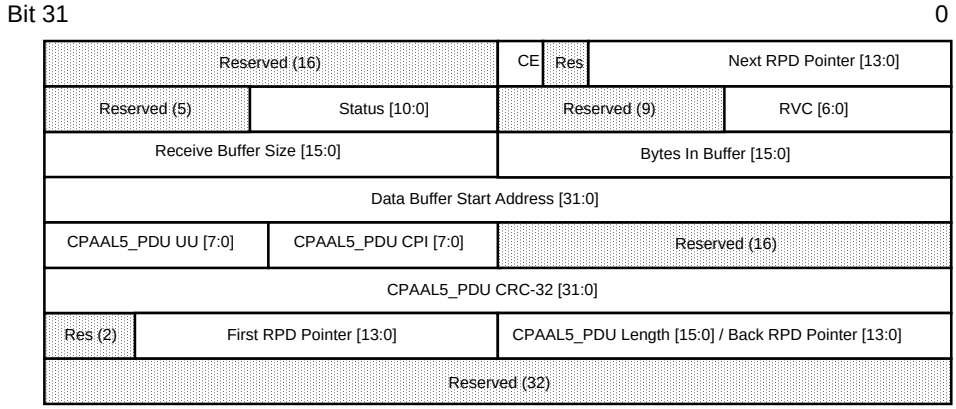
9.14.8.3 Fig. 9.17 RPDRR Queue Operation



9.14.9 Receive Packet Descriptor Data Structure

The thirty-two byte Receive Packet Descriptor (RPD) Data Structure is used by the LASAR-155 to describe a reassembled packet to the PCI Host. RPD's can be linked together to form a linked list to accommodate large packets. The data structure and the fields are described below:

9.14.9.1 Fig. 9.18 Receive Packet Descriptor



Field	Description
CE	The Chain End (CE) bit is used by the LASAR-155 to indicate the end of a linked list of RPDs presented to the PCI Host. When CE is set to logic 1, the current RPD is the last RPD of a linked list of RPDs. When CE is set to logic 0, the current RPD is not the last RPD of a linked list. When the current RPD is not the last of the linked list (CE=0), the Next RPD Pointer[13:0] field is valid; otherwise the field is not valid.
Next RPD Pointer [13:0]	The Next RPD Pointer is used to store RPDRs which permits the LASAR-155 to support linked lists of RPDs. As mentioned above, linked lists are terminated using the CE bit. If CE is set to logic 1, this field is not valid. Linked lists of RPDs are used by the LASAR-155 to pass the PCI Host multiple RPD packets.

Status [10:0]	The Status field is used by the LASAR-155 to indicate the status of the received packet. Below are the Status field bit definitions. When the bit is logic 1, the packet has experienced the indicated condition. Status[0] - cell of packet experienced congestion. One or more cells of received packet contained a cell with PTI value 010 or 011. Status[1] - cell of packet has, CLP=1. Status[2] - CPAAL5_PDU Oversize error. Packet received exceeds maximum size programmed in the RALP Max Rx PDU Length register (0x83). Status[3] - Unused. Status[4] - CPAAL5_PDU UU field non zero. Status[5] - CPAAL5_PDU CPI field non zero. Status[6] - CPAAL5_PDU LENGTH field zero. Status[7] - CPAAL5_PDU CRC-32 error. Status[8] - CPAAL5_SDU length error. Packet received contains a length field that does not equal the received length. Status[9] - Reserved Status[10] - Unused. Note: for multiple RPD packets, only the first RPD's Status field is valid. All other RPD Status fields of the linked list are invalid and should be ignored.
RVC[6:0]	The Receive Virtual Connection Code (RVC[6:0]) bits are used by the LASAR-155 to indicate which VC a RPD is associated with. The RVC bits are constructed from N (where N=0,1,2) bits of the Virtual Path Identifier (VPI) and M (where M=7,6,5) bits of the Virtual Channel Identifier. Selection of M and N are made using a COPS register. Note: for multiple RPD packets, only the first RPD's RVC field is valid. All other RPD RVC fields of the linked list are invalid and should be ignored.

Receive Buffer Size [15:0]	The Receive Buffer Size bits indicate the size in bytes of the current RPD's data buffer. This field must be configured by the PCI Host during initialization. Note, Receive Buffer Sizes must be an integer multiple of four. Non integer multiples are not supported. In addition, the minimum buffer size supported is forty-eight bytes.
Bytes in Buffer [15:0]	The Bytes in Buffer bits indicate the number of bytes actually used in the current RPD's packet buffer to store packet data.
Data Buffer Start Address[31:0]	The Data Buffer Start Address bits are used as a pointer to the packet buffer of the current RPD into PCI Host memory. Note, Receive Buffers must be DWORD aligned. For example, Data Buffer Start Address[1:0] is expected to be set to 00 binary.
CPAAL5_PDU UU [7:0]	The CPAAL5_PDU UU byte is the received User to User byte of the CPCS AAL Type 5 Protocol Data Unit associated with the current packet. Note: for multiple RPD packets, only the first RPD's CPAAL5_PDU UU field is valid. All other RPD CPAAL5_PDU UU fields of the linked list are invalid and should be ignored.
CPAAL5_PDU CPI [7:0]	The CPAAL5_PDU CPI byte is the received Common Part Indicator byte of the CPCS AAL Type 5 Protocol Data Unit associated with the current packet. Note: for multiple RPD packets, only the first RPD's CPAAL5_PDU CPI field is valid. All other RPD CPAAL5_PDU CPI fields of the linked list are invalid and should be ignored.

CPAAL5_PDU CRC-32 [31:0]	The CPAAL5_PDU CRC-32 word is the received CRC-32 field of the CPCS AAL Type 5 Protocol Data Unit associated with the current packet. Note: for multiple RPD packets, only the first RPD's CPAAL5_PDU CRC-32 field is valid. All other RPD CPAAL5_PDU CRC-32 fields of the linked list are invalid and should be ignored.
First RPD Pointer [13:0]	The First RPD Pointer is used to store a RPDR pointer to the first RPD of a linked list representing a multiple RPD packet. Note, this field is invalid for the first RPD of a linked list.
CPAAL5_PDU LENGTH [15:0]	The CPAAL5_PDU LENGTH word is the received LENGTH field of the CPCS AAL Type 5 Protocol Data Unit associated with the current packet. Note: for multiple RPD packets, only the first RPD's CPAAL5_PDU LENGTH field is valid. All other RPD CPAAL5_PDU LENGTH fields of the linked list are invalid and should be ignored.

9.14.10 Receive Management Descriptor Table

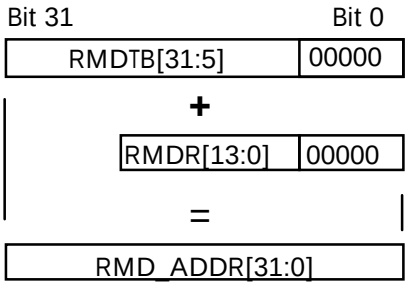
Each RMD resides in the Receive Management Descriptor Table. The Receive Management Descriptor table can contain a maximum of 16384 RMDs. The base of the Receive Management Descriptor Table is user programmable via the PCID Rx Management Descriptor Table Base register. Thus, as shown below, a RMD can be located using a Receive Management Descriptor Reference (RMDR) combined with the PCID Rx Management Descriptor Table Base register.

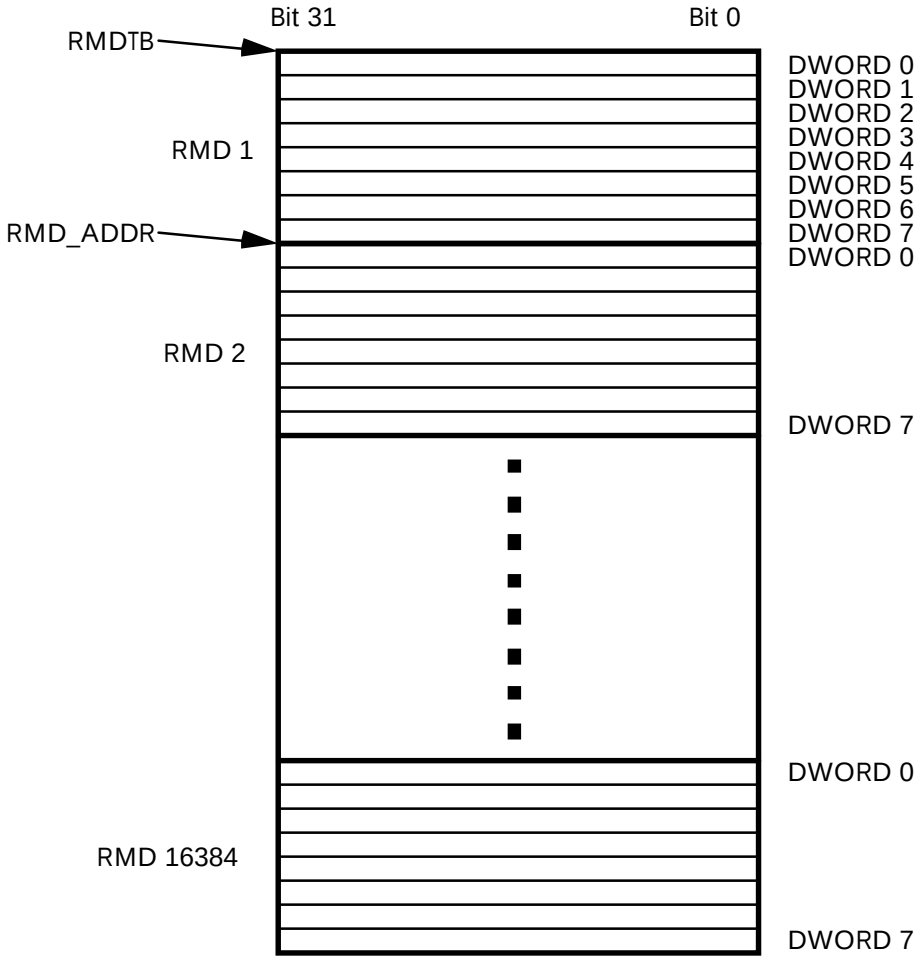
9.14.10.1 Fig. 9.19 Receive Management Descriptor Table

RMDTB[31:5] = Rx Management Descriptor Table Base register

RMDR[13:0] = Receive Management Descriptor Reference

RMD_ADDR[31:0] = Receive Management Descriptor Address





9.14.11 Receive Management Queues

RMDRs pointing to free RMD are passed from the PCI Host to the RRM using the Receive Management Descriptor Reference Free (RMDRF) Queue. In order to take advantage of burst PCI transfers, the RRM reads up to six RMDs from the RMDRF Queue and stores them locally. The RRM uses a free RMD to store OAM, Signaling and Control cells to pass to the PCI Host using the Receive Management Descriptor Reference Ready (RMDRR) Queue.

Both Queues reside in PCI Host memory and are defined using a common base pointer residing in the PCID Receive Queue Base register and eight offset pointers, four per queue. For each queue, two pointers are required to define the start and the end of a queue while two pointers are required for the current write and read locations within the queue. The read pointer always points to the last location read while the write pointer always points to the next location to be written.

A full condition for the queues is defined as the read and the write pointers being equal. An empty condition is defined as the read pointer being one less then the write pointer. The last location in a queue is not considered as part of the queue and thus is not a valid entry.

9.14.11.1 Fig. 9.20 RMDRF and RMDRR Queues

Receive Management Descriptor (RMD) Referance Queues

Base Address:

RQB[31:2] = Rx Queue Base register

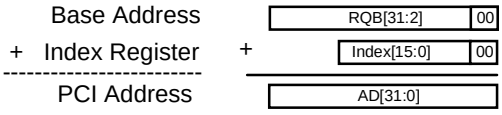
Index Registers:

Management Free Queue:

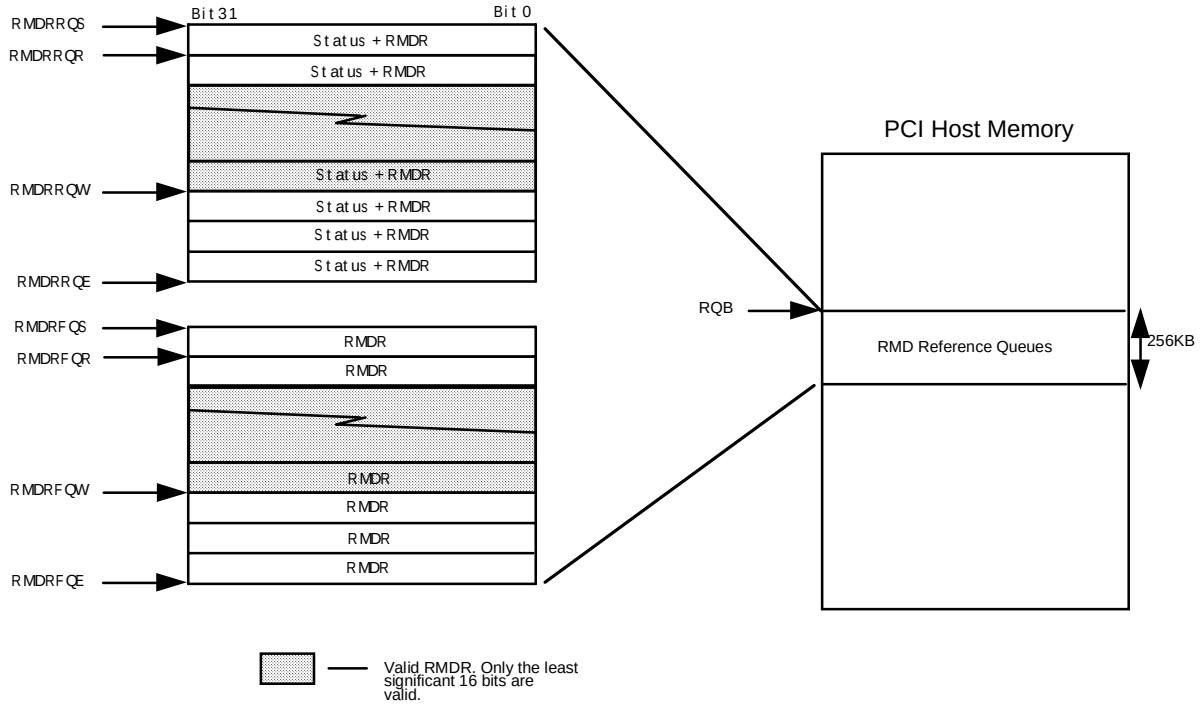
RMDRFQS[15:0] = RMDR Free Queue Start register
RMDRFQW[15:0] = RMDR Free Queue Write register
RMDRFQR[15:0] = RMDR Free Queue Read register
RMDRFQE[15:0] = RMDR Free Queue End register

Managemnet Ready Queue:

RMDRRQS[15:0] = RMDR Ready Queue Start register
RMDRRQW[15:0] = RMDR Ready Queue Write register
RMDRRQR[15:0] = RMDR Ready Queue Read register
RMDRRQE[15:0] = RMDR Ready Queue End register

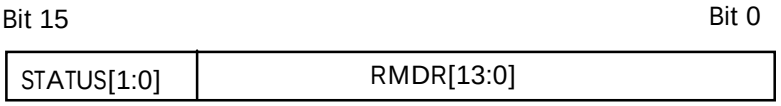


Rx Management Descriptor Reference Queue Memory Map



Each queue element is a sixteen bit structure consisting of a RMDR and several Status bits. Status bits are used by the RRM to indicate the type of cell passed to the PCI Host. Please refer below.

9.14.11.2 Fig. 9.21 RMDRR Queue Elements

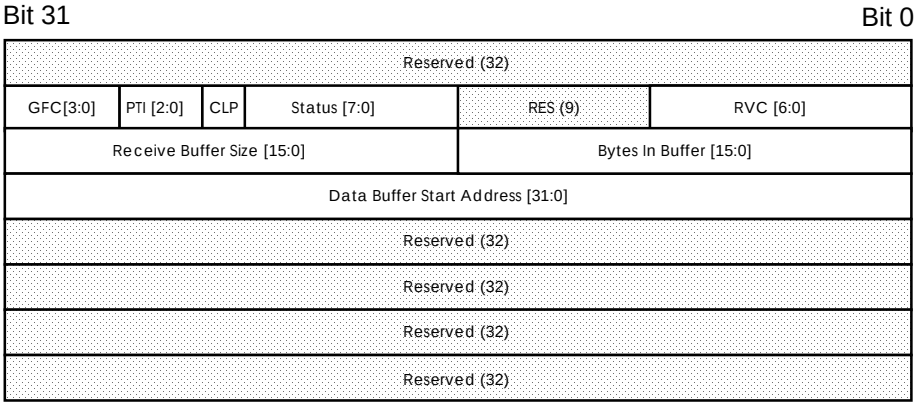


Status	Descriptor
00	valid cell
01	CRC-10 errored cell
10	valid Segment OAM F5 cell
11	valid End-to-end OAM F5 cell if Status[3] is set to zero in the RMD CRC errored OAM F5 cell if Status[3] is set to one in the RMD

9.14.12 Receive Management Descriptor Data Structure

The thirty-two byte Receive Management Descriptor (RMD) Data Structure is used by the LASAR-155 to describe a cell to the PCI Host. The data structure and the fields are described below:

9.14.12.1 Fig. 9.22 Receive Management Descriptor



Field	Description
GFC[3:0]	The GFC[3:0] bits are the received GFC bits in the associated cell header.
PTI[2:0]	The PTI[2:0] bits are the received PTI bits in the associated cell header.

CLP	The CLP bit is the received CLP bit in the associated cell header.
Status [7:0]	The Status field is used by the LASAR-155 to indicate the status of the received packet. Below are the Status field bit definitions. When the bit is logic one, the packet has experienced the indicated condition. Status[0] - cell experienced congestion. Cell received with PTI value 010 or 011. Status[1] - cell received with CLP=1. Status[2] - Unused. Status[3] - cell CRC-10 error. Status[4] - Unused. Status[5] - Unused. Status[6] - Unused. Status[7] - cell CRC-32 error.
RVC[6:0]	The Receive Virtual Connection Code (RVC[6:0]) bits are used by the LASAR-155 to indicate which VC a RMD is associated with. The RVC bits are constructed from N (where N=0,1,2) bits of the Virtual Path Identifier (VPI) and M (where M=7,6,5) bits of the Virtual Channel Identifier. Selection of M and N are made using a COPS register.
Receive Buffer Size [15:0]	The Receive Buffer Size bits indicate the size in bytes of the current RMD's data buffer. This field must be configured by the PCI Host during initialization and must be large enough to accommodate one cell (i.e. 48 or more bytes).
Bytes in Buffer [15:0]	The Bytes in Buffer bits indicate the number of bytes actually used in the current RMD's buffer to store cell data. For RMDs, this value should be between 1 to 48 bytes.
Data Buffer Start Address[31:0]	The Data Buffer Start Address bits are used as a pointer to the buffer of the current RMD into PCI Host memory. Note, Receive Buffers must be DWORD aligned. For example, Data Buffer Start Address[1:0] is expected to be set to 00 binary.

9.15 Microprocessor Interface

The microprocessor interface is provided for device configuration, control and monitoring by an external local microprocessor. For applications where local microprocessor control is not required and all device operations are performed by the PCI Host, the microprocessor interface allows the PCI Host access the LASAR-155 Local Bus.

When the interface is configured for slave mode operation, normal mode registers, test mode registers and the micro/PCI Host mailbox can be accessed through this port. Normal mode registers are required for normal operation, test mode registers are used to enhance the testability of the LASAR-155 and the micro/PCI Host mailbox allows communication between the microprocessor and PCI Host without external support devices.

When the interface is configured for master mode operation, the PCI Host can access the LASAR-155 Local Bus. The LASAR-155 Local Bus supports up to two devices without requiring any external logic.

9.16 Microprocessor and PCI Host Normal Mode Register Memory Map

The LASAR-155 supports three different normal mode register types. The register types can be distinguished by their master. The register types are defined below:

1) Microprocessor Only Access registers (MO) - these registers can only be accessed through the microprocessor interface and cannot be accessed through the PCI port.

2) PCI Host Only Access registers (PO) - these registers can only be accessed through the PCI Host interface and cannot be accessed directly using the microprocessor interface. However, indirect access via the microprocessor interface is provided.

3) Selectable Master registers (SM) - these registers can be accessed by either the PCI Host or the microprocessor at any given moment as configured by input, MPENB. Input MPENB must be set when the device is powered up. When these registers are accessed by the PCI Host, it must be on double word boundaries.

The register map for the PCI Host interface and the microprocessor interface is shown below. The first column indicates the type of register as detailed above. The second column contains the microprocessor addresses of the register if the register can be accessed using the interface. The third column contains the PCI interface DWORD address of the register if the register can be accessed using the interface. The PCI index address must be combined with a base address to form the PCI Interface address. The base address can be found in the LASAR-155 Memory Base Address register in the PCI Configuration memory space. The fourth column contains the name of the register.

9.16.1 Normal Mode Register Memory Map

Type	Address		Register
	Micro	PCI Offset	
SM	0x00	0x000	LASAR-155 Master Reset / Load Meters
SM	0x01	0x004	LASAR-155 Master Configuration
SM	0x02	0x008	LASAR-155 Master Interrupt Status
SM	0x03	0x00C	LASAR-155 Master Interrupt Enable
SM	0x04	0x010	LASAR-155 Master Clock Monitor
SM	0x05	0x014	LASAR-155 Master Control
SM	0x06	0x018	LASAR-155 Clock Synthesis Control and Status
SM	0x07	0x01C	LASAR-155 Clock Recovery Control and Status
SM	0x08-0x0F	0x020-0x03C	Reserved
SM	0x10	0x040	RSOP Control/Interrupt Enable
SM	0x11	0x044	RSOP Status/Interrupt Status
SM	0x12	0x048	RSOP Section BIP-8 LSB
SM	0x13	0x04C	RSOP Section BIP-8 MSB
SM	0x14	0x050	TSOP Control
SM	0x15	0x054	TSOP Diagnostic
SM	0x16-0x17	0x058-0x05C	TSOP Reserved
SM	0x18	0x060	RLOP Control/Status
SM	0x19	0x064	RLOP Interrupt Enable/Status
SM	0x1A	0x068	RLOP Line BIP-8/24 LSB
SM	0x1B	0x06C	RLOP Line BIP-8/24
SM	0x1C	0x070	RLOP Line BIP-8/24 MSB
SM	0x1D	0x074	RLOP Line FEBE LSB
SM	0x1E	0x078	RLOP Line FEBE
SM	0x1F	0x07C	RLOP Line FEBE MSB
SM	0x20	0x080	TLOP Control
SM	0x21	0x084	TLOP Diagnostic
SM	0x22	0x088	TLOP Reserved
SM	0x23	0x08C	TLOP Reserved
SM	0x24-0x2F	0x090-0x0BC	Reserved
SM	0x30	0x0C0	RPOP Status/Control
SM	0x31	0x0C4	RPOP Interrupt Status
SM	0x32	0x0C8	RPOP Reserved

SM	0x33	0x0CC	RPOP Interrupt Enable
SM	0x34	0x0D0	RPOP Reserved
SM	0x35	0x0D4	RPOP Reserved
SM	0x36	0x0D8	RPOP Reserved
SM	0x37	0x0DC	RPOP Path Signal Label
SM	0x38	0x0E0	RPOP Path BIP-8 LSB
SM	0x39	0x0E4	RPOP Path BIP-8 MSB
SM	0x3A	0x0E8	RPOP Path FEBE LSB
SM	0x3B	0x0EC	RPOP Path FEBE MSB
SM	0x3C-0x3F	0x0F0-0x0FC	RPOP Reserved
SM	0x40	0x100	TPOP Control/Diagnostic
SM	0x41	0x104	TPOP Pointer Control
SM	0x42	0x108	TPOP Reserved
SM	0x43	0x10C	TPOP Reserved
SM	0x44	0x110	TPOP Reserved
SM	0x45	0x114	TPOP Arbitrary Pointer LSB
SM	0x46	0x118	TPOP Arbitrary Pointer MSB
SM	0x47	0x11C	TPOP Reserved
SM	0x48	0x120	TPOP Path Signal Label
SM	0x49	0x124	TPOP Path Status
SM	0x4A-0x4F	0x128-0x13C	TPOP Reserved
SM	0x50	0x140	RACP Control/Status
SM	0x51	0x144	RACP Interrupt Enable/Status
SM	0x52	0x148	RACP Match Header Pattern
SM	0x53	0x14C	RACP Match Header Mask
SM	0x54	0x150	RACP Correctable HEC Error Count
SM	0x55	0x154	RACP Uncorrectable HEC Error Count
SM	0x56	0x158	RACP Receive Cell Counter (LSB)
SM	0x57	0x15C	RACP Receive Cell Counter
SM	0x58	0x160	RACP Receive Cell Counter (MSB)
SM	0x59	0x164	RACP Configuration
SM	0x5A-0x5F	0x168-0x17C	RACP Reserved
SM	0x60	0x180	TACP Control/Status
SM	0x61	0x184	TACP Idle/Unassigned Cell Header Pattern
SM	0x62	0x188	TACP Idle/Unassigned Cell Payload Octet Pattern
SM	0x63	0x18C	TACP FIFO Configuration
SM	0x64	0x190	TACP Transmit Cell Counter (LSB)
SM	0x65	0x194	TACP Transmit Cell Counter

SM	0x66	0x198	TACP Transmit Cell Counter (MSB)
SM	0x67	0x19C	TACP Configuration
SM	0x68-0x6F	0x1A0-0x1BC	Reserved
SM	0x70	0x1C0	SAR PMON Count Change
SM	0x71	0x1C4	SAR PMON Reserved
SM	0x72	0x1C8	SAR PMON Receive Unprovisioned VPI/VCI Errors (LSB)
SM	0x73	0x1CC	SAR PMON Receive Unprovisioned VPI/VCI Errors (MSB)
SM	0x74	0x1D0	SAR PMON Receive CRC-10 Errors (LSB)
SM	0x75	0x1D4	SAR PMON Receive CRC-10 Errors (MSB)
SM	0x76	0x1D8	SAR PMON Receive Non Zero Common Part Indicator Errors
SM	0x77	0x1DC	SAR PMON Receive SDU Length Errors
SM	0x78	0x1E0	SAR PMON Receive CRC-32 Errors
SM	0x79	0x1E4	SAR PMON Receive Oversize PDU Errors
SM	0x7A	0x1E8	SAR PMON Reserved
SM	0x7B	0x1EC	SAR PMON Receive PDU Abort Errors
SM	0x7C	0x1F0	SAR PMON Receive Buffer Errors
SM	0x7D	0x1F4	SAR PMON Receive PDU Count
SM	0x7E	0x1F8	SAR PMON Transmit Oversize SDU Errors
SM	0x7F	0x1FC	SAR PMON Transmit Count
SM	0x80	0x200	RALP Control
SM	0x81	0x204	RALP Interrupt Status
SM	0x82	0x208	RALP Interrupt Enable
SM	0x83	0x20C	RALP Max Rx PDU Length
SM	0x84	0x210	RALP Reserved
SM	0x85	0x214	RALP Reserved
SM	0x86	0x218	RALP Reserved
SM	0x87	0x21C	RALP Reserved
SM	0x88	0x220	TALP Control
SM	0x89	0x224	TALP Interrupt Status
SM	0x8A	0x228	TALP Diagnostic
SM	0x8B	0x22C	TALP Aggregate Peak Cell Rate
SM	0x8C	0x230	TALP Aggregate Bucket Capacity
SM	0x8D	0x234	TALP Multipurpose Port Peak Cell Rate
SM	0x8E	0x238	TALP Multipurpose Port Bucket Capacity
SM	0x8F	0x23C	TALP Reserved
SM	0x90	0x240	TATS Control/Interrupt Enable
SM	0x91	0x244	TATS Interrupt Status
SM	0x92	0x248	TATS Service Rate Queue Enables
SM	0x93	0x24C	TATS Service Rate Queue 1 Parameters
SM	0x94	0x250	TATS Service Rate Queue 2 Parameters

SM	0x95	0x254	TATS Service Rate Queue 3 Parameters
SM	0x96	0x258	TATS Service Rate Queue 4 Parameters
SM	0x97	0x25C	TATS Service Rate Queue 5 Parameters
SM	0x98	0x260	TATS Service Rate Queue 6 Parameters
SM	0x99	0x264	TATS Service Rate Queue 7 Parameters
SM	0x9A	0x268	TATS Service Rate Queue 8 Parameters
SM	0x9B-0x9F	0x26C-0x27C	TATS Reserved
SM	0xA0	0x280	COPS Control
SM	0xA1	0x284	COPS Parameter Access Control
SM	0xA2	0x288	COPS VC Number
SM	0xA3	0x28C	COPS VPI
SM	0xA4	0x290	COPS VCI
SM	0xA5	0x294	COPS VC Control and Status
SM	0xA6	0x298	COPS VC Parameters
SM	0xA7	0x29C	COPS Indirect Control
SM	0xA8	0x2A0	COPS Indirect Address
SM	0xA9	0x2A4	COPS Indirect Data
SM	0xAA-0xBF	0x2A8-0x2FC	COPS Reserved
MO	0xC0		PCID Microprocessor Control
MO	0xC1		PCID Microprocessor Interrupt Status
MO	0xC2		PCID Microprocessor Indirect Control
MO	0xC3		PCID Microprocessor Indirect Data Low Word
MO	0xC4		PCID Microprocessor Indirect Data High Word
MO	0xC5		PCID Microprocessor Write Mailbox Control
MO	0xC6		PCID Microprocessor Write Mailbox Data
MO	0xC7		PCID Reserved
MO	0xC8		PCID Microprocessor Read Mailbox Control
MO	0xC9		PCID Microprocessor Read Mailbox Data
MO	0xCA		PCID Reserved
MO	0xCB-0xFF		PCID Reserved
PO		0x300	PCID Control
PO		0x304	PCID Interrupt Status
PO		0x308	PCID Interrupt Enable
PO		0x30C	PCID Mailbox/Microprocessor Interrupt Status/Enable
PO		0x310	PCID Reserved
PO		0x314	PCID Rx Packet Descriptor Table Base
PO		0x318	PCID Rx Management Descriptor Table Base
PO		0x31C	PCID Rx Queue Base

PO		0x320	PCID Rx Packet Descriptor Reference Large Buffer Free Queue Start
PO		0x324	PCID Rx Packet Descriptor Reference Large Buffer Free Queue Write
PO		0x328	PCID Rx Packet Descriptor Reference Large Buffer Free Queue Read
PO		0x32C	PCID Rx Packet Descriptor Reference Large Buffer Free Queue End
PO		0x330	PCID Rx Packet Descriptor Reference Small Buffer Free Queue Start
PO		0x334	PCID Rx Packet Descriptor Reference Small Buffer Free Queue Write
PO		0x338	PCID Rx Packet Descriptor Reference Small Buffer Free Queue Read
PO		0x33C	PCID Rx Packet Descriptor Reference Small Buffer Free Queue End
PO		0x340	PCID Rx Packet Descriptor Reference Ready Queue Start
PO		0x344	PCID Rx Packet Descriptor Reference Ready Queue Write
PO		0x348	PCID Rx Packet Descriptor Reference Ready Queue Read
PO		0x34C	PCID Rx Packet Descriptor Reference Ready Queue End
PO		0x350	PCID Rx Management Descriptor Reference Free Queue Start
PO		0x354	PCID Rx Management Descriptor Reference Free Queue Write
PO		0x358	PCID Rx Management Descriptor Reference Free Queue Read
PO		0x35C	PCID Rx Management Descriptor Reference Free Queue End
PO		0x360	PCID Rx Management Descriptor Reference Ready Queue Start
PO		0x364	PCID Rx Management Descriptor Reference Ready Queue Write
PO		0x368	PCID Rx Management Descriptor Reference Ready Queue Read
PO		0x36C	PCID Rx Management Descriptor Reference Ready Queue End
PO		0x370	PCID Reserved
PO		0x374	PCID Reserved
PO		0x378	PCID Tx Descriptor Table Base
PO		0x37C	PCID Tx Queue Base
PO		0x380	PCID Tx Descriptor Reference Free Queue Start
PO		0x384	PCID Tx Descriptor Reference Free Queue Write
PO		0x388	PCID Tx Descriptor Reference Free Queue Read
PO		0x38C	PCID Tx Descriptor Reference Free Queue End

PO		0x390	PCID Tx Descriptor Reference High Priority Ready Queue Start
PO		0x394	PCID Tx Descriptor Reference High Priority Ready Queue Write
PO		0x398	PCID Tx Descriptor Reference High Priority Ready Queue Read
PO		0x39C	PCID Tx Descriptor Reference High Priority Ready Queue End
PO		0x3A0	PCID Tx Descriptor Reference Low Priority Ready Queue Start
PO		0x3A4	PCID Tx Descriptor Reference Low Priority Ready Queue Write
PO		0x3A8	PCID Tx Descriptor Reference Low Priority Ready Queue Read
PO		0x3AC	PCID Tx Descriptor Reference Low Priority Ready Queue End
PO		0x3B0	PCID Max Tx SDU Length
PO		0x3B4	RAS and TAS FIFO Pointers
PO		0x3B8-0x3C4	PCID Reserved
PO		0x3C8	PCID RAM Indirect Control
PO		0x3CC	PCID RAM Indirect Data Low Word
PO		0x3D0	PCID RAM Indirect Data High Word
PO		0x3D4	PCID Host Write Mailbox Control
PO		0x3D8	PCID Host Write Mailbox Data Word
PO		0x3DC	PCID Reserved
PO		0x3E0	PCID Host Read Mailbox Control
PO		0x3E4	PCID Host Read Mailbox Data
PO		0x3E8-0x3FC	PCID Reserved
SM	0x100	0x400	LASAR-155 Master Test
SM	0x101-0x1FF	0x404-0x7FC	Reserved for Test

10 NORMAL MODE REGISTER DESCRIPTIONS

Normal mode registers are used to configure and monitor the operation of the LASAR-155. Normal mode registers can be one of three types, Selectable Master registers, Microprocessor Only Access registers and PCI Host Only Access registers. Register description types are described above in the Microprocessor and PCI Host Register Memory Map section. When using the microprocessor interface, normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the LASAR-155 to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect LASAR-155 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the LASAR-155 operates as intended, reserved register bits must only be written with their default values. Similarly, writing to reserved registers should be avoided.

10.1 Selectable Master Registers

Selectable Master registers can be accessed by either the PCI Host or the microprocessor as configured by input, MPENB. It is expected that the master is selected when the device is powered up. For each register description below, the hexadecimal register number indicates the address of the register when accesses are made using the microprocessor port. The hexadecimal number in brackets indicates the PCI offset from the base address in the LASAR-155 Memory Base Address Register when accesses are made using the PCI Host Port.

10.1.1 Register 0x00 (0x000): LASAR-155 Master Reset / Load Meters

Bit	Type	Function	Default
Bit 15	R/W	RESET	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

Writing to this register simultaneously loads all the performance meter registers in the RSOP, RLOP, RPOP, RACP, TACP, SAR PMON blocks. A maximum of 7 µs are required to load all registers after a write.

RESET:
The RESET bit allows the LASAR-155 to be reset under software control. If the RESET bit is a logic one, the entire LASAR-155 except the PCI Interface is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the LASAR-155 out of reset. Holding the LASAR-155 in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset.

Note, unlike the hardware reset input, RSTB, the software reset bit, RESET does not force the LASAR-155's digital output pins tri-state. In addition, all register except the PCI Configuration registers are reset to their default values. The PCI Configuration register values are preserved. Note, for proper operation after a soft reset, the TRMEN bit in the PCID Control register must be cleared before software reset is released.

10.1.2 Register 0x01 (0x004): LASAR-155 Master Configuration

Bit	Type	Function	Default
Bit 15	R/W	AUTOXOFF	0
Bit 14	R/W	TBYP	0
Bit 13	R/W	RBYP	0
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	RATE[1]	1
Bit 8	R/W	RATE[0]	1
Bit 7	R/W	UNI_POTS	0
Bit 6	R/W	AUTOFEBE	1
Bit 5	R/W	AUTOLRDI	1
Bit 4	R/W	AUTOPRDI	1
Bit 3	R/W	TFIFOINV	0
Bit 2	R/W	RFIFOINV	0
Bit 1	R/W	RXDINV	0
Bit 0	R/W	STS1	0

STS1:
The STS1 bit configures the LASAR-155 to expect a STS-1 Physical Transmission Convergence sub layer. When STS1 is set to logic one, the LASAR-155 is configured for a STS-1 Physical Transmission Convergence sub layer. When STS1 is set to logic zero, the LASAR-155 is configured for a STS-3c (STM-1) Physical Transmission Convergence sub layer.

RXDINV:
The RXDINV bit selects the active polarity of the RXD+/- signals. The default configuration selects RXD+ to be active high and RXD- to be active low. When RXDINV is set to logic one, RXD+ to be active low and RXD- to be active high. Polarity invert (RXDINV) is not supported when line loopback (LLE) is enabled (If LLE = 1 then RXDINV must be set to 0).

RFIFOINV:
The RFIFOINV bit selects the active polarity of the RFIFOEB/RFIFOFB signal. The default configuration selects RFIFOEB/RFIFOFB to be active low. When RFIFOINV is set to logic one, the RFIFOEB/RFIFOFB signal becomes active high. If RXPHYBP is set to logic one, RFIFOINV is not used and should be set to logic zero.

TFIFOINV:
The TFIFOINV bit selects the active polarity of the TFIFOFB/TFIFOEB signal. The default configuration selects TFIFOFB/TFIFOEB to be active low. When TFIFOINV is set to logic one, the TFIFOFB/TFIFOEB signal becomes active high. If TXPHYBP is set to logic one, TFIFOINV is not used and should be set to logic zero.

AUTOPRDI
The AUTOPRDI bit determines whether STS path Remote Defect Indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, STS path RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), line AIS, loss of pointer (LOP), or STS path AIS.

AUTOLRDI
The AUTOLRDI bit determines whether the line Remote Defect Indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF) or line AIS.

AUTOFEBE
The AUTOFEBE bit determines whether line and path far end block errors are sent upon detection of an incoming line and path BIP error events. When AUTOFEBE is set to logic one, one line or path FEBE is inserted for each line or path BIP error event. When AUTOFEBE is set to logic zero, incoming line or path BIP error events do not generate FEBE events.

RATE[1:0]:
The RATE[1:0] bits select the operation rate of the LASAR-155. The default configuration selects STS-3c (STM-1) rate operation. The LASAR-155 will not operate correctly if a Reserved mode is selected.

RATE[1:0]	MODE
00	Reserved
01	Reserved
10	51.84 Mbit/s, STS-1
11	155.52 Mbit/s, STS-3c (STM-1)

UNI_POTS

The UNI_POTS bit selects the function for the RGFC/RLD, RCP/RLDCLK, TGFC/TLD and TCP/TLDCLK. When UNI_POTS is set to logic one, the signals are configured to source and sink the SONET Line Data Communication Channel (DCC). When UNI_POTS is set to logic zero, the signals are configured to source and sink the GFC bits in cell headers.

RBYP

The RBYP bit disables clock recovery. When RBYP is set to logic one, RXD+/- is sampled on the rising edge of RRCLK+/-. When RBYP is set to logic zero, the receive clock is recovered from the RXD+/- bit stream.

TBYP

The TBYP bit disables clock synthesis. When TBYP is set to logic one, transmit clock synthesis is disabled and TRCLK+/- becomes the line rate clock of 155.52 MHz or 51.84 MHz. When TBYP is set to logic zero, the transmit clock is synthesized from a 19.44 MHz or 6.48 MHz reference.

AUTOXOFF

The AUTOXOFF bit determines whether to use the received GFC codes to enforce an XON/XOFF protocol. When AUTOXOFF is set to logic one, receive GFC codes are used to XON and XOFF transmission. When AUTOXOFF is set to logic zero, the received GFC codes are ignored.

10.1.3 Register 0x02 (0x008): LASAR-155 Master Interrupt Status

Bit	Type	Function	Default
Bit 15	R	PCIDI	X
Bit 14	R	RALPI	X
Bit 13	R	TALPI	X
Bit 12	R	TATSI	X
Bit 11	R	SARPMONI	X
Bit 10	R	EXTINTBI	X
Bit 9		Unused	X
Bit 8	R	Reserved	X
Bit 7	R	TROOLI	X
Bit 6	R	LCDI	X
Bit 5	R	RDOOLI	X
Bit 4	R	TACPI	X
Bit 3	R	RACPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level. For interrupts PCIDI, RALPI, TALPI, TATSI, SARPMONI, EXTINTBI, TACPI, RACPI, RPOPI, RLOPI and RSOPI, further register accesses are required to the block in question to determine the cause of an active interrupt and to clear the interrupt. Interrupts TROOLI, LCDI and RDOOLI are cleared when this register is read.

RSOPI:
The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:
The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:
The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RACPI:
The RACPI bit is high when an interrupt request is active from the RACP block. The RACP interrupt sources are enabled in the RACP Interrupt Enable/Status Register.

TACPI:
The TACPI bit is high when an interrupt request is active from the TACP block. The TACP interrupt sources are enabled in the TACP Interrupt Control/Status Register.

RDOOLI:
The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the RDOOLV bit of the LASAR-155 Clock Recovery Control and Status register changes state. RDOOLV is a logic one if the divided down recovered clock frequency is not within 488 ppm of the RRCLK+/- frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods. RDOOLI is cleared when this register is read.

LCDI:
The LCDI interrupt bit is set high when entering and exiting loss of cell delineation. This bit is reset immediately after a read to this register. The LCD interrupt is enabled in the LASAR-155 Master Control Register.

TROOLI:
The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is set high when the TROOLV bit of the LASAR-155 Clock Synthesis Control and Status register changes state. TROOLV indicates the clock synthesis phase

locked loop is unable to lock to the reference on RRCLK+/- and is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the TRCLK+/- frequency. TROOLI is cleared when this register is read.

EXTINTBI
The EXTINTBI bit is the external interrupt status bit. When the LASAR-155 is configured for master operation (MPENB=1), EXTINTBI is high when an external device asserts an interrupt on input INTB. When the LASAR-155 is configured for slave operation (MPENB=0), EXTINTBI is not used and should be ignored.

SARPMONI:
The SARPMONI bit is high when an interrupt request is active from the SAR PMON block. The SAR PMON interrupt sources are enabled in the SAR PMON Count Change Register.

TATSI:
The TATSI bit is high when an interrupt request is active from the TATS block. The TATS interrupt sources are enabled in the TATS Control/Interrupt Enable Register.

TALPI:
The TALPI bit is high when an interrupt request is active from the TALP block. The TALP interrupt sources are enabled in the TALP Interrupt Enable Register.

RALPI:
The RALPI bit is high when an interrupt request is active from the RALP block. The RALP interrupt sources are enabled in the RALP Interrupt Enable Register.

PCIDI:
The PCIDI bit is high when an interrupt request is active from the PCID Microprocessor Interrupt Status Register. The PCID interrupt sources are enabled in the PCID Microprocessor Control Register.

10.1.4 Register 0x03 (0x00C): LASAR-155 Master Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	PCIDE	0
Bit 14	R/W	RALPE	0
Bit 13	R/W	TALPE	0
Bit 12	R/W	TATSE	0
Bit 11	R/W	SARPMONE	0
Bit 10	R/W	EXTINTBE	0
Bit 9		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	TROOLE	0
Bit 6	R/W	LCDE	0
Bit 5	R/W	RDOOLE	0
Bit 4	R/W	TACPE	0
Bit 3	R/W	RACPE	0
Bit 2	R/W	RPOPE	0
Bit 1	R/W	RLOPE	0
Bit 0	R/W	RSOPE	0

RSOPE, RLOPE, RPOPE, RACPE, TACPE, RDOOLE, LCDE, TROOLE, SARPMONE, EXTINTBE, TATSE, TALPE, RALPE, PCIDE:
The above enable bits control the generation of interrupts by the corresponding interrupt bits in the LASAR-155 Master Interrupt Status register. When the enable bit is set to logic one, the corresponding interrupt bit will generated an interrupt on output INTB or PCIINTB.

10.1.5 Register 0x04 (0x010): LASAR-155 Master Clock Monitor

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	SYSCLKA	X
Bit 4	R	PCICLKA	X
Bit 3	R	RRCLKA	X

Bit 2	R	TRCLKA	X
Bit 1	R	RCLKA	X
Bit 0	R	TCLKA	X

This register provides activity monitoring on LASAR-155 clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at regular intervals to detect clock failures.

TCLKA:
The TCLK active (TCLKA) bit monitors for low to high transitions on the TCLK output. TCLKA is set high on a rising edge of TCLK, and is set low when this register is read.

RCLKA:
The RCLK active (RCLKA) bit monitors for low to high transitions on the RCLK output. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

TRCLKA:
The TRCLK active (TRCLKA) bit monitors for low to high transitions on the TRCLK+ and TRCLK- inputs. TRCLKA is set high on a rising edge of TRCLK+, and is set low when this register is read.

RRCLKA:
The RRCLK active (RRCLKA) bit monitors for low to high transitions on the RRCLK+ and RRCLK- inputs. RRCLKA is set high on a rising edge of RRCLK+, and is set low when this register is read.

PCICLKA:
The PCICLK active (PCICLKA) bit monitors for low to high transitions on the PCICLK input. PCICLKA is set high on a rising edge of PCICLK, and is set low when this register is read.

SYSCLKA:
The SYSCLK active (SYSCLKA) bit monitors for low to high transitions on the SYSCLK input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read.

10.1.6 Register 0x05 (0x014): LASAR-155 Master Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	INIT	0
Bit 8	R	INIT_STAT	X
Bit 7		Unused	X
Bit 6	R	LCDV	X
Bit 5	R/W	FIXPTR	1
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LLE	0
Bit 1	R/W	DLE	0
Bit 0	R/W	LOOPT	0

This register controls the timing and high speed loopback features of the LASAR-155.

LOOPT:
The LOOPT bit selects the source of timing for the transmit section of the LASAR-155. When LOOPT is a logic zero, the transmitter timing is derived from inputs TRCLK+ and TRCLK-.

When LOOPT is a logic one, the transmitter timing is derived from the receiver inputs RXD+ and RXD- when clock recovery is enabled and from RRCLK+ and RRCLK- when clock recovery is disabled.

DLE:
The DLE bit enables the LASAR-155 diagnostic loopback. When DLE is a logic one, the transmit stream is connected to the receive stream. Note, whether loopback is through the CRU or not depends on the RBYP bit in the LASAR-155 Master Configuration register. Simultaneous diagnostic loopback and line loopback is not supported.

LLE:
The LLE bit enables the LASAR-155 line loopback. When LLE is a logic one, RXD+ and RXD-, are connected internally to TXD+ and TXD-, respectively. Simultaneous diagnostic loopback and line loopback is not supported. Polarity invert (RXDINV) is not supported when line loopback (LLE) is enabled (If LLE = 1 then RXDINV must be set to 0).

FIXPTR:
The FIXPTR bit disables transmit payload pointer adjustments. If the FIXPTR bit is a logic 1, the transmit payload pointer is set at 522. If FIXPTR is a logic zero, the payload pointer is controlled by the contents of the TPOP Pointer Control register.

LCDV:
The LCDV bit reflects the current loss of cell delineation state. LCDV becomes a logic 1 when an out of cell delineation state has persisted for 4 ms without any lower level alarms (LOS, LOP, Path AIS, Line AIS) occurring. LCDV becomes logic 0 when the SYNC state has been maintained for 4 ms.

LCDE:
The LCDE bit enables the loss of cell delineation (LCD) interrupt. When logic one, the LASAR-155 INTB or PCIINTB output is asserted when there is a change in the LCD state. When logic zero, the LASAR-155 INTB or PCIINTB output is not affected by the change in LCD state.

INIT_STAT:
The INIT_STAT bit indicates the initialization status of the LASAR-155. When the INIT bit is set high, the LASAR-155 initializes its internal RAMs and sets the INIT_STAT bit. The INIT_STAT bit remains set until the LASAR-155 has completed its initialization procedures. When initialization has completed, the LASAR-155 sets the INIT_STAT bit low.

INIT:
The INIT bit enables the internal initialization procedures. After startup and after every reset, the user must force the LASAR-155 to execute its initialization procedures before configuring the LASAR-155 for AAL Layer processing. When INIT is set high, the LASAR-155 starts its initialization procedures. Once started, initialization procedures are performed to completion. The INIT_STAT bit can be used to indicate when the initialization procedures are complete. The INIT bit must manually be set low.

The NVPI[3:0] and NVCI[3:0] fields in the COPS Control register must be set to the desired value before INIT is used to start the internal initialization procedure. The entire initialization procedure requires a maximum of 20 µs.

10.1.7 Register 0x06 (0x018): LASAR-155 Clock Synthesis Control and Status

Bit	Type	Function	Default
Bit 15	R	TBUS[2]	X
Bit 14	R	TBUS[1]	X
Bit 13	R	TBUS[0]	X
Bit 12	R	TDOOLV	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	TROOLV	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TREFSEL	0

This register controls the clock synthesis and reports the state of the transmit phase locked loop.

TREFSEL:
The transmit reference select (TREFSEL) bit determines the expected frequency of TRCLK+/-. If TREFSEL is a logic 0, the correct line clock frequency is synthesized if the reference frequency is 19.44 MHz. If TREFSEL is a logic 1, the reference frequency must be 6.48 MHz. TREFSEL only has effect if the TBYP bit in the LASAR-155 Master Configuration register is low.

TROOLV:
The transmit reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference on TRCLK+/-. TROOLV is a logic one if the divided down synthesized clock frequency not within 488 ppm of the TRCLK+/- frequency.

TBUS[2:0], TDOOLV:
The TBUS[2:0] and TDOOLV bits are provided for analog production test and should be ignored.

10.1.8 Register 0x07 (0x01C): LASAR-155 Clock Recovery Control and Status

Bit	Type	Function	Default
Bit 15	R	TBUS[2]	X
Bit 14	R	TBUS[1]	X
Bit 13	R	TBUS[0]	X
Bit 12	R	RROOLV	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RDOOLV	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RREFSEL	0

This register controls the clock recovery and reports the state of the receive phase locked loop.

RREFSEL:
The receive reference select (RREFSEL) bit determines the expected frequency of RRCLK+/-. If RREFSEL is a logic 0, the reference frequency is 19.44 MHz. If RREFSEL is a logic 1, the reference frequency must be 6.48 MHz. RREFSEL only has effect if the RBYP bit in the LASAR-155 Master Configuration register is low.

RDOOLV:
The receive data out of lock status indicates the clock recovery phase locked loop is unable to lock to the incoming data stream. RDOOLV is a logic one if the divided down recovered clock frequency not within 488 ppm of the RRCLK+/- frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods.

RROOLV:
The receive reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the receive reference (RRCLK+/-). RROOLV should be polled after a power up reset to determine when the CRU PLL is

operational. When RROOLV is a logic 1, the CRU is unable to lock to the receive reference. When RROOLV is a logic 0, the CRU is locked to the receive reference. The RROOLV bit may remain set at logic 1 for several hundred milliseconds after the removal of the power on reset as the CRU PLL locks to the receive reference clock.

TBUS[2:0]:
The TBUS[2:0] bits are provided for analog production test and should be ignored.

10.1.9 Register 0x10 (0x040): RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:
The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is set to logic one, an interrupt is generated when the out of frame alarm changes state.

LOFE:
The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:
The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:
The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

ALGO2:
The ALGO2 bit position selects the framing algorithm used to determine and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the first A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF:
The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:
The DDS bit is set to logic one to disable the descrambling of the STS-3c (STM-1) stream. When DDS is a logic zero, descrambling is enabled.

Reserved:
The reserved bit must be programmed to logic zero for proper operation.

10.1.10 Register 0x11 (0x044): RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:
The OOFV bit is read to determine the out of frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:
The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:
The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:
The OOFI bit is the out of frame interrupt status bit. OOFI is set high when a change in the out of frame state occurs. This bit is cleared when this register is read.

LOFI:
The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a

change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:
The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:
The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

10.1.11 Register 0x12 (0x048): RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

10.1.12 Register 0x13 (0x04C): RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:
Bits SBE[15:0] represent the number of section BIP-8 errors (B1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.13 Register 0x14 (0x050): TSOP Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:
The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET frame being set to 1 prior to scrambling except for the section overhead.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

DS:
The DS bit is set to logic one to disable the scrambling of the STS-3c (STM-1) or STS-1 stream. When DS is a logic zero, scrambling is enabled.

10.1.14 Register 0x15 (0x054): TSOP Diagnostic

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:
The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:
The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:
The DLOS bit controls the insertion of all zeros in the transmit stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

10.1.15 Register 0x18 (0x060): RLOP Control/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R	LAISV	0
Bit 0	R	FERFV	0

FERFV:
The FERFV bit is read to determine the far end receive failure state of the RLOP. When FERFV is high, the RLOP has declared line FERF.

LAISV:
The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.16 Register 0x19 (0x064): RLOP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	FERFE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	FERFI	X

FERFI:
The FERFI bit is the far end receive failure interrupt status bit. FERFI is set high when a change in the line FERF state occurs. This bit is cleared when this register is read.

LAISI:
The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:
The BIPEI bit is the line BIP-8/24 interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:
The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (Z2) is detected. This bit is cleared when this register is read.

FERFE:
The FERFE bit is an interrupt enable for the far end receive failure alarm. When

FERFE is set to logic one, an interrupt is generated when the FERF alarm changes state.

LAISE:
The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:
The BIPEE bit is an interrupt enable for the line BIP-8/24 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-8/24 error (B2) is detected.

FEBEE:
The FEBEE bit is an interrupt enable for the line far end block errors. When FEBEE is set to logic one, an interrupt is generated when a FEBE (Z2) is detected.

10.1.17 Register 0x1A (0x068): RLOP Line BIP-8/24 LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

10.1.18 Register 0x1B (0x06C): RLOP Line BIP-8/24

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

10.1.19 Register 0x1C (0x070): RLOP Line BIP-8/24 MSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]
Bits LBE[19:0] represent the number of line BIP-8/24 errors (B2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.20 Register 0x1D (0x074): RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

10.1.21 Register 0x1E (0x078): RLOP Line FEBE

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

10.1.22 Register 0x1F (0x07C): RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]
Bits LFE[19:0] represent the number of line FEBE errors (Z2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.23 Register 0x20 (0x080): TLOP Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	FERF	0

FERF:
The FERF bit controls the insertion of line far end receive failure (FERF). When FERF is set to logic one, the TLOP inserts line FERF into the transmit SONET stream. Line FERF is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte of the transmit stream.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.24 Register 0x21 (0x084): TLOP Diagnostic

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP	0

DBIP:
The DBIP bit controls the insertion of bit errors continuously in the line BIP byte(s) (B2). When DBIP is set to logic one, the B2 byte(s) are inverted.

10.1.25 Register 0x30 (0x0C0): RPOP Status/Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOP	X
Bit 4		Unused	X
Bit 3	R	PAIS	X
Bit 2	R	PRDI	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

This register allows the status of path level alarms to be monitored.

PRDI, PAIS,LOP:
The PRDI, PAIS, and LOP bits reflect the current state of the corresponding path level alarms.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.26 Register 0x31 (0x0C4): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgment of path level alarm and error event interrupts. These bits (and the interrupt) are cleared when this register is read.

FEBEI, BIPEI:
The BIPEI and FEBEI bits are set to logic one when the corresponding event, a path BIP-8 error or path FEBE is detected.

PRDII, PAISI, LOPI:
The PRDII, PAISI, and LOPI bits are set to logic one when a transition occurs in the corresponding alarm state.

PSLI:
The PSLI bit is set to logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register.

10.1.28 Register 0x33 (0x0CC): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:
When a 1 is written to the FEBEE interrupt enable bit position, the reception of one or more FEBEs will activate the interrupt output.

BIPEE:
When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt output.

PRDIE:
When a 1 is written to the PRDIE interrupt enable bit position, a change in the path Remote Defect Indication state will activate the interrupt output.

PAISE:
When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt output.

LOPE:
When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt output.

PSLE:
When a 1 is written to the PSLE interrupt enable bit position, a change in the path signal label will activate the interrupt output.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.32 Register 0x37 (0x0DC): RPOP Path Signal Label

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register allows the received path signal label byte to be read.

PSL[7:0]:
The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three consecutive frames.

10.1.33 Register 0x38 (0x0E0): RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

10.1.34 Register 0x39 (0x0E4): RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:
Bits PBE[15:0] represent the number of path BIP-8 errors (B3) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.35 Register 0x3A (0x0E8): RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PFE[7]	X
Bit 6	R	PFE[6]	X
Bit 5	R	PFE[5]	X
Bit 4	R	PFE[4]	X
Bit 3	R	PFE[3]	X
Bit 2	R	PFE[2]	X
Bit 1	R	PFE[1]	X
Bit 0	R	PFE[0]	X

10.1.36 Register 0x3B (0x0EC): RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PFE[15]	X
Bit 6	R	PFE[14]	X
Bit 5	R	PFE[13]	X
Bit 4	R	PFE[12]	X
Bit 3	R	PFE[11]	X
Bit 2	R	PFE[10]	X
Bit 1	R	PFE[9]	X
Bit 0	R	PFE[8]	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:
Bits PFE[15:0] represent the number of path FEBE errors (G1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.37 Register 0x40 (0x100): TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

This register allows insertion of path level alarms and diagnostic signals.

PAIS:
The PAIS bit controls the insertion of STS path alarm indication signal. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DB3:
The DB3 bit controls the inversion of the B3 byte value. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.38 Register 0x41 (0x104): TPOP Pointer Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:
The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

NSE:
The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

NDF:
The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the TPOP Arbitrary Pointer MSB Register is inserted

continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110B) is inserted in the payload pointer.

PLD:
The PLD bit controls the loading of the pointer value contained in the TPOP Arbitrary Pointer Registers. Normally, the TPOP Arbitrary Pointer Registers are written to set up the arbitrary new pointer value and a logic one is then written to this bit position to load the new pointer value.

If a legal value (i.e. 0 • pointer value • 782) is transferred from the TPOP Arbitrary Pointer Registers, the transmit payload pointer will immediately change to the corresponding byte position. If a value greater than 782 is transferred, the payload pointer remains unchanged.

This bit is automatically cleared after the new payload pointer has been loaded. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

SOS:
The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:
The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the TPOP Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated, although it is unlikely to be extracted by far end circuitry which should be in a loss of pointer state. If FTPTR is set to logic 1, the APTR[9:0] bits of the TPOP Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. If FTPTR is a logic 0, a valid pointer is inserted.

Reserved:
The reserved bit must be programmed to logic zero for proper operation.

10.1.41 Register 0x45 (0x114): TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7:0]:
The APTR[7:0] bits, along with the APTR[9:8] bits in the TPOP Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is transferred by writing a logic one to the PLD bit in the TPOP Pointer Control Register. A legal value (i.e. 0 • pointer value • 782) results in the transmit payload pointer immediately changing to the corresponding byte position. If a value greater than 782 is transferred, the payload pointer remains unchanged.

If the FTPTR bit in the TPOP Pointer Control register is a logic 1, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

10.1.42 Register 0x46 (0x118): TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	0
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9:8]:
The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

S[1:0]:
The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3:0]:
The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the TPOP Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

10.1.44 Register 0x48 (0x120): TPOP Path Signal Label

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	1
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	1
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label.

C2[7:0]:
The C2[7:0] bits are inserted in the C2 byte position.

10.1.45 Register 0x49 (0x124): TPOP Path Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

G1[2:0]:
The G1[2:0] bits are inserted in the unused bit positions in the path status byte.

PRDI:
The PRDI bit controls the insertion of STS path Remote Defect Indicator. When a logic one is written to this bit position, the PRDI bit position in the path status byte is set high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low.

FEBE[3:0]:
The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

10.1.52 Register 0x50 (0x140): RACP Control/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	OCDV	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	PASS	0
Bit 4	R/W	DISCOR	0
Bit 3	R/W	HECPASS	0
Bit 2	R/W	HECADD	1
Bit 1	R/W	DDSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:
The FIFORST bit is used to reset the internal four cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DDSCR:
The DDSCR bit controls the descrambling of the cell payload. When DDSCR is a logic one, cell payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled.

HECADD:
The HECADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HEC octet prior to comparison. When HECADD is a logic one, the polynomial is added, and the resulting HEC is compared. When HECADD is a logic zero, the polynomial is not added, and the unmodified HEC is compared.

HECPASS:
The HECPASS bit controls the dropping of cells based on the detection of an uncorrectable HEC error. When HECPASS is a logic zero, cells containing an uncorrectable HEC error are dropped. When HECPASS is a logic one, cells are passed to the RALP block regardless of errors detected in the HEC. In addition, the HEC verification finite state machine never exits in the correction mode. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

DISCOR:
The DISCOR bit disables the HEC error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HEC error.

PASS:
The PASS bit controls the function of the cell filter. When PASS is written with a logic zero, all cells matching the cell filter are dropped. When PASS is a logic one, the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to 0 is not performed. The default state of this bit together with the default states of the bits in the RACP Match Mask and RACP Match Pattern Registers enable the dropping of cells containing all zero VCI and VPI fields.

OCDV:
The OCDV bit indicates the cell delineation state. When OCDV is set high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states, and is hunting for the cell boundaries in the synchronous payload envelope. When OCDV is set low, the cell delineation state machine is in the 'SYNC' state and cells are passed to the RALP block.

Reserved:
The reserved bit must be programmed to logic zero for proper operation.

10.1.53 Register 0x51 (0x144): RACP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	OCDE	0
Bit 6	R/W	HECE	0
Bit 5	R/W	FOVRE	0
Bit 4	R	OCDI	X
Bit 3	R	CHECI	X
Bit 2	R	UHECI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:
The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register.

UHECI:
The UHECI bit is set high when an uncorrectable HEC error is detected. This bit is reset immediately after a read to this register.

CHECI:
The CHECI bit is set high when a correctable HEC error is detected. This bit is reset immediately after a read to this register.

OCDI:
The OCDI bit is set high when a change of cell delineation state has occurred. The OCDI bit is set high when the RACP block transitions from the PRESYNC state to the SYNC state and from the SYNC state to the HUNT state. This bit is reset immediately after a read to this register.

FOVRE:
The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic one, the interrupt is enabled.

HECE:
The HECE bit enables the generation of an interrupt due to the detection of a correctable or an uncorrectable HEC error. When HECE is set to logic one, the interrupts are enabled.

OCDE:
The OCDE bit enables the generation of an interrupt due to a change of cell delineation state. When OCDE is set to logic one, the interrupt is enabled.

10.1.54 Register 0x52 (0x148): RACP Match Header Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

CLP:
The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of cells matching this pattern.

PTI[2:0]:
The PTI[2:0] bits contain the pattern to match in the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of cells matching this pattern.

GFC[3:0]:
The GFC[3:0] bits contain the pattern to match in the first, second, third and fourth bits of the first octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

10.1.55 Register 0x53 (0x14C): RACP Match Header Mask

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	MGFC[3]	0
Bit 6	R/W	MGFC[2]	0
Bit 5	R/W	MGFC[1]	0
Bit 4	R/W	MGFC[0]	0
Bit 3	R/W	MPTI[2]	0
Bit 2	R/W	MPTI[1]	0
Bit 1	R/W	MPTI[0]	0
Bit 0	R/W	MCLP	0

MCLP:
The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

MPTI[2:0]:
The MPTI[2:0] bits contain the mask pattern for the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]:
The MGFC[3:0] bits contain the mask pattern for the first, second, third and fourth bits of the first octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

10.1.56 Register 0x54 (0x150): RACP Correctable HEC Error Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	CHEC[7]	X
Bit 6	R	CHEC[6]	X
Bit 5	R	CHEC[5]	X
Bit 4	R	CHEC[4]	X
Bit 3	R	CHEC[3]	X
Bit 2	R	CHEC[2]	X
Bit 1	R	CHEC[1]	X
Bit 0	R	CHEC[0]	X

CHEC[7:0]:
The CHEC[7:0] bits indicate the number of correctable HEC error events that occurred during the last accumulation interval. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the correctable HEC error count register address, or to the uncorrectable HEC error count register address.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.57 Register 0x55 (0x154): RACP Uncorrectable HEC Error Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	UHEC[7]	X
Bit 6	R	UHEC[6]	X
Bit 5	R	UHEC[5]	X
Bit 4	R	UHEC[4]	X
Bit 3	R	UHEC[3]	X
Bit 2	R	UHEC[2]	X
Bit 1	R	UHEC[1]	X
Bit 0	R	UHEC[0]	X

UHEC[7:0]:
The UHEC[7:0] bits indicate the number of uncorrectable HEC error events that occurred during the last accumulation interval. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the correctable HEC error count register address, or to the uncorrectable HEC error count register address.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.58 Register 0x56 (0x158): RACP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

10.1.59 Register 0x57 (0x15C): RACP Receive Cell Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

10.1.60 Register 0x58 (0x160): RACP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[18:0]:
The RCELL[18:0] bits indicate the number of cells received and passed to the RALP block during the last accumulation interval. Cells received and filtered due to HEC errors or Idle/Unassigned cell matches are not counted. The counter should be polled every second to avoid saturating. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the correctable HEC error count register addresses, the uncorrectable HEC error count register addresses or the receive cell counter register addresses.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.61 Register 0x59 (0x164): RACP Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	RGFCE[3]	1
Bit 6	R/W	RGFCE[2]	1
Bit 5	R/W	RGFCE[1]	1
Bit 4	R/W	RGFCE[0]	1
Bit 3	R/W	FSEN	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	HECFTR[1]	0
Bit 0	R/W	HECFTR[0]	0

HECFTR[1:0]:
The HEC filter bits, HECFTR[1:0], indicate the number of consecutive error free cells required while in detection mode before reverting back to correction mode. Please refer to Figure 9.3 for details.

HECFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HEC before resumption of Cell acceptance. This cell is accepted.
01	Two ATM cells with correct HEC before resumption of Cell acceptance. The last cell is accepted.
10	Four ATM cells with correct HEC before resumption of Cell acceptance. The last cell is accepted.
11	Eight ATM cells with correct HEC before resumption of Cell acceptance. The last cell is accepted.

FSEN:
The active high fix stuff control enable bit FSEN determines the payload mapping of ATM cells when STS-1 mapping is selected. When FSEN is set to logic one,

the RACP ignores the bytes in the two stuff columns. When FSEN is set to logic zero, the RACP assumes the entire SPE contains ATM cell payload.

RGFCE[3:0]:
The receive GFC enable bits, RGFCE[3:0], determine which generic flow control bits are presented on the RGFC. RGFCE[3] corresponds to the most significant GFC bit (first bit in the cell). If a RGFCE bit is a logic 1, the RGFC output changes in the appropriate bit location to the state of the associated GFC bit in the current cell; otherwise, RGFC remains in its current state.

Reserved:
The reserved bit must be programmed to logic one for proper operation.

10.1.62 Register 0x60 (0x180): TACP Control/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R/W	DHEC	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	HECADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:
The FIFORST bit is used to reset the internal four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DSCR:
The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HECADD:
The HECADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HEC octet prior to insertion in the synchronous payload envelope. When HECADD is a logic one, the polynomial is added, and the resulting HEC is inserted. When HECADD is a logic zero, the polynomial is not added, and the unmodified HEC is inserted.

DHEC:
The DHEC bit controls the insertion of HEC errors for diagnostic purposes. When DHEC is set to logic one, the HEC octet is inverted prior to insertion in the synchronous payload envelope.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.63 Register 0x61 (0x184): TACP Idle/Unassigned Cell Header Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

CLP:
The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding assigned cells need to be transmitted.

PTI[2:0]:
The PTI[2:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding assigned cells need to be transmitted.

GFC[3:0]:
The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding assigned cells need to be transmitted. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

10.1.64 Register 0x62 (0x188): TACP Idle/Unassigned Cell Payload Octet Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	ICP[7]	0
Bit 6	R/W	ICP[6]	1
Bit 5	R/W	ICP[5]	1
Bit 4	R/W	ICP[4]	0
Bit 3	R/W	ICP[3]	1
Bit 2	R/W	ICP[2]	0
Bit 1	R/W	ICP[1]	1
Bit 0	R/W	ICP[0]	0

ICP[7:0]:
The ICP[7:0] bits contain the pattern inserted in the payload octets of the idle or unassigned cell. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding assigned cells need to be transmitted. Bit ICP[7] corresponds to the most significant bit of the octet, the first bit transmitted.

10.1.65 Register 0x63 (0x18C): TACP FIFO Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

FIFODP[1:0]:
The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the TACP must be minimized. When the FIFO is filled to the specified depth, the TACP back pressures the cell stream from the TALP block. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.66 Register 0x64 (0x190): TACP Transmit Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

10.1.67 Register 0x65 (0x194): TACP Transmit Cell Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

10.1.68 Register 0x66 (0x198): TACP Transmit Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[18:0]:
The TCELL[18:0] bits indicate the number of cells from the TALP block that are inserted into the SPE during the last accumulation interval. Idle/Unassigned cells inserted into the SPE are not counted.

A write to any one of the TACP Transmit Cell Counter registers loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the TACP Transmit Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the transmit cell count register space.

The error count can also be polled by writing to the LASAR-155 Master Reset / Load Meters register. Writing to the register loads all the error counter registers in the SAR PMON, RSOP, RLOP, RPOP, RACP and TACP blocks.

10.1.69 Register 0x67 (0x19C): TACP Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TGFCE[3]	0
Bit 6	R/W	TGFCE[2]	0
Bit 5	R/W	TGFCE[1]	0
Bit 4	R/W	TGFCE[0]	0
Bit 3	R/W	FSEN	1
Bit 2	R/W	H4INSB	0
Bit 1	R/W	FIXBYTE[1]	0
Bit 0	R/W	FIXBYTE[0]	0

FIXBYTE[1:0]:
The FIXBYTE[1:0] bits identify the byte pattern inserted into fixed byte columns of the synchronous payload envelope.

FIXBYTE[1]	FIXBYTE[0]	BYTE
0	0	00H
0	1	55H
1	0	AAH
1	1	FFH

H4INSB:
The active low H4 insert enable, H4INSB bit determines the contents of the H4 byte in the outgoing SPE. If H4INSB is set to logic one, the H4 byte is set to the value of 00 hexadecimal. If H4INSB is set to logic zero, the H4 byte is set to the cell indicator offset value.

FSEN:
The active high fix stuff control enable, FSEN bit determines the payload mapping of ATM cells for STS-1 mapping. When FSEN is set to logic one, the

TACP does not map ATM cells into the two fixed stuff columns. When FSEN is set to logic zero, the TACP maps cells into the entire SPE.

TGFCE[3:0]:
The GFC enable bits, TGFCE[3:0], enable the insertion of the associated GFC bit by the TGFC serial input. If TGFCE[3] is a logic 1, first bit of the 4 bit serial sequence is inserted into the most significant GFC bit transmitted. Likewise, if TGFCE[0] is a logic 1, last bit of the sequence is inserted into the least significant GFC bit transmitted. If a bit is logic 0, the associated GFC bit value is supplied by the TALP block for the case of an assigned cell, or from the Idle/Unassigned Cell Header Control register for the case of unassigned cells.

10.1.70 Register 0x70 (0x1C0): SAR PMON Count Change

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	R	INTR	X
Bit 13	R	OVR	X
Bit 12	R	RUVPI/VCI_CH	X
Bit 11	R	RCRC10_CH	X
Bit 10	R	RNZCPI_CH	X
Bit 9	R	RSDUL_CH	X
Bit 8	R	RCRC32_CH	X
Bit 7	R	ROVPDU_CH	X
Bit 6	R	Reserved	X
Bit 5	R	RPDUAB_CH	X
Bit 4	R	RPBE_CH	X
Bit 3	R	RMBE_CH	X
Bit 2	R	RPDU_CH	X
Bit 1	R	TOVSDU_CH	X
Bit 0	R	TPDU_CH	X

The SAR PMON Count Change register indicates if a SAR PMON counter has changed since the last time the SAR PMON counters were polled. The SAR PMON Count Change register can be loaded by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally change detect latches to the above register within 1µs.

TPDU_CH:
When logic one, the TPDU_CH bit indicates that the SAR PMON Transmit PDU Count register has incremented since the last accumulation interval.

TOVSDU_CH
When logic one, the TOVSDU_CH bit indicates that the SAR PMON Transmit Oversize SDU Errors register has incremented since the last accumulation interval.

RPDU_CH:
When logic one, the RPDU_CH bit indicates that the SAR PMON Receive PDU Count register has incremented since the last accumulation interval.

RMBE_CH:
When logic one, the RMBE_CH bit indicates that the SAR PMON Receive Buffer Errors register has incremented since the last accumulation interval.

RPBE_CH:
When logic one, the RPBE_CH bit indicates that the SAR PMON Receive Buffer Errors register has incremented since the last accumulation interval.

RPDUAB_CH:
When logic one, the RPDUAB_CH bit indicates that the SAR PMON Receive PDU Abort Errors register has incremented since the last accumulation interval.

ROVPDU_CH:
When logic one, the ROVPDU_CH bit indicates that the SAR PMON Receive Oversize PDU Errors Count register has incremented since the last accumulation interval.

RCRC32_CH:
When logic one, the RCRC32_CH bit indicates that the SAR PMON Receive CRC-32 Errors register has incremented since the last accumulation interval.

RSDUL_CH:
When logic one, the RSDUL_CH bit indicates that the SAR PMON Receive SDU Length Errors register has incremented since the last accumulation interval.

RNZCPI_CH:
When logic one, the RNZCPI_CH bit indicates that the SAR PMON Receive Non

Zero Common Part Indicator Errors register has incremented since the last accumulation interval.

RCRC10_CH:
When logic one, the RCRC10_CH bit indicates that the SAR PMON Receive CRC-10 Errors register has incremented since the last accumulation interval.

RUVPI/VCI_CH:
When logic one, the RUVPI/VCI_CH bit indicates that the SAR PMON Receive Unprovisioned VPI/VCI Errors register has incremented since the last accumulation interval.

OVR:
The overrun (OVR) bit indicates the overrun status of the SAR PMON Holding Registers. A logic one in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the Holding Registers have been overwritten. A logic zero indicates that no overrun has occurred. This bit is reset to logic zero when this register is read.

INTR:
The interrupt (INTR) bit indicates the current status of the internal interrupt signal. A logic one in this bit position indicates that a transfer of counter values to the SAR PMON Holding Registers has occurred; a logic zero indicates that no transfer has occurred. This bit is set to logic zero when this register is read. The value of the INTR bit is not affected by the value of the INTE bit.

INTE:
The interrupt enable (INTE) bit controls the operation of the appropriate interrupt output. A logic one in the INTE bit position enables the SAR PMON to generate a microprocessor interrupt when the counter values are transferred to the SAR PMON Holding Registers. A logic zero in the INTE bit position disables the SAR PMON from generating an interrupt. When the SAR PMON is reset, the INTE bit is set to logic zero, disabling the interrupt. The interrupt is cleared when this register is read.

10.1.71 Register 0x72 (0x1C8): SAR PMON Receive Unprovisioned VPI/VCI Errors (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RUVPI/VCIE [15:0]	X

10.1.72 Register 0x73 (0x1CC): SAR PMON Receive Unprovisioned VPI/VCI Errors (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 3		Unused	X
Bit 2 to Bit 0	R	RUVPI/VCIE [18:16]	X

RUVPI/VCIE[18:0]:
RUVPI/VCI[18:0] represents the number of ATM cells received on unprovisioned VPI/VCI VCs since the last time the counter was polled.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.73 Register 0x74 (0x1D0): SAR PMON Receive CRC-10 Errors (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RCRC10E [15:0]	X

10.1.74 Register 0x75 (0x1D4): SAR PMON Receive CRC-10 Errors (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 3		Unused	X
Bit 2 to Bit 0	R	RCRC10E [18:16]	X

RCRC10E[18:0]:
RCRC10E[18:0] represents the number of ATM cells with CRC-10 errors since the last time the counter was polled.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.75 Register 0x76 (0x1D8): SAR PMON Receive Non Zero Common Part Indicator Errors

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RNZCPIE[15:0]	X

RNZCPIE[15:0]:
RNZCPIE[15:0] represents the number of non zero CPAAL5_PDU CPI fields that were received since the last time the counter was polled.

The counter is polled by writing to any SAR PMON register or by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.76 Register 0x77 (0x1DC): SAR PMON Receive SDU Length Errors

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RSDULE[15:0]	X

RSDULE[15:0]:
RSDULE[15:0] represents the number of CPAAL5_PDUs with a non zero LENGTH field which did not match the actual received SDU length since the last time the counter was polled.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.77 Register 0x78 (0x1E0): SAR PMON Receive CRC-32 Errors

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RCRC32E [15:0]	X

RCRC32E[15:0]:
RCRC32E[15:0] represents the number of CPAAL5_PDUs with CRC-32 errors received since the last time the counter was polled.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.78 Register 0x79 (0x1E4): SAR PMON Receive Oversize PDU Errors

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ROVPDUE [15:0]	X

ROVPDUE[15:0]:
ROVPDUE[15:0] represents the number of CPAAL5_PDUs that were received with PDU lengths exceeding some defined maximum length since the last time the counter was polled. Please refer to the RALP Max Rx PDU Length register for the maximum allowed length.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.79 Register 0x7B (0x1EC): SAR PMON Receive PDU Abort Errors

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RPDUABE [15:0]	X

RPDUABE[15:0]:
RPDUABE[15:0] represents the number of received CPAAL5_PDUs that were aborted since the last time the counter was polled. A forward abort is accumulated when a CPAAL5_PDU is received with a zero length field.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.80 Register 0x7C (0x1F0): SAR PMON Receive Buffer Errors

Bit	Type	Function	Default
Bit 15 to Bit 8	R	RPBE[7:0]	X
Bit 7 to Bit 0	R	RMBE[7:0]	X

RMBE[7:0]:
RMBE[7:0] represents the number of times the LASAR-155 ran out of Receive Management Descriptors (i.e. management buffers) since the last time the counter was polled. When the LASAR-155 runs out of descriptors, it back pressures to the line.

RPBE[7:0]:
RPBE[7:0] represents the number of times the LASAR-155 ran out of Receive Packet Descriptors (i.e. packet buffers) since the last time the counter was polled. When the LASAR-155 runs out of descriptors, it back pressures to the line.

These counters are polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.81 Register 0x7D (0x1F4): SAR PMON Receive PDU Count

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RPDU[15:0]	X

RPDU[15:0]:
RPDU[15:0] represents the number of CPAAL5_PDUs received since the last time the counter was polled.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.82 Register 0x7E (0x1F8): SAR PMON Transmit Oversize SDU Errors

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TOVSDUE [15:0]	X

TOVSDUE[15:0]:
TOVSDUE[15:0] represents the number of oversized transmit CPAAL5_PDUs that were aborted since the last time the counter was polled. Please refer to the PCID Max Tx SDU Length register for the maximum allowable value.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.83 Mkt : hide register in mkt datasheet

10.1.84 Eng : Register 0x7F (0x1FC): SAR PMON Transmit PDU Count

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TPDU[15:0]	X

TPDU[15:0]:
TPDU[15:0] represents the number of packets transmitted since the last time the counter was polled.

The counter is polled by writing to the LASAR-155 Master Reset / Load Meters register. Such a write transfers the internally accumulated error count to the above register within 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

10.1.85 Register 0x80 (0x200): RALP Control

Bit	Type	Function	Default
Bit 15	R/W	REAS_EN	0
Bit 14	R/W	REAS_DM	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	MRPDU_EN	0
Bit 6	R/W	CRC-10_DIS	1
Bit 5	R/W	PTI_10X_ED	1
Bit 4	R/W	PTI_110_ED	1
Bit 3	R/W	PTI_111_ED	1
Bit 2	R/W	PTI_10X_RD	1
Bit 1	R/W	PTI_110_RD	1
Bit 0	R/W	PTI_111_RD	1

The RALP Control register allow user control over the RALP block.

PTI_111_RD:
The PTI_111_RD bit controls whether to discard cells with Payload Type Indicator (PTI) header fields equal to 111B or to pass the cells to the PCI Host. A PTI field equal to 111B is unassigned and is considered invalid. When PTI_111_RD is set to logic one, cells with PTI fields equal to 111B are dropped. When PTI_111_RD is set to logic zero, the cells are passed to the PCI Host.

PTI_110_RD:
The PTI_110_RD bit controls whether to discard cells with Payload Type Indicator (PTI) header fields equal to 110B or to pass the cells to the PCI Host. A PTI field equal to 110B is currently reserved. When PTI_110_RD is set to logic one, cells with PTI fields equal to 110B are dropped. When PTI_110_RD is set to logic zero, the cells are passed to the PCI Host.

PTI_10X_RD:
The PTI_110X_RD bit controls whether to discard or pass cells to the PCI Host, with Payload Type Indicator (PTI) header fields equal to 100B or 101B. A PTI field equal to 100B or 101B identifies a segment F5 OAM cells or an end-to-end F5 OAM cells. When PTI_10X_RD is set to logic one, F5 OAM ATM cells are dropped. When PTI_10X_RD is set to logic zero, the cells are passed to the PCI Host.

PTI_111_ED:
The PTI_111_ED bit controls whether to discard cells with Payload Type Indicator (PTI) header fields equal to 111B or to copy the cells to the Multipurpose Port. A PTI field equal to 111B is unassigned and is considered invalid. When PTI_111_ED is set to logic one, cells with PTI fields equal to 111B are dropped. When PTI_111_ED is set to logic zero, the cells are copied to the Multipurpose Port.

PTI_110_ED:
The PTI_110_ED bit controls whether to discard cells with Payload Type Indicator (PTI) header fields equal to 110B or to copy the cells to the Multipurpose Port. A PTI field equal to 110B is currently reserved. When PTI_110_ED is set to logic one, cells with PTI fields equal to 110B are dropped. When PTI_110_ED is set to logic zero, the cells are copied to the Multipurpose Port.

PTI_10X_ED:
The PTI_10X_ED bit controls whether to discard or pass cells to the Multipurpose Port, with Payload Type Indicator (PTI) header fields equal to 100B or 101B. A PTI field equal to 100B or 101B identifies a segment F5 OAM cells or an end-to-end F5 OAM cell. When PTI_10X_ED is set to logic one, F5 OAM ATM

cells are dropped. When PTI_10X_ED is set to logic zero, the cells are copied to the Multipurpose Port.

CRC-10_DIS:
The CRC-10_DIS bit controls whether to discard or pass ATM cells with CRC-10 error. When CRC-10_DIS is set to logic one, ATM cells with CRC-10 errors are dropped. When CRC-10_DIS is set to logic zero, the cells are passed.

MRPDU_EN:
The MRPDU_EN bit controls whether to enforce the user programmed maximum receive CPAAL5_PDU length. If MRPDU_EN is set to logic one, the maximum length of the CPAAL5_PDU is user programmable using the RALP Max Rx PDU Length register. CPAAL5_PDUs that exceed this length are prematurely terminated. All successive bytes from this CPAAL5_PDU are dropped until the start of the next CPAAL5_PDU.

If MRPDU_EN is set to logic zero, the RALP block will not enforce a maximum PDU length.

REAS_DM:
The REAS_DM bit selects the reassembly disable mode. Two modes to disable the RALP block from reassembling CPAAL5_PDUs are provided. When REAS_DM is set to logic one and the REAS_EN bit is used to disable reassembling, the RALP block will immediately stop reassembly on all VCs.

When REAS_DM is set to logic zero and the REAS_EN bit is used to disable reassembling, the RALP block will not start any new reassembles but will continue to complete the current CPAAL5_PDUs under reassembly. In this manner, graceful system shutdown can be accomplished. An interrupt is generated when all of the VCs complete their packet reassemblies.

Note, regardless of the state REAS_DM is set to, management cells (PTI = 100, 101, 110, 111) are immediately filtered when reassembly is disabled (i.e. REAS_EN = 0).

REAS_EN:
The REAS_EN bit is used to enable and disable the RALP from processing cells and reassembling packets. When REAS_EN is set to logic one, the RALP is allowed to start processing. Packet reassembling does not proceed on a VC until the VC is provisioned as indicated in the receive VC parameter data structures accessed through the COPS registers. Once provisioned, the RALP block looks for the start of a new CPAAL5_PDU before starting reassembly.

When REAS_EN is set to logic zero, the RALP block terminates all reassemblies. Termination can be either immediate or graceful as controlled using the REAS_DM bit.

10.1.86 Register 0x81 (0x204): RALP Interrupt Status

Bit	Type	Function	Default
Bit 15	R	UVPI/VCII	X
Bit 14	R	CRC10I	X
Bit 13	R	NZCPII	X
Bit 12	R	SDULI	X
Bit 11	R	CRC32I	X
Bit 10	R	OVPDUI	X
Bit 9	R	Reserved	X
Bit 8	R	F5OAMDI	X
Bit 7	R	PTIDI	X
Bit 6	R	RSOCI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RESEM_ACTI	X
Bit 2	R	CEXOVI	X
Bit 1	R	PDUABI	X
Bit 0	R	RESEM_ACTV	X

The RALP Interrupt Status register indicates the status of the RALP block and the error conditions identified by the RALP block. Interrupt bits are cleared when this register is read.

RESEM_ACTV:
The RESEM_ACTV bit indicates whether there are any active reassembles. When RESEM_ACTV is logic one, the RALP is current reassembling one or more CPAAL5_PDUs. When RESEM_ACTV is logic zero, no reassembles are active.

PDUABI:
The PDUABI interrupt bit indicates when the RALP received a CPAAL5_PDU with an forward abort indication (length field = 0).

CEXOVI:
The CEXOVI interrupt bit indicates when the RALP had to abort a transfer on the Multipurpose Port due to an overflow. An overflow occurs during a cell transfer when the RALP samples RFIFOFB low. CEXOVI is set high when an overflow condition is detected.

RESEM_ACTI:
The RESEM_ACTI interrupt bit indicates when the RALP transitions into and out of a state where it is reassembling packets. When RESEM_ACTI is high, a transition has been made. The RESEM_ACTV bit indicates which state the RALP is actually in.

RSOCI:
The RSOCI interrupt bit should only be used when operating with an external PHY Layer device such as the PMC SUNI-PDH. When RSOCI is high, the received receive start of cell (RSOC) indication on input RSOC was detected in an unexpected location. In such an event, the RALP block starts accumulating a new cell and discards any residue bytes from the previous incomplete cell.

PTIDI:
The PTIDI interrupt bit indicates the reception of a cell with a PTI field equal to 110B or 111B. When PTIDI is high, the RALP has received one or more cells with a PTI field equal to 110B or 111B.

F5OAMDI:
The F5OAMDI interrupt bit indicates the reception of a F5 OAM cell. When F5OAMDI is high, the RALP block has received one or more F5 OAM cells.

OVPDUI:
The OVPDUI interrupt bit indicates that the RALP block has detected a CPAAL5_PDU length violation. If OVPDUI is high, the RALP block has

terminated one or more reassemblies due to a maximum receive PDU length violation. The maximum length can be set by the user using the RALP Max Rx PDU Length register or can be the default of 65,535 bytes.

Note, the OVPDUI interrupt will only be generated if the CPAAL5_PDU length exceeds the value in the RALP Max Rx PDU Length register by 40 bytes.

CRC32I:
The CRC32I interrupt bit indicates that the RALP block has detected a CPAAL5_PDU CRC-32 error. If CRC32I is high, the RALP block has detected one or more CRC-32 errors.

SDULI:
The SDULI interrupt bit indicates that the RALP has detected a CPAAL5_PDU received length mismatch error. When SDULI is high, one or more received CPAAL5_SDUs have different lengths then indicated in the corresponding CPAAL5_PDU LENGTH field. LENGTH fields of zero which indicate forward abort errors do not result in a SDULI interrupt.

NZCPII:
The NZCPII interrupt bit indicates the reception of a non zero CPAAL5_PDU Common Part Indicator (CPI) field. When NZCPII is high, the RALP block has received one or more CPAAL5_PDUs with non zero CPI fields.

CRC10I:
The CRC10I interrupt bit indicates that the RALP block has detected an ATM cell CRC-10 error. If CRC10I is high, the RALP block has detected one or more CRC-10 errors. Errored cells can be either passed or dropped using the CRC-10_DIS bit in the RALP Control register.

CRC-10 is verified only for VCs configured to receive management data (QUEUE_SEL=00B) or for VCs configured to expect packet data (QUEUE_SEL=11B). When configured for packet data, only cells with PTI = 100B (segment F5 OAM), 101B (end to end F5 OAM) and 110B (Resource Management) are checked for correct CRC-10.

UVPI/VCII:
The UVPI/VCII interrupt bit indicates whether the RALP block received a unprovisioned cell whose VPI and VCI fields which could not be associated with an open VC. If UVPI/VCII is high, one or more unprovisioned cells were received.

10.1.87 Register 0x82 (0x208): RALP Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	UVPI/VCIE	0
Bit 14	R/W	CRC10E	0
Bit 13	R/W	NZCPIE	0
Bit 12	R/W	SDULE	0
Bit 11	R/W	CRC32E	0
Bit 10	R/W	OVPDUE	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	F5OAMDE	0
Bit 7	R/W	PTIDE	0
Bit 6	R/W	RSOCE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RESEM_ACTE	0
Bit 2	R/W	CEXOVE	0
Bit 1	R/W	PDUABE	0
Bit 0		Unused	X

The RALP Interrupt Enable register is used to control the generation of interrupt from the RALP block.

UVPI/VCIE, CRC10E, NZCPIE, SDULE, CRC32E, OVPDUE, F5OAMDE, PTIDE, RSOCE, RESEM_ACTE, CEXOVE, PDUABE:
The listed enable bits control interrupt generation by the corresponding interrupt bits in the RALP Interrupt Status register. When the enable bit is set to logic one, the corresponding interrupt will generate either a microprocessor interrupt or a PCI Host interrupt as determined by the MPENB input.

10.1.88 Register 0x83 (0x20C): RALP Max Rx PDU Length

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	MRPDU[15:0]	FFFFH

MRPDU[15:0]:
MRPDU[15:0] represents the user programmable maximum length of the receive CPAAL5 Protocol Data Unit (PDU). Whether this maximum value is enforced depends on the MRPDU_EN bit in the RALP Control register.

Note, MRPDU[15:0] must be an integer multiple of 48 or 0xFFFF. In addition if the current CPAAL5_PDU exceeds MRPDU[15:0] by 48 bytes, all following bytes for the current CPAAL5_PDU will be dropped.

10.1.89 Register 0x88 (0x220): TALP Control

Bit	Type	Function	Default
Bit 15	R/W	CIN_ERRE	0
Bit 14	R/W	TAS_ERRE	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	CIN_CL_EN	0
Bit 5	R/W	CIN_F5_EN	0
Bit 4	R/W	CIN_F4_EN	0
Bit 3	R/W	CIN_PR_EN	0
Bit 2	R/W	AGG_PR_EN	0
Bit 1	R/W	CINPORT_EN	0
Bit 0	R/W	CINPORT_PR	0

The TALP Control register is used to configure the TALP block.

CINPORT_PR:
The CINPORT_PR bit selects the priority of the multipurpose port. When CINPORT_PR is set to logic one and CINPORT_EN is set to logic one, cells sourced by the multipurpose port take priority over cells (segmented packets) sourced from the PCI Host. When CINPORT_PR is set to logic zero and CINPORT_EN is set to logic one, cells sourced from the PCI Host take priority over cells scheduled by the multipurpose port. When CINPORT_EN is set to logic zero, CINPORT_PR is ignored.

CINPORT_EN:
The CINPORT_EN bit enables the multipurpose port. When CINPORT_EN is set to logic one, the TALP block allows cells to be sourced from the multipurpose port. When CINPORT_EN is set to logic zero, cells can only be sourced from the PCI Host.

It should be noted that the state of the CINPORT_EN bit should be set when the LASAR-155 is initially configured after reset. Enabling or disabling the multipurpose port while it is processing cells can cause erroneous behavior.

AGG_PR_EN:
The AGG_PR_EN bit enables control of cell transmission rate of the aggregate traffic sourced from the PCI Host. When AGG_PR_EN is set to logic one, aggregate rate enforcement is enabled. When AGG_PR_EN is logic zero, aggregate rate enforcement is not enforced. Actual rates can be programmed using the TALP Aggregate Peak Cell Rate and TALP Aggregate Bucket Capacity registers.

When the TALP Aggregate Peak Cell Rate and TALP Aggregate Bucket Capacity registers are being modified, the AGG_PR_EN bit should be set to zero to disable rate enforcement.

CIN_PR_EN:
The CIN_PR_EN bit enables control of cell transmission rate of the traffic sourced from the multipurpose port. When CIN_PR_EN is set to logic one, rate enforcement is enabled. When CIN_PR_EN is logic zero, rate enforcement is not enforced. Actual rates can be programmed using the TALP Multipurpose Port Peak Cell Rate and TALP Multipurpose Port Bucket Capacity registers.

When the TALP Multipurpose Port Peak Cell Rate and TALP Multipurpose Port Bucket Capacity registers are being modified, the CIN_PR_EN bit should be set to zero to disable rate enforcement.

CIN_F4_EN:
The CIN_F4_EN bit enables the TALP to calculate the CRC-10 on the F4 OAM cells sourced from the Multipurpose Port. When CIN_F4_EN is set to one, the TALP calculates and inserts the CRC-10 field for all F4 OAM cells sourced from the Multipurpose Port. When CIN_F4_EN is set to zero, the TALP does not calculate and insert the CRC-10 field into the F4 OAM cells.

CIN_F5_EN:
The CIN_F5_EN bit enables the TALP to calculate the CRC-10 on the F5 OAM cells sourced from the Multipurpose Port. When CIN_F5_EN is set to one, the TALP calculates and inserts the CRC-10 field for all F5 OAM cells sourced from the Multipurpose Port. When CIN_F5_EN is set to zero, the TALP does not calculate and insert the CRC-10 field into the F5 OAM cells.

CIN_CL_EN:
The CIN_CL_EN bit enables the TALP to calculate the CRC-10 on all cells sourced from the Multipurpose Port. When CIN_CL_EN is set to one, the TALP calculates and inserts the CRC-10 field for all cells sourced from the Multipurpose Port. When CIN_CL_EN is set to zero, the TALP does not calculate and insert the CRC-10 field into the cells.

TAS_ERRE:
The TAS_ERRE bit enables the TALP to generate an interrupt when an abort condition is detected on the data transfers from the PCID. When the TAS_ERRE bit is set to one, the TALP will generate an interrupt via the TALP Interrupt Status register when an abort condition is detected by the TALP on the data transfer from the PCID. When the TAS_ERRE bit is set to zero, the TALP does not generate an interrupt when the abort condition is detected.

CIN_ERRE:
The CIN_ERRE bit enables the TALP to generate an interrupt when an abort condition is detected on the Multipurpose Port. When the CIN_ERRE bit is set to one, the TALP will generate an interrupt via the TALP Interrupt Status register when an abort condition is detected by the Multipurpose Port. When the CIN_ERRE bit is set to zero, the TALP does not generate an interrupt when the abort condition is detected. An abort condition is detected if the TSOC input is sampled high in an unexpected location.

10.1.90 Register 0x89 (0x224): TALP Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CIN_ERRI	X
Bit 0	R	TAS_ERRI	X

The TALP Interrupt Status register indicates the status of the TALP and the error conditions identified by the TALP. Interrupt bits are cleared when this register is read.

TAS_ERRI:
The TAS_ERRI bit is set when an abort condition is detected by the TALP on data transfers from the PCID. An abort condition is indicated by the start of cell indication being sampled in an incorrect location.

CIN_ERRI:
The CIN_ERRI bit is set when an abort condition is detected by the Multipurpose Port. An abort condition is indicated by the start of cell indication (TSOC = 1) being sampled in an incorrect location.

10.1.91 Register 0x8A (0x228): TALP Diagnostic

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DCRC-32	0
Bit 1	R/W	DCPI	0
Bit 0	R/W	DCRC-10	0

The TALP Diagnostic register is used to generate a variety of error conditions for diagnostics.

DCRC-10:
The DCRC-10 bit is used to invert the calculated ATM cell CRC-10 field for diagnostic purposes. While DCRC-10 is set to logic one, the generated CRC-10 is inverted before being transmitted.

DCPI:
The DCPI bit is used to invert the CPAAL5_PDU CPI field for diagnostic purposes. While DCPI is set to logic one, the CPI field sourced from the PCID block is inverted before being transmitted.

DCRC-32:
The DCRC-32 bit is used to invert the calculated CPAAL5_PDU CRC-32 field for diagnostic purposes. While DCRC-32 is set to logic one, the generated CRC-32 is inverted before being transmitted.

10.1.92 Register 0x8B: (0x22C) TALP Aggregate Peak Cell Rate

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	APR_PS[2]	0
Bit 9	R/W	APR_PS[1]	0
Bit 8	R/W	APR_PS[0]	0
Bit 7	R/W	APR_CNT[7]	0
Bit 6	R/W	APR_CNT[6]	0
Bit 5	R/W	APR_CNT[5]	0
Bit 4	R/W	APR_CNT[4]	0
Bit 3	R/W	APR_CNT[3]	0
Bit 2	R/W	APR_CNT[2]	0
Bit 1	R/W	APR_CNT[1]	0
Bit 0	R/W	APR_CNT[0]	0

Note, when the TALP Aggregate Peak Cell Rate register is being modified, the AGG_PR_EN bit located in the TALP Control register, should be set to zero.

APR_CNT[7:0]:
APR_CNT[7:0] specifies the aggregate peak cell rate. APR_CNT[7:0] is the roll over value of the aggregate peak cell rate counter which is clocked using a prescaled version of SYSCLK. Prescaling is controlled using the APR_PS[2:0] field. Below is an example for transmission at the peak cell rates of 64 Kbps and 10 Mbit/s given a 33 MHz SYSCLK. Please refer to the TATS register descriptions for different peak cell rates and SYSCLK frequencies.

SYSCLK F = 33 MHz					
Prescale (APR_PS)	4	16	64	256	1024
Peak Clock Period PCP= 1/F * APR_PS ns	121.21	484.85	1939.39	7757.58	31030.3
Peak Cell Rate (PCR)	APR_CNT = [(1/PCR) * 53 * 8 * (1/PCP)] - 1				
64000 bps	INVALID	INVALID	INVALID	INVALID	214
10000000 bps	INVALID	86	21	4	0

APR_PS[2:0]:
APR_PS[2:0] specifies the prescale to be applied to the SYSCLK before it is used to clock the aggregate peak cell rate counter. The prescale values are outlined below.

APR_PS[2:0]	Prescale
000	none
001	4
010	16
011	64
100	256
101	1024
11x	Reserved

10.1.93 Register 0x8C (0x230): TALP Aggregate Bucket Capacity

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	ASR_CNT[2]	0
Bit 9	R/W	ASR_CNT[1]	0
Bit 8	R/W	ASR_CNT[0]	0
Bit 7	R/W	AB_CAP[7]	0
Bit 6	R/W	AB_CAP[6]	0
Bit 5	R/W	AB_CAP[5]	0
Bit 4	R/W	AB_CAP[4]	0
Bit 3	R/W	AB_CAP[3]	0
Bit 2	R/W	AB_CAP[2]	0
Bit 1	R/W	AB_CAP[1]	0
Bit 0	R/W	AB_CAP[0]	0

Note, when the TALP Aggregate Bucket Capacity register is being modified, the AGG_PR_EN bit located in the TALP Control register, should be set to zero.

AB_CAP[7:0]:
The AB_CAP[7:0] bits define the size of the aggregate token bucket. Tokens are added to the bucket at the sustainable cell rate as determined by the ASR_CNT[2:0] field. Tokens are consumed at the peak cell rate as determined by the TALP Aggregate Peak cell rate register. As controlled by the AGG_PR_EN bit in the TALP Control register, cell transmission is only allowed when the aggregate token bucket is not empty. If the bucket is empty, transmission proceeds at the bucket fill rate (i.e. sustainable cell rate).

ASR_CNT[2:0]:
The ASR_CNT[2:0] bits are used to select the sustainable cell rate based on a derivative of the peak cell rate. ASR_CNT[2:0] is the roll over value of the aggregate sustainable rate counter which is clocked using the aggregate peak cell rate counter. For example, given an aggregate peak cell rate of 10 Mbit/s, to obtain a sustainable cell rate of 2 Mbit/s, the ASR_CNT[2:0] field should be set to four 100B.

10.1.94 Register 0x8D (0x234): TALP Multipurpose Port Peak Cell Rate

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	CIN_PS[2]	0
Bit 9	R/W	CIN_PS[1]	0
Bit 8	R/W	CIN_PS[0]	0
Bit 7	R/W	CINPR_CNT[7]	0
Bit 6	R/W	CINPR_CNT[6]	0
Bit 5	R/W	CINPR_CNT[5]	0
Bit 4	R/W	CINPR_CNT[4]	0
Bit 3	R/W	CINPR_CNT[3]	0
Bit 2	R/W	CINPR_CNT[2]	0
Bit 1	R/W	CINPR_CNT[1]	0
Bit 0	R/W	CINPR_CNT[0]	0

Note, when the TALP Multipurpose Port Peak Cell Rate register is being modified, the CIN_PR_EN bit located in the TALP Control register, should be set to zero.

CINPR_CNT[7:0]:
CINPR_CNT[7:0] specifies the Multipurpose Port peak cell rate. CINPR_CNT[7:0] is the roll over value of the Multipurpose Port peak cell rate counter which is clocked using a prescaled version of SYSCLK. Prescaling is controlled using the CIN_PS[2:0] field. Below is an example for transmission at the peak cell rates of 64 Kbps and 10 Mbit/s given a 33 MHz SYSCLK.

SYSCLK F = 33 MHz					
Prescale (CIN_PS)	4	16	64	256	1024
Peak Clock Period PCP= 1/F * CIN_PS ns	121.21	484.85	1939.39	7757.58	31030.3
Peak Cell Rate (PCR)	CINPR_CNT = [(1/PCR) * 53 * 8 * (1/PCP)] - 1				
64000 bps	INVALID	INVALID	INVALID	INVALID	214
10000000 bps	INVALID	86	21	4	0

CIN_PS[2:0]:
CIN_PS[2:0] specifies the prescale to be applied to the SYSCLK before it is used to clock the multipurpose port peak cell rate counter. The prescale values are outlined below.

CIN_PS[2:0]	Prescale
000	none
001	4
010	16
011	64
100	256
101	1024
11x	Reserved

10.1.95 Register 0x8E (0x238): TALP Multipurpose Port Bucket Capacity

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	CINSR_CNT[2]	0
Bit 9	R/W	CINSR_CNT[1]	0
Bit 8	R/W	CINSR_CNT[0]	0
Bit 7	R/W	CINB_CAP[7]	0
Bit 6	R/W	CINB_CAP[6]	0
Bit 5	R/W	CINB_CAP[5]	0
Bit 4	R/W	CINB_CAP[4]	0
Bit 3	R/W	CINB_CAP[3]	0
Bit 2	R/W	CINB_CAP[2]	0
Bit 1	R/W	CINB_CAP[1]	0
Bit 0	R/W	CINB_CAP[0]	0

Note, when the TALP Multipurpose Port Bucket Capacity register is being modified, the CIN_PR_EN bit located in the TALP Control register, should be set to zero.

CINB_CAP[7:0]:
The CINB_CAP[7:0] bits define the size of the multipurpose port token bucket. Tokens are added to the bucket at the sustainable cell rate as determined by the CINSR_CNT[2:0] field. Tokens are consumed at the peak cell rate as determined by the TALP Multipurpose Port Peak Cell Rate register. As controlled by the CIN_PR_EN bit in the TALP Control register, cell transmission is only allowed when the multipurpose port token bucket contains tokens. If the bucket is empty, transmission proceeds at the bucket fill rate (i.e. sustainable cell rate).

CINSR_CNT[2:0]:
The CINSR_CNT[2:0] bits are used to select the sustainable cell rate based on a derivative of the peak cell rate. CINSR_CNT[2:0] is the roll over value of the multipurpose port sustainable rate counter which is clocked using the multipurpose port peak cell rate counter. For example, given a multipurpose port peak cell rate of 10 Mbit/s, to obtain a multipurpose port cell rate of 5 Mbit/s, the CINSR_CNT[2:0] field should be set to 001B.

10.1.96 Register 0x90 (0x240): TATS Control/Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	QSTARV_EN	0
Bit 14	R/W	AGR_CBRC_EN	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	CBS_CNT[7]	1
Bit 6	R/W	CBS_CNT[6]	1
Bit 5	R/W	CBS_CNT[5]	1
Bit 4	R/W	CBS_CNT[4]	1
Bit 3	R/W	CBS_CNT[3]	1
Bit 2	R/W	CBS_CNT[2]	1
Bit 1	R/W	CBS_CNT[1]	1
Bit 0	R/W	CBS_CNT[0]	1

The TATS Control/Interrupt Enable register is used to configure and control the TATS block.

CBS_CNT[7:0]:
The CBS_CNT[7:0] bits indicate the Credit Basket Size for Credit Based Rate Control (CBRC) enforcement. VBR VCs are subject to peak cell rate and sustainable cell rate shaping as dictated by the TATS Service Rate Queues. In addition VBR VCs can also be constrained by an internal credit basket whose size is specified using the CBS_CNT value.

Cell credits are expected to be generated by the downstream ATM entity and relayed to the LASAR-155 device using the GFC header field in receive ATM cells. Based on the reception of the appropriate GFC codepoint, the CBRC credit basket is topped off. Each cell transmitted on a VC with CBRC consumes a single credit regardless of the VC. Cells associated with CBRC VCs are only allowed to be sent if there is an available credit in the aggregate CBRC credit basket. If a credit is not available, transmission on CBRC VCs is quenched.

AGR_CBRC_EN:
The AGR_CBRC_EN bit enables aggregate CBRC VC traffic enforcement using the CBRC credit basket. When AGR_CBRC_EN is logic one, aggregate CBRC

VC traffic enforcement using the credit basket scheme is enforced with the basket size specified using the CBS_CNT field. When AGR_CBRC_EN is logic zero, CBRC enforcement is not performed.

QSTARV_EN:
The QSTRAV_EN bit enables the block level Service Rate Queue Starvation interrupts, SRQ[8:1]_STARVI as listed in the TATS Interrupt Status register. When the enable bit is set to logic one, the corresponding interrupt will generate either a microprocessor interrupt or a PCI Host interrupt as determined by the MPENB input.

10.1.97 Register 0x91 (0x244): TATS Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SRQ8_STARVI	X
Bit 6	R	SRQ7_STARVI	X
Bit 5	R	SRQ6_STARVI	X
Bit 4	R	SRQ5_STARVI	X
Bit 3	R	SRQ4_STARVI	X
Bit 2	R	SRQ3_STARVI	X
Bit 1	R	SRQ2_STARVI	X
Bit 0	R	SRQ1_STARVI	X

The TATS Interrupt Status register indicates the error conditions identified by the TATS block. Interrupt bits are cleared when this register is read.

SRQ[8:1]_STARVI:
The eight SRQ[8:1]_STARVI interrupt bits indicate if the corresponding Service Rate Queue has experienced a starvation condition. When one of the SRQ[8:1]_STARVI bits is high, the associated queue has experienced a starvation condition. The LASAR-155 performs no special action when a queue has starved.

Starvation conditions can occur as a result of over subscription. If a SRQ cannot be serviced and its rate counter expires, the SRQ is deemed to have starved. Starvation can be caused by any SRQ blocking out any other SRQ from service or by a SRQ taking too long to service its VCs and having its rate counter expire.

10.1.98 Register 0x92 (0x248): TATS Service Rate Queue Enables

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	SRQ8_EN	0
Bit 6	R/W	SRQ7_EN	0
Bit 5	R/W	SRQ6_EN	0
Bit 4	R/W	SRQ5_EN	0
Bit 3	R/W	SRQ4_EN	0
Bit 2	R/W	SRQ3_EN	0
Bit 1	R/W	SRQ2_EN	0
Bit 0	R/W	SRQ1_EN	0

SRQ[8:1]_EN:
The SRQ[8:1]_EN bits enable transmission on the corresponding Service Request Queues. When SRQ[N]_EN is set to logic one, transmission on all VCs associated with the Service Rate Queue are allowed to transmit at the peak cell rate as specified by the corresponding TATS Service Rate Queue Parameters register. When SRQ[N]_EN is set to logic zero, transmission on all VCs associated with the corresponding Service Rate Queue is squelched.

Reserved:
The reserved bits must be programmed to logic zero for proper operation.

10.1.99 Register 0x93-0x96 (0x24C-0x258): TATS Service Rate Queue 1, 2, 3, 4 Parameters

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	SRQn_PS[2]	0
Bit 9	R/W	SRQn_PS[1]	0
Bit 8	R/W	SRQn_PS[0]	0
Bit 7	R/W	SRQn_CNT[7]	0
Bit 6	R/W	SRQn_CNT[6]	0
Bit 5	R/W	SRQn_CNT[5]	0
Bit 4	R/W	SRQn_CNT[4]	0
Bit 3	R/W	SRQn_CNT[3]	0
Bit 2	R/W	SRQn_CNT[2]	0
Bit 1	R/W	SRQn_CNT[1]	0
Bit 0	R/W	SRQn_CNT[0]	0

For the above register bits, n = 1, 2, 3 or 4.

The four TATS Service Rate Queue Parameter registers are used to set the peak cell rates for the four low priority queues. Note, low priority queues are serviced in a round-robin fashion only if there are no outstanding requests for service from high priority queues. Servicing of low priority queues can be preempted by high priority queues.

When modifying the SRQn_CNT[7:0] value or the SRQn_PS[2:0] value the corresponding SRQ counter should be disabled using the appropriate SRQ[N]_EN bit in the TATS Service Rate Queue Enables register.

SRQn_CNT[7:0]:
The SRQn_CNT[7:0] bits specify the peak cell rates supported by Service Rate Queues (SRQ) 1, 2, 3 and 4. For example, SRQ1_CNT[7:0] is the roll over value of the SRQ 1 counter. The counter is clocked using a prescaled version of SYSCLK as determined using the corresponding SRQn_PS[2:0] field. Every time the counter rolls over, one cell is allowed to be transmitted on each VC associated with the SRQ. Whether a cell is in fact transmitted is determined by per VC traffic parameters. A SRQn_CNT[7:0] value of 0 will disable the corresponding SRQ.

Below are examples of SRQn_CNT values to support various peak cell rate transmissions using various SYSCLK frequencies.

SYSCLK F = 25 MHz					
Prescale (SRQ_PS)	4	16	64	256	1024
Peak Clock Period PCP= 1/F * SRQ_PS ns	160	640	2560	10240	40960
Peak Cell Rate (PCR) bps	SRQ_CNT=(1/PCR) * 424 * (1/PCP)-1				
32000	INVALID	INVALID	INVALID	INVALID	INVALID
64000	INVALID	INVALID	INVALID	INVALID	161
128000	INVALID	INVALID	INVALID	INVALID	80
256000	INVALID	INVALID	INVALID	161	39
512000	INVALID	INVALID	INVALID	80	19
1000000	INVALID	INVALID	165	40	9
1544000	INVALID	INVALID	106	26	6
2048000	INVALID	INVALID	80	19	4
5000000	INVALID	132	32	7	INVALID
10000000	INVALID	65	16	INVALID	INVALID
16000000	165	40	15	INVALID	INVALID
25000000	105	26	6	INVALID	INVALID
45000000	58	14	INVALID	INVALID	INVALID
50000000	52	12	INVALID	INVALID	INVALID
100000000	26	6	INVALID	INVALID	INVALID
155000000	16	INVALID	INVALID	INVALID	INVALID

SYSCLK F = 33 MHz					
Prescale (SRQ_PS)	4	16	64	256	1024
Peak Clock Period PCP= 1/F * SRQ_PS ns	121.21	484.85	1939.39	7757.58	31030.3
Peak Cell Rate (PCR) bps	SRQ_CNT=(1/PCR) * 424 * (1/PCP)-1				
32000	INVALID	INVALID	INVALID	INVALID	INVALID
64000	INVALID	INVALID	INVALID	INVALID	213
128000	INVALID	INVALID	INVALID	INVALID	106
256000	INVALID	INVALID	INVALID	213	52
512000	INVALID	INVALID	INVALID	106	26
1000000	INVALID	INVALID	218	54	13
1544000	INVALID	INVALID	141	34	8
2048000	INVALID	INVALID	106	26	6
5000000	INVALID	174	43	10	INVALID
10000000	INVALID	86	21	4	INVALID
16000000	218	54	13	INVALID	INVALID
25000000	139	34	8	INVALID	INVALID
45000000	77	18	4	INVALID	INVALID
50000000	69	16	INVALID	INVALID	INVALID
100000000	34	8	INVALID	INVALID	INVALID
155000000	22	5	INVALID	INVALID	INVALID

SRQn_PS[2:0]:

The SRQn_PS[2:0] bits specify the prescales to be applied to the SYSCLK clock before it is applied to the individual SRQ 1, 2, 3, and 4 counters. For example, SRQ1_PS[2:0] defines the prescale applied to the SYSCLK clock before it is used to clock the SRQ 1 counter. The prescales are defined below.

SRQ_PS[2:0]	Prescale
000	none
001	4
010	16
011	64
100	256
101	1024
11x	Reserved

10.1.100 Register 0x97-0x9A (0x25C-268): TATS Service Rate Queue 5, 6, 7, 8 Parameters

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	SRQn_PS[2]	0
Bit 9	R/W	SRQn_PS[1]	0
Bit 8	R/W	SRQn_PS[0]	0
Bit 7	R/W	SRQn_CNT[7]	0
Bit 6	R/W	SRQn_CNT[6]	0
Bit 5	R/W	SRQn_CNT[5]	0
Bit 4	R/W	SRQn_CNT[4]	0
Bit 3	R/W	SRQn_CNT[3]	0
Bit 2	R/W	SRQn_CNT[2]	0
Bit 1	R/W	SRQn_CNT[1]	0
Bit 0	R/W	SRQn_CNT[0]	0

For the above register bits, n = 5, 6, 7 or 8.

The four TATS Service Rate Queue Parameter registers are used to set the peak cell rates for the four high priority queues. Note, high priority queues are serviced in a round-robin fashion. Once the TATS block starts servicing a high priority queue, it completes servicing the queue before it considers servicing other queues.

When modifying the SRQn_CNT[7:0] value or the SRQn_PS[2:0] value the corresponding SRQ counter should be disabled using the appropriate SRQn_EN bit in the TATS Service Rate Queue Enables register.

SRQn_CNT[7:0]:
The SRQn_CNT[7:0] bits specify the peak cell rates supported by Service Rate Queues (SRQ) 5, 6, 7 and 8. For example, SRQ4_CNT[7:0] is the roll over value of the SRQ 4 counter. The counter is clocked using a prescaled version of SYSCLK as determined using the corresponding SRQn_PS[2:0] field. Every time the counter rolls over, one cell is allowed to be transmitted on each VC associated with the SRQ.

Please refer to the TATS Service Rate Queue 1, 2, 3, 4 Parameter register descriptions for examples of SRQn_CNT values to support various peak cell rate transmissions using various SYSCLK frequencies.

SRQn_PS[2:0]:
The SRQn_PS[2:0] bits specify the prescales to be applied to the SYSCLK clock before it is applied to the individual SRQ 5, 6, 7, and 8 counters. For example, SRQ5_PS[2:0] defines the prescale applied to the SYSCLK clock before it is used to clock the SRQ 5 counter. The prescales are defined below.

SRQ_PS[2:0]	Prescale
000	none
001	4
010	16
011	64
100	256
101	1024
11x	Reserved

10.1.101 Register 0xA0 (0x280): COPS Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	NVPI[3]	0
Bit 6	R/W	NVPI[2]	0
Bit 5	R/W	NVPI[1]	0
Bit 4	R/W	NVPI[0]	0
Bit 3	R/W	NVCI[3]	0
Bit 2	R/W	NVCI[2]	0
Bit 1	R/W	NVCI[1]	0
Bit 0	R/W	NVCI[0]	0

The COPS Control register can be used to configure the COPS. This register must be configured before the initialization procedure is activated using the INIT bit in the LASAR-155 Master Control register.

NVCI[3:0]:
The NVCI[3:0] bits define the number of VCI bits that are used to identify a VC. The combination of the NVCI[3:0] bits and the NVPI[3:0] bits should select the 7 bits required to identify the 128 supported VCs.

NVCI[3:0]	Descriptor
0000	Reserved
0001	Reserved
0010	Reserved
0011	Reserved
0100	Reserved
0101	5 VCI bits
0110	6 VCI bits
0111	7 VCI bits
1xxx	Reserved

NVPI[3:0]:
The NVPI[3:0] bits define the number of VPI bits that are used to identify a VC. The combination of the NVCI[3:0] bits and the NVPI[3:0] bits should select the 7 bits required to identify the 128 supported VCs.

NVPI[3:0]	Descriptor
0000	0 VPI bits
0001	1 VPI bits
0010	2 VPI bits
0011	Reserved
01xx	Reserved
1xxx	Reserved

10.1.102 Register 0xA1 (0x284): COPS Parameter Access Control

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RD/WRB	0
Bit 0	R/W	RX/TXB	0

The COPS Parameter Access Control register can be used to configure receive and transmit VC parameters. A write to this register cause either a write or read to the internal transmit or receive VC parameter tables as controlled by the RD/WRB and RX/TXB bits respectively. The values read from and written to the VC parameter tables can be found in the COPS VPI, COPS VCI, COPS VC Control and Status and COPS VC Parameters registers. A read of this register just returns the current register value.

To write to the VC parameter tables, the COPS VC Number, COPS VPI, COPS VCI, COPS VC Control and Status and COPS VC Parameters registers should be set first. Next this register should be written to initialize the VC parameter table write. The write is complete when the BUSY bit goes to logic zero.

To read from a VC parameter table, the COPS VC Number register should be set first. Next, this register should be written and the BUSY bit monitored. When BUSY transitions to logic zero, the VC parameter table values can be read from the COPS VPI, COPS VCI, COPS VC Control and Status and COPS VC Parameters registers.

RX/TXB:
The RX/TXB bit selects either to access the receive or transmit VC parameter table when a write is performed on this register. When RX/TXB is set to logic

one, the receive VC parameter table is accessed. When RX/TXB is set to logic zero, the transmit VC parameter table is accessed.

RD/WRB:
The RD/WRB bit selects whether to initiate a read from or a write to a VC parameter table when a write is performed on this register. When RD/WRB is set to logic one, a read is performed. When RD/WRB is set to logic zero, a write is performed. The selection of which VC parameter table to access is control by the RX/TXB bit.

BUSY:
The BUSY bit indicates when a VC parameter table access is in progress. When busy is logic one, a VC parameter table read or write is in progress. When BUSY is logic zero, the previous access has completed.

For a Receive VC provisioning request the BUSY bit will return to zero after the COPS initializes the Receive VC Parameter Data structure. For a Receive VC unprovisioning request the BUSY bit will return to zero after the COPS updates the Receive VC Parameter Data structure.

For a Transmit VC provisioning or unprovisioning request the BUSY bit will return to zero after the COPS has received an acknowledge from the transmit DMA controller in the PCID block. Unprovisioning can be held off until the entire transmit pipeline is flush of cells from the unprovisioned VC. It should be noted that the PCI block will not generate an acknowledge and thus BUSY bit will not return to zero, unless the TRMEN bit is set in the PCID Control register before a transmit VC provision / unprovision command is issued. In addition when unprovisioning a VC the SRQ[3:0] value, located in the COPS VC Control and Status register, should be the same as when the VC was provisioned.

10.1.103 Register 0xA2 (0x288): COPS VC Number

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14 to Bit 7	R/W	Reserved	00H
Bit 6 to Bit 0	R/W	VCNUM[6:0]	XXH

The COPS VC Number register is used to program the Receive and Transmit VC Parameter Tables located in the parameter memory.

VCNUM[6:0]:
The VCNUM[6:0] field specifies the VC to be programmed. The COPS uses the VCNUM[6:0] field to generate the address of the VC to be programmed. The VCNUM[6:0] field should reflect the number of VC supported, as indicated by the NVCI[3:0] and NVPI[3:0] fields. For example if NVCI[3:0] = 5 and NVPI[3:0] = 2, then 7 bits are being used to generate the VC number. The maximum value that VCNUM[6:0] should take in the above example is 127.

10.1.104 Register 0xA3 (0x28C): COPS VPI (RX/TXB = 1, Rx Table)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	VPI[7]	0
Bit 6	R/W	VPI[6]	0
Bit 5	R/W	VPI[5]	0
Bit 4	R/W	VPI[4]	0
Bit 3	R/W	VPI[3]	0
Bit 2	R/W	VPI[2]	0
Bit 1	R/W	VPI[1]	0
Bit 0	R/W	VPI[0]	0

The COPS VPI register's definition depends on the value of the RX/TXB bit in the COPS Parameter Access Control register. When RX/TXB is set high as shown above, the COPS VPI register can be used to check the ATM cell header fields for receive VCs.

VPI[7:0]:
VPI[7:0] can be used to identify cells belonging to the referenced VC.

10.1.105 Register 0xA3 (0x28C): COPS VPI (RX/TXB = 0, Tx Table)

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	0
Bit 7	R/W	VPI[7]	0
Bit 6	R/W	VPI[6]	0
Bit 5	R/W	VPI[5]	0
Bit 4	R/W	VPI[4]	0
Bit 3	R/W	VPI[3]	0
Bit 2	R/W	VPI[2]	0
Bit 1	R/W	VPI[1]	0
Bit 0	R/W	VPI[0]	0

The COPS VPI register's definition depends on the value of the RX/TXB bit in the COPS Parameter Access Control register. When RX/TXB is set low as shown above, the COPS VPI register can be used to generate the ATM cell header fields for transmit VCs.

VPI[7:0]:
VPI[7:0] can be used to set the ATM VPI cell header field of every transmit cell of the referenced VC.

CLP:
The CLP bit can be used to set the default value of the ATM Cell Loss Priority cell header field. The default value can be overridden using the Transmit Descriptor on a CPAAL5_PDU by CPAAL5_PDU basis.

PTI[2:0]:
The PTI[2:0] bits can be used to set the default value of the ATM Payload Type Indicator cell header field. The default value can be overridden using the Transmit Descriptor on a CPAAL5_PDU by CPAAL5_PDU basis.

GFC[3:0]:
The GFC[3:0] bits can be used to set the default value of the ATM Generic Flow Control cell header field. The default value can be overwritten using external pins.

10.1.106 Register 0xA4 (0x290): COPS VCI

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	VCI[15:0]	0000H

The COPS VCI register is used to program the ATM cell header fields for receive and transmit VCs.

VCI[15:0]:
For the transmit VC Parameter Table, VCI[15:0] can be used to set the ATM VCI cell header field of every transmit cell of the referenced VC.

For the receive VC Parameter Table, VCI[15:0] can be used to identify cells belonging to the referenced VC.

10.1.107 Register 0xA5 (0x294): COPS VC Control and Status (RX/TXB = 1, Rx Table)

Bit	Type	Function	Default
Bit 15 to Bit 8	R/W	CTL[7:0]	00H
Bit 7 to Bit 0	R	STATUS[7:0]	00H

The COPS VC Control and Status register's definition depends on the value of the RX/TXB bit in the COPS Parameter Access Control register. When RX/TXB is set high as shown above, the COPS VC Control and Status register can be used to control and monitor receive VCs.

STATUS[7:0]:
The STATUS[7:0] bits indicate the current status of a receive VC as identified using the VCNUM[6:0] bits.

Field	Description
STATUS[7]	Reserved

STATUS[6]	The MAX_PDU_ABORT bit indicates that reassembly of the current packet was terminated due to the packet being larger than the specified maximum length in the RALP Max Rx PDU Length register. The MAX_PDU_ABORT bit is only used for VCs reassembling packet data. When MAX_PDU_ABORT is set to one, the current packet was terminated due to the packet being larger than the specified maximum length in the Max Rx PDU Length register. When MAX_PDU_ABORT is set to zero the current packet is not larger than the length specified in the Max Rx PDU Length register. The LASAR-155 sets the MAX_PDU_ABORT bit when it determines that the above error condition occurred. MAX_PDU_ABORT is cleared when the last cell of the aborted packet is received.
STATUS[5]	Reserved
STATUS[4]	Reserved
STATUS[3]	The CLP_RCVD bit indicates that the packet under reassembly includes a cell with its CLP bit equal to one. The CLP_RCVD bit is only used for VCs reassembling packet data. When CLP_RCVD is set to one, the packet under reassembly includes a cell with its CLP bit equal to one. When CLP_RCVD is set to zero, the packet under reassembly does not include any cells with the CLP bit equal to one. The LASAR-155 sets the CLP_RCVD bit when it receives a cell with the CLP bit set to one. CLP_RCVD is cleared by the LASAR-155 when reassembly on the current packet is complete.

STATUS[2]	CG_RCVD bit Indicates that the packet under reassembly includes a cell that experienced congestion. The CG_RCVD bit is only used for VCs reassembling packet data. When CG_RCVD is set to one, the packet under reassembly includes a cell with the PTI[2:0] field indicating congestion. When CG_RCVD is set to zero, the packet under reassembly does not include any cells with the PTI[2:0] field indicating congestion. The LASAR-155 sets the CG_RCVD bit when it receives a cell with the with the PTI[2:0] (010 or 011) field indicating congestion. CG_RCVD is cleared by the LASAR-155 when reassembly on the current packet is complete.
STATUS[1]	ACTV_RSMB bit Indicates that a packet is actively being reassembled on the VC. The ACTV_RSMB bit is only used for VCs reassembling packet data as indicated when QUEUE_SEL[1:0] in the CTL[7:0] field is set to '11B'. When ACTV_RSMB is set to one, a packet is being reassembled. When ACTV_RSMB is set to zero, a packet is not being reassembled. The LASAR-155 sets the ACTV_RSMB bit when it begins reassembly of a packet. ACTV_RSMB is cleared by the LASAR-155 when reassembly on the packet ends.
STATUS[0]	Reserved

CTL[7:0]:
The CTL[7:0] bits control cell reassembly on a per receive VC basis as identified using the VCNUM[6:0] bits of the COPS VC Number register.

Field	Description
CTL[7]	The VC_REAS_EN bit is used to enable and disable cell processing and packet reassembly on a per VC basis. Global enabling and disabling is controlled using the REAS_EN bit in the RALP Control register. When VC_REAS_EN and REAS_EN are set to logic one, cell processing and packet reassembly is allowed to begin. When VC_REAS_EN is set to logic zero or REAS_EN is set to logic zero, reassembly is terminated on the specified VC. Termination can be either immediate or graceful as controlled using the REAS_DM bit in the RALP Control register.
CTL[6]	Reserved
CTL[5]	Reserved
CTL[4]	Reserved

CTL[3:2]	The QUEUE_SEL[1:0] bits control whether cells on a VC should be directed to the Receive Packet Queue (RPQ) or the Receive Management Queue (RMQ). In addition, the QUEUE_SEL[1:0] bits control the type of CRC check to apply to the cells directed to the RMQ. If cells are directed to the RPQ, the CRC-10 is automatically applied to management cells (PTI = 100, 101, 110) while no CRC check is applied to user cells (PTI = 000, 001, 010, 011). Users cells are reassembled into CPAAL5_PDUs which are in turn automatically verified using the CRC-32. For packet data, no CRC is applied to cells with a PTI = 111. The encoding of QUEUE_SEL[1:0] is described below. 00 - RMQ, CRC-10 01 - RMQ, CRC-32 10 - RMQ, no CRC check 11 - RPQ for all user cells (PTI = 0XX). RMQ for all management cells (PTI = 1XX).
CTL[1]	The VC_PACKET_QUEUE_ENB bit controls if user cells ((PTI = 000, 001, 010, 011) are copied to the Receive Packet Queue (RPQ). When VC_PACKET_QUEUE_ENB is set to zero, user cells are copied to the PCI Host. When VC_PACKET_QUEUE_ENB is set to one, user cells are not copied to the PCI Host.
CTL[0]	The CEX_EN bit controls if user cells ((PTI = 000, 001, 010, 011) are copied to the Multipurpose Port. When CEX_EN is set to zero, user cells are not copied to the Multipurpose Port. When CEX_EN is set to one, user cells are copied to the Multipurpose Port.

10.1.108 Register 0xA5 (0x294): COPS VC Control and Status (RX/TXB = 0, Tx Table)

Bit	Type	Function	Default
Bit 15 to Bit 12	R/W	CTL[3:0]	0H
Bit 11 to Bit 8	R	STATUS[3:0]	XH
Bit 7 to Bit 4	R/W	SUB_SRQ_R [3:0]	0H
Bit 3 to Bit 0	R/W	SRQ[3:0]	0H

The COPS VC Control and Status register's definition depends on the value of the RX/TXB bit in the COPS Parameter Access Control register. When RX/TXB is set low as shown above, the COPS VC Control and Status register can be used to control and monitor transmit VCs.

SRQ[3:0]:
The SRQ[3:0] bits identify the Service Rate Queue to associate the transmit VC identified using the VCNUM[6:0] bits. The bit definitions are defined below.

SRQ	Service Rate Queue Selected
0000	SRQ1
0001	SRQ2
0010	SRQ3
0011	SRQ4
0100	SRQ5
0101	SRQ6
0110	SRQ7
0111	SRQ8
1xxx	Reserved

SUB_SRQ_R[3:0]:
The SUB_SRQ_R[3:0] bits select the prescale to apply the selected Service Rate Queue's (SRQ) Peak Cell Rate (PCR) to define a VC's PCR (VC_PCR). Prescale selection is illustrated below.

SUB_SRQ_R	Prescale Factor
0000	1
0001	1/2
0010	1/4
0011	Reserved
01xx	Reserved
1xxx	Reserved

A VC_PCR is defined using the formula below:

VC_PCR = SRQ PCR * Prescale Factor

i.e. Given SRQ PCR = 10 Mbit/s, SUB_SRQ_R = 0001

VC_PCR = 10 Mbit/s * 1/2 = 5 Mbit/s

STATUS[3:0]:
The STATUS[3:0] bits indicate the current status of a transmit VC as identified using the VCNUM[6:0] bits.

Field	Description
STATUS[3]	Reserved.
STATUS[2]	Reserved.
STATUS[1]	Active segmentation. Indicates that a CPAAL5_PDU is actively being segmented on the VC. When set to logic one active, segmentation is occurring.
STATUS[0]	Enabled for segmentation. When this bit is set transmit segmentation is enabled on this VC. When this bit is cleared the VC is disabled.

CTL[3:0]:
The CTL[3:0] bits control cell segmentation on a per transmit VC basis as identified using the VCNUM[6:0] bits.

Field	Description
CTL[3]	VC_SEG_EN The VC_SEG_EN bit is used to provision and unprovision Transmit VCs. When VC_SEG_EN is set low a VC is unprovisioned. When VC_SEG_EN is set high a VC is provisioned. Note, the TRMEN bit in the PCID Control register must be set to logic one before provisioning is performed. In addition when unprovisioning a VC the SRQ[3:0] value, located in the COPS VC Control and Status register, should be the same as when the VC was provisioned.
CTL[2]	VC_CBRC_EN The VC_CBRC_EN bit selects whether a VC is configured for VBR or VBR plus CBRC services. When configured for CBRC services, transmission over the VC is subject to a credit basket. When VC_CBRC_EN is set to logic zero, a VC is configured for VBR services. When VC_CBRC_EN is set to logic one, a VC is configured for VBR plus CBRC services.
CTL[1]	Reserved
CTL[0]	Reserved

10.1.109 Register 0xA6 (0x298) : COPS VC Parameters (RX/TXB = 0, Tx Table)

Bit	Type	Function	Default
Bit 15 to Bit 12	R/W	UTIL[3:0]	0H
Bit 11 to Bit 0	R/W	BUCKET_DEF [11:0]	000H

The COPS VC Parameters register is used to access transmit VC parameters (RX/TXB=0). This register is not used when receive VC parameters (RX/TXB=1) need to be accessed.

BUCKET_DEF[11:0]:
The BUCKET_DEF[11:0] bits can be used to program the size of the per transmit VC token bucket size. The VC token bucket size defines the Maximum Burst Size (MBS) for a VC.

Tokens are added to a bucket at the sustainable cell rate (SCR) as determined by the VC_PCR value and the UTIL field. Tokens are consumed at the VC_PCR rate. VC_PCR is defined in the COPS VC Control and Status register. If the bucket is empty, transmission proceeds at the bucket fill rate (i.e. SCR). For transmission to occur the BUCKET_DEF must be at least one. If BUCKET_DEF = 0, no transmission occurs.

The equation below defines the bucket size and in turn the MBS. For a selected UTIL, the BUCKET_DEF value chosen should result in an integer MBS.

MBS = (BUCKET_DEF*UTIL) / (1-UTIL)

Below are the ranges of MSB for selected UTIL values.

UTIL	Min MBS	BUCKET_DEF	Max MBS	BUCKET_DEF
1/8	1	8	585	4095
1/7	1	7	682	4092
1/6	1	6	819	4095
1/5	1	5	1023	4092
1/4	1	4	1365	4095
1/3	1	3	2047	4094
1/2	1	2	4094	4094
1/1	unbound	1	unbound	1

UTIL[3:0]:
The UTIL[3:0] bits select the scaled version of the VC PCR to be used as the per VC Sustainable Cell Rate (VC SCR). VC_PCR is defined in the COPS VC Control and Status register. Please refer below.

UTIL[3:0]	VC SCR
0000	VC_PCR
0001	1/2 * VC_PCR
0010	1/3 * VC_PCR
0011	1/4 * VC_PCR
0100	1/5 * VC_PCR

0101	1/6 * VC_PCR
0110	1/7 * VC_PCR
0111	1/8 * VC_PCR
1xxx	Reserved

10.1.110 Register 0xA7 (0x29C): COPS Indirect Control

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RD/WRB	X
Bit 13 to Bit 11	R/W	PRAMSEL[2:0]	0H
Bit 10 to Bit 2		Reserved	000H
Bit 1 to Bit 0	R/W	PADR[17:16]	00

The COPS Indirect Control register can be used to access the internal receive and transmit VC parameter tables. A write to this register cause either an indirect write or read to the internal location specified by the PADR[17:0] field. This register should not be accessed by users.

PADR[17:16]:
The PADR[17:16] bits are the most significant bits of the PADR[17:0] address field.

PRAMSEL[2:0]:
The PRAMSEL[2:0] bits are used to select which table is being accessed.

PRAMSEL[2:0]	Table
000	TVC_TABLE (Transmit VC Parameter Table)
001	TVL_TABLE (Transmit VC Link Table)
010	RVC_TABLE (Receive VC Parameter Table)
011	Reserved
1xx	Reserved

RD/WRB:
The RD/WRB bit selects whether to initiate an indirect read from or an indirect write to a VC parameter table when a write is performed on this register. When RD/WRB is set to logic one, a read is performed. When RD/WRB is set to logic zero, a write is performed.

BUSY:
The BUSY bit indicates when a VC parameter table indirect access is in progress. When busy is logic one, a read or write is in progress. When BUSY is logic zero, the previous access has completed.

10.1.111 Register 0xA8 (0x2A0): COPS Indirect Address

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PADR[15:0]	0000H

PADR[15:0]:
The PADR[15:0] bits are used to indirectly address into the VC parameter tables.

10.1.112 Register 0xA9 (0x2A4): COPS Indirect Data

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PDATA[15:0]	0000H

PDATA[15:0]:
The PDATA[15:0] bits reports the data read from a VC parameter table location after an indirect read operation has completed. The data to be written to a VC parameter table location must be set up in this register before an indirect write operation. Data read from this register reflects the value written until the completion of a subsequent indirect read operation.

10.2 10.2. Microprocessor Only Access Registers

Microprocessor Only registers can only be accessed by the microprocessor. For each register description below, the hexadecimal register number indicates the address of the register.

10.2.1 Register 0xC0: PCID Microprocessor Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PTOMP_ORE	0
Bit 3	R/W	MRA_ROE	0
Bit 2	R/W	PTOMPE	0
Bit 1	R/W	MWA_ROE	0
Bit 0	R/W	MPTOPE	0

PTOMP_ORE, MRA_ROE, PTOMPE, MWA_ROE, MPTOPE:
The above enable bits control interrupt generation by the corresponding interrupt bits in the PCID Microprocessor Interrupt Status register. When the enable bit is set to logic one, the corresponding interrupt will generate a microprocessor interrupt on output INTB. It should be noted that the PCIDE bit, located in the LASAR-155 Master Interrupt Enable register, must be set to logic one to generate an interrupt on the INTB output.

10.2.2 Register 0xC1: PCID Microprocessor Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X

Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	PTOMP_ORI	X
Bit 3	R	MRA_ROI	X
Bit 2	R	PTOMPI	X
Bit 1	R	MWA_ROI	X
Bit 0	R	MPTOPI	X

The PCID Microprocessor Interrupt Status register indicates the status of the PCID mailboxes. Interrupt bits are cleared when this register is read.

MPTOPI:
The MPTOPI bit is set high when the PCI Host sets the MASTER bit high in the PCID Host Read Mailbox Control register. The MASTER bit is set high to pass control of the microprocessor to PCI Host mailbox back to the microprocessor.

MWA_ROI:
The MWA_ROI bit is set high if the MWA value rolled over while writing to the microprocessor to PCI Host mailbox.

PTOMPI:
The PTOMPI bit is set high when the PCI Host sets the MASTER bit high in the PCID Host Write Mailbox Control register. The MASTER bit is set high to pass control of the PCI Host to microprocessor mailbox to the microprocessor.

MRA_ROI:
The MRA_ROI bit is set high if the MRA value rolled over while reading from the PCI Host to microprocessor mailbox.

PTOMP_ORI:
The PTOMP_ORI bit is set high if the PCI Host takes control of the PCI Host to microprocessor mailbox from the microprocessor.

10.2.3 Register 0xC2: PCID Microprocessor Indirect Control

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RD/WRB	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11 to Bit 2	R/W	MIADDR[11:2]	000H
Bit 1		Unused	X
Bit 0		Unused	X

The PCID Microprocessor Indirect Control register can be used to access the internal RAMs of the PCID block. A write to this register cause either an indirect write or read to the internal location specified by the MIADDR[11:2] field. This register should not be accessed by users.

MIADDR[11:2]:
The MIADDR[11:2] bits are used to indirectly address PCID internal RAM locations. Only the DWORD address of each RAM needs to be specified. MIADDR[1:0] is always set to 00b. The PCID memory map is described below.

Address	Description
0x000 - 0x3FF	Reserved. No accesses should be made to these locations since the BUSY bit does not clear.
0x400 - 0x7FC	Receive VC Descriptor Reference Table
0x800 - 0xFFC	Transmit VC Descriptor Reference Table

RD/WRB:
The RD/WRB bit selects whether to initiate an indirect read from or an indirect write to PCID memory location when a write is performed on this register. When RD/WRB is set to logic one, a read is performed. When RD/WRB is set to logic zero, a write is performed.

BUSY:
The BUSY bit indicates when an access is in progress. When busy is logic one, a read or write PCID memory access is in progress. When BUSY is logic zero, the previous access has completed.

10.2.4 Register 0xC3: PCID Microprocessor Indirect Data Low Word

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	MIDATA[15:0]	0000H

MIDATA[15:0]:
The MIDATA[15:0] bits form the low word of the MIDATA[31:0] field.

10.2.5 Register 0xC4: PCID Microprocessor Indirect Data High Word

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	MIDATA[31:16]	0000H

MIDATA[31:16]:
The MIDATA[31:16] bits form the high word of the MIDATA[31:0] field.

MIDATA[31:0] reports the data read from a PCID memory location after an indirect read operation has completed. The data to be written to a PCID memory location must be set up in these registers before an indirect write operation. Data read from these registers reflects the value written until the completion of a subsequent indirect read operation.

Each element in the transmit descriptor table consists of three 32-bit words and each element in the receive packet descriptor table consists of two 32-bit words. It is possible to access a table entry while the indirect interface is modifying or reading the same entry. The programmer must therefore exercise caution when accessing these tables through the indirect data registers.

10.2.6 Register 0xC5: PCID Microprocessor Write Mailbox Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	MWA[5]	0
Bit 12	R/W	MWA[4]	0
Bit 11	R/W	MWA[3]	0
Bit 10	R/W	MWA[2]	0
Bit 9	R/W	MWA[1]	0
Bit 8	R/W	MWA[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	MASTER	1

MASTER:
The MASTER bit is used to indicate the current master of the microprocessor to PCI Host mailbox. When set to logic one, the microprocessor is the master, When set to logic zero, the PCI Host is the master.

After the microprocessor has filled the microprocessor to PCI Host mailbox with a message, the microprocessor should set MASTER to logic zero to enable PCI Host mailbox reads. When the PCI Host has completed its accesses, it will set the MASTER bit to logic one to return the control of the mailbox to the microprocessor. An interrupt can be generated using the MPTOPE bit in the PCID Microprocessor Control register.

If for some reason the microprocessor must obtain control of the microprocessor to PCI Host mailbox when the PCI Host is the master, the microprocessor can take control of the mailbox by setting the MASTER bit to logic one. This action is not recommended.

Note, when the microprocessor transfers control of the microprocessor to PCI Host mailbox to the PCI Host, the value of MWA should be set to 0x3F. Address 0x3F is not a valid address for the Microprocessor Write Mailbox. The

sequence for transferring control is :

1) Write MWA=0x3F and keep the MASTER bit set to one.
2) Keep MWA=0x3F and set the MASTER bit to zero.

MWA[5:0]:
The MWA[5:0] bits specify the address of the microprocessor to PCI Host mailbox location the microprocessor wishes to access. MWA[5:0] is automatically post incremented after every access to the PCID Microprocessor Write Mailbox Data register. If the address reaches its limit, it wraps around to the start of the mailbox. The MWA_ROI bit in the PCID Microprocessor Interrupt Status register will be set high if this occurs.

Note, Address 0x3F is not a valid address for the Microprocessor Write Mailbox.

10.2.7 Register 0xC6: PCID Microprocessor Write Mailbox Data

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	MWD[15:0]	XXXXH

MWD[15:0]:
The MWD[15:0] bits are used to write data to the microprocessor to PCI Host mailbox. The mailbox location is specified using the MWA value in the PCID Microprocessor Write Mailbox Control register. Data written to the microprocessor to PCI Host mailbox can also be read back and verified using this register. To allow burst mailbox accesses, MWA is automatically post incremented after every access.

10.2.8 Register 0xC8: PCID Microprocessor Read Mailbox Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	MRA[5]	0
Bit 12	R/W	MRA[4]	0
Bit 11	R/W	MRA[3]	0
Bit 10	R/W	MRA[2]	0
Bit 9	R/W	MRA[1]	0
Bit 8	R/W	MRA[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	MASTER	0

MASTER:
The MASTER bit is used to indicate the current master of the PCI Host to microprocessor mailbox. When set to logic one, the microprocessor is the master, When set to logic zero, the PCI Host is the master. Note, the microprocessor cannot set high this bit. It can only force this bit low.

The MASTER bit will be set high by the PCI Host to indicate that the microprocessor can access the mailbox for a read. The MASTER bit is set low by the microprocessor to return control of the mailbox to the PCI Host.

If for some reason the PCI Host takes control of the PCI to microprocessor mailbox when the microprocessor is the master, the microprocessor is alerted using the PTOMP_ORI bit in the PCID Microprocessor Interrupt Status register.

MRA[5:0]:
The MRA[5:0] bits specify the address of the PCI Host to microprocessor mailbox location the microprocessor wishes to read from. MRA[5:0] is automatically post incremented after every read of the PCID Microprocessor Read Mailbox Data register. If the address reaches its limit, it wraps around to the start of the

mailbox. The MRA_ROI bit in the PCID Microprocessor Interrupt Status register will be set high if this occurs.

10.2.9 Register 0xC9: PCID Microprocessor Read Mailbox Data

Bit	Type	Function	Default
Bit 15 to Bit 0	R	MRD[15:0]	XXXXH

MRD[15:0]:
The MRD[15:0] bits are used to read data from the PCI Host to microprocessor mailbox. The mailbox location is specified using the MRA value in the PCID Microprocessor Read Mailbox Control register. To allow burst mailbox reads, MRA is automatically post incremented after every read.

10.4 PCI Host Only Access Registers

PCI Host Only registers can only be accessed the PCI Host. For each register description below, the hexadecimal number in brackets indicates the PCI offset from the base address in the LASAR-155 Memory Base Address Register when accesses are made using the PCI Host Port.

10.4.1 Register 0x300: PCID Control

Bit	Type	Function	Default
Bit 31 to Bit 19		Unused	XXXXH
Bit 18	R/W	TRMEN	0
Bit 17	R/W	SOE_E	0
Bit 16	R/W	TXVC_UPIE	0
Bit 15	R/W	RMQ_INTR[2]	0
Bit 14	R/W	RMQ_INTR[1]	0
Bit 13	R/W	RMQ_INTR[0]	0
Bit 12	R/W	RPQ_INTR[2]	0
Bit 11	R/W	RPQ_INTR[1]	0
Bit 10	R/W	RPQ_INTR[0]	0
Bit 9	R/W	TXREQ_FD[1]	1
Bit 8	R/W	TXREQ_FD[0]	0
Bit 7	R/W	TXSDU_FD[2]	1
Bit 6	R/W	TXSDU_FD[1]	1
Bit 5	R/W	TXSDU_FD[0]	1
Bit 4	R/W	TXPDU_UU_S	0
Bit 3	R/W	TXPDU_CPI_S	0
Bit 2	R/W	TXFQ_E	1
Bit 1	R/W	ENDIAN	1
Bit 0	R/W	ARBMD	0

ARBMD:
The arbitration mode (ARBMD) bit specifies which arbitration scheme the PCID DMA controllers shall use. When ARBMD is set high a fair rotational round-robin scheme is used to service the receive and transmit DMA requests. When ARBMD is set low, the receive management queue DMA requests have priority over the receive packet queue DMA requests which in turn have priority the transmit DMA requests.

ENDIAN:

The ENDIAN bit selects either Big Endian or Little Endian format when reading from and writing to Receive and Transmit Descriptor Buffer memory locations. When ENDIAN is set high, Little Endian format is selected. When ENDIAN is set low, Big Endian format is selected. Please refer below for each format's byte ordering.

Big Endian Format

		Bit 31	Bit 16	Bit 15	Bit 0
Address	00	SDU BYTE 0	SDU BYTE 1	SDU BYTE 2	SDU BYTE 3
	04	SDU BYTE 4	SDU BYTE 5	SDU BYTE 6	SDU BYTE 7
		•	•	•	•
		•	•	•	•
		•	•	•	•
	n-3	SDU BYTE n-3	SDU BYTE n-2	SDU BYTE n-1	SDU BYTE n

Little Endian Format

		Bit 31	Bit 16	Bit 15	Bit 0
Address	00	SDU BYTE 3	SDU BYTE 2	SDU BYTE 1	SDU BYTE 0
	04	SDU BYTE 7	SDU BYTE 6	SDU BYTE 5	SDU BYTE 4
		•	•	•	•
		•	•	•	•
		•	•	•	•
	n-3	SDU BYTE n	SDU BYTE n-1	SDU BYTE n-2	SDU BYTE n-3

TXFQ_E:
The Transmit Free Queue FIFO enable bit (TXFQ_E) controls the operation of the internal Transmit Descriptor Free Queue FIFO memory. This FIFO memory is used to temporarily store Free transmit descriptors inside the PCID device in order to reduce the number of PCI bus accesses.

When this bit is set high the six element internal TDR Free Queue FIFO memory is enabled and free TDRs are stored in the FIFO until an IOC TDR, the FIFO fills up or the PCID Transmit Request Machine is idle. When either event occurs, the FIFO is flushed and all TDRs are burst written into the TDRF queue located in PCI Host memory.

When set low all TDRs are written directly to the TDRF queue.

TXPDU_CPI_S:
The TXPDU_CPI_S bit selects the source of CPAAL5 _PDU Common Part indicator (CPI) byte. If TXPDU_CPI_S is set to logic one, the LASAR-155 device fills all transmit CPAAL5_PDU CPI bytes with 00H. If TXPDU_CPI_S is set to logic zero, the LASAR-155 uses the CPI byte provided in the Transmit Descriptors.

TXPDU_UU_S:
The TXPDU_UU_S bit selects the source of CPAAL5 _PDU User to User (UU) byte. If TXPDU_UU_S is set to logic one, the LASAR-155 device fills all transmit CPAAL5_PDU UU bytes with 00H. If TXPDU_UU_S is set to logic zero, the LASAR-155 uses the UU byte provided in the Transmit Descriptors.

TXSDU_FD[2:0]:
The TXSDU_FD[2:0] bits specify the depth of the internal Transmit ATM SDU FIFO (TAS FIFO). The TAS FIFO is used to store cells retrieved by the PCID block and queued for transmission. The depth of the TAS FIFO can be adjusted to allow for flexible system design.

TXSDU_FD[2:0]	TAS FIFO Depth
000	1 cell
001	2 cells
010	3 cells
011	4 cells
100	5 cells
101	6 cells

110	7 cells
111	8 cells

TXREQ_FD[1:0]:
The TXREQ_FD[1:0] bits specify the depth of the internal Transmit Request FIFO (TR FIFO). The TR FIFO is used to buffer requests for transmit data from the TATS block to the PCID block . The depth of the TR FIFO can be adjusted to allow for flexible system design.

TXREQ_FD[1:0]	TAS FIFO Depth
00	1 request
01	4 request
10	8 request
11	Reserved

RPQ_INTR[2:0]:
The RPQ_INTR[2:0] bits specify the number of Receive Packet Descriptors (RPD) that are queued by the LASAR-155 onto the Receive Packet Ready Queue before the LASAR-155 interrupts the PCI Host. The interrupt can be masked using the PCID Interrupt Enable register.

RPQ_INTR[2:0]	number of RPD
000	1
001	4
010	8
011	16
100	32
101	reserved
110	reserved
111	reserved

RMQ_INTR[2:0]:
The RMQ_INTR[2:0] bits specify the number of Receive Management Descriptors (RMD) that are queued by the LASAR-155 onto the Receive Management Ready Queue before the LASAR-155 interrupts the PCI Host. The interrupt can be masked using the PCID Interrupt Enable register.

RMQ_INTR[2:0]	number of RMD
000	1
001	4
010	8
011	16
100	32
101	reserved
110	reserved
111	reserved

TXVC_UPIE:
The transmit VC unprovisioning (TXVC_UPIE) bit selects the VC unprovision process. When TXVC_UPIE is set high, the TRM will unprovision the selected VC immediately. When TXVC_UPIE is set low, the TRM will flush its internal FIFOs of cells before unprovisioning a VC. Please refer to the COPS registers for VC unprovisioning and provisioning registers.

SOE_E:
The stop on error enable (SOE_E) bit determines the action the PCI controller will take when a system or parity error occurs. When set high the PCI controller will disconnect the PCI REQB signal from the PCI bus. This will prevent the PCID from becoming a master device on the PCI bus when either the SERR or DPR bits in the PCI Command/Status register are set high. The SERR and DPR bits can be controlled via the SERREN and PERREN bits, respectively, in the PCI Command/Status register. When the SOE_E bit is set low the PCI controller will continue to allow master transactions on the PCI bus. Setting this bit low when an error has occurred will reactivate the PCI REQB signal.

TRMEN:
The Transmit Request Machine Enable (TRMEN) bit enables the transmit DMA controller. When TRMEN is set high, the transmit DMA controller is allowed to process the transmit ready queues, segment packets and provision / unprovision VCs. When TRMEN is set low, the transmit DMA controller is held in an idle state. Before setting the TRMEN bit high, all transmit queue registers should be initialized.

Note, if the TRMEN bit is set low, the transmit DMA controller will not process provision / unprovision requests initiated using the COPS registers.

10.4.2 Register 0x304: PCID Interrupt Status

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R	TXREQF_OVRI	X
Bit 14	R	TXSDUF_UDRI	X
Bit 13	R	RXSDUF_OVRI	X
Bit 12	R	TXVC_IDLI	X
Bit 11	R	RMQ_ERRI	X
Bit 10	R	RMQ_RDYI	X
Bit 9	R	RPQ_ERRI	X
Bit 8	R	RPQ_RDYI	X
Bit 7	R	IOCI	X
Bit 6	R	MAX_SDUI	X
Bit 5	R	SERRI	X
Bit 4	R	PERRI	X
Bit 3	R	TDFQ_ERRI	X
Bit 2	R	RPDR_ERRI	X
Bit 1	R	RMDR_ERRI	X
Bit 0	R	MPEN	X

The PCID Interrupt Status register indicates the status of the PCID. Interrupt bits are cleared when this register is read.

MPEN:

The MPEN bit indicates the presence of the external local microprocessor. When set to logic one, the LASAR-155 is operating in slave mode (MPENB=0) and the microprocessor is present. If MPEN is set the logic zero, the local processor is not installed and the PCI Host can access the internal LASAR-155 registers, the expansion ROM and external device memory spaces.

RMDR_ERRI:
The RMDR_ERRI bit is set high when the LASAR-155 has a Receive Management Descriptor to return to the PCI Host and there is no space available in the Receive Management Descriptor Ready Queue. The LASAR-155 will back pressure until space is available in the queue.

RPDR_ERRI:
The RPDR_ERRI bit is set high when the LASAR-155 has a Receive Packet Descriptor to return to the PCI Host and there is no space available in the Receive descriptor Ready Queue. The LASAR-155 will back pressure until space is available in the queue.

TDFQ_ERRI:
The TDFQ_ERRI bit is set high when the LASAR-155 has a Transmit Descriptor to return to the Host and there is no space available in the Transmit descriptor Free Queue. The LASAR-155 will back pressure until space is available in the queue.

PERRI:
The Parity Error interrupt bit is set high if the LASAR-155 is an initiator and detects a data parity error or if a target reports a parity error to the LASAR-155 using the PERRB signal. This bit is controlled only by the PERR_E signal in the PCID Interrupt Enable register and is not dependent on any signals from the PCI Command/Status register.

SERRI:
The System Error bit is set high to signal all address parity errors, data parity errors on Special Cycle commands, and all errors other than parity. This bit is controlled only by the SERR_E signal in the PCID Interrupt Enable register and is not dependent on any signals from the PCI Command/Status register.

MAX_SDUI:
The MAX_SDUI bit is set high if the length of the transmit SDU being processed

is greater than the maximum SDU size as indicated by the MTSDU[15:0] field in the PCID Max Tx SDU Length register.

IOCI:
The IOCI bit is set high after the segmentation of a TD's by the PCID. The generation of interrupts by the PCID can be controlled on a per TD basis by the IOC bit in the TD. If the PCID receives a TD with the IOC bit set and the interrupt on completion feature is enabled, all locally buffered free TDs will be returned to the free queue before the IOCI bit is set.

RPQ_RDYI:
The RPQ_RDYI bit is set high when the number of elements written onto the Receive Packet Ready Queue by the LASAR-155 since the last interrupt is equal to the number specified using the RPQ_INTR bits in the PCID Control register.

RPQ_ERRI:
The RPQ_ERRI bit is set high when the PCID block requires a Receive Packet Descriptor and the Receive Packet Descriptor Free Queue is empty. The LASAR-155 will back pressure until a Receive Packet Descriptor is available in the queue.

RMQ_RDYI:
The RMQ_RDYI bit is set high when the number of elements written onto the Receive Management Ready Queue by the LASAR-155 since the last interrupt is equal to the number specified using the RMQ_INTR bits in the PCID Control register.

RMQ_ERRI:
The RMQ_ERRI bit is set high when the PCID block requires a Receive Management Descriptor and the Receive Management Descriptor Free Queue is empty. The LASAR-155 will back pressure until a Receive Management Descriptor is available in the queue.

TXVC_IDLI:
The TXVC_IDLI bit is set high when the PCID receives a transmit request from the TATS block on a VC that is not provisioned or if a packet is queue for a VC that is not provisioned. Under normal operating conditions, this error should never occur.

RXSDUF_OVRI:
The RXSDUF_OVRI bit is set high when an FIFO overrun condition is detected

by the internal Receive ATM SDU FIFO. Under normal operating conditions, this error should never occur.

TXSDUF_UDRI:
The TXSDUF_UDRI bit is set high when an FIFO underrun condition is detected by the internal Transmit ATM SDU FIFO. Under normal operating conditions, this error should never occur.

TXREQF_OVRI:
The TXREQF_OVRI bit is set high when an FIFO overrun condition is detected by the internal Transmit Request FIFO. Under normal operating conditions, this error should never occur.

10.4.3 Register 0x308: PCID Interrupt Enable

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TXREQF_OVRE	0
Bit 14	R/W	TXSDUF_UDRE	0
Bit 13	R/W	RXSDUF_OVRE	0
Bit 12	R/W	TXVC_IDLE	0
Bit 11	R/W	RMQ_ERRE	0
Bit 10	R/W	RMQ_RDYE	0
Bit 9	R/W	RPQ_ERRE	0
Bit 8	R/W	RPQ_RDYE	0
Bit 7	R/W	IOCE	0
Bit 6	R/W	MAX_SDUE	0
Bit 5	R/W	SERR_E	0
Bit 4	R/W	PERR_E	0
Bit 3	R/W	TDFQ_ERRE	0
Bit 2	R/W	RPDR_ERRE	0
Bit 1	R/W	RMDR_ERRE	0
Bit 0	R/W	PONS_E	0

PONS_E:

Report PERR on SERR error (PONS_E) controls the source of system errors. When set high all parity errors will be signaled to the host via the SERRB output signal.

RMDR_ERRE, RPDR_ERRE, TDFQ_ERRE, PERR_E, SERR_E, MAX SDUE, IOCE, RPQ_RDYE, RPQ_ERRE, RMQ_RDYE, RMQ_ERRE, TXVC_IDLE, RXSDUF_OVRE, TXSDUF_UDRE, TXREQF_OVRE:

The above enable bits control the generation of interrupts based on the interrupt bits in the PCID Interrupt Status register. When the enable bit is set to logic one, the corresponding interrupt will generate a PCI Host interrupt on output PCIINTB.

10.4.4 Register 0x30C: PCID Mailbox / Microprocessor Interrupt Status / Enable

Bit	Type	Function	Default
Bit 31 to Bit 15		Unused	XXXXH
Bit 14	R/W	EXTIE	0
Bit 13	R/W	MPTOP_ORE	0
Bit 12	R/W	HWA_ROE	0
Bit 11	R/W	PTOMPE	0
Bit 10	R/W	HRA_ROE	0
Bit 9	R/W	MPTOPE	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	EXTI	X
Bit 4	R	MPTOP_ORI	X
Bit 3	R	HWA_ROI	X
Bit 2	R	PTOMPI	X
Bit 1	R	HRA_ROI	X
Bit 0	R	MPTOPI	X

The PCID Mailbox/Microprocessor Interrupt Status/Enable register indicates the status of the PCID mailbox and the Microprocessor Interface. All interrupt bits except EXTI are cleared when this register is read. EXTI is cleared only when the primary source of the interrupt (an internal LASAR-155 register or the INTB input) is cleared.

MPTOPI:
The MPTOPI bit is set high when the microprocessor sets the MASTER bit low in the PCID Microprocessor Write Mailbox Control register. The MASTER bit is set low to pass control of the microprocessor to PCI Host mailbox to the PCID Host.

HRA_ROI:
The HRA_ROI bit is set high if the HRA value rolled over while reading from the microprocessor to PCI Host mailbox.

PTOMPI:
The PTOMPI bit is set high when the microprocessor sets the MASTER bit low in

the PCID Microprocessor Read Mailbox Control register. The MASTER bit is set low to pass control of the PCI Host to microprocessor mailbox to the PCID Host.

HWA_ROI:
The HWA_ROI bit is set high if the HWA value rolled over while accessing the PCI Host to microprocessor mailbox.

MPTOP_ORI:
The MPTOP_ORI bit is set high if the microprocessor takes control of the microprocessor to PCI Host mailbox from the PCI Host.

EXTI:
The EXTI bit is a level sensitive bit and is not cleared on a read of this register. EXTI set high if an interrupt service request is required by a block in the LASAR-155 other than the PCID or from an external device on the LASAR-155 local bus via the INTB input. EXTI should only be used if the local microprocessor is not present (MPENB=1); otherwise, EXTI should be ignored.

When EXTI is set to logic one, the LASAR-155 Master Interrupt Status register should be read to determine the source of the interrupt.

MPTOPE, HRA_ROE, PTOMPE, HWA_ROE, MPTOP_ORE, EXTIE :
The above enable bits control interrupt generation by the corresponding interrupt bits in this register. When the enable bit is set to logic one, the corresponding interrupt will generate a PCI Host interrupt on output PCIINTB.

10.4.6 Register 0x314: PCID Rx Packet Descriptor Table Base

Bit	Type	Function	Default
Bit 31 to Bit 0	R/W	RPDTB[31:0]	XXXXXXXXH

RPDTB[31:0]:
The RPDTB[31:0] bits define the base of the Receive Packet Descriptor Table. These registers are initialized by the PCI Host. To calculate the physical address of a RPD, the 14 bit RPD offset must be added to bits 31 to 5 of the PCID Receive Packet Descriptor Table Base (RPDTB[31:5]).

The table must be on a 32 byte boundary and thus the least significant 5 bits must be written to logic 0.

10.4.7 Register 0x318: PCID Rx Management Descriptor Table Base

Bit	Type	Function	Default
Bit 31 to Bit 0	R/W	RMDTB[31:0]	XXXXXXXXH

RMDTB[31:0]:
The RMDTB[31:0] bits define the base of the Receive Management Descriptor Table. These registers are initialized by the PCI Host. To calculate the physical address of a RMD, the 14 bit RMD offset must be added to bits 31 to 5 of the PCID Receive Management Descriptor Table Base (RMDTB[31:5]).

The table must be on a 32 byte boundary and thus the least significant 5 bits must be written to logic 0.

10.4.8 Register 0x31C: PCID Rx Queue Base

Bit	Type	Function	Default
Bit 31 to Bit 0	R/W	RQB[31:0]	XXXXXXXXH

RQB[31:0]:
The RQB[31:0] bits define the base address of the Receive Packet Descriptor Reference Large Buffer Free, Receive Packet Descriptor Reference Small Buffer Free, Receive Packet Descriptor Reference Ready, Receive Management Descriptor Reference Free and Receive Management Descriptor Reference Ready queues. This register is initialized by the PCI Host. To calculate the physical address of a particular receive queue element, the RQB bits are added to the appropriate queue start, end, read or write index registers to form the physical address.

The base address must be DWORD aligned and thus the least significant 2 bits must be written to logic 0.

10.4.9 Register 0x320: PCID Rx Packet Descriptor Reference Large Buffer Free Queue Start

10.4.9.1

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRLFQS[15]	X
Bit 14	R/W	RPDRLFQS[14]	X
Bit 13	R/W	RPDRLFQS[13]	X
Bit 12	R/W	RPDRLFQS[12]	X
Bit 11	R/W	RPDRLFQS[11]	X
Bit 10	R/W	RPDRLFQS[10]	X
Bit 9	R/W	RPDRLFQS[9]	X
Bit 8	R/W	RPDRLFQS[8]	X
Bit 7	R/W	RPDRLFQS[7]	X
Bit 6	R/W	RPDRLFQS[6]	X
Bit 5	R/W	RPDRLFQS[5]	X
Bit 4	R/W	RPDRLFQS[4]	X
Bit 3	R/W	RPDRLFQS[3]	X
Bit 2	R/W	RPDRLFQS[2]	X
Bit 1	R/W	RPDRLFQS[1]	X
Bit 0	R/W	RPDRLFQS[0]	X

RPDRLFQS[15:0]:
The RPDRLFQS[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Large Buffer Free Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the RPDRLF queue, the RPDRLFQS bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.10 Register 0x324: PCID Rx Packet Descriptor Reference Large Buffer Free Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRLFQW[15]	X
Bit 14	R/W	RPDRLFQW[14]	X
Bit 13	R/W	RPDRLFQW[13]	X
Bit 12	R/W	RPDRLFQW[12]	X
Bit 11	R/W	RPDRLFQW[11]	X
Bit 10	R/W	RPDRLFQW[10]	X
Bit 9	R/W	RPDRLFQW[9]	X
Bit 8	R/W	RPDRLFQW[8]	X
Bit 7	R/W	RPDRLFQW[7]	X
Bit 6	R/W	RPDRLFQW[6]	X
Bit 5	R/W	RPDRLFQW[5]	X
Bit 4	R/W	RPDRLFQW[4]	X
Bit 3	R/W	RPDRLFQW[3]	X
Bit 2	R/W	RPDRLFQW[2]	X
Bit 1	R/W	RPDRLFQW[1]	X
Bit 0	R/W	RPDRLFQW[0]	X

RPDRLFQW[15:0]:
The RPDRLFQW[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Large Buffer Free Queue Write pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical address the RPDRLFQW bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.11 Register 0x328: PCID Rx Packet Descriptor Reference Large Buffer Free Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRLFQR[15]	X
Bit 14	R/W	RPDRLFQR[14]	X
Bit 13	R/W	RPDRLFQR[13]	X
Bit 12	R/W	RPDRLFQR[12]	X
Bit 11	R/W	RPDRLFQR[11]	X
Bit 10	R/W	RPDRLFQR[10]	X
Bit 9	R/W	RPDRLFQR[9]	X
Bit 8	R/W	RPDRLFQR[8]	X
Bit 7	R/W	RPDRLFQR[7]	X
Bit 6	R/W	RPDRLFQR[6]	X
Bit 5	R/W	RPDRLFQR[5]	X
Bit 4	R/W	RPDRLFQR[4]	X
Bit 3	R/W	RPDRLFQR[3]	X
Bit 2	R/W	RPDRLFQR[2]	X
Bit 1	R/W	RPDRLFQR[1]	X
Bit 0	R/W	RPDRLFQR[0]	X

RPDRLFQR[15:0]:
The RPDRLFQR[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Large Buffer Free Queue Read pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical read pointer address of the RPDRLF queue, the RPDRLFQR bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.12 Register 0x32C: PCID Rx Packet Descriptor Reference Large Buffer Free Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRLFQE[15]	X
Bit 14	R/W	RPDRLFQE[14]	X
Bit 13	R/W	RPDRLFQE[13]	X
Bit 12	R/W	RPDRLFQE[12]	X
Bit 11	R/W	RPDRLFQE[11]	X
Bit 10	R/W	RPDRLFQE[10]	X
Bit 9	R/W	RPDRLFQE[9]	X
Bit 8	R/W	RPDRLFQE[8]	X
Bit 7	R/W	RPDRLFQE[7]	X
Bit 6	R/W	RPDRLFQE[6]	X
Bit 5	R/W	RPDRLFQE[5]	X
Bit 4	R/W	RPDRLFQE[4]	X
Bit 3	R/W	RPDRLFQE[3]	X
Bit 2	R/W	RPDRLFQE[2]	X
Bit 1	R/W	RPDRLFQE[1]	X
Bit 0	R/W	RPDRLFQE[0]	X

RPDRLFQE[15:0]:
The RPDRLFQE[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Large Buffer Free Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the RPDRLF queue, the RPDRLFQE bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.13 Register 0x330: PCID Rx Packet Descriptor Reference Small Buffer Free Queue Start

10.4.13.1

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRSFQS[15]	X
Bit 14	R/W	RPDRSFQS[14]	X
Bit 13	R/W	RPDRSFQS[13]	X
Bit 12	R/W	RPDRSFQS[12]	X
Bit 11	R/W	RPDRSFQS[11]	X
Bit 10	R/W	RPDRSFQS[10]	X
Bit 9	R/W	RPDRSFQS[9]	X
Bit 8	R/W	RPDRSFQS[8]	X
Bit 7	R/W	RPDRSFQS[7]	X
Bit 6	R/W	RPDRSFQS[6]	X
Bit 5	R/W	RPDRSFQS[5]	X
Bit 4	R/W	RPDRSFQS[4]	X
Bit 3	R/W	RPDRSFQS[3]	X
Bit 2	R/W	RPDRSFQS[2]	X
Bit 1	R/W	RPDRSFQS[1]	X
Bit 0	R/W	RPDRSFQS[0]	X

RPDRSFQS[15:0]:
The RPDRSFQS[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Small Buffer Free Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the RPDRSF queue, the RPDRSFQS bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.14 Register 0x334: PCID Rx Packet Descriptor Reference Small Buffer Free Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRSFQW[15]	X
Bit 14	R/W	RPDRSFQW[14]	X
Bit 13	R/W	RPDRSFQW[13]	X
Bit 12	R/W	RPDRSFQW[12]	X
Bit 11	R/W	RPDRSFQW[11]	X
Bit 10	R/W	RPDRSFQW[10]	X
Bit 9	R/W	RPDRSFQW[9]	X
Bit 8	R/W	RPDRSFQW[8]	X
Bit 7	R/W	RPDRSFQW[7]	X
Bit 6	R/W	RPDRSFQW[6]	X
Bit 5	R/W	RPDRSFQW[5]	X
Bit 4	R/W	RPDRSFQW[4]	X
Bit 3	R/W	RPDRSFQW[3]	X
Bit 2	R/W	RPDRSFQW[2]	X
Bit 1	R/W	RPDRSFQW[1]	X
Bit 0	R/W	RPDRSFQW[0]	X

RPDRSFQW[15:0]:
The RPDRSFQW[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Small Buffer Free Queue Write pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical address the RPDRSFQW bits are added with to RQB field in the PCID Rx Queue Base register.

10.4.15 Register 0x338: PCID Rx Packet Descriptor Reference Small Buffer Free Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRSFQR[15]	X
Bit 14	R/W	RPDRSFQR[14]	X
Bit 13	R/W	RPDRSFQR[13]	X
Bit 12	R/W	RPDRSFQR[12]	X
Bit 11	R/W	RPDRSFQR[11]	X
Bit 10	R/W	RPDRSFQR[10]	X
Bit 9	R/W	RPDRSFQR[9]	X
Bit 8	R/W	RPDRSFQR[8]	X
Bit 7	R/W	RPDRSFQR[7]	X
Bit 6	R/W	RPDRSFQR[6]	X
Bit 5	R/W	RPDRSFQR[5]	X
Bit 4	R/W	RPDRSFQR[4]	X
Bit 3	R/W	RPDRSFQR[3]	X
Bit 2	R/W	RPDRSFQR[2]	X
Bit 1	R/W	RPDRSFQR[1]	X
Bit 0	R/W	RPDRSFQR[0]	X

RPDRSFQR[15:0]:
The RPDRSFQR[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Small Buffer Free Queue Read pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical read pointer address of the RPDRSF queue, the RPDRSFQR bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.16 Register 0x33C: PCID Rx Packet Descriptor Reference Small Buffer Free Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRSFQE[15]	X
Bit 14	R/W	RPDRSFQE[14]	X
Bit 13	R/W	RPDRSFQE[13]	X
Bit 12	R/W	RPDRSFQE[12]	X
Bit 11	R/W	RPDRSFQE[11]	X
Bit 10	R/W	RPDRSFQE[10]	X
Bit 9	R/W	RPDRSFQE[9]	X
Bit 8	R/W	RPDRSFQE[8]	X
Bit 7	R/W	RPDRSFQE[7]	X
Bit 6	R/W	RPDRSFQE[6]	X
Bit 5	R/W	RPDRSFQE[5]	X
Bit 4	R/W	RPDRSFQE[4]	X
Bit 3	R/W	RPDRSFQE[3]	X
Bit 2	R/W	RPDRSFQE[2]	X
Bit 1	R/W	RPDRSFQE[1]	X
Bit 0	R/W	RPDRSFQE[0]	X

RPDRSFQE[15:0]:
The RPDRSFQE[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Small Buffer Free Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the RPDRSF queue, the RPDRSFQE bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.17 Register 0x340: PCID Rx Packet Descriptor Reference Ready Queue Start

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRRQS[15]	X
Bit 14	R/W	RPDRRQS[14]	X
Bit 13	R/W	RPDRRQS[13]	X
Bit 12	R/W	RPDRRQS[12]	X
Bit 11	R/W	RPDRRQS[11]	X
Bit 10	R/W	RPDRRQS[10]	X
Bit 9	R/W	RPDRRQS[9]	X
Bit 8	R/W	RPDRRQS[8]	X
Bit 7	R/W	RPDRRQS[7]	X
Bit 6	R/W	RPDRRQS[6]	X
Bit 5	R/W	RPDRRQS[5]	X
Bit 4	R/W	RPDRRQS[4]	X
Bit 3	R/W	RPDRRQS[3]	X
Bit 2	R/W	RPDRRQS[2]	X
Bit 1	R/W	RPDRRQS[1]	X
Bit 0	R/W	RPDRRQS[0]	X

RPDRRQS[15:0]:
The RPDRRQS[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Ready Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the RPDRR queue, the RPDRRQS bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.18 Register 0x344: PCID Rx Packet Descriptor Reference Ready Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRRQW[15]	X
Bit 14	R/W	RPDRRQW[14]	X
Bit 13	R/W	RPDRRQW[13]	X
Bit 12	R/W	RPDRRQW[12]	X
Bit 11	R/W	RPDRRQW[11]	X
Bit 10	R/W	RPDRRQW[10]	X
Bit 9	R/W	RPDRRQW[9]	X
Bit 8	R/W	RPDRRQW[8]	X
Bit 7	R/W	RPDRRQW[7]	X
Bit 6	R/W	RPDRRQW[6]	X
Bit 5	R/W	RPDRRQW[5]	X
Bit 4	R/W	RPDRRQW[4]	X
Bit 3	R/W	RPDRRQW[3]	X
Bit 2	R/W	RPDRRQW[2]	X
Bit 1	R/W	RPDRRQW[1]	X
Bit 0	R/W	RPDRRQW[0]	X

RPDRRQW[15:0]:
The RPDRRQW[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Ready Queue Write pointer address. This registers is initialized by the PCI Host and is updated by the LASAR-155. To calculate the physical write pointer address of the RPDRR queue, the RPDRRQW bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.19 Register 0x348: PCID Rx Packet Descriptor Reference Ready Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRRQR[15]	X
Bit 14	R/W	RPDRRQR[14]	X
Bit 13	R/W	RPDRRQR[13]	X
Bit 12	R/W	RPDRRQR[12]	X
Bit 11	R/W	RPDRRQR[11]	X
Bit 10	R/W	RPDRRQR[10]	X
Bit 9	R/W	RPDRRQR[9]	X
Bit 8	R/W	RPDRRQR[8]	X
Bit 7	R/W	RPDRRQR[7]	X
Bit 6	R/W	RPDRRQR[6]	X
Bit 5	R/W	RPDRRQR[5]	X
Bit 4	R/W	RPDRRQR[4]	X
Bit 3	R/W	RPDRRQR[3]	X
Bit 2	R/W	RPDRRQR[2]	X
Bit 1	R/W	RPDRRQR[1]	X
Bit 0	R/W	RPDRRQR[0]	X

RPDRRQR[15:0]:
The RPDRRQR[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Ready Queue Read pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical read pointer address of the RPDRR queue, the RPDRRQR bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.20 Register 0x34C: PCID Rx Packet Descriptor Reference Ready Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RPDRRQE[15]	X
Bit 14	R/W	RPDRRQE[14]	X
Bit 13	R/W	RPDRRQE[13]	X
Bit 12	R/W	RPDRRQE[12]	X
Bit 11	R/W	RPDRRQE[11]	X
Bit 10	R/W	RPDRRQE[10]	X
Bit 9	R/W	RPDRRQE[9]	X
Bit 8	R/W	RPDRRQE[8]	X
Bit 7	R/W	RPDRRQE[7]	X
Bit 6	R/W	RPDRRQE[6]	X
Bit 5	R/W	RPDRRQE[5]	X
Bit 4	R/W	RPDRRQE[4]	X
Bit 3	R/W	RPDRRQE[3]	X
Bit 2	R/W	RPDRRQE[2]	X
Bit 1	R/W	RPDRRQE[1]	X
Bit 0	R/W	RPDRRQE[0]	X

RPDRRQE[15:0]:
The RPDRRQE[15:0] bits define bits 17 to 2 of the Receive Packet Descriptor Reference Ready Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the RPDRR queue, the RPDRRQE bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.21 Register 0x350: PCID Rx Management Descriptor Reference Free Queue Start

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRFQS[15]	X
Bit 14	R/W	RMDRFQS[14]	X
Bit 13	R/W	RMDRFQS[13]	X
Bit 12	R/W	RMDRFQS[12]	X
Bit 11	R/W	RMDRFQS[11]	X
Bit 10	R/W	RMDRFQS[10]	X
Bit 9	R/W	RMDRFQS[9]	X
Bit 8	R/W	RMDRFQS[8]	X
Bit 7	R/W	RMDRFQS[7]	X
Bit 6	R/W	RMDRFQS[6]	X
Bit 5	R/W	RMDRFQS[5]	X
Bit 4	R/W	RMDRFQS[4]	X
Bit 3	R/W	RMDRFQS[3]	X
Bit 2	R/W	RMDRFQS[2]	X
Bit 1	R/W	RMDRFQS[1]	X
Bit 0	R/W	RMDRFQS[0]	X

RMDRFQS[15:0]:
The RMDRFQS[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Free Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the RMDRF queue, the RMDRFQS bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.22 Register 0x354: PCID Rx Management Descriptor Reference Free Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRFQW[15]	X
Bit 14	R/W	RMDRFQW[14]	X
Bit 13	R/W	RMDRFQW[13]	X
Bit 12	R/W	RMDRFQW[12]	X
Bit 11	R/W	RMDRFQW[11]	X
Bit 10	R/W	RMDRFQW[10]	X
Bit 9	R/W	RMDRFQW[9]	X
Bit 8	R/W	RMDRFQW[8]	X
Bit 7	R/W	RMDRFQW[7]	X
Bit 6	R/W	RMDRFQW[6]	X
Bit 5	R/W	RMDRFQW[5]	X
Bit 4	R/W	RMDRFQW[4]	X
Bit 3	R/W	RMDRFQW[3]	X
Bit 2	R/W	RMDRFQW[2]	X
Bit 1	R/W	RMDRFQW[1]	X
Bit 0	R/W	RMDRFQW[0]	X

RMDRFQW[15:0]:
The RMDRFQW[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Free Queue Write pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical write pointer address of the RMDRF queue, the RMDRFQW bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.23 Register 0x358: PCID Rx Management Descriptor Reference Free Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRFQR[15]	X
Bit 14	R/W	RMDRFQR[14]	X
Bit 13	R/W	RMDRFQR[13]	X
Bit 12	R/W	RMDRFQR[12]	X
Bit 11	R/W	RMDRFQR[11]	X
Bit 10	R/W	RMDRFQR[10]	X
Bit 9	R/W	RMDRFQR[9]	X
Bit 8	R/W	RMDRFQR[8]	X
Bit 7	R/W	RMDRFQR[7]	X
Bit 6	R/W	RMDRFQR[6]	X
Bit 5	R/W	RMDRFQR[5]	X
Bit 4	R/W	RMDRFQR[4]	X
Bit 3	R/W	RMDRFQR[3]	X
Bit 2	R/W	RMDRFQR[2]	X
Bit 1	R/W	RMDRFQR[1]	X
Bit 0	R/W	RMDRFQR[0]	X

RMDRFQR[15:0]:
The RMDRFQR[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Free Queue Read pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical read pointer address of the RMDRF queue, the RMDRFQR bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.24 Register 0x35C: PCID Rx Management Descriptor Reference Free Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRFQE[15]	X
Bit 14	R/W	RMDRFQE[14]	X
Bit 13	R/W	RMDRFQE[13]	X
Bit 12	R/W	RMDRFQE[12]	X
Bit 11	R/W	RMDRFQE[11]	X
Bit 10	R/W	RMDRFQE[10]	X
Bit 9	R/W	RMDRFQE[9]	X
Bit 8	R/W	RMDRFQE[8]	X
Bit 7	R/W	RMDRFQE[7]	X
Bit 6	R/W	RMDRFQE[6]	X
Bit 5	R/W	RMDRFQE[5]	X
Bit 4	R/W	RMDRFQE[4]	X
Bit 3	R/W	RMDRFQE[3]	X
Bit 2	R/W	RMDRFQE[2]	X
Bit 1	R/W	RMDRFQE[1]	X
Bit 0	R/W	RMDRFQE[0]	X

RMDRFQE[15:0]:
The RMDRFQE[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Free Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the RMDRF queue, the RMDRFQE bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.25 Register 0x360: PCID Rx Management Descriptor Reference Ready Queue Start

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRRQS[15]	X
Bit 14	R/W	RMDRRQS[14]	X
Bit 13	R/W	RMDRRQS[13]	X
Bit 12	R/W	RMDRRQS[12]	X
Bit 11	R/W	RMDRRQS[11]	X
Bit 10	R/W	RMDRRQS[10]	X
Bit 9	R/W	RMDRRQS[9]	X
Bit 8	R/W	RMDRRQS[8]	X
Bit 7	R/W	RMDRRQS[7]	X
Bit 6	R/W	RMDRRQS[6]	X
Bit 5	R/W	RMDRRQS[5]	X
Bit 4	R/W	RMDRRQS[4]	X
Bit 3	R/W	RMDRRQS[3]	X
Bit 2	R/W	RMDRRQS[2]	X
Bit 1	R/W	RMDRRQS[1]	X
Bit 0	R/W	RMDRRQS[0]	X

RMDRRQS[15:0]:
The RMDRRQS[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Ready Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the RMDRR queue, the RMDRRQS bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.26 Register 0x364: PCID Rx Management Descriptor Reference Ready Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRRQW[15]	X
Bit 14	R/W	RMDRRQW[14]	X
Bit 13	R/W	RMDRRQW[13]	X
Bit 12	R/W	RMDRRQW[12]	X
Bit 11	R/W	RMDRRQW[11]	X
Bit 10	R/W	RMDRRQW[10]	X
Bit 9	R/W	RMDRRQW[9]	X
Bit 8	R/W	RMDRRQW[8]	X
Bit 7	R/W	RMDRRQW[7]	X
Bit 6	R/W	RMDRRQW[6]	X
Bit 5	R/W	RMDRRQW[5]	X
Bit 4	R/W	RMDRRQW[4]	X
Bit 3	R/W	RMDRRQW[3]	X
Bit 2	R/W	RMDRRQW[2]	X
Bit 1	R/W	RMDRRQW[1]	X
Bit 0	R/W	RMDRRQW[0]	X

RMDRRQW[15:0]:
The RMDRRQW[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Ready Queue Write pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical write pointer address of the RMDRR queue, the RMDRRQW bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.27 Register 0x368: PCID Rx Management Descriptor Reference Ready Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRRQR[15]	X
Bit 14	R/W	RMDRRQR[14]	X
Bit 13	R/W	RMDRRQR[13]	X
Bit 12	R/W	RMDRRQR[12]	X
Bit 11	R/W	RMDRRQR[11]	X
Bit 10	R/W	RMDRRQR[10]	X
Bit 9	R/W	RMDRRQR[9]	X
Bit 8	R/W	RMDRRQR[8]	X
Bit 7	R/W	RMDRRQR[7]	X
Bit 6	R/W	RMDRRQR[6]	X
Bit 5	R/W	RMDRRQR[5]	X
Bit 4	R/W	RMDRRQR[4]	X
Bit 3	R/W	RMDRRQR[3]	X
Bit 2	R/W	RMDRRQR[2]	X
Bit 1	R/W	RMDRRQR[1]	X
Bit 0	R/W	RMDRRQR[0]	X

RMDRRQR[15:0]:
The RMDRRQR[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Ready Queue Read pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical read pointer address of the RMDRR queue, the RMDRRQR bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.28 Register 0x36C: PCID Rx Management Descriptor Reference Ready Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	RMDRRQE[15]	X
Bit 14	R/W	RMDRRQE[14]	X
Bit 13	R/W	RMDRRQE[13]	X
Bit 12	R/W	RMDRRQE[12]	X
Bit 11	R/W	RMDRRQE[11]	X
Bit 10	R/W	RMDRRQE[10]	X
Bit 9	R/W	RMDRRQE[9]	X
Bit 8	R/W	RMDRRQE[8]	X
Bit 7	R/W	RMDRRQE[7]	X
Bit 6	R/W	RMDRRQE[6]	X
Bit 5	R/W	RMDRRQE[5]	X
Bit 4	R/W	RMDRRQE[4]	X
Bit 3	R/W	RMDRRQE[3]	X
Bit 2	R/W	RMDRRQE[2]	X
Bit 1	R/W	RMDRRQE[1]	X
Bit 0	R/W	RMDRRQE[0]	X

RMDRRQE[15:0]:
The RMDRRQE[15:0] bits define bits 17 to 2 of the Receive Management Descriptor Reference Ready Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the RMDRR queue, the RMDRRQE bits are added to the RQB field in the PCID Rx Queue Base register.

10.4.29 Register 0x378: PCID Tx Descriptor Table Base

Bit	Type	Function	Default
Bit 31 to Bit 0	R/W	TDTB[31:0]	XXXXXXXXH

TDTB[31:0]:
The TDTB[31:0] bits define the base of the Transmit Descriptor Table. These registers are initialized by the PCI Host. To calculate the physical address of a TD, the 14 bit TD offset must be added to bits 31 to 5 of the PCID Transmit Descriptor Table Base (TDTB[31:5]).

The table must be on a 32 byte boundary and thus the least significant 5 bits must be written to logic 0.

10.4.30 Register 0x37C: PCID Tx Queue Base

Bit	Type	Function	Default
Bit 31 to Bit 0	R/W	TQB[31:0]	XXXXXXXXH

TQB[31:0]:
The TQB[31:0] bits define the base address for the Transmit Descriptor Reference Free and Transmit Descriptor Reference Ready queue addresses. This register is initialized by the PCI Host. To calculate the physical address of a particular transmit queue element, the TQB bits are added to the appropriate queue start, end, read or write pointers to form the physical address.

The base address must be DWORD aligned and thus the least significant 2 bits must be written to logic 0.

10.4.31 Register 0x380: PCID Tx Descriptor Reference Free Queue Start

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRFQS[15]	X
Bit 14	R/W	TDRFQS[14]	X
Bit 13	R/W	TDRFQS[12]	X
Bit 12	R/W	TDRFQS[13]	X
Bit 11	R/W	TDRFQS[11]	X
Bit 10	R/W	TDRFQS[10]	X
Bit 9	R/W	TDRFQS[9]	X
Bit 8	R/W	TDRFQS[8]	X
Bit 7	R/W	TDRFQS[7]	X
Bit 6	R/W	TDRFQS[6]	X
Bit 5	R/W	TDRFQS[5]	X
Bit 4	R/W	TDRFQS[4]	X
Bit 3	R/W	TDRFQS[3]	X
Bit 2	R/W	TDRFQS[2]	X
Bit 1	R/W	TDRFQS[1]	X
Bit 0	R/W	TDRFQS[0]	X

TDRFQS[15:0]:
The TDRFQS[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Free Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the TDRF queue, the TDRFQS bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.32 Register 0x384: PCID Tx Descriptor Reference Free Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRFQW[15]	X
Bit 14	R/W	TDRFQW[14]	X
Bit 13	R/W	TDRFQW[13]	X
Bit 12	R/W	TDRFQW[12]	X
Bit 11	R/W	TDRFQW[11]	X
Bit 10	R/W	TDRFQW[10]	X
Bit 9	R/W	TDRFQW[9]	X
Bit 8	R/W	TDRFQW[8]	X
Bit 7	R/W	TDRFQW[7]	X
Bit 6	R/W	TDRFQW[6]	X
Bit 5	R/W	TDRFQW[5]	X
Bit 4	R/W	TDRFQW[4]	X
Bit 3	R/W	TDRFQW[3]	X
Bit 2	R/W	TDRFQW[2]	X
Bit 1	R/W	TDRFQW[1]	X
Bit 0	R/W	TDRFQW[0]	X

TDRFQW[15:0]:
The TDRFQW[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Free Queue Write pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical write pointer address of the TDRF queue, the TDRFQW bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.33 Register 0x388: PCID Tx Descriptor Reference Free Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRFQR[15]	X
Bit 14	R/W	TDRFQR[14]	X
Bit 13	R/W	TDRFQR[13]	X
Bit 12	R/W	TDRFQR[12]	X
Bit 11	R/W	TDRFQR[11]	X
Bit 10	R/W	TDRFQR[10]	X
Bit 9	R/W	TDRFQR[9]	X
Bit 8	R/W	TDRFQR[8]	X
Bit 7	R/W	TDRFQR[7]	X
Bit 6	R/W	TDRFQR[6]	X
Bit 5	R/W	TDRFQR[5]	X
Bit 4	R/W	TDRFQR[4]	X
Bit 3	R/W	TDRFQR[3]	X
Bit 2	R/W	TDRFQR[2]	X
Bit 1	R/W	TDRFQR[1]	X
Bit 0	R/W	TDRFQR[0]	X

TDRFQR[15:0]:
The TDRFQR[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Free Queue Read pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical read pointer address of the TDRF queue, the TDRFQR bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.34 Register 0x38C: PCID Tx Descriptor Reference Free Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRFQE[15]	X
Bit 14	R/W	TDRFQE[14]	X
Bit 13	R/W	TDRFQE[13]	X
Bit 12	R/W	TDRFQE[12]	X
Bit 11	R/W	TDRFQE[11]	X
Bit 10	R/W	TDRFQE[10]	X
Bit 9	R/W	TDRFQE[9]	X
Bit 8	R/W	TDRFQE[8]	X
Bit 7	R/W	TDRFQE[7]	X
Bit 6	R/W	TDRFQE[6]	X
Bit 5	R/W	TDRFQE[5]	X
Bit 4	R/W	TDRFQE[4]	X
Bit 3	R/W	TDRFQE[3]	X
Bit 2	R/W	TDRFQE[2]	X
Bit 1	R/W	TDRFQE[1]	X
Bit 0	R/W	TDRFQE[0]	X

TDRFQE[15:0]:
The TDRFQE[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Free Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the TDRF queue, the TDRFQE bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.35 Register 0x390: PCID Tx Descriptor Reference High Priority Ready Queue Start

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRHRQS[15]	X
Bit 14	R/W	TDRHRQS[14]	X
Bit 13	R/W	TDRHRQS[13]	X
Bit 12	R/W	TDRHRQS[12]	X
Bit 11	R/W	TDRHRQS[11]	X
Bit 10	R/W	TDRHRQS[10]	X
Bit 9	R/W	TDRHRQS[9]	X
Bit 8	R/W	TDRHRQS[8]	X
Bit 7	R/W	TDRHRQS[7]	X
Bit 6	R/W	TDRHRQS[6]	X
Bit 5	R/W	TDRHRQS[5]	X
Bit 4	R/W	TDRHRQS[4]	X
Bit 3	R/W	TDRHRQS[3]	X
Bit 2	R/W	TDRHRQS[2]	X
Bit 1	R/W	TDRHRQS[1]	X
Bit 0	R/W	TDRHRQS[0]	X

TDRHRQS[15:0]:
The TDRHRQS[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference High Priority Ready Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the TDRHR queue, the TDRHRQS bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.36 Register 0x394: PCID Tx Descriptor Reference High Priority Ready Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRHRQW[15]	X
Bit 14	R/W	TDRHRQW[14]	X
Bit 13	R/W	TDRHRQW[13]	X
Bit 12	R/W	TDRHRQW[12]	X
Bit 11	R/W	TDRHRQW[11]	X
Bit 10	R/W	TDRHRQW[10]	X
Bit 9	R/W	TDRHRQW[9]	X
Bit 8	R/W	TDRHRQW[8]	X
Bit 7	R/W	TDRHRQW[7]	X
Bit 6	R/W	TDRHRQW[6]	X
Bit 5	R/W	TDRHRQW[5]	X
Bit 4	R/W	TDRHRQW[4]	X
Bit 3	R/W	TDRHRQW[3]	X
Bit 2	R/W	TDRHRQW[2]	X
Bit 1	R/W	TDRHRQW[1]	X
Bit 0	R/W	TDRHRQW[0]	X

TDRHRQW[15:0]:
The TDRHRQW[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference High Priority Ready Queue Write pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical write pointer address of the TDRHR queue, the TDRHRQW bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.37 Register 0x398: PCID Tx Descriptor Reference High Priority Ready Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRHRQR[15]	X
Bit 14	R/W	TDRHRQR[14]	X
Bit 13	R/W	TDRHRQR[13]	X
Bit 12	R/W	TDRHRQR[12]	X
Bit 11	R/W	TDRHRQR[11]	X
Bit 10	R/W	TDRHRQR[10]	X
Bit 9	R/W	TDRHRQR[9]	X
Bit 8	R/W	TDRHRQR[8]	X
Bit 7	R/W	TDRHRQR[7]	X
Bit 6	R/W	TDRHRQR[6]	X
Bit 5	R/W	TDRHRQR[5]	X
Bit 4	R/W	TDRHRQR[4]	X
Bit 3	R/W	TDRHRQR[3]	X
Bit 2	R/W	TDRHRQR[2]	X
Bit 1	R/W	TDRHRQR[1]	X
Bit 0	R/W	TDRHRQR[0]	X

TDRHRQR[15:0]:
The TDRHRQR[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference High Priority Ready Queue Read pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical read pointer address of the TDRHR queue, the TDRHRQR bits are added to the TQB field in the PCID Tx Queue Base register.

10.4.38 Register 0x39C: PCID Tx Descriptor Reference High Priority Ready Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRHRQE[15]	X
Bit 14	R/W	TDRHRQE[14]	X
Bit 13	R/W	TDRHRQE[13]	X
Bit 12	R/W	TDRHRQE[12]	X
Bit 11	R/W	TDRHRQE[11]	X
Bit 10	R/W	TDRHRQE[10]	X
Bit 9	R/W	TDRHRQE[9]	X
Bit 8	R/W	TDRHRQE[8]	X
Bit 7	R/W	TDRHRQE[7]	X
Bit 6	R/W	TDRHRQE[6]	X
Bit 5	R/W	TDRHRQE[5]	X
Bit 4	R/W	TDRHRQE[4]	X
Bit 3	R/W	TDRHRQE[3]	X
Bit 2	R/W	TDRHRQE[2]	X
Bit 1	R/W	TDRHRQE[1]	X
Bit 0	R/W	TDRHRQE[0]	X

TDRHRQE[15:0]:
The TDRHRQE[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference High Priority Ready Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the TDRHR queue, the TDRHRQE bits are added with the TQB field in the PCID Tx Queue Base register.

10.4.39 Register 0x3A0: PCID Tx Descriptor Reference Low Priority Ready Queue Start

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRLRQS[15]	X
Bit 14	R/W	TDRLRQS[14]	X
Bit 13	R/W	TDRLRQS[13]	X
Bit 12	R/W	TDRLRQS[12]	X
Bit 11	R/W	TDRLRQS[11]	X
Bit 10	R/W	TDRLRQS[10]	X
Bit 9	R/W	TDRLRQS[9]	X
Bit 8	R/W	TDRLRQS[8]	X
Bit 7	R/W	TDRLRQS[7]	X
Bit 6	R/W	TDRLRQS[6]	X
Bit 5	R/W	TDRLRQS[5]	X
Bit 4	R/W	TDRLRQS[4]	X
Bit 3	R/W	TDRLRQS[3]	X
Bit 2	R/W	TDRLRQS[2]	X
Bit 1	R/W	TDRLRQS[1]	X
Bit 0	R/W	TDRLRQS[0]	X

TDRLRQS[15:0]:
The TDRLRQS[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Low Priority Ready Queue Start address. This register is initialized by the PCI Host. To calculate the physical start address of the TDRLR queue, the TDRLRQS bits are added with the TQB field in the PCID Tx Queue Base register.

10.4.40 Register 0x3A4: PCID Tx Descriptor Reference Low Priority Ready Queue Write

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRLRQW[15]	X
Bit 14	R/W	TDRLRQW[14]	X
Bit 13	R/W	TDRLRQW[13]	X
Bit 12	R/W	TDRLRQW[12]	X
Bit 11	R/W	TDRLRQW[11]	X
Bit 10	R/W	TDRLRQW[10]	X
Bit 9	R/W	TDRLRQW[9]	X
Bit 8	R/W	TDRLRQW[8]	X
Bit 7	R/W	TDRLRQW[7]	X
Bit 6	R/W	TDRLRQW[6]	X
Bit 5	R/W	TDRLRQW[5]	X
Bit 4	R/W	TDRLRQW[4]	X
Bit 3	R/W	TDRLRQW[3]	X
Bit 2	R/W	TDRLRQW[2]	X
Bit 1	R/W	TDRLRQW[1]	X
Bit 0	R/W	TDRLRQW[0]	X

TDRLRQW[15:0]:
The TDRLRQW[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Low Priority Ready Queue Write pointer address. This registers is initialized and updated by the PCI Host. To calculate the physical write pointer address of the TDRLR queue, the TDRLRQW bits are added with the TQB field in the PCID Tx Queue Base register.

10.4.41 Register 0x3A8: PCID Tx Descriptor Reference Low Priority Ready Queue Read

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRLRQR[15]	X
Bit 14	R/W	TDRLRQR[14]	X
Bit 13	R/W	TDRLRQR[13]	X
Bit 12	R/W	TDRLRQR[12]	X
Bit 11	R/W	TDRLRQR[11]	X
Bit 10	R/W	TDRLRQR[10]	X
Bit 9	R/W	TDRLRQR[9]	X
Bit 8	R/W	TDRLRQR[8]	X
Bit 7	R/W	TDRLRQR[7]	X
Bit 6	R/W	TDRLRQR[6]	X
Bit 5	R/W	TDRLRQR[5]	X
Bit 4	R/W	TDRLRQR[4]	X
Bit 3	R/W	TDRLRQR[3]	X
Bit 2	R/W	TDRLRQR[2]	X
Bit 1	R/W	TDRLRQR[1]	X
Bit 0	R/W	TDRLRQR[0]	X

TDRLRQR[15:0]:
The TDRLRQR[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Low Priority Ready Queue Read pointer address. This registers is initialized by the PCI Host and updated by the LASAR-155. To calculate the physical read pointer address of the TDRLR queue, the TDRLRQR bits are added with the TQB field in the PCID Tx Queue Base register.

10.4.42 Register 0x3AC: PCID Tx Descriptor Reference Low Priority Ready Queue End

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R/W	TDRLRQE[15]	X
Bit 14	R/W	TDRLRQE[14]	X
Bit 13	R/W	TDRLRQE[13]	X
Bit 12	R/W	TDRLRQE[12]	X
Bit 11	R/W	TDRLRQE[11]	X
Bit 10	R/W	TDRLRQE[10]	X
Bit 9	R/W	TDRLRQE[9]	X
Bit 8	R/W	TDRLRQE[8]	X
Bit 7	R/W	TDRLRQE[7]	X
Bit 6	R/W	TDRLRQE[6]	X
Bit 5	R/W	TDRLRQE[5]	X
Bit 4	R/W	TDRLRQE[4]	X
Bit 3	R/W	TDRLRQE[3]	X
Bit 2	R/W	TDRLRQE[2]	X
Bit 1	R/W	TDRLRQE[1]	X
Bit 0	R/W	TDRLRQE[0]	X

TDRLRQE[15:0]:
The TDRLRQE[15:0] bits define bits 17 to 2 of the Transmit Descriptor Reference Low Priority Ready Queue End address. This register is initialized by the PCI Host. To calculate the physical end address of the TDRLR queue, the TDRLRQE bits are added with the TQB field in the PCID Tx Queue Base register.

10.4.43 Register 0x3B0: PCID Max Tx SDU Length

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15 to Bit 0	R/W	MTSDU[15:0]	FFFFH

MTSDU[15:0]:
MTSDU[15:0] represents the user programmable maximum length of the transmit CPAAL5 Service Protocol Unit (SDU) in bytes. If the PCI Host presents a CPAAL5_SDU that exceeds the maximum, the LASAR-155 will indicate an error via an interrupt bit and return the CPAAL5_SDU to the PCI Host on the Transmit Descriptor Reference Free Queue immediately.

10.4.44 Register 0x3B4: PCID RAS and TAS FIFO Pointers

Bit	Type	Function	Default
Bit 31 to Bit 20		Unused	XXXH
Bit 19 to Bit 17	R	TWPTR[2:0]	XH
Bit 16 to Bit 14	R	TRPTR[2:0]	XH
Bit 13 to Bit 7	R	RWPTR[6:0]	XXH
Bit 6 to Bit 0	R	RRPTR[6:0]	XXH

RRPTR[6:0]:
The RAS FIFO Read Pointer (RRPTR) bits specify the value of the RAS FIFO Read pointer in units of cells. When a read is made to this register, the current value of the RAS FIFO Read pointer is latched. The RRPTR is advanced for each cell read from the RAS FIFO.

RWPTR[6:0]:
The RAS FIFO Write Pointer (RWPTR) bits specify the value of the RAS FIFO Write pointer in units of cells. When a read is made to this register, the current value of the RAS FIFO Write pointer is latched. The RWPTR is not advanced for the first cell written into the RAS FIFO, thereafter, it is advanced for each cell written into the RAS FIFO.

TRPTR[2:0]:
The TAS FIFO Read Pointer (TRPTR) bits specify the value of the TAS FIFO Read pointer in units of cells. When a read is made to this register, the current value of the TAS FIFO Read pointer is latched. The TRPTR is advanced before the first available cell is read from the TAS FIFO, thereafter, it is advanced for each cell read from the TAS FIFO.

TWPTR[2:0]:
The TAS FIFO Write Pointer (TWPTR) bits specify the value of the TAS FIFO

Write pointer in units of cells. When a read is made to this register, the current value of the TAS FIFO Write pointer is latched. The TWPTR is advanced for each cell written to the TAS FIFO.

10.4.45 Register 0x3C8: PCID RAM Indirect Control

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15	R	BUSY	X
Bit 14	R/W	RD/WRB	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11 to Bit 2	R/W	IRADDR[11:2]	000H
Bit 1		Unused	X
Bit 0		Unused	X

The PCID RAM Indirect Control register can be used to access the internal RAMs of the PCID block. A write to this register cause either an indirect write or read to the internal location specified by the IRADDR[11:2] field. This register should not be accessed by users. This register can only be used to access the PCID internal memory when a local microprocessor is not present in the system (MPENB = 1).

IRADDR[11:2]:
The IRADDR[11:2] bits are used to indirectly address PCID RAM locations. Only the DWORD address of each RAM needs to be specified. IRADDR[1:0] is always set to 00b. The PCID RAM memory map is described below.

Address	Description
0x000 - 0x3FF	Reserved. Accesses should not be made to this address space. When accesses are made, the BUSY bit is set but not cleared.
0x400 - 0x7FC	Receive VC Descriptor Reference Table
0x800 - 0xFFC	Transmit VC Descriptor Reference Table

RD/WRB:
The RD/WRB bit selects whether to initiate an indirect read from or an indirect write to PCID RAM location when a write is performed on this register. When

RD/WRB is set to logic one, a read is performed. When RD/WRB is set to logic zero, a write is performed.

BUSY:
The BUSY bit indicates when an access is in progress. When busy is logic one, a read or write PCID RAM access is in progress. When BUSY is logic zero, the previous access has completed.

10.4.46 Register 0x3CC: PCID RAM Indirect Data Low Word

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15 to Bit 0	R/W	IRDATA[15:0]	0000H

IRDATA[15:0]:
The IRDATA[15:0] bits form the low word of the IRDATA[31:0] field.

10.4.47 Register 0x3D0: PCID RAM Indirect Data High Word

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15 to Bit 0	R/W	IRDATA[31:16]	0000H

IRDATA[31:16]:
The IRDATA[31:16] bits form the high word of the IRDATA[31:0] field.

IRDATA[31:0] reports the data read from a PCID memory location after an indirect read operation has completed. The data to be written to a PCID memory location must be set up in these registers before an indirect write operation. Data read from these registers reflects the value written until the completion of a subsequent indirect read operation.

Each element in the transmit descriptor table consists of three 32-bit words and each element in the receive packet descriptor table consists of two 32-bit words. It is possible to access a table entry while the indirect interface is modifying or reading the same entry. The programmer must therefore exercise caution when accessing these tables through the indirect data registers.

10.4.48 Register 0x3D4: PCID Host Write Mailbox Control

Bit	Type	Function	Default
Bit 31 to Bit 14		Unused	XXH
Bit 13 to Bit 8	R/W	HWA[5:0]	00H
Bit 7 to Bit 1		Unused	XXH
Bit 0	R/W	MASTER	0

MASTER:
The MASTER bit is used to indicate the current master of the PCI Host to microprocessor mailbox. When set to logic one, the microprocessor is the master, When set to logic zero, the PCI Host is the master.

After the PCI Host has filled the PCI Host to microprocessor with a message, the PCI Host should set MASTER to logic one to enable microprocessor mailbox reads. When the microprocessor has completed its accesses, it will set the MASTER bit to logic zero to return the control of the mailbox to the PCI Host . An interrupt can be generated using the PTOMPE bit in the PCID Mailbox/Microprocessor Interrupt Status/Enable register.

If for some reason the PCI Host must obtain control of the PCI Host to microprocessor mailbox when the microprocessor is the master, the PCI Host can take control of the mailbox by setting the MASTER bit to logic zero. This action is not recommended.

HWA[5:0]:
The HWA[5:0] bits specify the start address of the PCI Host to microprocessor mailbox location the PCI Host wishes to access. HWA[5:0] is automatically post incremented after every write to or read from the PCID Host Write Mailbox Data register. If the address reaches its limit, it wraps around to the start of the mailbox. The HWA_ROI bit in the PCID Mailbox/Microprocessor Interrupt Status/Enable register will be set high if this occurs.

10.4.49 Register 0x3D8: PCID Host Write Mailbox Data

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15 to Bit 0	R/W	HWD[15:0]	XXXXH

HWD[15:0]:
The HWD[15:0] bits are used to write data to or read data from the PCI Host to microprocessor mailbox. The mailbox location is specified using the HWA value in the PCID Host Write Mailbox Control register. To allow burst mailbox accesses, HWA is automatically post incremented after every access.

10.4.50 Register 0x3E0: PCID Host Read Mailbox Control

Bit	Type	Function	Default
Bit 31 to Bit 14		Unused	XXXXH
Bit 13 to Bit 8	R/W	HRA[5:0]	00H
Bit 7 to Bit 1		Unused	XXH
Bit 0	R/W	MASTER	1

MASTER:
The MASTER bit is used to indicate the current master of the microprocessor to PCI Host mailbox. When set to logic one, the microprocessor is the master, When set to logic zero, the PCI Host is the master. Note, the PCI Host cannot set this bit low. It can only force this bit high.

The MASTER bit will be set low by the microprocessor to indicate that the PCI Host can access the mailbox for reads. The MASTER bit is set high by the PCI Host to return control of the mailbox to the microprocessor.

If for some reason the microprocessor takes control of the microprocessor to PCI Host mailbox when the PCI Host is the master, the PCI Host is alerted using the MPTOP_ORI bit in the PCID Mailbox/Microprocessor Interrupt Status/Enable register.

HRA[5:0]:
The HRA[5:0] bits specify the address of the microprocessor to PCI Host mailbox location the PCI Host wishes to read from. HRA[5:0] is automatically post incremented after every read of the PCID Host Read Mailbox Data register. If the address reaches its limit, it wraps around to the start of the mailbox. The HRA_ROI bit in the PCID Mailbox/Microprocessor Interrupt Status/Enable register will be set high if this occurs.

10.4.51 Register 0x3E4: PCID Host Read Mailbox Data

Bit	Type	Function	Default
Bit 31 to Bit 16		Unused	XXXXH
Bit 15 to Bit 0	R	HRD[15:0]	XXXXH

HRD[15:0]:
The HRD[15:0] bits are used to read data from the microprocessor to PCI Host mailbox. The mailbox location is specified using the HRA value in the PCID Host Read Mailbox Control register. To allow burst mailbox reads, HRA is automatically post incremented after every read.

11 PCI CONFIGURATION REGISTER DESCRIPTIONS

The following PCI configuration registers are implemented by the PCI Interface. These registers can only be accessed when the PCI Interface is a target and a configuration cycle is in progress as indicated using the IDSEL input.

11.1.1 PCI Configuration Register Memory Map

Register	Address	Description
0x00	0x00	Vendor Identification / Device Identification
0x01	0x04	Command / Status
0x02	0x08	Revision Identifier / Class Code
0x03	0x0C	Cache Line Size / Latency Timer / BIST / Header Type
0x04	0x10	LASAR-155 Memory Base Address Register
0x05	0x14	External Device Memory Base Address Register
0x06	0x18	Unused Base Address Register
0x07	0x1C	Unused Base Address Register
0x08	0x20	Unused Base Address Register
0x09	0x24	Unused Base Address Register
0x0A	0x28	Reserved
0x0B	0x2C	Reserved
0x0C	0x30	Expansion ROM Base Address Register
0x0D	0x34	Reserved
0x0E	0x38	Reserved
0x0F	0x3C	Interrupt Lines / Interrupt Pins / MIN_GNT / MAX_LAT

11.1.2 Register 0x00 (0x00): Vendor Identification / Device Identification

Bit	Type	Function	Default
Bit 31 to Bit 16	R	DEVID[15:0]	7375H
Bit 15 to Bit 0	R	VNDRID[15:0]	11F8H

VNDRID[15:0]:
The VNDRID[15:0] bits define the manufacturer of the device.

DEVID[15:0]:
The DEVID[15:0] bits contain the LASAR-155's device identification code, 7375H.

11.1.3 Register 0x01 (0x04): Command / Status

Bit	Type	Function	Default
Bit 31	R/W	PERR	0
Bit 30	R/W	SERR	0
Bit 29	R/W	MABT	0
Bit 28	R/W	RTABT	0
Bit 27	R/W	TABT	0
Bit 26	R	DVSLT[1]	0
Bit 25	R	DVSLT[0]	1
Bit 24	R/W	DPR	0
Bit 23	R	FBTBE	1
Bit 22 to Bit 16	R	Reserved	00H
Bit 15 to Bit 10	R	Reserved	00H
Bit 9	R	FBTBEN	0
Bit 8	R/W	SERREN	0
Bit 7	R	ADSTP	0
Bit 6	R/W	PERREN	0
Bit 5	R	VGASNP	0
Bit 4	R	MWAI	0
Bit 3	R	SPCEN	0
Bit 2	R/W	MSTREN	0
Bit 1	R/W	MCNTRL	0
Bit 0	R	IOCNTRL	0

The lower 16 bits of this register are the PCI Command register. The PCI Command register provides basic control over the LASAR-155's ability to respond to PCI accesses.

The upper 16 bits of this register are the PCI Status register. The PCI Status register tracks the status of PCI bus related events. Reads to the Status register behave normally. Writes to the Status register are slightly different in that bits can be reset, but not set. A bit is reset whenever the Status register is written, and the data in the corresponding bit location is a one.

IOCNTRL:
IOCNTRL is set to zero. The LASAR-155 device does not support I/O accesses.

MCNTRL:
When MCNTRL is set to one, the LASAR-155 shall respond to PCI bus memory accesses. Clearing MCNTRL disables memory accesses.

MSTREN:
When MSTREN is set to one, the LASAR-155 can act as an initiator. Clearing MSTREN disables the LASAR-155 from becoming an initiator.

SPCEN:
The LASAR-155 does not decode PCI special cycles; therefore the SPCEN bit is forced low.

MWAI:
The LASAR-155 does not generate memory write and invalidate commands; therefore the MWAI bit is forced low.

VGASNP:
The LASAR-155 is not a VGA device; therefore the VGASNP bit is forced low.

PERREN:
When the PERREN bit is set to one, the LASAR-155 can report parity errors. Clearing the PERREN bit causes the LASAR-155 to ignore parity errors.

ADSTP:
The LASAR-155 does not perform address and data stepping; therefore the ADSTP bit is forced low.

SERREN:
When the SERREN bit is set high, the LASAR-155 can drive the SERRB line. Clearing the SERREN bit disables the SERRB line. SERREN and PERREN must be set to report an address parity error.

FBTBEN:
As an Initiator, the LASAR-155 does not generate fast back-to-back cycles; therefore the FBTBEN bit is forced low.

FBTBE:
The FBTBE bit shall be hardwired to one to indicate the LASAR-155 does support fast back-to-back transactions with other targets.

DPR:
The Data Parity Reported (DPR) bit is set high, if the LASAR-155 is an initiator and asserted or detected a parity error on the PERRB signal while the PERREN bit is set in the Command register. The DPR bit shall be cleared by the PCI Host.

DVSLT[1:0]:
The device select timing (DEVSLT) bits specify the allowable timings for the assertion of DEVSELB by the LASAR-155. The encodings are 00B for fast, 01B for medium, 10B for slow and 11B is not used. The LASAR-155 allows for medium timing.

TABT:
The target abort (TABT) bit set high by the LASAR-155 whenever it terminates a transaction with a target abort. The TABT bit shall be cleared by the PCI Host.

RTABT:
The received target abort (RTABT) bit is set high by the LASAR-155 when it is the initiator and its transaction is terminated by a target abort. The RTABT bit shall be cleared by the PCI Host.

MABT:
The master abort (MABT) bit is set high by the LASAR-155 when it is an initiator and its transaction is terminated by a master abort and a special cycle was not in progress. The MABT bit shall be cleared by the PCI Host.

SERR:
The System Error (SERR) bit is set high whenever the PCID asserts the SERRB output. The SERR bit shall be cleared by the PCI Host.

PERR:
The Parity Error (PERR) bit is set high whenever the PCID detects a parity error, even if parity error handling is disabled by clearing PERREN bit in the Command register. The PERR bit shall be cleared by the PCI Host.

11.1.4 Register 0x02 (0x08): Revision Identifier / Class Code

Bit	Type	Function	Default
Bit 31 to Bit 24	R	CCODE[23:16]	02H
Bit 23 to Bit 16	R	CCODE[15:8]	03H
Bit 15 to Bit 8	R	CCODE[7:0]	00H
Bit 7 to Bit 0	R	REVID[7:0]	02H

REVID[7:0]:
The revision identifier (REVID[7:0]) bits specify the LASAR-155's device specific revision identifier, 02H.

CCODE[23:0]:
The class code (CCODE[23:0]) bits are divided into three groupings: CCODE[23:16] define the base class of the device, CCODE[15:8] define the sub-class of the device and CCODE[7:0] specify a register specific programming interface.

LASAR-155 Base Class = 02H, Network Controller.

LASAR-155 Sub-class = 03H, ATM Network controller.

LASAR-155 Programming Interface = 00H, Default.

11.1.5 Register 0x03 (0x0C): Cache Line Size / Latency Timer / BIST / Header Type

Bit	Type	Function	Default
Bit 31 to Bit 24	R	Reserved	00H
Bit 23	R	MLTFNC	0
Bit 22 to Bit 16	R	HDTYPE[6:0]	00H
Bit 15 to Bit 8	R/W	LT[7:0]	00H
Bit 7 to Bit 0	R	Reserved	00H

LT[7:0]:
The latency timer (LT[7:0]) bits specify in units of the PCI clock, the value of the latency timer for the LASAR-155. At reset the value is zero.

HDTYPE[6:0]:
The header type (HDTYPE[7:0]) bits specify the layout of the base address registers. Only one encoding is supported as indicated using 00H.

MLTFNC:
The multi-function (MLTFNC) bit is set to zero to specify that the LASAR-155 supports only one function.

11.1.6 Register 0x04 (0x10): LASAR-155 Memory Base Address Register

Bit	Type	Function	Default
Bit 31 to Bit 12	R/W	BSAD[27:8]	XXXH
Bit 11 to Bit 4	R	BSAD[7:0]	00H
Bit 3	R	PRFTCH	0
Bit 2	R	TYPE[1]	0
Bit 1	R	TYPE[0]	0
Bit 0	R	MSI	0

The LASAR-155 supports memory mapping only. At boot-up the LASAR-155 internal registers are mapped to memory by the device driver. It is up to the device driver to decide which space to use and to return the unused space to the operating system. The device driver can disable the memory space through the PCI Configuration Command register.

MSI:
The memory space indicator (MSI) indicates whether the registers on the PCI Bus map into memory. MSI is forced low to indicate that the LASAR-155 supports memory mapped registers.

TYPE[1:0]:
The TYPE field indicates where the memory can be mapped. The encoding 00B indicates the memory may be located anywhere in the 32 bit address space, 01B indicates that the memory must be mapped below 1 Meg in memory space, 10B indicate the base register is 64 bits and the encoding 11B is reserved.

TYPE is set to 00B to indicate that LASAR-155 memory can be mapped anywhere in a 32 bit address space.

PRFTCH:
The prefetchable (PRFTCH) bit is set high if there are no side effects on reads and data is returned on all the lanes regardless of the byte enables. Otherwise the bit is cleared.

PREFTCH is hardwired low since the LASAR-155 can clear interrupt bits on reads. Otherwise, there are no additional side effects on reads and the LASAR-155 drives all data lanes.

BSAD[27:0]:
The Base Address (BSAD[27:0]) bits define the size and location of the memory space required for the LASAR-155. The BSAD[27:0] bits correspond to the most significant 28 bits of the PCI address space.

The size of the address space required can be determined by writing all ones to the LASAR-155 Memory Base Address register and then reading from it. By scanning the returned value from the least significant bit upwards, the size of the required address space can be determined. The binary weighted value of the first one bit found (after the configuration bits) indicates the required amount of space. The BSAD[7:0] bits are forced low to indicate that the LASAR-155 requires 4K bytes of memory space.

After determining the memory requirements of the PCID, the PCI Host can map the LASAR-155 to its desired location by modifying the BSAD[27:8] bits in the LASAR-155 Memory Base Address register.

11.1.7 Register 0x05 (0x14): External Device Memory Base Address Register

Bit	Type	Function	Default
Bit 31 to Bit 14	R/W	EAD[27:10]	XXXH
Bit 13 to Bit 4	R	EAD[9:0]	000H
Bit 3	R	PRFTCH	0
Bit 2	R	TYPE[1]	0
Bit 1	R	TYPE[0]	0
Bit 0	R	MSI	0

The LASAR-155 supports memory mapping for the devices on the LASAR-155 Local Bus. At boot-up the External device area is mapped to memory by the device driver. It is up to the device driver to decide which space to use and to return the unused space to the operating system. The device driver can disable memory space through the PCI Configuration Command register. The external memory space is only valid when the microprocessor is not present (MPENB=1). In addition, the external memory space in not visible when the Expansion ROM is enabled.

MSI:
MSI is forced low to indicate that the LASAR-155 supports memory mapped registers for the LASAR-155 Local Bus.

TYPE[1:0]:
The TYPE field indicates where the memory can be mapped. The encoding 00B indicates the memory may be located anywhere in the 32 bit address space, 01B indicates that the memory must be mapped below 1 Meg in memory space, 10B indicate the base register is 64 bits and the encoding 11B is reserved.

TYPE is set to 00B to indicate that LASAR-155 Local Bus memory can be mapped anywhere in a 32 bit address space.

PRFTCH:
The prefetchable (PRFTCH) bit is set high if there are no side effects on reads and data is returned on all the lanes regardless of the byte enables. Otherwise the bit is cleared.

PREFTCH is hardwired low since the devices on the LASAR-155 Local Bus can clear interrupt bits on reads. Otherwise, there are no additional side effects on reads and the LASAR-155 drives all data lanes.

EAD[27:0]:
The Base Address (EAD[27:0]) bits defines the size and location of the memory space required for the External device area LASAR-155 Local Bus. The EAD[27:0] bits correspond to the most significant 28 bits of the PCI address space.

The size of the address space required can be determined by writing all ones to External Device Memory Base Address register and then reading from it. By scanning the returned value form the least significant bit upwards, the size of the required address space can be determined. The binary weighted value of the first one bit found (after the configuration bits) indicates the required amount of space. The EAD[9:0] bits are forced low to indicate that the LASAR-155 Local Bus requires 16K bytes of memory space.

After determining the memory requirements of the External Device space, the PCI Host can map the area to its desired location by modifying the BSAD[27:10] bits in the External Device Memory Base Address register.

11.1.8 Register 0x0C (0x30): Expansion ROM Base Address

Bit	Type	Function	Default
Bit 31 to Bit 16	R/W	XRBS[20:5]	XXXH
Bit 15 to Bit 11	R	XRBS[4:0]	00H
Bit 10 to Bit 1	R	Reserved	000H
Bit 0	R/W	ENABLE	0

ENABLE:
The ENABLE bit determines whether the LASAR-155 accepts accesses to its Expansion ROM. When this bit is set high, the address decoding for the Expansion ROM is enabled using the base address specified in this register. The PCID can only respond to Expansion ROM accesses if it is enabled for memory accesses via the Command register. If the ENABLE bit is set low, the LASAR-155's Expansion ROM address space is disabled.

Note, after accessing the Expansion ROM, the ROM should be disabled to allow External Device Memory accesses.

XRBS[20:0]:
The Expansion ROM Base (XRBS[20:0]) bits defines the size and location of the memory space provided for an Expansion ROM . The XRBS[20:0] bits correspond to the 21 most significant bits of the PCI address space.

The size of the address space provided for the Expansion ROM can be determined by writing all ones to Expansion ROM Base Address register and then reading from it. By scanning the returned value from the least significant bit upwards, the size of the required address space can be determined. The binary weighted value of the first one bit found (after the configuration bits) indicates the required amount of space. The XRBS[4:0] bits are forced low to indicate that the LASAR-155 supports a 64K bytes Expansion ROM space.

After determining the memory requirements of the Expansion ROM, the PCI Host can map the Expansion ROM to its desired location by modifying the XRBS[20:5] bits in the Expansion ROM Base Address register.

11.1.9 Register 0x0F (0x3C): Interrupt Lines / Interrupt Pins / MIN_GNT / MAX_LAT

Bit	Type	Function	Default
Bit 31 to Bit 24	R	MAXLAT[7:0]	04H
Bit 23 to Bit 16	R	MINGNT[7:0]	02H
Bit 15 to Bit 8	R	INTPIN[7:0]	01H
Bit 7 to Bit 0	R/W	INTLNE[7:0]	00H

INTLNE[7:0]:
The interrupt line (INTLNE[7:0]) field is used to indicate interrupt line routing information. The values in this register are system specific and should be set by the PCI Host.

INTPIN[7:0]:
The interrupt pin (INTPIN[7:0]) field is used to specify the interrupt pin the LASAR-155 uses. Since the LASAR-155 shall use INTAB on the PCI bus, the value in this register is set to one.

MINGNT[7:0]:
The Minimum Grant (MINGNT[7:0]) field specifies how long of a burst period the bus master needs (in increments of 250 nsec). The value is 500 nsec.

MAXLAT[7:0]:
The Maximum Latency (MAXLAT[7:0]) field specifies how often a bus master needs access to the PCI bus (in increments of 250 nsec). The value is 1 µs.

12 TEST FEATURES DESCRIPTION

Simultaneously forcing the MPENB, CSB, RDB and WRB inputs low causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the LASAR-155. Test mode registers (as opposed to normal mode registers) are selected when MPENB is low and TRS (A[8]) is high or when MPENB is high and the PCI Host accesses LASAR-155 memory locations.

Test mode registers may also be used for board testing. When all of the blocks within the LASAR-155 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the LASAR-155 also supports a standard IEEE 1149.1 five signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port with the exception of the PECL pins and the analog pins.

12.1 Test Mode Register Memory Map

Address	Register
0x00-0xFF	Normal Mode Registers
0x100	Master Test
0x101	Analog Test Register 0
0x102-0x10D	Reserved
0x10E	GED Test Register 0
0x10F	GED Test Register 1
0x110	RSOP Test Register 0
0x111	RSOP Test Register 1
0x112	RSOP Test Register 2
0x113	RSOP Test Register 3
0x114	TSOP Test Register 0
0x115	TSOP Test Register 1
0x116	TSOP Test Register 2
0x117	TSOP Test Register 3
0x118	RLOP Test Register 0
0x119	RLOP Test Register 1

0x11A	RLOP Test Register 2
0x11B	RLOP Test Register 3
0x11C- 0x11F	Reserved
0x120	TLOP Test Register 0
0x121	TLOP Test Register 1
0x122	TLOP Test Register 2
0x123	TLOP Test Register 3
0x124- 0x12F	Reserved
0x130	RPOP Test Register 0
0x131	RPOP Test Register 1
0x132	RPOP Test Register 2
0x133	RPOP Test Register 3
0x134	RPOP Test Register 4
0x135	RPOP Test Register 5
0x136- 0x13F	Reserved
0x140	TPOP Test Register 0
0x141	TPOP Test Register 1
0x142	TPOP Test Register 2
0x143	TPOP Test Register 3
0x144	TPOP Test Register 4
0x145- 0x14F	Reserved
0x150	RACP Test Register 0
0x151	RACP Test Register 1
0x152	RACP Test Register 2
0x153	RACP Test Register 3
0x155- 0x15F	Reserved
0x160	TACP Test Register 0
0x161	TACP Test Register 1
0x162	TACP Test Register 2
0x164- 0x16F	Reserved
0x170	SAR PMON Test Register 0
0x171	SAR PMON Test Register 1
0x172- 0x17F	Reserved
0x180	RALP Test Register 0

0x181	RALP Test Register 1
0x182	RALP Test Register 2
0x183	RALP Test Register 3
0x184	RALP Test Register 4
0x185	RALP Test Register 5
0x186	RALP Test Register 6
0x187	RALP Test Register 7
0x188	TALP Test Register 0
0x189	TALP Test Register 1
0x18A	TALP Test Register 2
0x18B	TALP Test Register 3
0x18C	TALP Test Register 4
0x18D-0x18F	Reserved
0x190	TATS Test Register 0
0x191	TATS Test Register 1
0x192	TATS Test Register 2
0x193	TATS Test Register 3
0x194	TATS Test Register 4
0x195	TATS Test Register 5
0x196-0x19F	Reserved
0x1A0	COPS Test Register 0
0x1A1	COPS Test Register 1
0x1A2	COPS Test Register 2
0x1A3	COPS Test Register 3
0x1A4	COPS Test Register 4
0x1A5	COPS Test Register 5
0x1A6	COPS Test Register 6
0x1A7-0x1BF	Reserved
0x1C0	PCID Test Register 0
0x1C1	PCID Test Register 1
0x1C2	PCID Test Register 2
0x1C3	PCID Test Register 3
0x1C4	PCID Test Register 4
0x1C5	PCID Test Register 5
0x1C6	PCID Test Register 6
0x1C7	PCID Test Register 7
0x1C8	PCID Test Register 8

0x1C9- 0x1FF	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

12.1.1 Register 0x100: Master Test

Bit	Type	Function	Default
Bit 15 to 6		Unused	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable LASAR-155 test features. All bits, except PMCTST, are reset to zero by a reset of the LASAR-155.

HIZIO, HIZDATA:
The HIZIO and HIZDATA bits control the tri-state modes of the LASAR-155 . While the HIZIO bit is a logic one, all output pins of the LASAR-155 except the data bus D[15:0], TDO, RXPHYBP and TXPHYBP are tri-stated. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:
The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the LASAR-155 for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:
The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the LASAR-155 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:
The PMCTST bit is used to configure the LASAR-155 for PMC's manufacturing tests. When PMCTST is set to logic one, the LASAR-155 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:
The PMCATST bit is used to configure the analog portion of the LASAR-155 for PMC's manufacturing tests. When PMCATST is set to logic one, the LASAR-155 microprocessor port becomes the test access port used to run the PMC manufacturing analog test vectors. The PMCATST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

12.2 Test Mode 0 Details

In test mode 0, the LASAR-155 allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register should be set to logic one.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 00H: 10FH, 111H, 115H, 119H, 121H, 131H, 141H, 151H, 161H, 171H, 181H, 189H, 191H, 1A1H, 1C1H. Clock edges must be provided on inputs SYSCLK and PCICLK.

Reading the following address locations returns the values on the indicated inputs:

Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
182H	RFIFOXB		RSOC[1]					
18CH				TXPHYBP	TSOC[2]	TFIFOFB		
1C6H			LOCKB[3]	IDSEL	GNTB[3]	PERRB[3]	PAR	DEVSELB[3]
1C7H	AD[15]	AD[14]	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]	AD[8]
1C8H	AD[31]	AD[30]	AD[29]	AD[28]	AD[27]	AD[26]	AD[25]	AD[24]

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
162H	XOFF[4]	TGFC						
182H	RDAT[7][1]	RDAT[6][1]	RDAT[5][1]	RDAT[4][1]	RDAT[3][1]	RDAT[2][1]	RDAT[1][1]	RDAT[0][1]
183H							RXPHYBP	
18CH	TDAT[7][2]	TDAT[6][2]	TDAT[5][2]	TDAT[4][2]	TDAT[3][2]	TDAT[2][2]	TDAT[1][2]	TDAT[0][2]
1C2H							SYSCLK	PCICLK
1C6H	STOPB[3]	FRAMEB[3]	TRDYB[3]	IRDYB[3]	C_BEB[3]	C_BEB[2]	C_BEB[1]	C_BEB[0]
1C7H	AD[7]	AD[6]	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]
1C8H	AD[23]	AD[22]	AD[21]	AD[20]	AD[19]	AD[18]	AD[17]	AD[16]

The following inputs cannot be read using the IOTST feature: D_A[15:9], D[8:0], A[8:0], ALE, CSB, WRB, RDB, RSTB, INTB, TRSTB, TMS, TCK, and TDI.

1. To read RDAT and RSOC, the RXPHYBP input must be set to 1.
2. To read TDAT and TSOC, the TXPHYBP input must be set to 0.
3. These signals are inverted internally, so a 0 on the input would return a 1 in the register.
4. To read XOFF, AUTOXOFF must be set to 0 in the Master Configuration Register.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
003H						INTB[1]		
186H				RRDENB	RSOC[2]			
18CH				TWRENB	TSOC[3]			

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
110H	RCLK					RFP		
114H					TCLK			
116H								TFPO
150H				RCP[4]	RGFC[5]	RALM		
160H							TCP	
186H	RDAT[7][2]	RDAT[6][2]	RDAT[5][2]	RDAT[4][2]	RDAT[3][2]	RDAT[2][2]	RDAT[1][2]	RDAT[0][2]
18CH	TDAT[7][3]	TDAT[6][3]	TDAT[5][3]	TDAT[4][3]	TDAT[3][3]	TDAT[2][3]	TDAT[1][3]	TDAT[0][3]

The following outputs cannot be controlled using the IOTST feature: CSB, RDB, WRB, D_A[15:9], D[8:0], A[8:0], ALE, TDO, and the entire PCI bus.

1. INTB corresponds to output INTB. INTB is an open drain output and should be pulled high for proper operation. Writing a logic zero to the INTB bit allows the LASAR-155 to drive INTB low. Writing a logic 1 to the INTB bit tri-states the INTB output.
2. To control RDAT and RSOC, the RXPHYBP input must be 0.
3. To control TDAT and TSOC, the TXPHYBP input must be 1.
4. The RCP output is delayed by 3 SYSCLK cycles, and it can only be set high for one SYSCLK cycle. To do this, set RCP high, wait 2 clock cycles and then set RCP low. The output will then pulse high.
5. The RGFC output is delayed by 3 SYSCLK cycles.

12.3 Analog Test

To simply the development of production test vectors for the CSU155 and CRU155 to facilitate bench testing of the analog circuitry, special test access is provided outside the normal scope of CBI constraints.

Two analog pins are provided to sense internal analog nodes.

The following signal mapping is always in effect to provide controllability:

Primary input	Internal Signal
XOFF	ACCELB
TDAT[7]	ATST_IN[7]
TDAT[6]	ATST_IN[6]
TDAT[5]	ATST_IN[5]
TDAT[4]	ATST_IN[4]
TDAT[3]	ATST_IN[3]
TDAT[2]	ATST_IN[2]
TDAT[1]	ATST_IN[1]
TDAT[0]	ATST_IN[0]

Observation test points are provided through the microprocessor port. By holding CSB and RDB low, the real time states of the internal signals may be monitored on D[7:0]. Alternatively, microprocessor reads can provide periodic samples of the signal states. Registers 0x06 and 0x07 provide the visibility into the digital portion of the CRU and CSU blocks.

12.3.1 Register 0x101: Analog Test Access

Bit	Type	Function	Default
Bit 15 to 8		Unused	X
Bit 7	R	CSU.ATST_OUT[3]	X
Bit 6	R	CSU.ATST_OUT[2]	X
Bit 5	R	CSU.ATST_OUT[1]	X
Bit 4	R	CSU.ATST_OUT[0]	X
Bit 3	R	CRU.ATST_OUT[1]	X
Bit 2	R	CRU.ATST_OUT[0]	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides observability of the Clock Synthesis and Recovery Unit output test buses.

12.4 JTAG Test Port

The LASAR-155 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits
Version number - 0H
Part Number - 7375H
Manufacturer's identification code - 0CDH
Device identification - 073750CDH

Boundary Scan Register

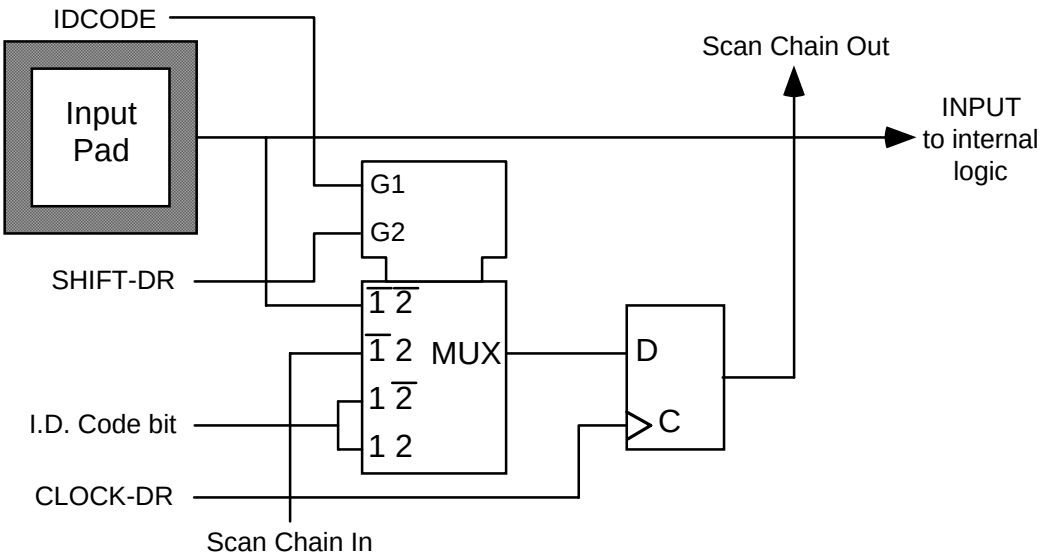
The boundary scan register is made up of 145 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells form the ID code register, and carry the code 073750CDH. The cells are arranged as follows:

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
INTB	144	IN_CELL	0	RFIFOEB	88	IN_CELL	
MPENB	143	IN_CELL	0	RSOC	87	IO_CELL	
RSTB	142	IN_CELL	0	RDAT[7:0]	86:79	IO_CELL	
A[8:0]	141:133	IO_CELL	001110011	RRDENB	78	OUT_CELL	
ALE	132	IO_CELL	0	TXPHYBP (8)	77	IN_CELL	
CSB	131	IO_CELL	1	TFIFOFB	76	IN_CELL	
WRB	130	IO_CELL	1	TSOC	75	IO_CELL	
RDB	129	IO_CELL	1	TDAT[7:0]	74:67	IO_CELL	
D_A[15:9]	128:122	IO_CELL	0101000	TWRENB	66	OUT_CELL	
D[8:0]	121:113	IO_CELL	011001101	PCICLK	65	IN_CELL	
MASTERB (1)	112	OUT_CELL		GNTB	64	IN_CELL	
HI_OENB (2)	111	OUT_CELL		LOCKB	63	IN_CELL	
LO_OENB (3)	110	OUT_CELL		IDSEL	62	IN_CELL	
HIZ (4)	109	OUT_CELL		AD[31:0]	61:30	IO_CELL	
RDATENB (5)	108	OUT_CELL		C_BEB[3:0]	29:26	IO_CELL	
TDATENB (6)	107	OUT_CELL		FRAMEB	25	IO_CELL	
logic zero	106	OUT_CELL		IRDYB	24	IO_CELL	
no connect	105	IN_CELL		TRDYB	23	IO_CELL	
no connect	104	IN_CELL		STOPB	22	IO_CELL	
RCLK	103	OUT_CELL		DEVSELB	21	IO_CELL	
RFP	102	OUT_CELL		PAR	20	IO_CELL	
RALM	101	OUT_CELL		PERRB	19	OUT_CELL	
RGFC	100	OUT_CELL		REQB	18	OUT_CELL	
RCP	99	OUT_CELL		SERRB	17	OUT_CELL	
XOFF	98	IN_CELL		PCIINTB	16	OUT_CELL	
TCP	97	OUT_CELL		ADDIRB[7:0] (9)	15:8	OUT_CELL	
TGFC	96	IN_CELL		PARDIRB (10)	7	OUT_CELL	
TCLK	95	OUT_CELL		CBEDIRB (11)	6	OUT_CELL	
TFPO	94	OUT_CELL		FRMDIRB (12)	5	OUT_CELL	
TXDN	93	OUT_CELL		PERDIRB (13)	4	OUT_CELL	
TXDP	92	OUT_CELL		IRDYDIRB (14)	3	OUT_CELL	
TXC	91	OUT_CELL		TRDYDIRB (15)	2	OUT_CELL	
logic zero	90	OUT_CELL		REQB_OEB (16)	1	OUT_CELL	
RXPHYBP [7]	89	IN_CELL		INTB	0	OUT_CELL	

NOTES:
1. MASTERB selects the direction of the A[8:0], ALE, CSB, WRB, RDB, D_A[15:9] and D[8:0] signals.
2. HI_OENB is the active low output enable for D_A[15:9].
3. LO_OENB is the active low output enable for D[8:0].

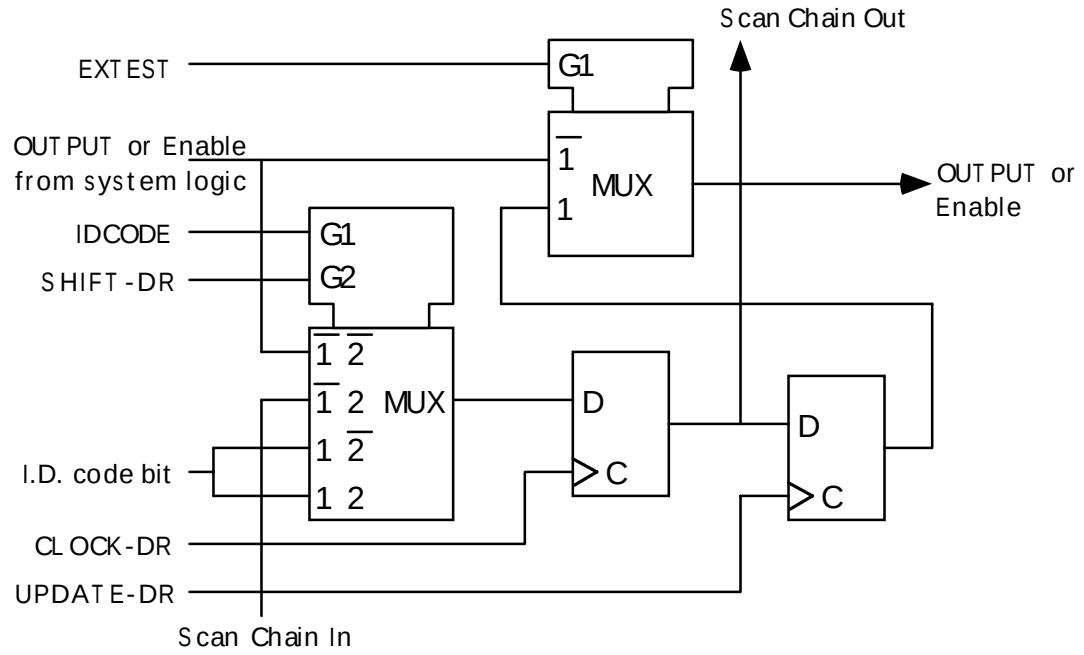
4. HIZ is the active low output enable for all OUT_CELL types except D_A[15:9], D[8:0], RDAT[7:0], and INTB.
5. RDATENB is the active low output enable for RSOC and RDAT[7:0].
6. TDATENB is the active low output enable for TSOC and TDAT[7:0].
7. RXPHYBP selects the direction of RSOC and RDAT[7:0].
8. TXPHYBP selects the direction of TSOC and TDAT[7:0].
9. ADDIRB[7:0] selects the direction of AD[31:0].
10. PARDIRB selects the direction of PAR.
11. CBEDIRB selects the direction of C_BEB[3:0].
12. FRMDIRB selects the direction of FRAMEB.
13. PERDIRB selects the direction of PERRB.
14. IRDYDIRB selects the direction of IRDYB.
15. TRDYDIRB selects the direction of TRDYB.
16. REQB_OEB is the active low output enable for REQB.

12.4.1.1 Fig. 12.1 Input Observation Cell (IN_CELL)

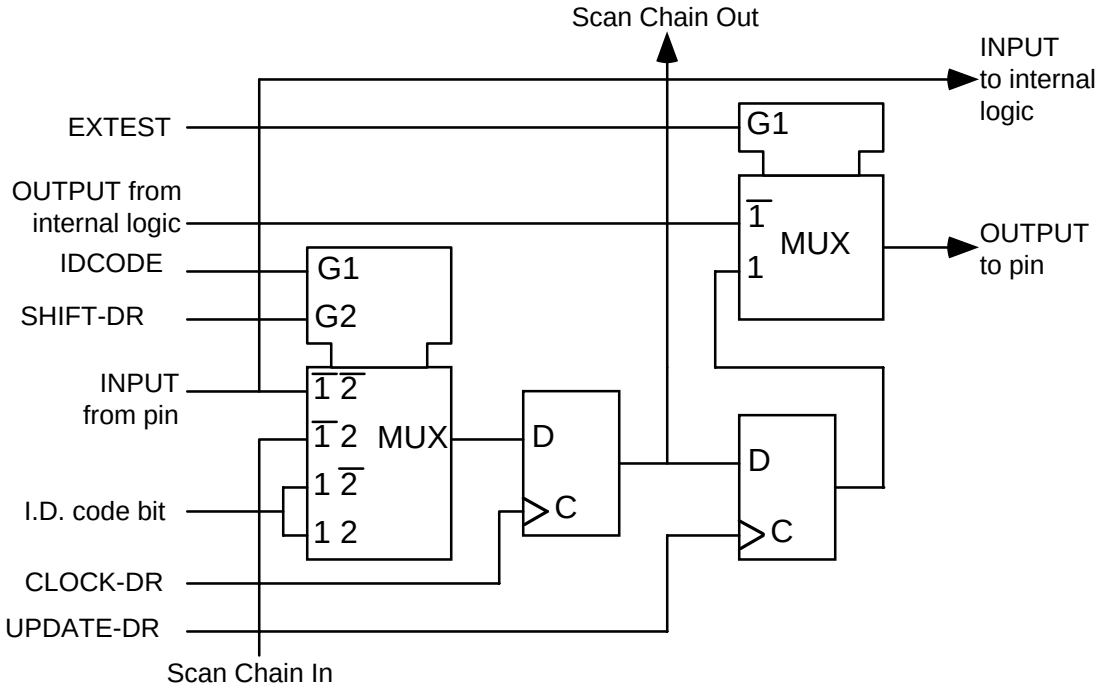


In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

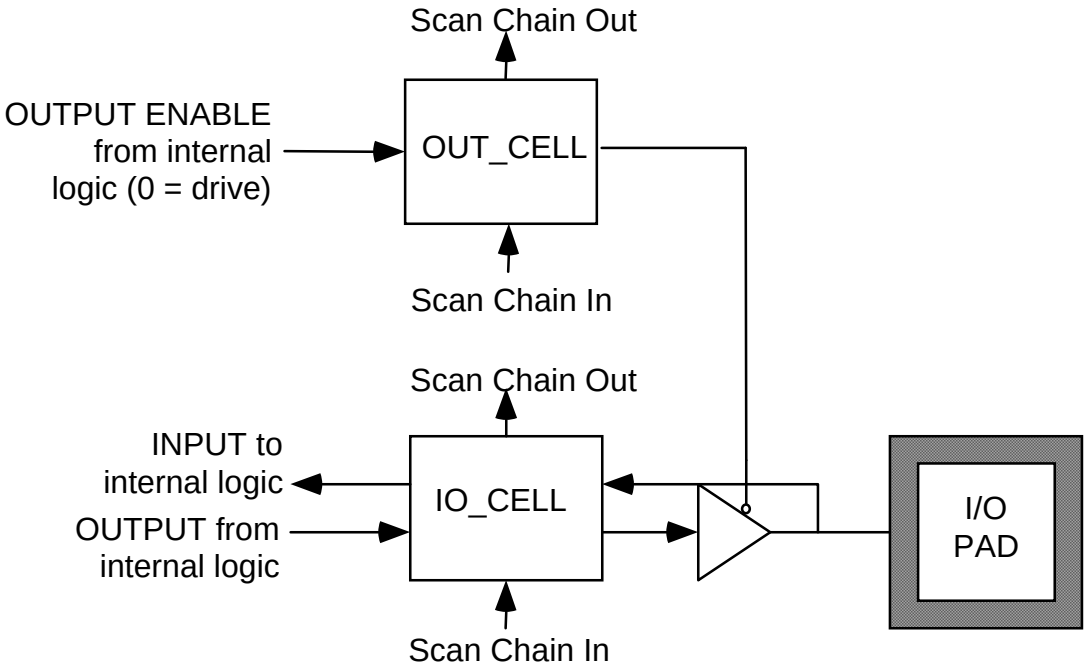
12.4.1.2 Fig. 12.2 Output Cell (OUT_CELL)



12.4.1.3 Fig. 12.3 Bidirectional Cell (IO_CELL)



12.4.1.4 Fig. 12.4 Layout of Output Enable and Bidirectional Cells



13 OPERATION

This section presents PCB design recommendations, tutorial information on the SONET/SDH and ATM protocols, operating details for the JTAG boundary scan feature and interface details for external FIFOs, ROMs and PHY devices.

13.1 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines *must* be followed in order to ensure proper operation.

1.) Connect digital and analog grounds together at a point where the ground reference is clean and as free as possible of digital return currents. Typically, this means as close as possible to the PCB connector where ground is brought into the card.

2.) Provide separate +5 volt analog transmit, +5 volt analog receive, and +5 volt digital supplies, but otherwise connect the supply voltages together at a point where the supply is clean and as free as possible of digitally induced switching noise. Typically, this means as close as possible to the PCB connector where +5 volts is brought into the card. In some systems separate regulation is required for the transmit and receive analog supplies.

3.) Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistor does not lower the supply voltage below the recommended operating voltage.

4.) Ferrite beads are recommended for TAVD1, TAVD2, RAVD1 and RAVD2.

5.) Separate high-frequency decoupling capacitors are recommended for each analog power (TAVD1, TAVD2, RAVD1 and RAVD2) pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into the reference circuitry powered by TAVD1 and RAVD1.

6.) The high speed serial streams (TXD+/- and RXD+/-) must be routed with controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

13.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. The recommended power supply sequencing is as follows:

1.) VDD_DC power must be supplied either before VDD_AC or simultaneously with VDD_AC to prevent current flow through the ESD protection devices which exist between VDD_DC and VDD_AC power supplies. Connection to a common VDD power plane is the recommended standard practice for customer applications.

2.) To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDD_DC power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification (20 mA).

3.) Analog power supplies must be applied after both VDD_DC and VDD_AC have been applied or the they must be current limited to the maximum latchup current specification (100 mA). To prevent forward biasing the ESD protection diode between AVD supplies and VDD_DC, the differential voltage measured between these power supplies must be less than 0.5 volt. This recommended differential voltage is to include peak to peak noise on the VDD_DC power supply as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply. If the VDD power supply is relatively quiet, VDD can be filtered using a ferrite bead and a high frequency decoupling capacitor to supply AVD. The relative power sequencing of the multiple AVD power supplies is not important.

4.) Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDD and AVD discharge times will not damage the device.

13.3 Interfacing to ECL or PECL Devices

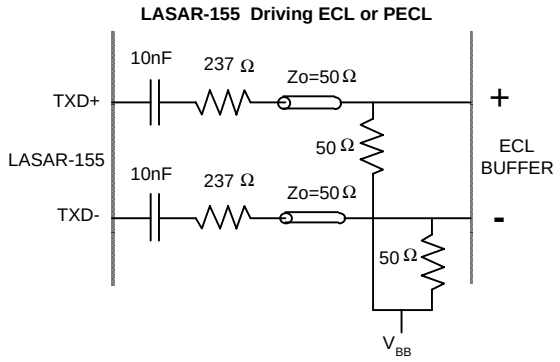
Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. The figure below

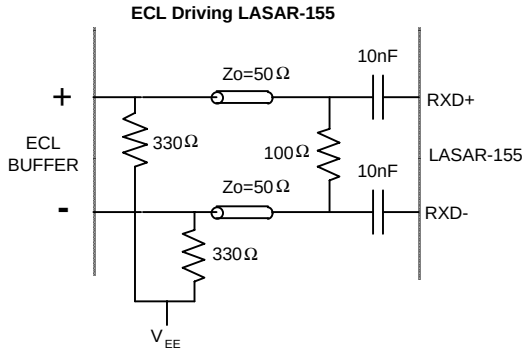
illustrates the recommended configuration. The capacitors AC couple the outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the 237 Ω and 50 Ω resistors divide the voltage down to a nominally 800mV swing. The 50 Ω resistors also terminate the signals.

Similarly, the RXD+/- inputs to the LASAR-155 are AC coupled as shown below. The LASAR-155 inputs are self-biasing to improve operating speed and waveform symmetry. For this reason, the DC blocking capacitors are always required, even when interfacing to PECL drivers. The only exception are the ALOS+/- inputs which must be DC coupled because of their low frequency content.

Ceramic coupling capacitors are recommended.

13.3.1.1 Fig. 13.1 Interfacing LASAR-155 to ECL or PECL



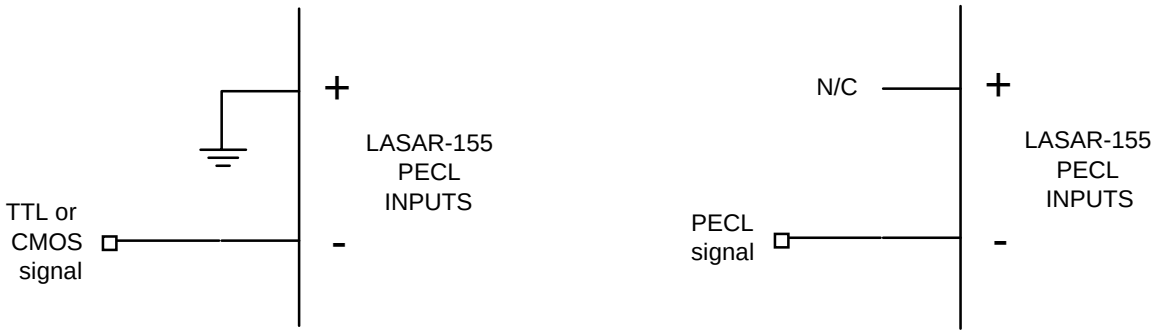


13.3.1.2 Fig. 13.2. Driving Differential Inputs Single Ended

In some applications it may be more cost effective or technically desirable to drive the RRCLK+/-, TRCLK+/- or ALOS+/- inputs with a single ended TTL or CMOS signal. The figure below illustrates the suggested configuration to achieve this. Note that the RXD+/- inputs do not support single ended operation and must always be driven by a differential source.

Note, for non looped-timed applications requiring minimum intrinsic jitter in the transmit data, TRCLK+/- must be driven differentially.

13.3.1.3 Fig. 13.3 Single Ended Driving Differential Inputs



For TTL or CMOS signals, the positive input must be grounded. The negative input should be connected directly to a TTL or attenuated CMOS signal. The input voltage for logic 0 should be below 800 mV, and for logic 1 should be above 2.5 V.

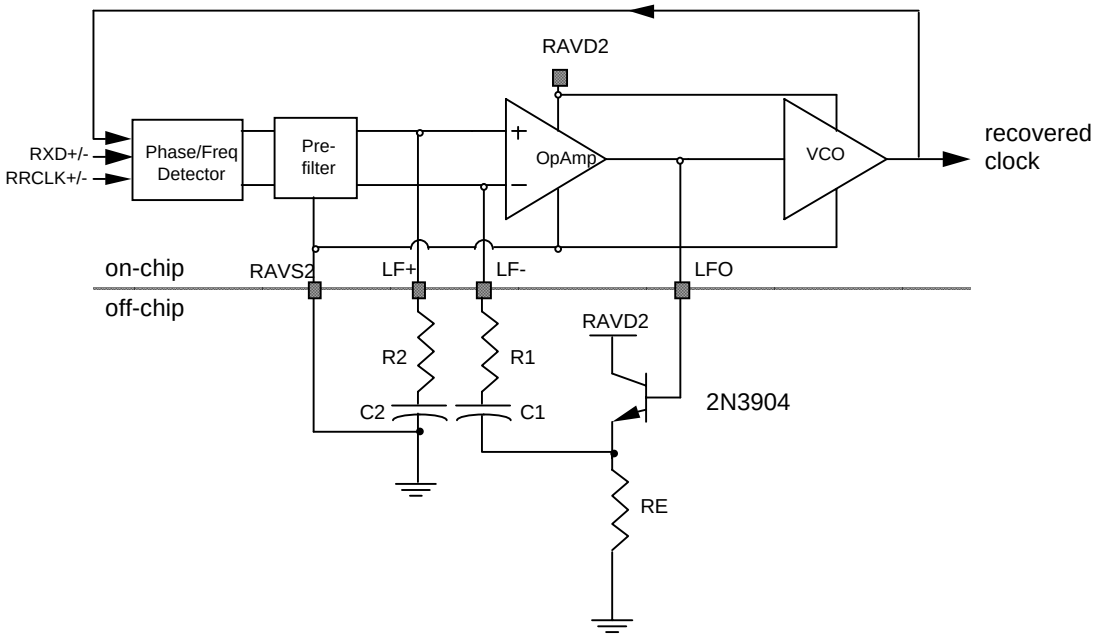
A similar arrangement can be used for an ALOS single ended ECL or pseudo-ECL signal. The positive input must be unconnected. The ALOS pseudo-ECL signal may be directly connected to the negative input.

These configurations logically invert the input signal.

13.4 Clock Recovery Passives

Below is an abstraction of the clock recovery phase lock loop illustrating the connections to external passive components. The figure illustrates the unity gain buffer loop filter application where the integral op-amp output is buffered through a unity gain amplifier to minimize the effect of its finite output impedance on the transfer function of the PLL. The unity gain buffer loop filter circuit exceeds SONET/SDH jitter tolerance and jitter transfer specifications and is recommended for all designs.

13.4.1.1 Fig. 13.4 Clock Recovery Circuit



Line Rate (Mbit/s)	R1 (•±1%)	R2 (•±1%)	C1, C2 min (µF±10%)	RE (•±1%)
155.52	68.1	90.9	4.7	100
51.84	68.1	90.9	15	100

Note: The component values shown are provisional, and are subject to change. Please contact PMC-Sierra for current information.

The capacitors (C1, C2) determine the amount of "peaking" in the jitter transfer curve. The capacitor values can be ±10%. The capacitors should be non-polarized because when the LASAR-155 is held in reset, the capacitors are reverse-biased at approximately 2.0V. Also, for some process extremes, the capacitors may operate with a D.C. reverse-bias of up to 1.0V.

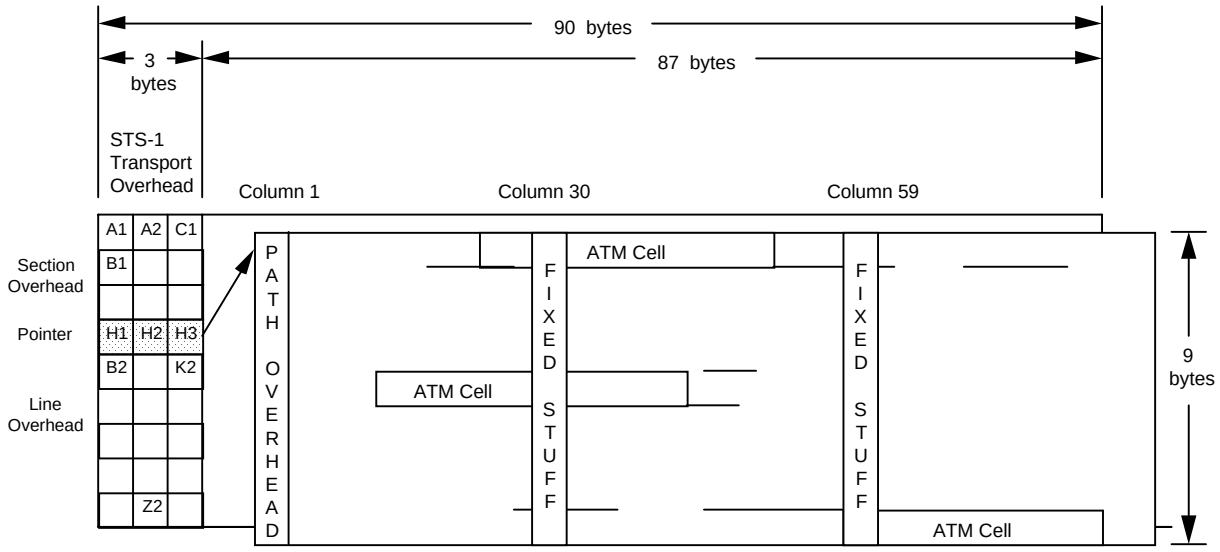
The recommended values for the capacitors may not be readily available in non-polarized versions. In this case, two polarized capacitors can be connected "back-to-back" (in series, anode-to-anode) to implement each capacitance. Since these back-to-back capacitors will be in series, they should be of twice the value of the desired capacitance. This back-to-back configuration effectively creates a "bi-polar" capacitor.

13.5 ATM Mapping and SONET Overhead Byte Usage

The LASAR-155 processes the ATM cell mappings for STS-3c (STM-1) and STS-1 as shown below. The LASAR-155 processes the subset of the complete transport and path overhead required to support ATM UNIs.

Below, the STS-1 mapping is displayed. The LASAR-155 supports two STS-1 mappings, one with the indicated stuff columns containing fixed stuff bytes and the other with the indicated stuff columns used for ATM cells.

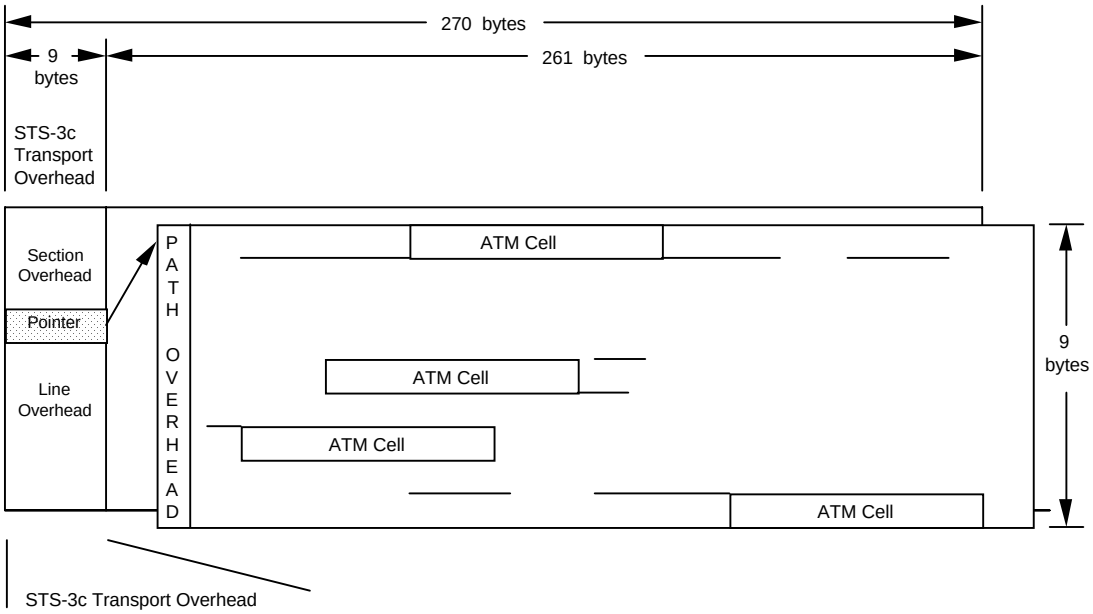
13.5.1.1 Fig. 13.5 STS-1 Mapping



* Fixed stuff columns optionally filled with cells

Below, the STS-3c (STM-1) mapping is shown. In this mapping, no stuff columns are included in the SPE. The entire SPE is used for ATM cells.

13.5.1.2 Fig. 13.6 STS-3c (STM-1) Mapping



STS-3c Transport Overhead

A1	A1	A1	A2	A2	A2	C1	C1	C1
B1								
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2				K2		
					Z2			

Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the STS-3c (STM-1) or STS-1 bit serial stream.

C1: The identification bytes identify the individual STS-1s in the byte interleaved STS-3c (STM-1) stream. C1 is not scrambled by the frame synchronous SONET scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function.

H1, H2: The pointer value bytes locate the start of the synchronous payload envelope (SPE) in the SONET/SDH frame.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

K2: The K2 byte is used to identify line layer maintenance signals. Line FERF is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern 110B. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern 111B and the entire SPE is set to an all ones pattern.

Z2: The growth byte provides a line far end block error function for remote performance monitoring. When configured for STS-1 mode, the first and only Z2 byte is used. When configured for STS-3c (STM-1), the third Z2 byte is used.

Path Overhead Bytes

J1: The Path Trace byte is used to repetitively transmit a 64-byte or 16-byte, fixed length string. When not used, this byte should be set to 64 NULL characters. NULL is defined by the ASCII code, 0x00.

B3: The path bit interleaved parity byte provides a path error monitoring function.

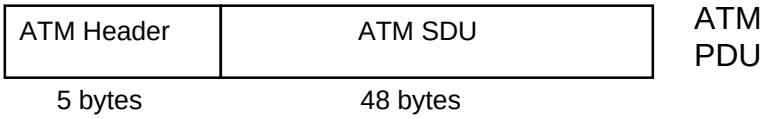
C2: The path signal level indicator identifies the SPE mapping. For ATM mappings, the identification code is 13H.

G1: The path status byte provides a path far end block error (path FEBE) function, and provides control over the path Remote Defect Indication (RDI) maintenance signal.

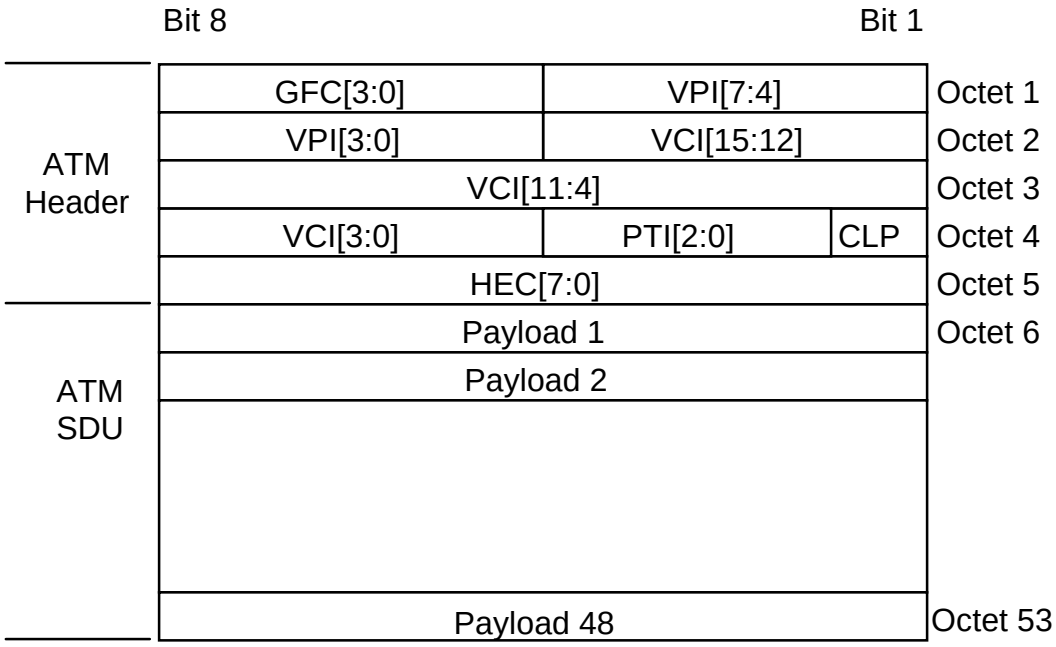
13.6 ATM Cell Format

The ATM cell format is shown below. The LASAR-155 processes the complete ATM cell header to support Network Interface Card applications.

13.6.1.1 Fig. 13.7 ATM Cell Structure



13.6.1.2 Fig. 13.8 Cell Fields



Cell Header Fields

GFC[3:0]: The Generic Flow Control field is used by terminals implementing control access mode operation. The codepoints defining actions for controlled access terminals is currently for further study. For uncontrolled terminals, the GFC fields should be set to 0H.

In the transmit direction, the LASAR-155 sources the GFC field from an external serial stream on input TGFC or from the user programmable per VC parameter RAM. The GFC field in the per VC parameter RAM should be supplied by the user when the VC is

provisioned. By default, the LASAR-155 uses the per VC parameter RAM GFC value unless overwritten by the value on input, TGFC.

In the receive direction, the LASAR-155 extracts the received GFC value from cell headers and serialize it on output, RGFC. In addition if enabled, the receive GFC values are internally looped to the transmit side to implement an aggregate XON/OFF protocol based on GFC[3].

VPI[7:0]: The Virtual Path Identifier field and the VCI field are used to identify a VC.

In the transmit direction, the LASAR-155 sources the VPI field from the user programmable per VC parameter RAM. The VPI field in the per VC parameter RAM should be supplied by the user when the VC is provisioned. The VC is identified by a combination of the VPI and VCI bits.

In the receive direction, the LASAR-155 uses the received VPI and VCI fields to identify the VC. Once the VC is identified, the full received VPI field is used to compare with the VPI value in the per VC Parameter RAM. If there is a mismatch, the LASAR-155 drops the cell, increments an error counter and informs the microprocessor or PCI Host.

VCI[15:0]: The Virtual Channel Identifier field with the VPI field is used to identify a VC.

In the transmit direction, the LASAR-155 sources the VCI field from the user programmed per VC parameter RAM. The VCI field in the per VC parameter RAM should be supplied by the user when the VC is provisioned. The VC is identified by a combination of the VPI and VCI bits.

In the receive direction, the LASAR-155 uses the received VPI and VCI fields to identify the VC. Once the VC is identified, the full received VCI field is used to compare with the VCI value in the per VC Parameter RAM. If there is a mismatch, the LASAR-155 drops the cell, increments an error counter and informs the microprocessor or PCI Host.

PTI[2:0]: The Payload Type Indicator field is used to identify the contents of the Payload field. The PTI codepoints are listed below:

PTI Coding	Interpretation
000	User_Data_cell, Congestion_Experienced=False, SDU_Type=0
001	User_Data_cell, Congestion_Experienced=False, SDU_Type=1
010	User_Data_cell, Congestion_Experienced=True, SDU_Type=0
011	User_Data_cell, Congestion_Experienced=True, SDU_Type=1
100	Segment OAM F5 flow cell
101	End-to-end OAM F5 flow cell
110	Resource Management Cell
111	Reserved

In the transmit direction, the LASAR-155 sources the PTI field from the user programmed per VC parameter RAM or from the TD associated with the CPAAL5_PDU under segmentation or the F5 OAM cell. Selection can be made using a bit in the TD.

In the receive direction, the LASAR-155 examines the PTI fields and processes them accordingly. If configured F5 OAM Flow cells are passed to the Receive Management Descriptor Reference Ready Queue. SDU_Type=1 cells are used to indicate the last cell of a CPAAL5_PDU reassembly on a VC.

CLP: The Cell Loss Priority bit is used to indicate the priority of a cell. A cell with CLP=1 has a greater loss priority then a cell with CLP=0.

In the transmit direction, the LASAR-155 sources the CLP bit from the user programmed per VC parameter RAM or from the TD associated with the CPAAL5_PDU under segmentation or from the TD associated with the F5 OAM cell. Selection can be made using a bit in the TD.

In the receive direction, the LASAR-155 extracts the CLP bit and provides the indication to the PCI Host on a per cell basis using a Receive Management Descriptor. For reassembled CPAAL5_PDUs, the LASAR-155 provided an aggregate ORed version of CLP over all cells of the CPAAL5_PDU to the PCI Host using a Receive Packet Descriptor.

HEC[7:0]: The Header Error Correction field provides a CRC check over the entire ATM Cell header. Please refer to the Functional Description section for the CRC polynomial.

In the transmit direction, the LASAR-155 automatically generates and inserts this field.

In the receive direction, the LASAR-155 automatically verifies the CRC-8 over the ATM Cell header. Single bit error correction is performed and apparent multi bit errors are detected. Cells with HEC errors can be optionally dropped. Both correctable and uncorrectable HEC error cells are counted.

Payload: The Payload field is used to carry the ATM SDU. The Payload is expected to be 48 octets. For F5 OAM Flow cells, the 10 LSBs can optionally contain a CRC-10 check over the payload field.

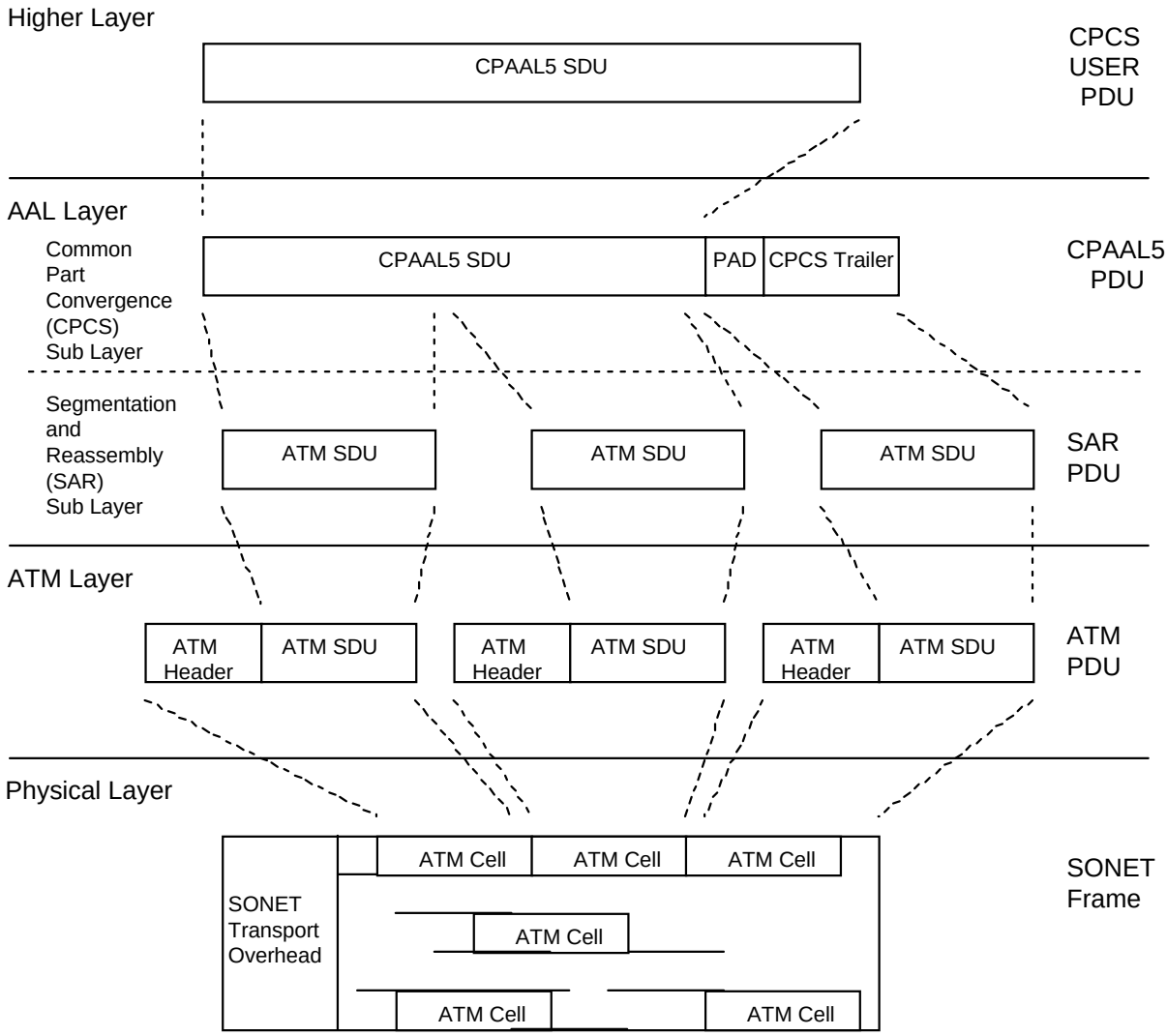
In the transmit direction, the LASAR-155 automatically fills the payload field with segmented portions of CPAAL5_PDUs. For F5 OAM cells or any cells directly sourced from the PCI Host, the LASAR-155 can optionally provide the 10 bit CRC-10 value.

In the receive direction, the LASAR-155 extracts the ATM SDU from the payload field and associates the ATM SDU with a CPAAL5_PDU under reassembly. For F5 OAM Flow cells or any other cell, the LASAR-155 can optionally verify a 10 bit CRC-10 over the entire payload field. CRC-10 errors are counted and the microprocessor and/or the PCI Host is optionally alerted of the event.

13.7 CPCS AAL Type 5 Format

The CPCS AAL Type 5 Format (CPAAL5) cell format is shown below. In the CPAAL5_PDU Processing figure, how the LASAR-155 processes a CPAAL5 Service Data Unit (SDU) from a CPCS user entity is illustrated.

13.7.1.1 Fig. 13.9 CPAAL5_PDU Processing

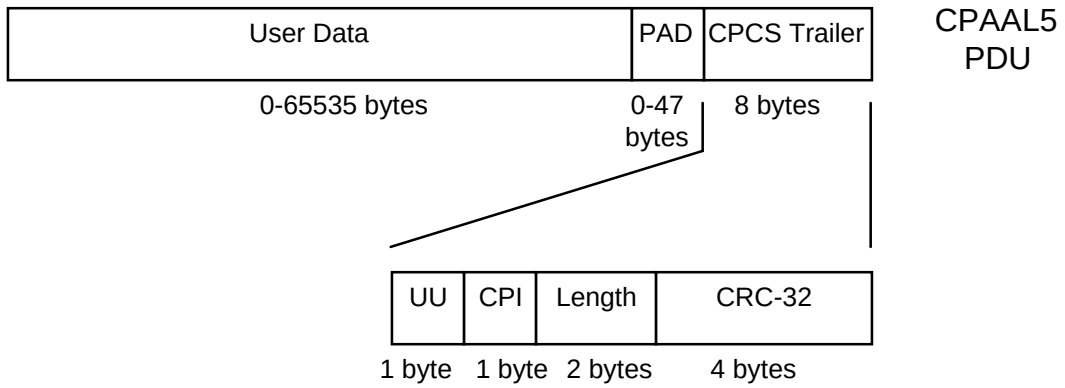


In the transmit direction, the CPAAL5_SDU from the higher layer CPAAL5 user entity is passed to the AAL Layer entity where it is encapsulated with a CPCS trailer to form a CPAAL5_PDU. The CPAAL5_PDU is then segmented into 48 byte ATM

SDUs and passed to the ATM Layer entity. The ATM Layer entity combines the ATM SDU with a five byte ATM header to form the ATM PDU or an ATM cell. ATM cells are then passed to the Physical Layer entity where they are mapped into SONET frames. In the receive direction, the processing is just the reverse order of the transmit processing. The LASAR-155 performs all actions required by the AAL Layer, ATM Layer and Physical Layer entities.

In the CPAAL5_PDU Fields figure, the CPAAL5_PDU fields are illustrated.

13.7.1.2 Fig. 13.10 CPAAL5_PDU Fields



User Data: The User Data field is used to carry the CPAAL5_SDU from the CPAAL5 User entity. The User Data field must be byte aligned and can have a length of 0 to 65,535 bytes.

In the transmit direction, the LASAR-155 provides Transmit Descriptors (TD) to the PCI Host to allow the PCI Host to provide to the LASAR-155 CPAAL5 SDUs. The SDUs must be byte aligned in a TD's packet buffer.

In the receive direction, the LASAR-155 uses the Receive Packet Descriptors (RPD) to pass reassembled CPAAL5_SDUs to the PCI Host.

Pad: The Pad field is used to align the CPAAL5_PDU to 48 octet boundaries. The Pad field length should always be in the range, 0-47 bytes.

In the transmit direction, the LASAR-155 automatically generates the Pad field.

In the receive direction, the LASAR-155 automatically strips off the Pad field before passing the CPAAL5_SDU to the PCI Host.

UU: The User-to-User field contains the User-to-User Information octet that can be used by CPAAL5 Users to communicate.

In the transmit direction, the LASAR-155 can automatically pad out this octet with 00H or use the byte in the TD provided by the CPAAL5 User. Selection is made using the PCID Control register.

In the receive direction, the LASAR-155 extracts this octet from the reassembled CPAAL5_PDU and provides the byte to the PCI Host using a RPD.

CPI: The Common Part Indicator field is currently reserved for future CPAAL5 User functions. This field should be coded to 00H

In the transmit direction, the LASAR-155 can automatically pad out this octet with 00H or use the a byte in the TD provided by the CPAAL5 User. Selection is made using the PCID Control register.

In the receive direction, the LASAR-155 extracts this octet from the reassembled CPAAL5_PDU and provides the byte to the PCI Host using a RPD. In addition, the LASAR-155 counts the number of non zero CPI PDUs received and optionally alerts the microprocessor and/or the PCI Host of a non zero CPI violation.

Length: The Length field is used to indicate the length of the User Data field or to indicate a forward abort. When the Length field is zero, the transmit CPAAL5 entity is indicating to the receive CPAAL5 entity that an abort condition exists and the User Data field contains a incomplete CPAAL5_SDU. When the Length field is not zero, the Length field contains the length of the CPAAL5_SDU in the User Data field.

In the transmit direction, the PCI Host must provide the CPAAL5_SDU's length in a TD. This length can be optionally compared to a programmable maximum transmission length before the CPAAL5_SDU is encapsulated, segmented and transmitted. To indicate a forward abort condition, the PCI Host must set the Packet Length field of the last TD of an aborted packet to zero. In addition the PCI Host must also set the M bit of the TD to zero and the CE bit to one, indicating an end of packet.

In the receive direction, the LASAR-155 continuously monitors the CPAAL5_PDU assembly length and optionally terminates any reassemblies which exceed a programmed maximum. The terminated reassemblies are counted and the microprocessor and/or the PCI Host is alerted of the event. For CPAAL5_PDUs that are successfully reassembled, the LASAR-155 extracts the received Length field, verifies the Length field with the actual received length and provides the Length field to the PCI Host using a RPD. Length mismatches are counted and the microprocessor and/or the PCI Host is alerted.

CRC-32: The four octet CRC-32 field provides a CRC check over the entire CPAAL5_PDU. Please refer to the Functional Description section for the CRC polynomial.

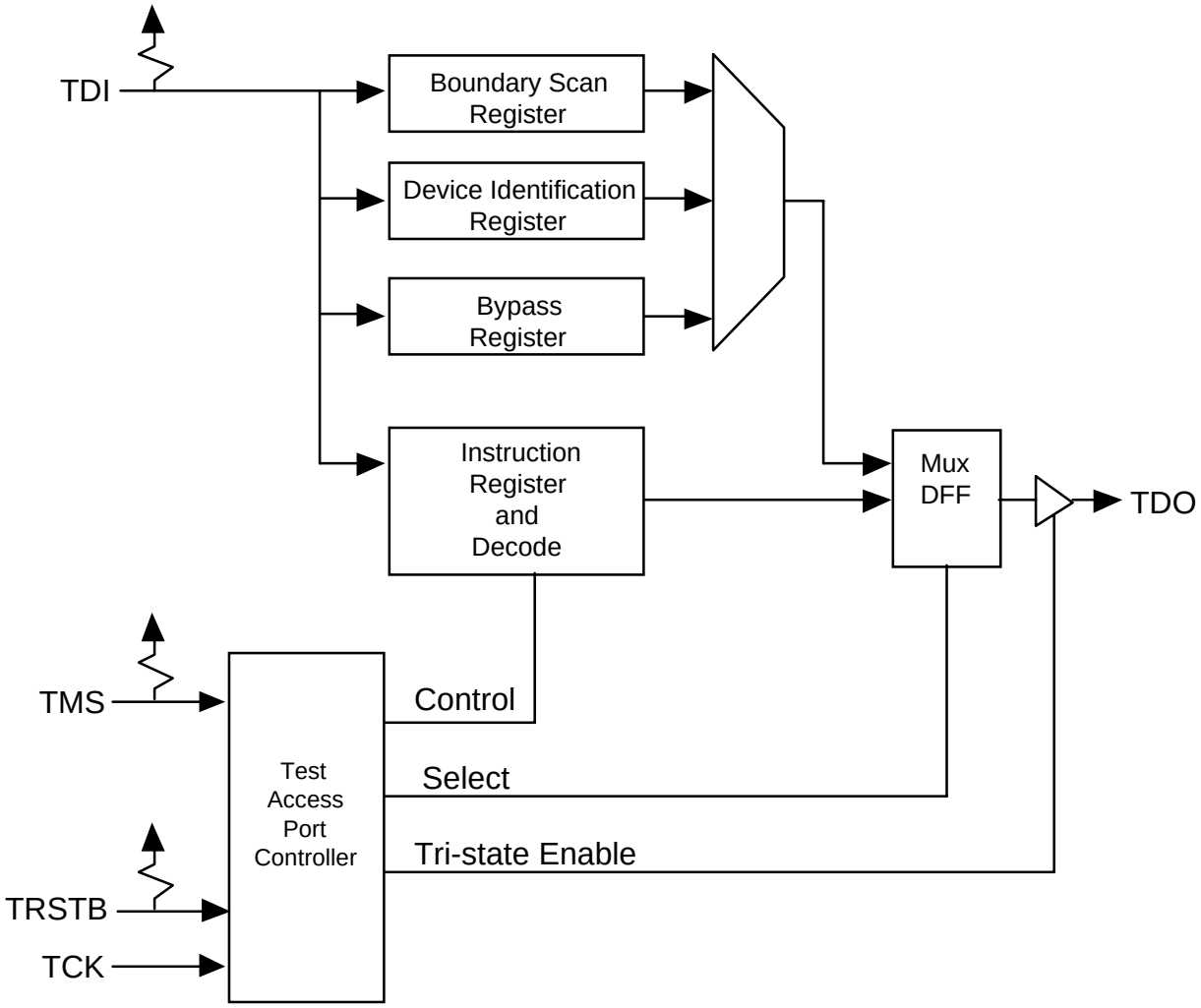
In the transmit direction, the LASAR-155 automatically generates and inserts this field.

In the receive direction, the LASAR-155 automatically verifies the CRC-32 over the reassembled CPAAL5_PDU. CRC-32 errors are counted and the microprocessor and/or the PCI Host is optionally alerted.

13.8 JTAG Support

The LASAR-155 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

13.8.1.1 Fig. 13.11 Boundary Scan Architecture



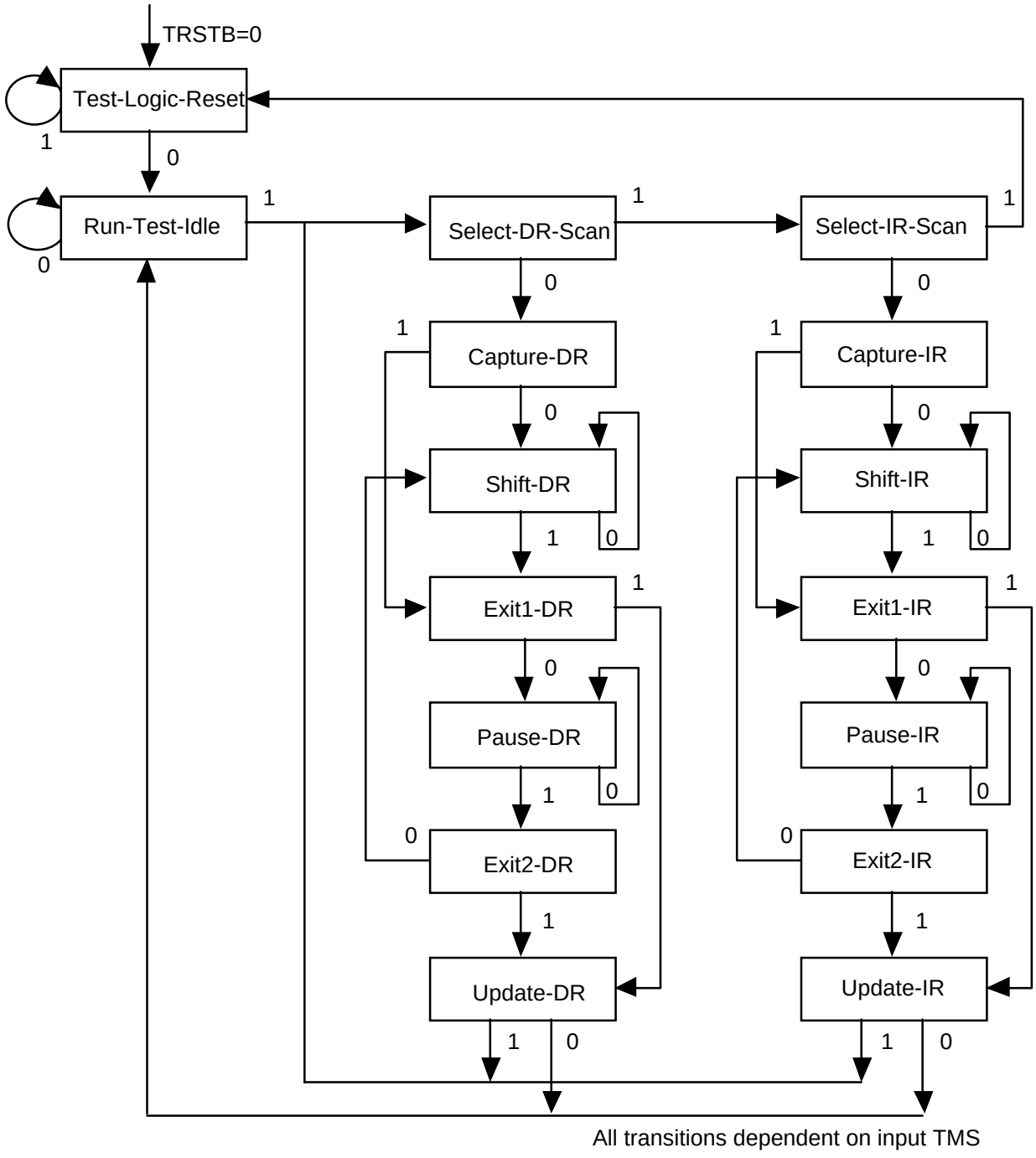
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

13.8.1.2 Fig. 13.12 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

INTEST

The internal test instruction is used to exercise the device's internal core logic. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Update-DR state, patterns shifted in on input, TDI are used to drive primary inputs. During the

Capture-DR state, primary outputs are sampled and loaded into the boundary scan register.

13.9 Multipurpose Port FIFO Connections

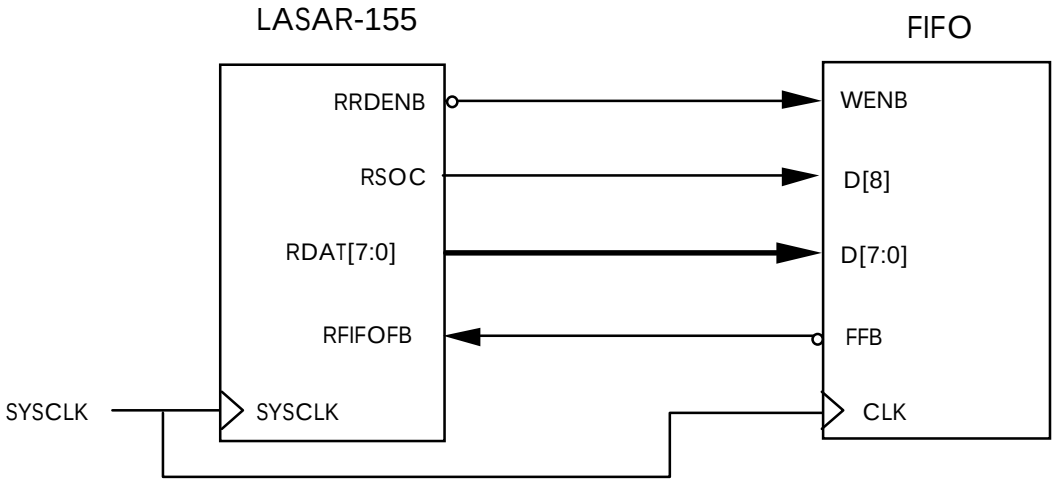
When configured as an insertion/extraction port (RXPHYBY=0, TXPHYBP=0), the Multipurpose Port is designed to interface to many commonly available FIFOs. Some of the FIFOs the Multipurpose Port can interface to are:

Integrated Device Technology, IDT72421
Texas Instruments, SN74ACT2211L
Paradigm, PDM42205

A connection diagram is shown for interfacing to an external FIFO when the Multipurpose Port is configured to extract cells from the LASAR-155. The diagram is general but the signals described are found on many FIFOs.

13.9.1.1

13.9.1.2 Fig. 13.13 Multipurpose Port Connection Diagram (RXPHYBP=0)

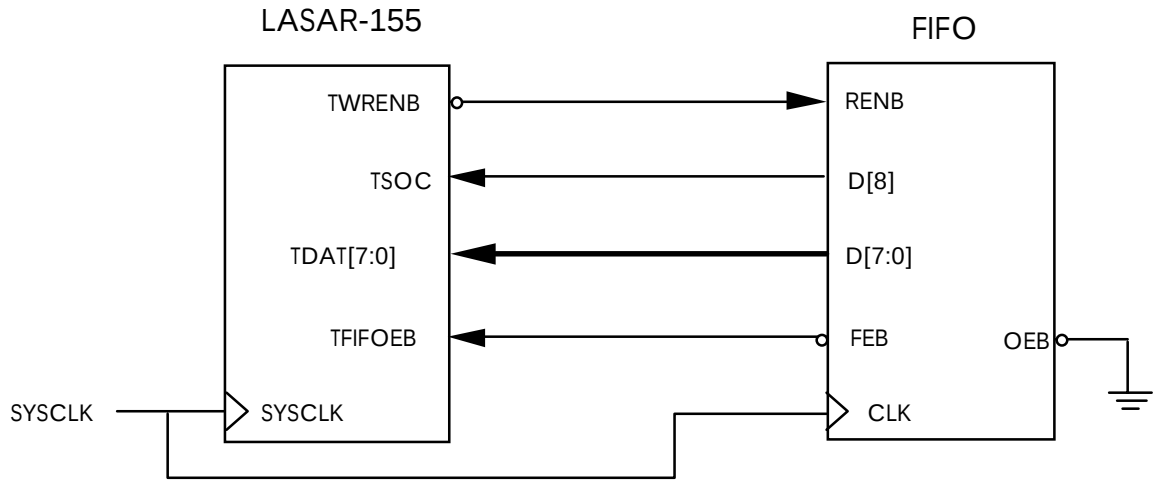


A connection diagram is shown for interfacing to an external FIFO when the Multipurpose Port is configured to insert cells into the LASAR-155. The diagram is general but the signals described are found on many FIFOs.

13.10 Multipurpose Port External PHY Connections

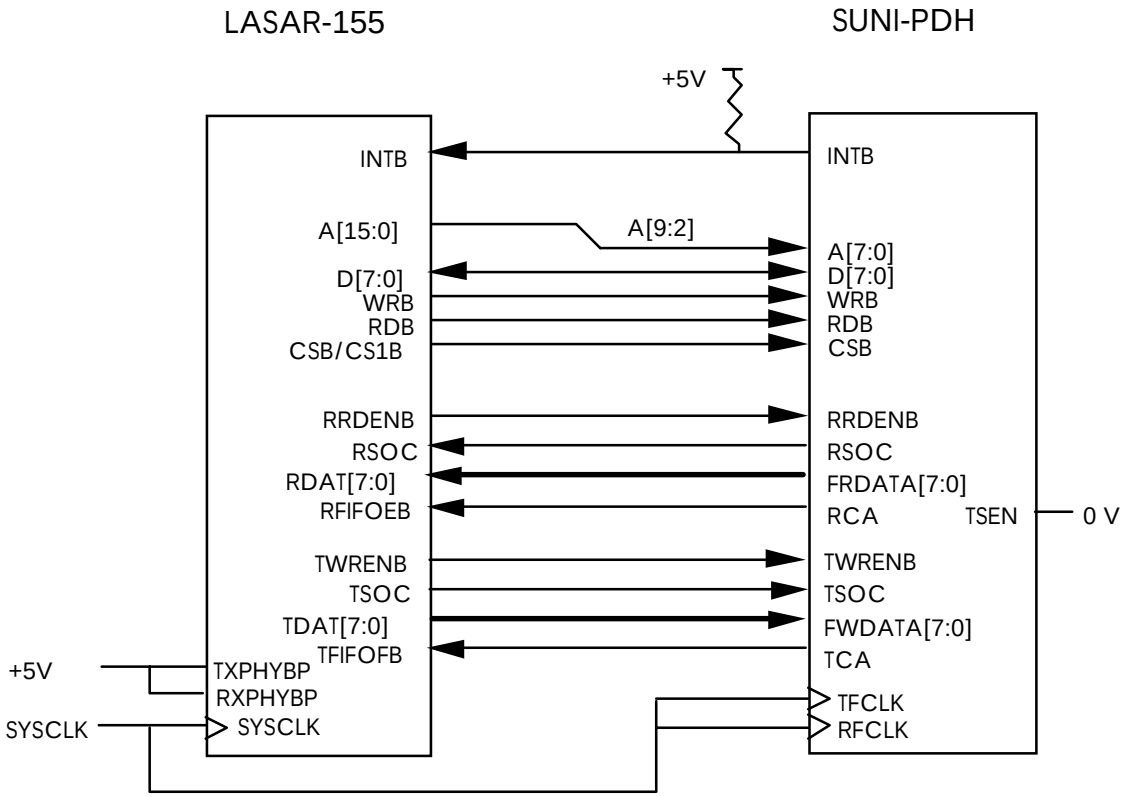
13.10.1.1

13.10.1.2 Fig. 13.14 Multipurpose Port Connection Diagram (TXPHYBP=0)



When the LASAR-155 is configured for PHY bypass (RXPHYBP=1, TXPHYBP=1), the LASAR-155's Multipurpose Port can be directly interfaced with an external ATM Physical Layer device. The PMC PM7345, SUNI-PDH can be used to interface to T3, E3, T1, E1 transmission systems as shown below. Since the data bus to the external ATM Physical Layer device is a eight bit interface, the LASAR-155 must access the Physical Layer device as bytes on Dword boundaries.

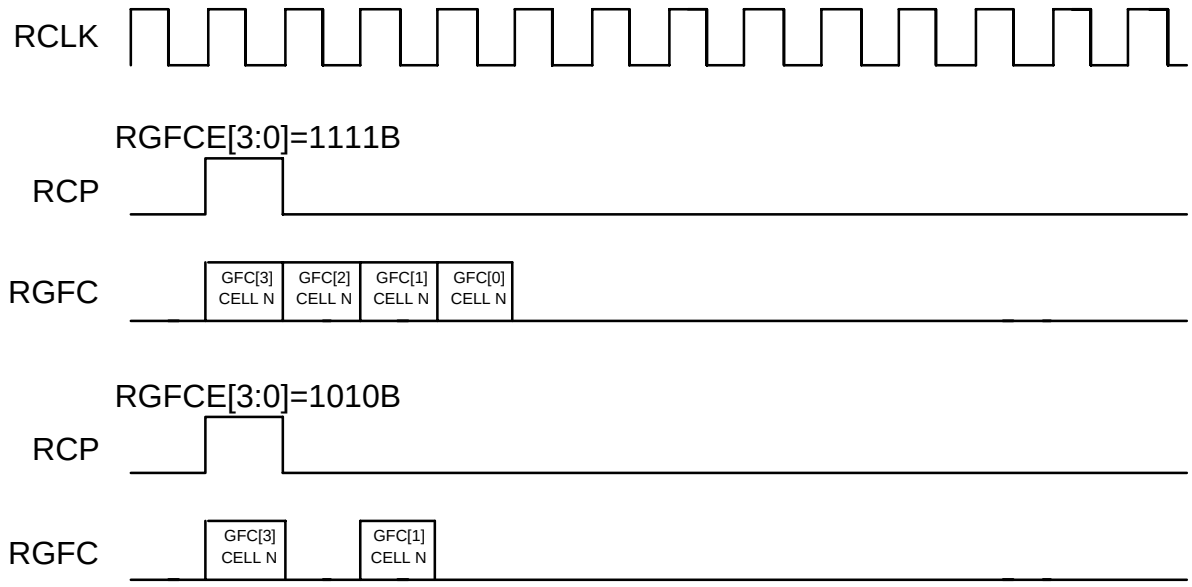
13.10.1.3 Fig. 13.15 LASAR-155 to SUNI-PDH Interface



14 FUNCTIONAL TIMING

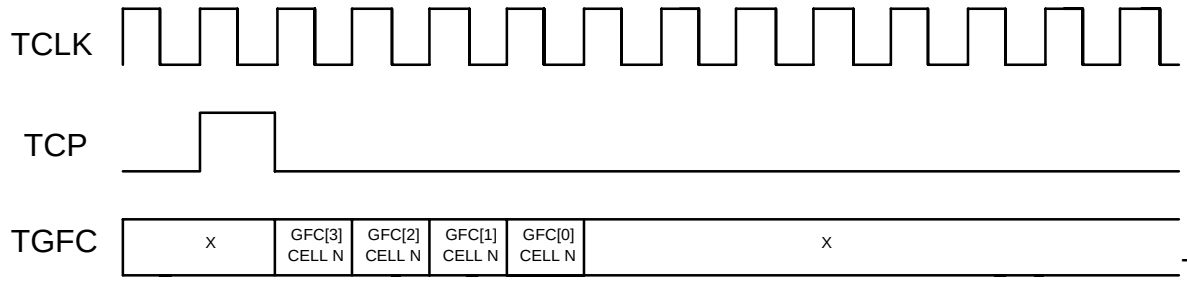
14.1 GFC and Data Link Access

14.1.1.1 Fig. 14.1 GFC Extraction Port



The GFC Extraction Port Diagram illustrates the relationship between the receive cell pulse, RCP signal and the receive serial GFC output. Extraction of the GFC[3:0] bits is controlled by the four RGFC enable (RGFCE[3:0]) bits in the RACP Configuration register. The output value in each GFC bit position can be forced low by setting the corresponding RGFCE bit to zero. The serial link is inactive (forced low) if the LASAR-155 is out of cell delineation or if the current cell contains an uncorrectable header.

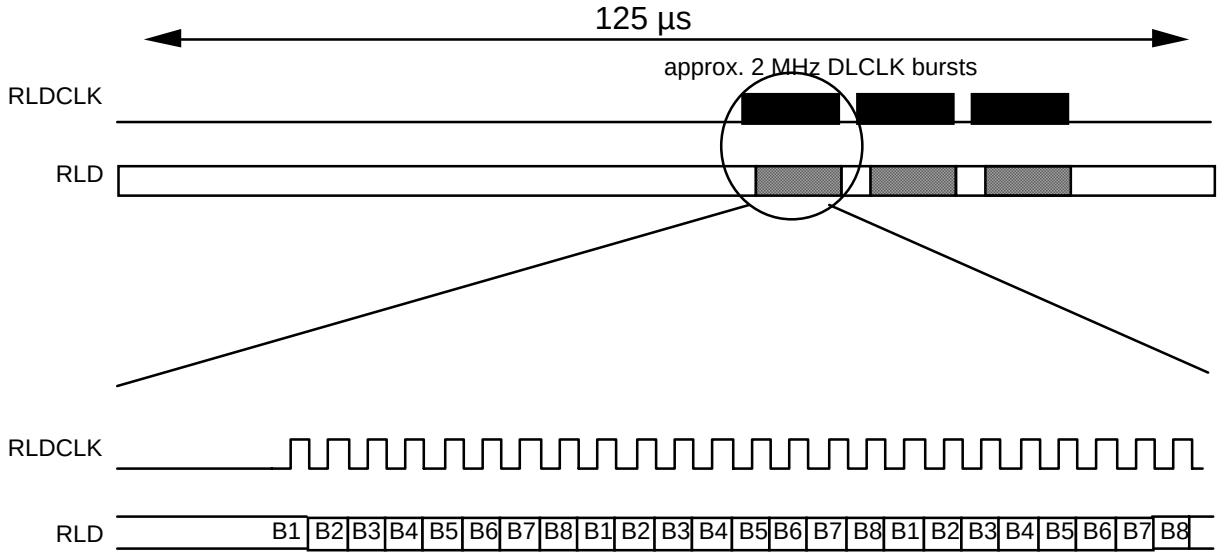
14.1.1.2 Fig. 14.2 GFC Insertion Port



The GFC Insertion Port Diagram illustrates the relationship between the transmit cell

pulse, TCP output and the transmit generic flow control, TGFC input. The MSB (GFC) of the four bit GFC code on the TGFC input is identified using the TCP output. The LASAR-155 accumulates the code and transmits the code in the next transmit cell. If the next transmit cell is an idle/unassigned cell, the GFC code provided in the Idle/Unassigned Cell Header Pattern register is overwritten. If the next transmit cell is sourced from the TALP block , the GFC code inserted by the TALP block is overwritten.

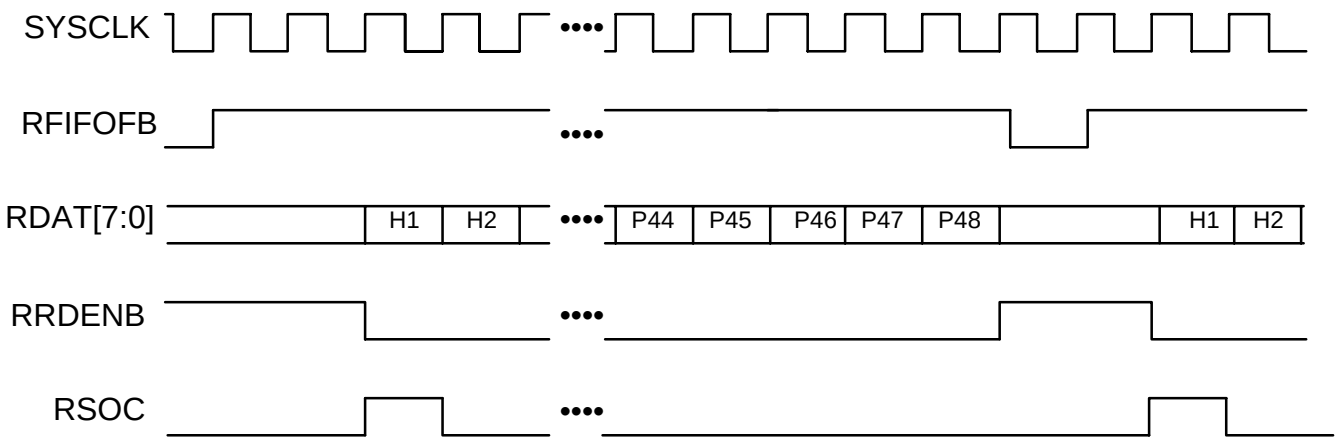
14.1.1.3 Fig. 14.3 SONET Line Overhead Data Link Clock and Data Extraction



The SONET Line Overhead Data Link Clock and Data Extraction timing diagram shows the relationship between the RLD serial data outputs and the associated RLDCLK clock. RLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. RLD is updated on the falling RLDCLK edge.

14.2 Multipurpose Port Interface

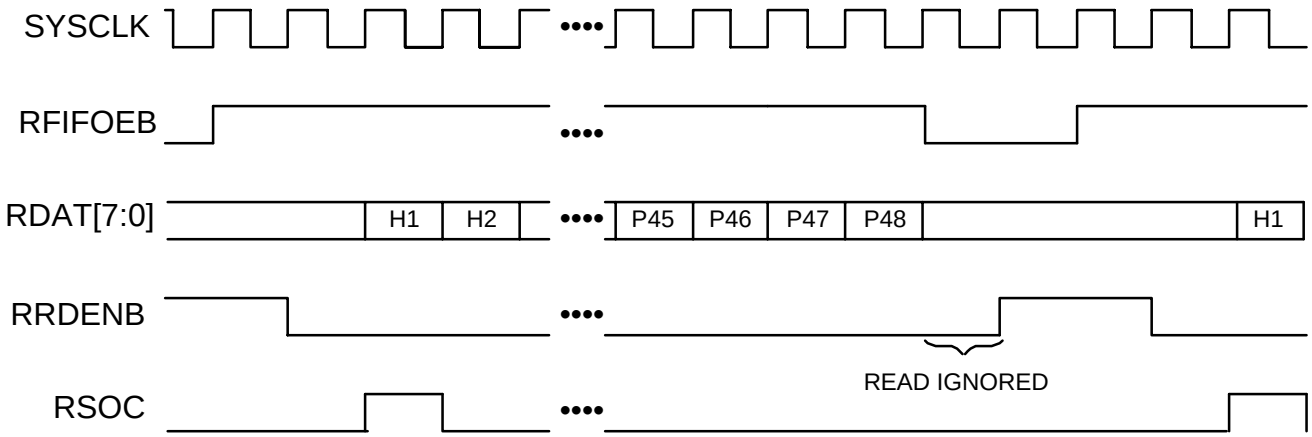
14.2.1.1 Fig. 14.4 Receive Cell Extraction Port (RXPHYBP=0)



The Receive Cell Extract Port (RXPHYBP=0) figure illustrates the LASAR-155's Receive Multipurpose port when configured to source cell to an external device (i.e. a Synchronous FIFO). When RXPHYBP is forced low, pins RSOC and RDAT[7:0] become outputs.

When the active low Receive FIFO Full input, RFIFOFB is deasserted, the LASAR-155 assumes that an external device can accept a byte and forces output RRDENB low to indicate a byte is available on outputs, RDAT[7:0]. At anytime, the external device can throttle back the reception of words by deasserting RFIFOFB. However since the LASAR-155's does not have internal cell storage, throttling is not recommended. If throttling results in an internal overflow, the LASAR-155 will abort bursting out the current cell.

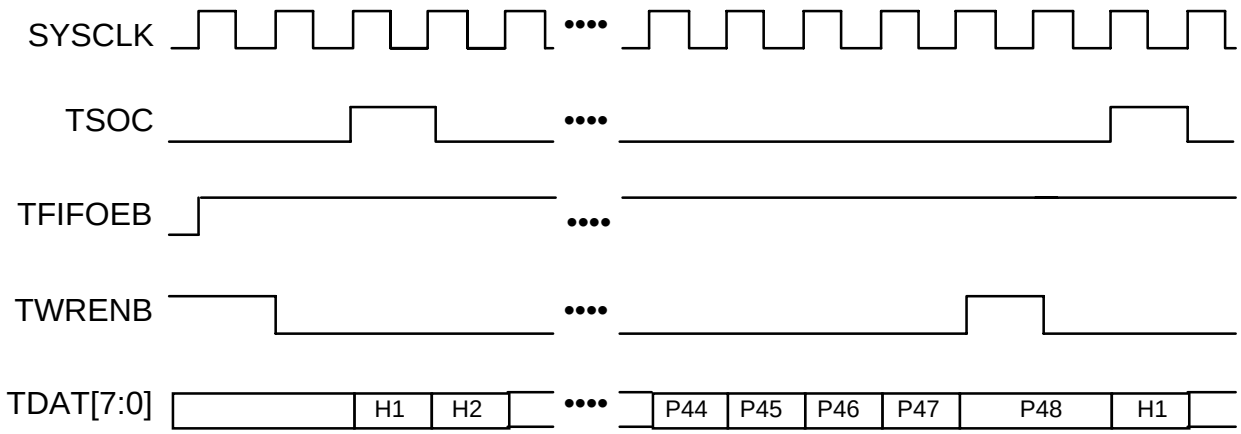
14.2.1.2 Fig. 14.5 Receive External PHY Device (RXPHYBP=1)



The Receive External PHY Device (RXPHYBP=1) figure illustrates the LASAR-155 operating with an external Physical Layer device. Interworking with an external physical layer device is selected by forcing input RXPHYBP high. When RXPHYBP is forced high, pins RSOC and RDAT[7:0] become inputs.

When the active low Receive FIFO Empty input, RFIFOEB is deasserted a cell is available (assuming interworking with a Physical Layer device with a cell based FIFO). RFIFOEB remains high until the Physical Layer device's receive FIFO is empty. RFIFOEB remains low for a minimum of one SYSCLK clock cycle and then can transition high to indicate that there are additional cells available in the Physical Layer device's FIFO. At anytime, the LASAR-155 can throttle back the reception of words by deasserting RRDENB.

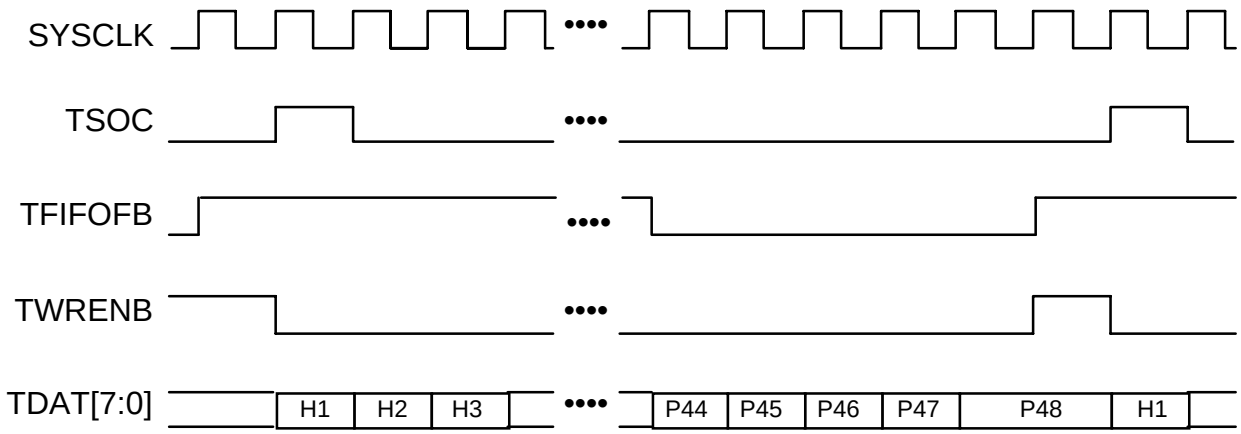
14.2.1.3 Fig. 14.6 Transmit Cell Insertion Port (TXPHYBP=0)



The Transmit Cell Insert Port (TXPHYBP=0) figure illustrates the LASAR-155's Transmit Multipurpose port when configured to sink cell from an external device (i.e. a Synchronous FIFO). When TXPHYBP is forced low, pins TSOC and TDAT[7:0] become inputs.

When the active low Transmit FIFO Empty input, TFIFOEB is deasserted, the LASAR-155 assumes that the external device has data to source and forces output TWRENB low to indicate the LASAR-155 can accept bytes. At anytime, the LASAR-155 can throttle back the external device by deasserting TWRENB.

14.2.1.4 Fig. 14.7 Transmit External PHY Device (TXPHYBP=1)



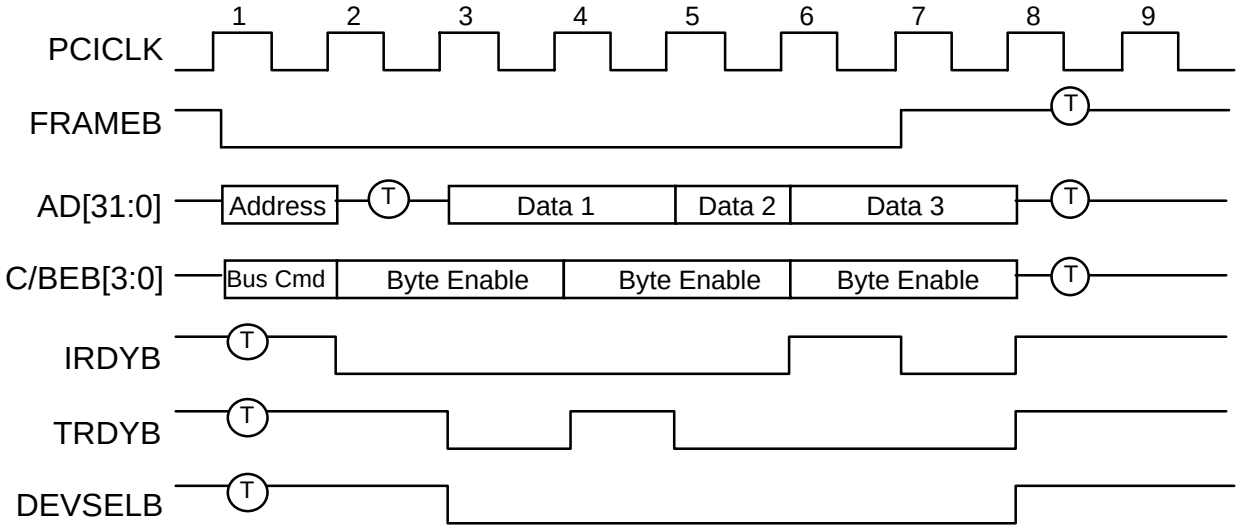
The Transmit External PHY Device (TXPHYBP=1) figure illustrates the LASAR-155 operating with an external Physical Layer device. Interworking with an external physical layer device is selected by forcing input TXPHYBP high. When TXPHYBP is forced high, pins TSOC and TDAT[7:0] become outputs.

If working with an Physical Layer device with cell based FIFOs, when the active low Transmit FIFO Full input, TFIFOFB deasserts high, a space for a cell is available in the Physical Layer device's FIFO. If TFIFOFB is deasserted and the LASAR-155 is ready to write a byte, the LASAR-155 assert TWRENB low. At anytime, if the LASAR-155 does not have a byte to write, it can deassert TWRENB. The LASAR-155 uses output TSOC to indicate the first octet of a cell.

TFIFOFB remains high until the Physical Layer device's transmit FIFO is almost full. Almost full implies that the transmit FIFO can accept at most an additional four writes.

14.3 PCI Interface

14.3.1.1 Fig. 14.8 PCI Read Cycle



A PCI burst read cycle is shown above. The cycle is valid for target and initiator accesses. The target is responsible for incrementing the address during the data burst. The 'T' symbol stands for a turn around cycle. A turn around cycle is required on all signals which can be driven by more than one agent.

During Clock 1, the initiator drives FRAMEB to indicate the start of a cycle. It also drives the address onto the AD[31:0] bus and drives the C/BEB[3:0] lines with the read command. In the above example the command would indicate a burst read. The IRDYB, TRDYB and DEVSELB signals are in turnaround mode (i.e. no agent is driving the signals for this clock cycle). This cycle on the PCI bus is called the address phase.

During Clock 2, the initiator ceases to drive the AD[31:0] bus in order that the target can drive it in the next cycle. The initiator also drives the C/BEB[3:0] lines with the byte enables for the read data. IRDYB is driven active by the initiator to indicate it is ready to accept the data transfer. All subsequent cycles on the PCI bus are called data phases.

During Clock 3, the target claims the transaction by driving DEVSELB active. It also places the first data word onto the AD[31:0] bus and drives TRDYB to indicate to the initiator that the data is valid.

During Clock 4, the initiator latches in the first data word. The target negates TRDYB to indicate to the initiator that it is not ready to transfer another data word.

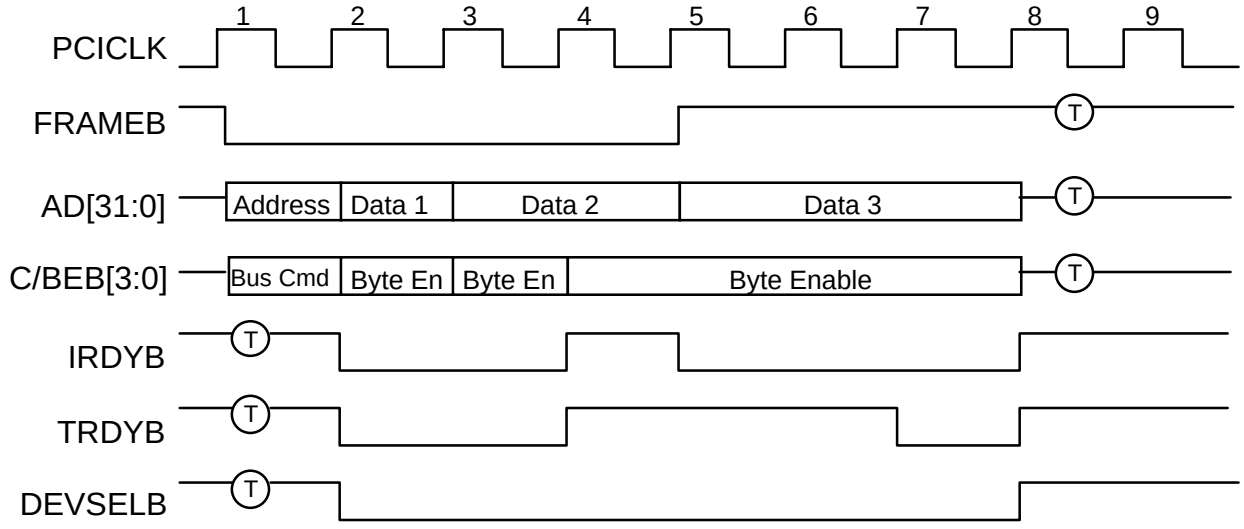
During Clock 5, the target places the second data word onto the AD[31:0] bus and drives TRDYB to indicate to the initiator that the data is valid.

During Clock 6, the initiator latches the second data word and negates IRDYB to indicate to the target that it is not ready for the next transfer. The target shall drive the third data word until the initiator accepts it.

During Clock 7, the initiator asserts IRDYB to indicate to the target it is ready for the third data word. It also negates FRAMEB since this shall be the last transfer.

During Clock 8, the initiator latches in the last word and negates IRDYB. The target, having seen FRAMEB negated in the last clock cycle, negates TRDYB and DEVSELB. All of the above signals shall be driven to their inactive state in this clock cycle, except for FRAMEB which shall be tristated. The target shall stop driving the AD[31:0] bus and the initiator shall stop driving the C/BEB[3:0] bus, this shall be the turnaround cycle for these signals.

14.3.1.2 Fig. 14.9 PCI Write Cycle



The PCI Write Diagram illustrates a PCI burst write transaction. The cycle is valid for target and initiator accesses. The target is responsible for incrementing the address for the duration of the data burst. The 'T' symbol stands for a turn around cycle. A turn around cycle is required on all signals which can be driven by more than one agent.

During clock 1, the initiator drives FRAMEB to indicate the start of a cycle. It also drives the address onto the AD[31:0] bus and drives the C/BEB[3:0] lines with the write command (in the above example the command would indicate a burst write). The IRDYB, TRDYB and DEVSELB signals are in turnaround mode (no agent is driving the signals for this clock cycle). This cycle on the PCI bus is called the address phase.

During clock 2, the initiator ceases to drive the address onto the AD[31:0] bus and starts driving the first data word. The initiator also drives the C/BEB[3:0] lines with the byte enables for the write data. IRDYB is driven active by the initiator to indicate it is ready to accept the data transfer. The target claims the transaction by driving DEVSELB active and drives TRDYB to indicate to the initiator that it is ready to accept the data. All subsequent cycles on the PCI bus are called data phases.

During clock 3, the target latches in the first data word. The initiator starts to drive the next data word onto the AD[31:0] lines.

During clock 4, the target latches in the second data word. Both the initiator and the target indicate that they are not ready to transfer any more data by negating the ready lines.

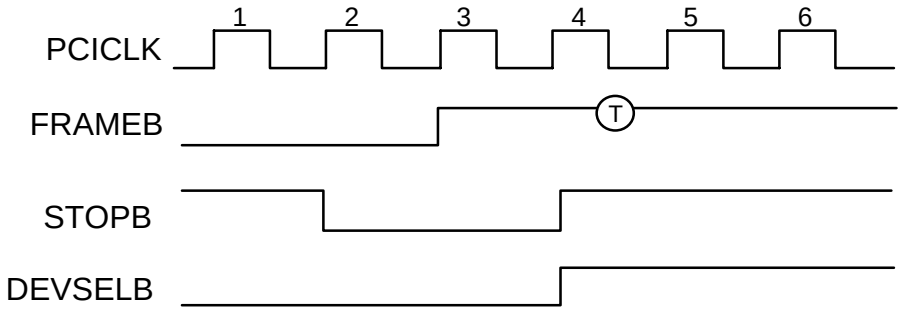
During clock 5, the initiator is ready to transfer the next data word so it drives the AD[31:0] lines with the third data word and asserts IRDYB. The initiator negates FRAMEB since this is the last data phase of this cycle. The target is still not ready so a wait state shall be added.

During clock 6, the target is still not ready so another wait state is added.

During clock 7, the target asserts TRDYB to indicate that it is ready to complete the transfer.

During clock 8, the target latches in the last word and negates TRDYB and DEVSELB, having seen FRAMEB negated previously. The initiator negates IRDYB. All of the above signals shall be driven to their inactive state in this clock cycle except for FRAMEB which shall be tristated.

14.3.1.3 Fig. 14.10 PCI Target Disconnect



The PCI Target Disconnect Diagram illustrates the case when the target wants to prematurely terminate the current cycle. Note, when the LASAR-155 is the target, it never prematurely terminates the current cycle.

A target can terminate the current cycle by asserting the STOPB signal to the initiator. Whether data is transferred or not depends on the state of the ready signals at the time that the target disconnects. If the LASAR-155 is the initiator and the target terminates the current access, the LASAR-155 will retry the access after two PCI bus cycles.

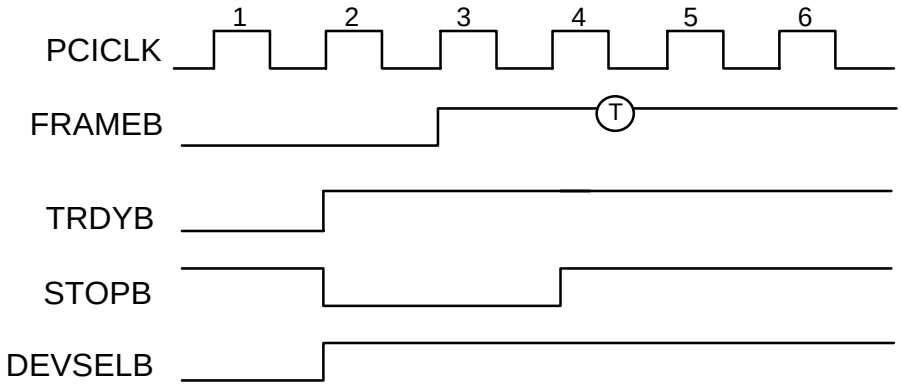
During clock 1, an access is in progress.

During clock 2, the target indicates that it wishes to disconnect by asserting STOPB. Data may be transferred depending on the state of the ready lines.

During clock 3, the initiator negates FRAMEB to signal the end of the cycle.

During clock 4, the target negates STOPB and DEVSELB in response to the FRAMEB signal being negated.

14.3.1.4 Fig. 14.11 PCI Target Abort



The PCI Target Abort Diagram illustrates the case when the target wants to abort the current cycle. Note, when the LASAR-155 is the target, it never abort the current cycle. A target abort is an indication of a serious error and no data is transferred.

A target can terminate the current cycle by asserting STOPB and negating DEVSELB. If the LASAR-155 is the initiator and the target aborts the current access, the abort condition is reported to the PCI Host.

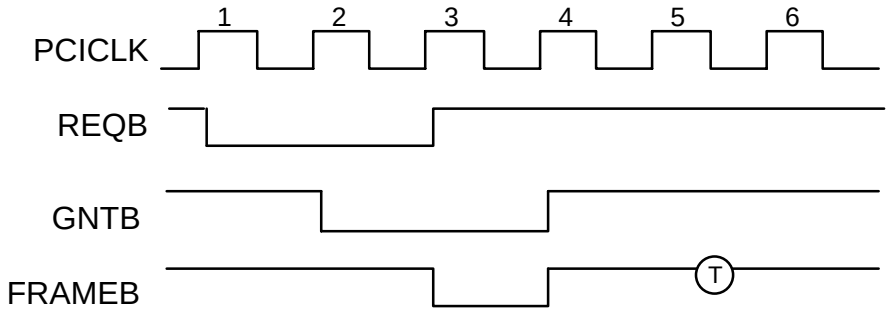
During clock 1, a cycle is in progress.

During clock 2, the target negates DEVSELB and TRDYB and asserts STOPB to indicate an abort condition to the initiator.

During clock 3, the initiator negates FRAMEB in response to the abort request.

During clock 4, the target negates STOPB signal in response to the FRAMEB signal being negated.

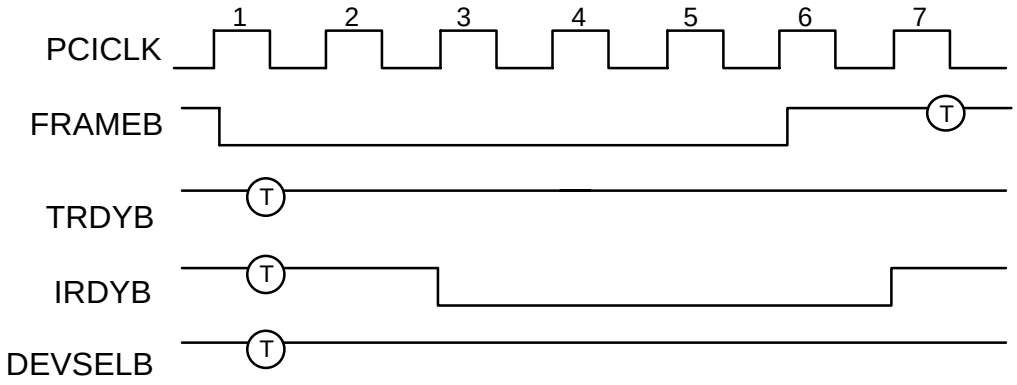
14.3.1.5 Fig. 14.12 PCI Bus Request Cycle



The PCI Bus Request Cycle Diagram illustrates the case when the initiator is requesting the bus from the bus arbiter.

When the LASAR-155 is the initiator, it requests the PCI bus by asserting its REQB output to the central arbiter. The arbiter grants the bus to the LASAR-155 by asserting the GNTB line. The LASAR-155 will wait till both the FRAMEB and IRDYB lines are idle before starting its access on the PCI bus. The arbiter can remove the GNTB signal at any time, but the LASAR-155 will complete the current transfer before relinquishing the bus.

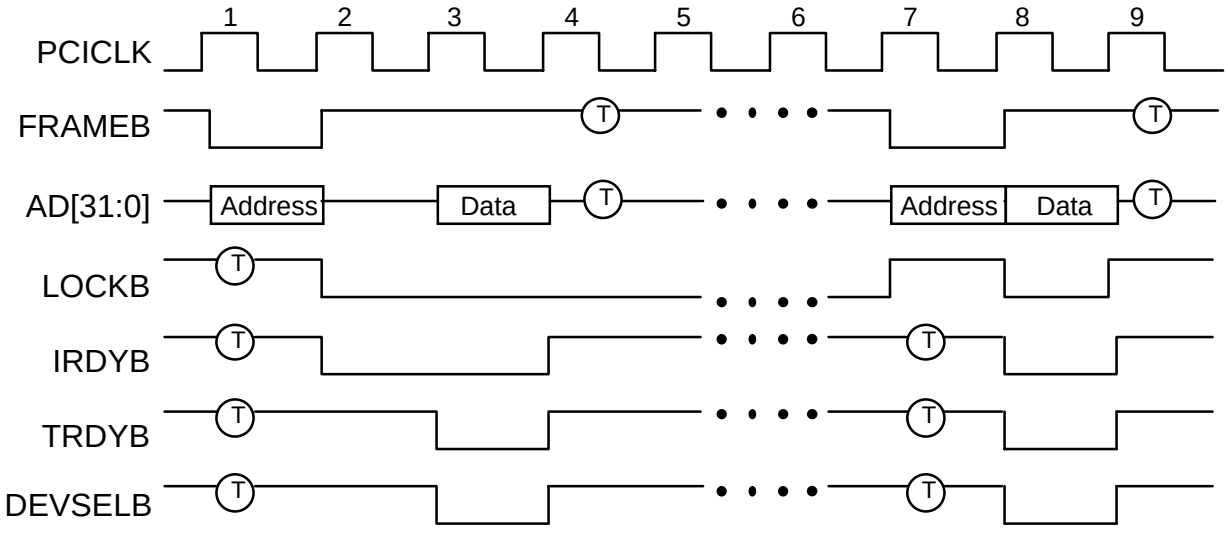
14.3.1.6 Fig. 14.13 PCI Initiator Abort Termination



The PCI Initiator Abort Termination Diagram illustrates the case when the initiator aborts a transaction on the PCI bus.

An initiator may terminate a cycle if no target claims it within five clock cycles. A target may not have responded because it was incapable of dealing with the request or a bad address was generated by the initiator. IRDYB must be valid one clock after FRAMEB is deasserted as in a normal cycle. When the LASAR-155 is the initiator and aborts the transaction, it reports the error condition to the PCI Host.

14.3.1.7 Fig. 14.14 PCI Exclusive Lock Cycle



The PCI Exclusive Lock Cycle Diagram illustrates the case when the current initiator locks the PCI bus. The LASAR-155 will never initiate an lock but will behave appropriately when acting as a target.

During clock 1, the present initiator has gained access of the LOCKB signal and the PCI bus. The first cycle of a locked access must be a read cycle. The initiator asserts FRAMEB and drives the address of the target on the AD[31:0] lines.

During clock 2, the present initiator asserts LOCKB to indicate to the target that a locked cycle is in progress.

During clock 3, the target samples the asserted LOCKB signal and marks itself locked. The data cycle has to complete in order for the lock to be maintained. If for some reason the cycle was aborted, the initiator must negate LOCKB.

During clock 4, the data transfer completes and the target is locked.

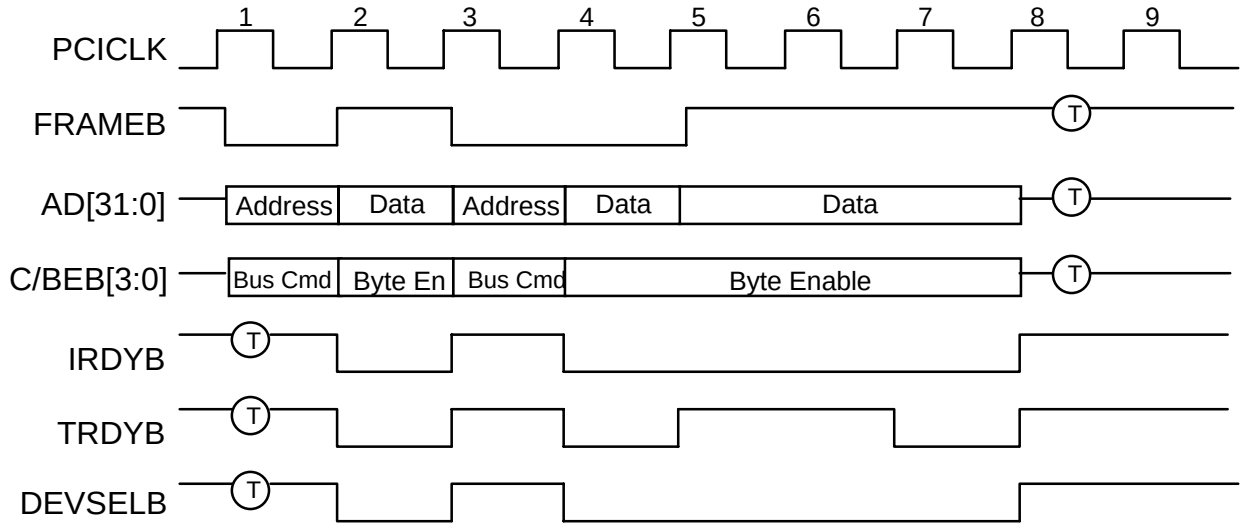
During clock 6, another initiator may use the PCI bus but it cannot use the LOCKB signal. If the other initiator attempts to access the locked target that it did not lock, the target would reject the access.

During clock 7, the same initiator that locked this target accesses the target. The initiator asserts FRAMEB and negates LOCKB to re-establish the lock.

During clock 8, the target samples LOCKB deasserted and locks itself.

During clock 9, the initiator does not want to continue the lock so it negates LOCKB. The target samples LOCKB and FRAMEB deasserted it removes its lock.

14.3.1.8 Fig. 14.15 PCI Fast Back to Back



Fast back-to-back transactions are used by an initiator to conduct two consecutive transactions on the PCI bus without the required idle cycle between them. This can only occur if there is a guarantee that there will be no contention between the initiator or targets involved in the two transactions. In the first case, an initiator may perform fast back-to-back transactions if the first transaction is a write and the second transaction is to the same target. All targets must be able to decode the above transaction. In the second case all of the targets on the PCI bus support fast back-to-back transactions, as indicated in the PCI Status configuration register. The PCID shall only support the first type of fast back-to-back transactions.

During clock 1, the initiator drives FRAMEB to indicate the start of a cycle. It also drives the address onto the AD[31:0] bus and drives the C/BEB[3:0] lines with the write command. In this example the command would indicate a single write. The IRDYB, TRDYB and DEVSELB signals are in turnaround mode and are not being driven for this clock cycle. This cycle on the PCI bus is called the address phase.

During clock 2, the initiator ceases to drive the address onto the AD[31:0] bus and starts driving the data element. The initiator also drives the C/BEB[3:0] lines with the byte enables for the write data. IRDYB is driven active by the initiator to indicate that the data is valid.

The initiator negates FRAMEB since this the last data phase of this cycle. The target claims the transaction by driving DEVSELB active and drives TRDYB to indicate to the initiator that it is ready to accept the data.

During clock 3, the target latches in the data element and negates TRDYB and DEVSELB, having seen FRAMEB negated previously. The initiator negates IRDYB and drives FRAMEB to start the next cycle. It also drives the address onto the AD[31:0] bus and drives the C/BEB[3:0] lines with the write command. In this example the command would indicate a burst write.

During clock 4, the initiator ceases to drive the address onto the AD[31:0] bus and starts driving the first data element. The initiator also drives the C/BEB[3:0] lines with the byte enables for the write data. IRDYB is driven active by the initiator to indicate that the data is valid. The target claims the transaction by driving DEVSELB active and drives TRDYB to indicate to the initiator that it is ready to accept the data.

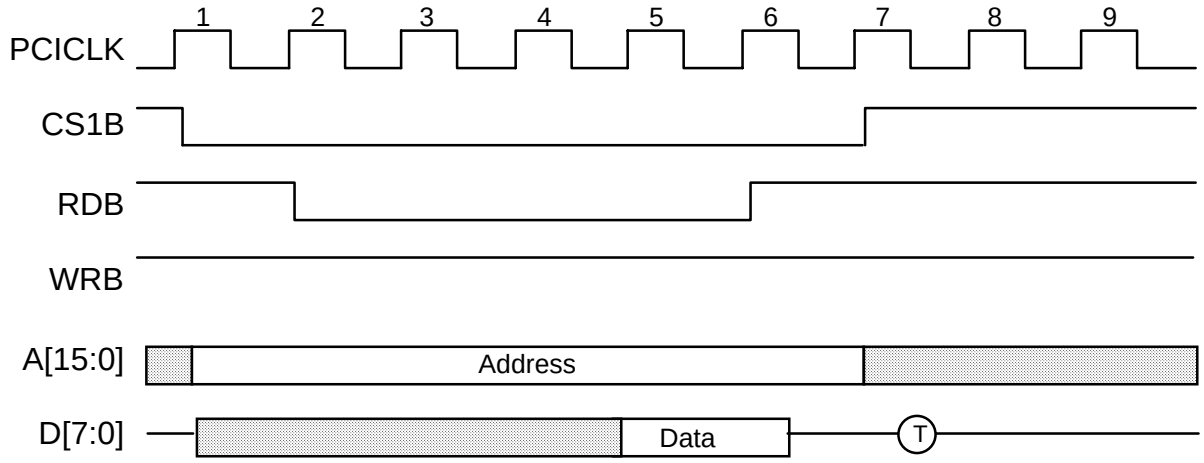
During clock 5, the initiator is ready to transfer the next data element so it drives the AD[31:0] lines with the second data element . The initiator negates FRAMEB since this is the last data phase of this cycle. The target accepts the first data element and negates TRDYB to indicate its is not ready for the next data element.

During clock 6, the target is still not ready so a wait state shall be added.

During clock 7, the target asserts TRDYB to indicate that it is ready to complete the transfer.

During clock 8, the target latches in the last element and negates TRDYB and DEVSELB, having seen FRAMEB negated previously. The initiator negates IRDYB. All of the above signals shall be driven to their inactive state in this clock cycle, except for FRAMEB which shall be tristated. The target stops driving the AD[31:0] bus and the initiator stops driving the C/BEB[3:0] bus. This shall be the turnaround cycle for these signals.

14.3.1.9 Fig. 14.16 Microprocessor Interface Read Cycle (Master Mode)



The LASAR-155 can access its Local Bus when the Microprocessor Interface is configured for master mode operation. A read transaction using CS1B is shown above. The read timing using CS2B is the same as for CS1B. The LASAR-155 Local Bus can support devices with read times of up to 120 ns. Since the timing of the Microprocessor Interface is based on PCICLK, the minimum and maximum read cycle times will depend on the frequency of PCICLK.

During clock 1, the LASAR-155 drives CS1B and outputs the address of the location to be read.

During clock 2, the LASAR-155 drives RDB.

During clock 3, the LASAR-155 waits for the device to output data.

During clock 4, the LASAR-155 waits for the device to output data.

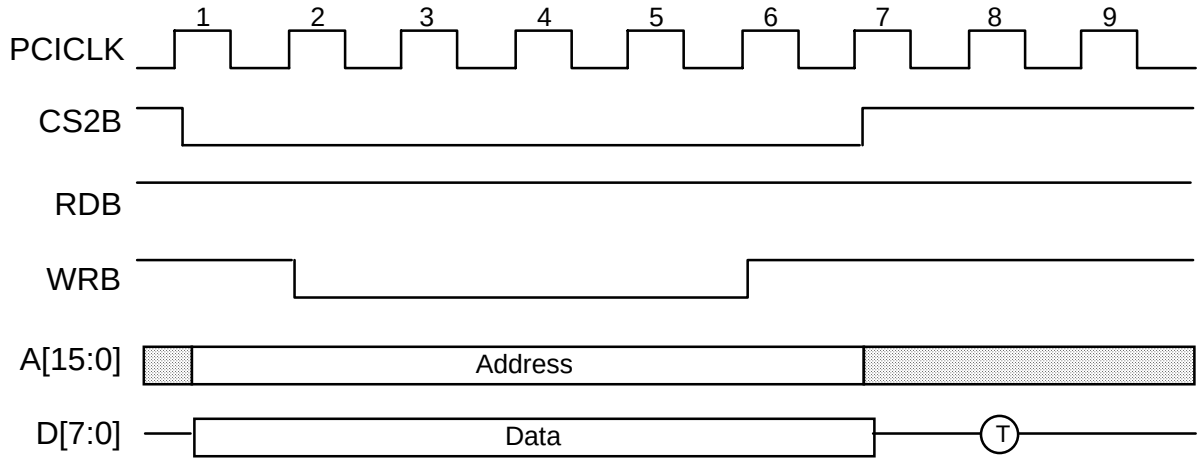
During clock 5, the LASAR-155 waits for the device to output data.

During clock 6, the LASAR-155 latches in the data and negates RDB.

During clock 7, the LASAR-155 negates CS1B and stops outputting a valid address.

During clock 8, the LASAR-155 Local Bus will be idle in this cycle to allow turning around the bus if the next cycle is a write.

14.3.1.10 Fig. 14.17 Microprocessor Interface Write Cycle (Master Mode)



The LASAR-155 can access its Local Bus when the Microprocessor Interface is configured for master mode operation. A write transaction using CS2B is shown above. The write timing using CS1B is the same as for CS2B. The LASAR-155 Local Bus can support devices with write times of up to 120 ns. Since the timing of the Microprocessor Interface is based on PCICLK, the minimum and maximum write cycle times will depend on the frequency of PCICLK.

During clock 1, the LASAR-155 drives CS2B and outputs the address and data for the location to be written to.

During clock 2, the LASAR-155 drives WRB.

During clock 3, the LASAR-155 waits for the device to accept the data.

During clock 4, the LASAR-155 waits for the device to accept the data.

During clock 5, the LASAR-155 waits for the device to accept the data.

During clock 6, the LASAR-155 negates WRB.

During clock 7, the LASAR-155 negates CS2B and stops outputting valid address and data.

During clock 8, the LASAR-155 Local Bus will be idle in this cycle to allow turning around the bus if the next cycle is a read.

15 ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

16 CHARACTERISTICS

(T_C = 0°C to +70°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.5	5	5.5	Volts	Note 4.
A_{VD}	Power Supply	4.5	5	5.5	Volts	Note 4.
V_{IL} (TTL)	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage for TTL inputs.
V_{PIL}	Input Low Voltage (ALOS+/- Only)	A_{VD} - 1.8		A_{VD} - 1.6	Volts	Input LOW Voltage referenced to RAVD3.
V_{IH} (TTL)	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage for TTL inputs.
V_{PIH}	Input High Voltage (ALOS+/- Only)	A_{VD} - 1.0		A_{VD} - 0.8	Volts	Input HIGH Voltage referenced to RAVD3.
V_{PSWG}	Input Voltage Swing (RXD+/-, RRCLK+/-, TRCLK+/- Only)	550			mV	$\|V_{PIH} - V_{PIL}\|$. Only valid for AC coupling.
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	I_{OL} = -4 mA for all outputs except PCI, PCICLKO, TXD+ and TXD-. I_{OL} = -8 mA for PCICLKO. Notes 3, 4.
V_{OH}	Output or Bidirectional High Voltage	V_{DD} - 1.0	4.7		Volts	I_{OH} = 4 mA for all outputs except PCI, PCICLKO, TXD+ and TXD-. I_{OH} = +8 mA for PCICLKO. Notes 3, 4.
V_{TXOL}	Output Low Voltage (TXD+/- Only)			0.4	Volts	I_{OL} = -6 mA for TXD+, and TXD-, Note 5.
V_{TXOH}	Output High Voltage (TXD+/- Only)	3.9			Volts	I_{OH} = 6 mA for TXD+, and TXD-, Note 5.

V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		0.6		Volts	Note 4.
I_{ILPU}	Input Low Current	65	250	525	µA	V_{IL} = GND, Notes 1, 3, 4.
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	All pins except PCICLK. PCICLK pin typical capacitance = 10 pF. Excludes package. Package Typically 2 pF. Note 4.
C_{OUT}	Output Capacitance		5		pF	All pins. Excludes package. Package Typically 2 pF. Note 4.
C_{IO}	Bidirectional Capacitance		5		pF	All pins. Excludes package. Package Typically 2 pF. Note 4.
L_{PIN}	Pin Inductance		20		nH	All PCI pins. Note 4.
I_{DDOP}	Operating Current.			 557 599	 mA mA	V_{DD} = 5.5 V, Outputs Unloaded. TXD+/- = RXD+/- =51.84 Mbit/s, TXD+/- = RXD+/- =155.52 Mbit/s

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.

2. Input pin or bidirectional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.

5. The values for V_{TXOL} and V_{TXOH} ensure a minimum 550 mV swing at the ECL buffer input when the circuit shown in figure 13.1, "Interfacing LASAR-155 to ECL or PECL" is used to attenuate TXD+ and TXD-.

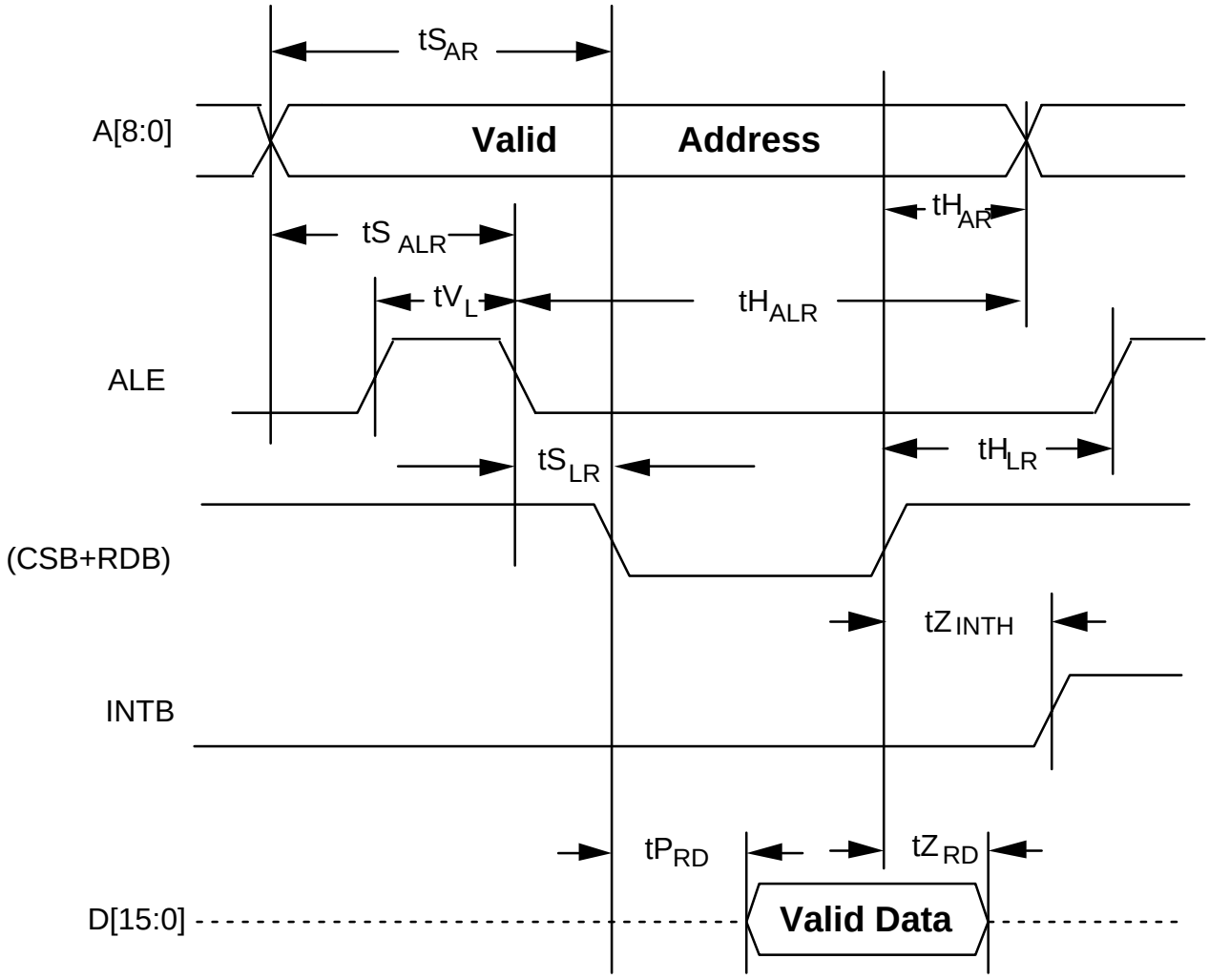
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_C = 0°C to +70°C, V_{DD} = 5 V ±10%)

Microprocessor Interface Slave Read Access (Fig. 17.1)

Symbol	Parameter	Min	Typ	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10			ns
tH_{AR}	Address to Valid Read Hold Time	5			ns
tS_{ALR}	Address to Latch Set-up Time	10			ns
tH_{ALR}	Address to Latch Hold Time	10			ns
tV_L	Valid Latch Pulse Width	20			ns
tS_{LR}	Latch to Read Set-up		0		ns
tH_{LR}	Latch to Read Hold		5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay			70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state			20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50		ns

17.1.1.1 Fig. 17.1 Microprocessor Interface Slave Read Timing



Notes on Microprocessor Interface Slave Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architecture's, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameter tH_{AR} is not applicable if address latching is used.

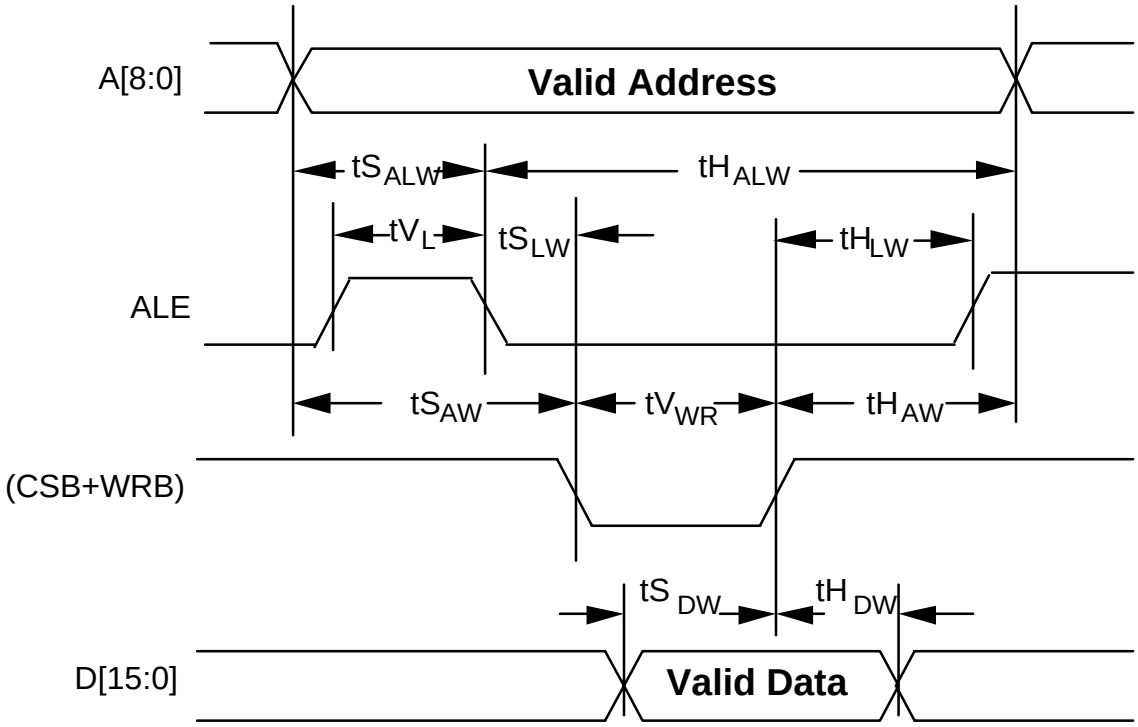
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Microprocessor Interface Slave Write Access (Fig. 17.2)

Symbol	Parameter	Min	Typ	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10			ns
tS_{DW}	Data to Valid Write Set-up Time	20			ns
tS_{ALW}	Address to Latch Set-up Time	10			ns
tH_{ALW}	Address to Latch Hold Time	10			ns
tV_L	Valid Latch Pulse Width	20			ns
tS_{LW}	Latch to Write Set-up		0		ns
tH_{LW}	Latch to Write Hold		5		ns
tH_{DW}	Data to Valid Write Hold Time	5			ns
tH_{AW}	Address to Valid Write Hold Time	5			ns
tV_{WR}	Valid Write Pulse Width	40			ns

17.1.1.2 Fig. 17.2 Microprocessor Interface Slave Write Timing



Notes on Microprocessor Interface Slave Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architecture's, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameter tH_{AW} is not applicable if address latching is used.

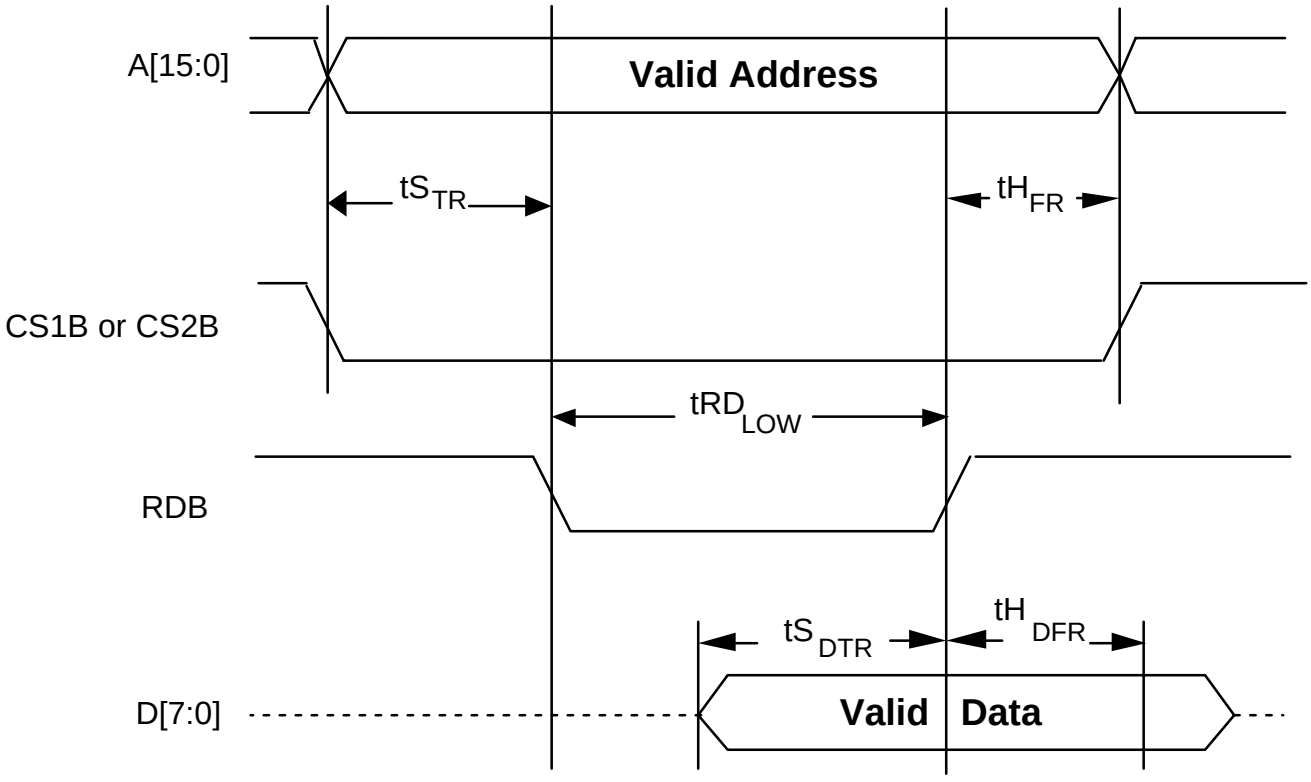
5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Microprocessor Interface Master Read Access (Fig. 17.3)

Symbol	Parameter	Min	Max	Units
T_{CLK}	PCICLK Cycle	30		ns
tS_{TR}	Address and CS1B or CS2B Set-up to Read low	T_{CLK}-5		ns
tH_{FR}	Address and CS1B or CS2B Hold Time from Read high	T_{CLK}-5		ns
tRD_{LOW}	Read low pulse width	4*T_{CLK}-9		ns
tS_{DTR}	Data Set-up to Read high	30		ns
tH_{DFR}	Data Hold from read high	0		ns

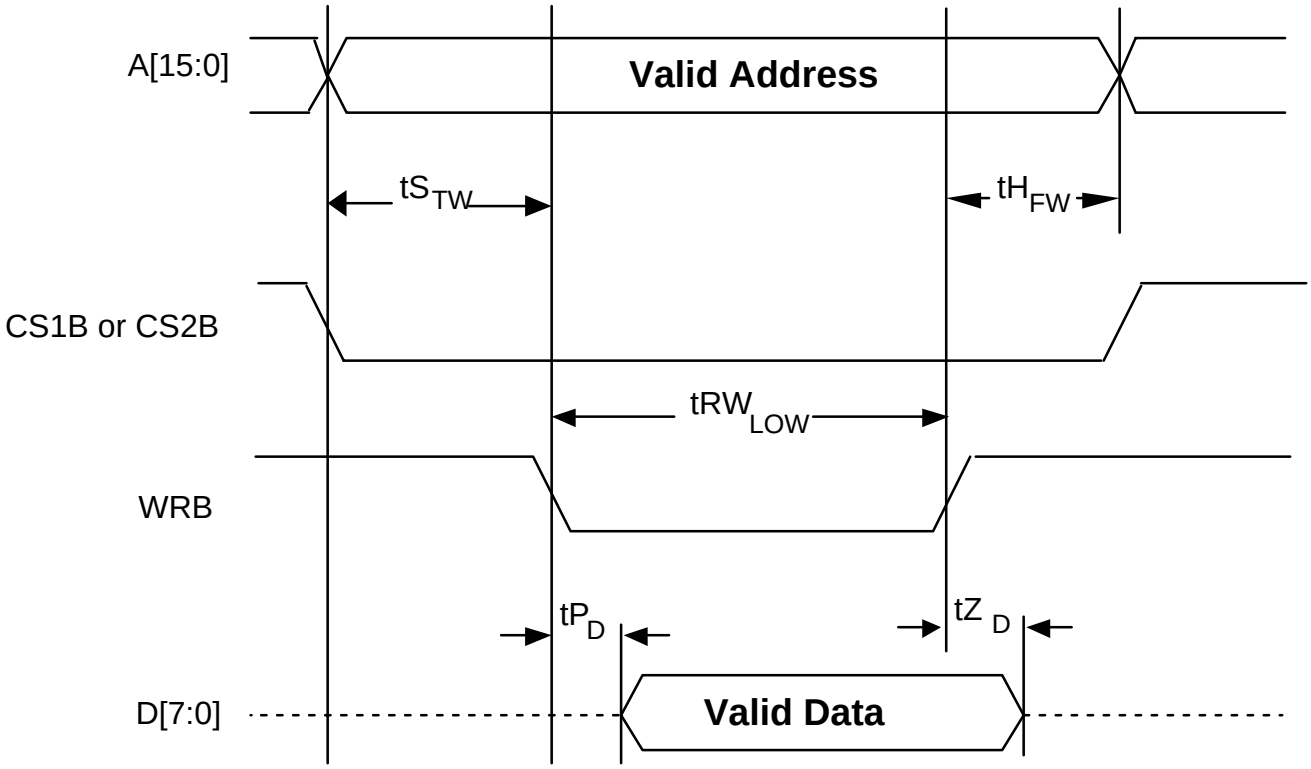
17.1.1.3 Fig. 17.3 Microprocessor Interface Master Read Timing



Microprocessor Interface Master Write Access (Fig. 17.4)

Symbol	Parameter	Min	Max	Units
T_{CLK}	PCICLK Cycle	30		ns
tS_{TW}	Address and CS1B or CS2B Set-up to Write low	T_{CLK}-5		ns
tH_{FW}	Address and CS1B or CS2B Hold Time from Write high	T_{CLK}-5		ns
tWR_{LOW}	Write low pulse width	4*T_{CLK}-9		ns
tP_D	Write low pulse to data valid		10	ns
tZ_D	Write high to data Tri-state	TCLK-5		ns

17.1.1.4 Fig. 17.4 Microprocessor Interface Master Write Timing



18 LASAR-155 TIMING CHARACTERISTICS

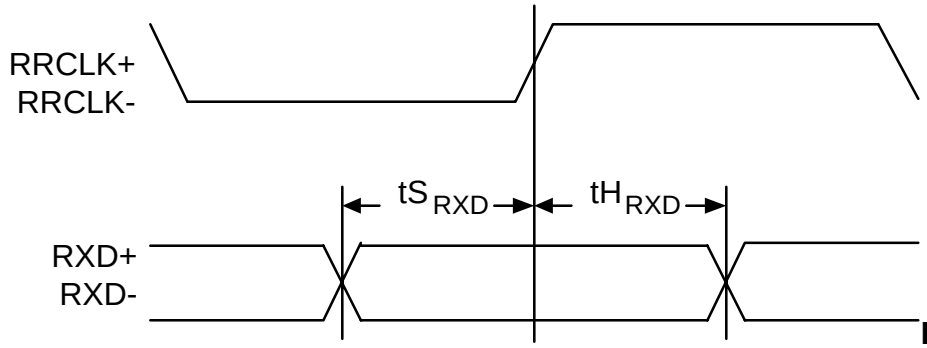
(T_C = 0°C to +70°C, V_{DD} = 5 V ±10%)

Line Side Receive Interface (Fig. 18.1)

Symbol	Description	Min	Max	Units
	RRCLK+/RRCLK- Duty Cycle 51.84 or 155.52 MHz (RBYP bit high) 19.44 or 6.48 MHz (RBYP bit low)	 45 30	 55 70	 %
	RRCLK+/RRCLK- Frequency Tolerance†	-20	+20	ppm
tS_{RXD}	RXD+/RXD- Setup time to RRCLK+/RRCLK- (RBYP bit high)	2		ns
tH_{RXD}	RXD+/RXD- Hold time to RRCLK+/RRCLK- (RBYP bit high)	1		ns

† The specification may be relaxed to +/- 50 ppm if the LASAR-155 is not loop timed or is used for a private UNI (LAN) interface.

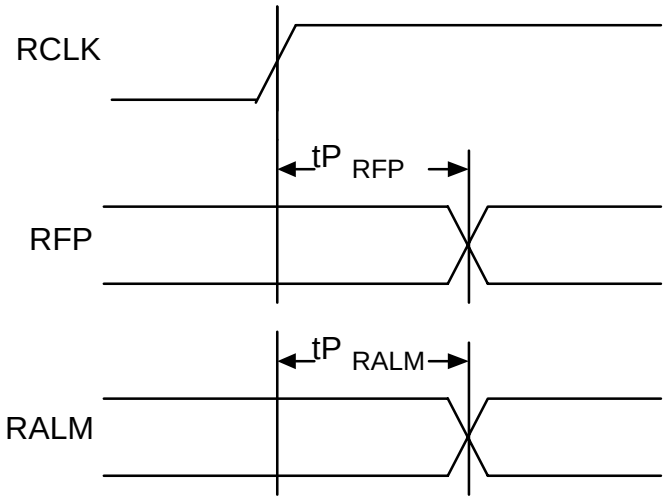
18.1.1.1 Fig. 18.1 Line Side Receive Interface Timing



Receive Line Output (Fig. 18.2)

Symbol	Description	Typical	Units
tP_{RFP}	RCLK High to RFP Valid	1	ns
tP_{RALM}	RCLK High to RALM Valid	1	ns

18.1.1.2 Fig. 18.2 Receive Output Timing

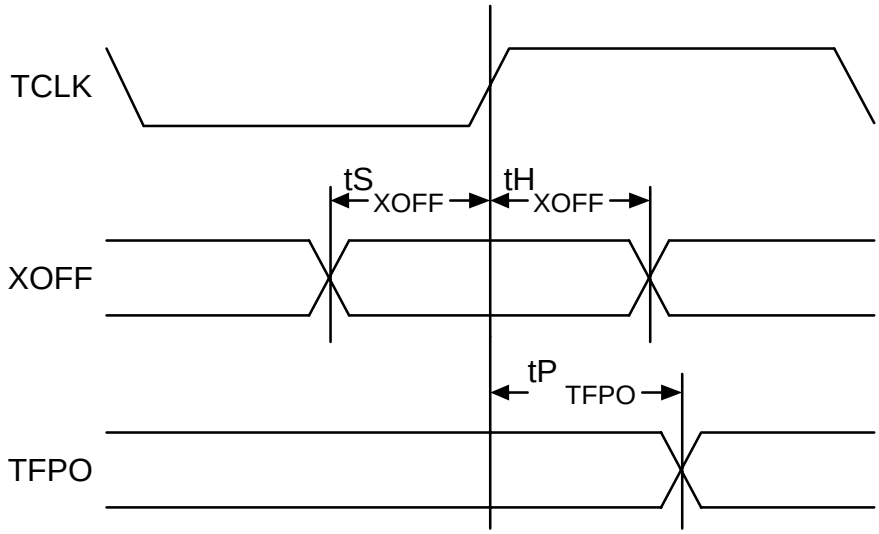


Line Side Transmit Interface (Fig. 18.3)

Symbol	Description	Min	Typ	Max	Units
	TRCLK+/TRCLK- Duty Cycle 51.84 or 155.52 MHz (TBYP high) 19.44 or 6.48 MHz (TBYP low)	 45 30		 55 70	 %
	TRCLK+/TRCLK- Frequency Tolerance †	-20		+20	ppm
tS_{XOFF}	XOFF Setup time to TCLK		8		ns
tH_{XOFF}	XOFF Hold time to TCLK		1		ns
tPT_{FPO}	TCLK High to TFPO Valid		1		ns
$tP_{TXDdiff}$	TXC+/TXC- Low to TXD+/TXD- Valid		-2 to 2		ns
tP_{TXDneg}	TXC+ Low to TXD+ Valid		-3 to 2		ns
tP_{TXDpos}	TXC- High to TXD+ Valid		-2 to 3		ns

† The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET free run accuracy specification.

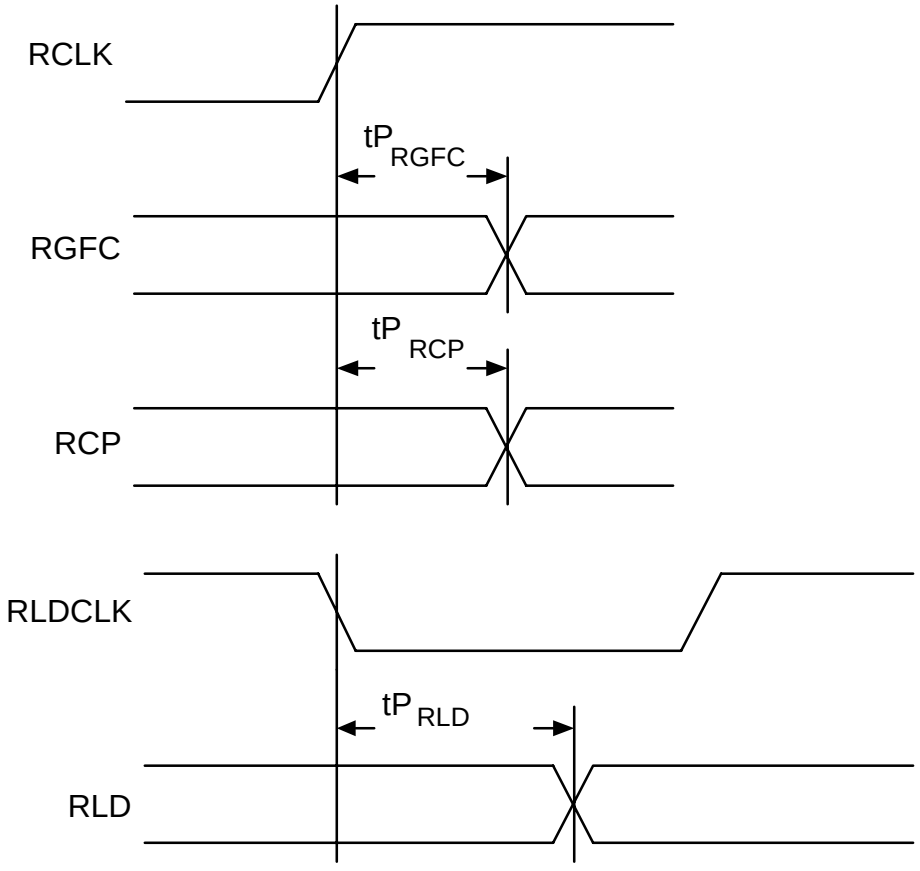
18.1.1.3 Fig. 18.3 Line Side Transmit Interface Timing


TCLK
tS
XOFF
tH
XOFF
XOFF
tP
TFPO
TFPO

GFC Extract and Receive Line Datalink Port (Fig. 18.4)

Symbol	Description	Typical	Units
tP_{RGFC}	RCLK High to RGFC Valid	2	ns
tP_{RCP}	RCLK High to RCP Valid	2	ns
tP_{RLD}	RLDCLK Low to RLD Valid	0	ns

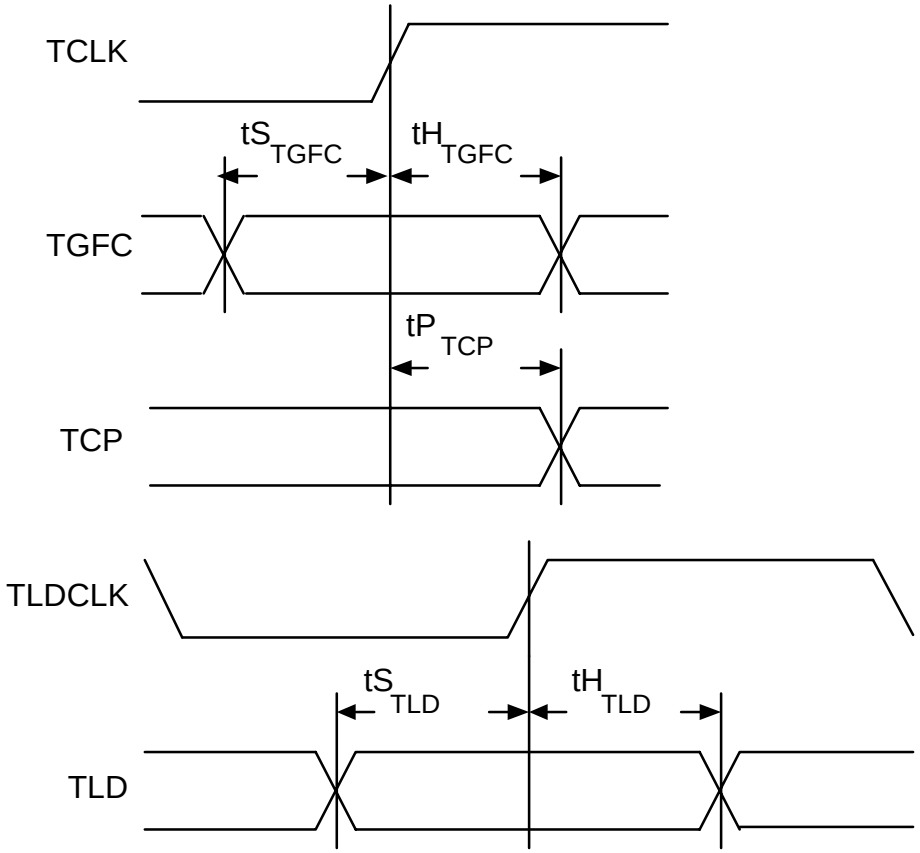
18.1.1.4 Fig. 18.4 GFC Extract and Receive Line Datalink Port Timing



GFC Insert and Transmit Line Datalink Port (Fig. 18.5)

Symbol	Description	Typical	Units
tS_{TGFC}	TGFC Set-up time to TCLK	8	ns
tH_{TGFC}	TGFC Hold time to TCLK	1	ns
tP_{TCP}	TCLK High to TCP Valid	5	ns
tS_{TLD}	TLD Set-up Time to TLDCLK	11	ns
tH_{TLD}	TLD Hold Time to TLDCLK	10	ns

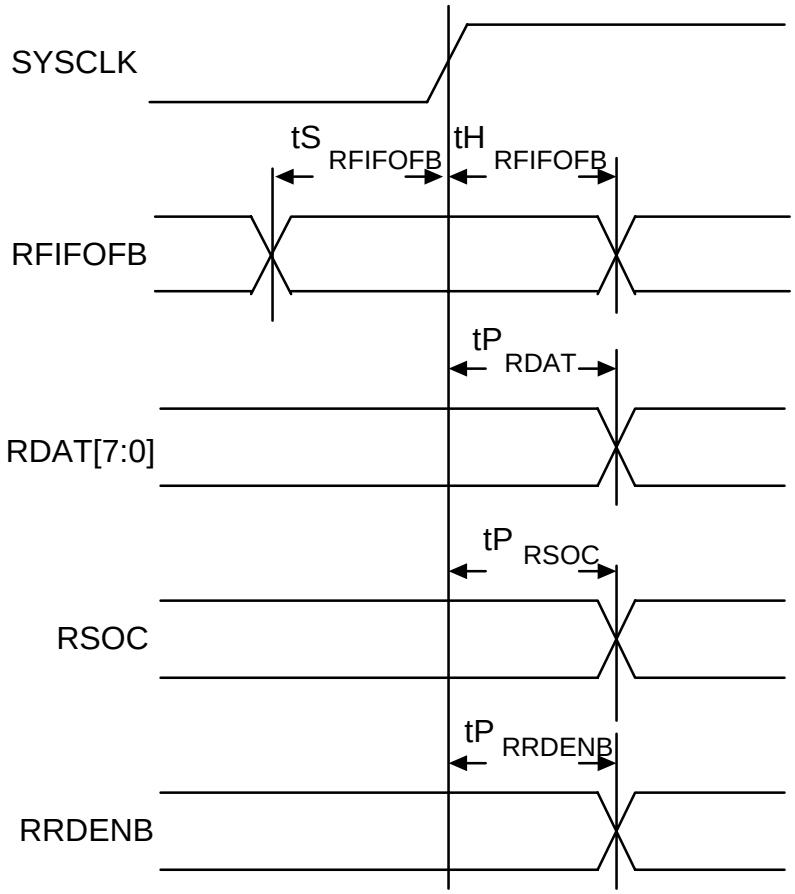
18.1.1.5 Fig. 18.5 GFC Insert and Transmit Line Datalink Timing



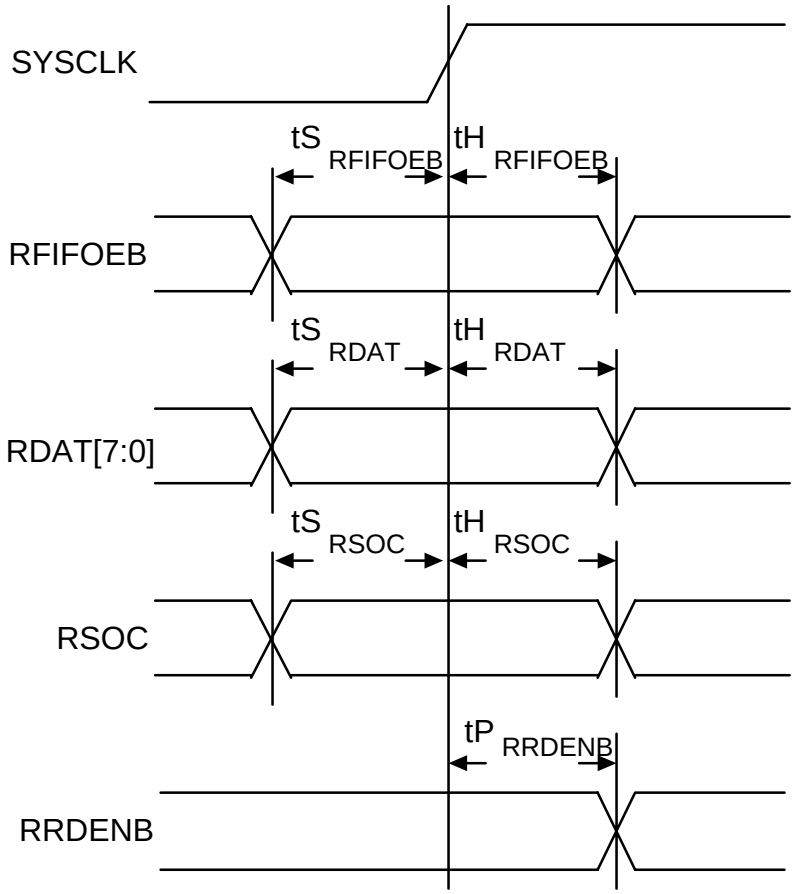
Receive Multipurpose Port (Fig. 18.6 and Fig. 18.7)

Symbol	Description	Min	Typ	Max	Units
	SYSCLK Frequency	25		33	MHz
	SYSCLK Duty Cycle	45		55	%
$tS_{RFIFOFB}$	RFIFOFB/RFIFOEB to SYSCLK High Setup	10			ns
$tH_{RFIFOFB}$	RFIFOFB/RFIFOEB High to SYSCLK Hold	1			ns
tS_{RDAT}	RDAT[7:0] to SYSCLK High Setup	10			ns
tH_{RDAT}	RDAT[7:0] High to SYSCLK Hold		1		ns
tP_{RDAT}	SYSCLK High to RDAT[7:0] Valid	2		26	ns
tS_{RSOC}	RSOC to SYSCLK High Setup	10			ns
tH_{RSOC}	RSOC High to SYSCLK Hold		9		ns
tP_{RSOC}	SYSCLK High to RSOC Valid	2		26	ns
tP_{RRDENB}	SYSCLK High to RRDENB Valid		15		ns

18.1.1.6 Fig. 18.6 Receive Multipurpose Port (RXPHYBP=0) Timing



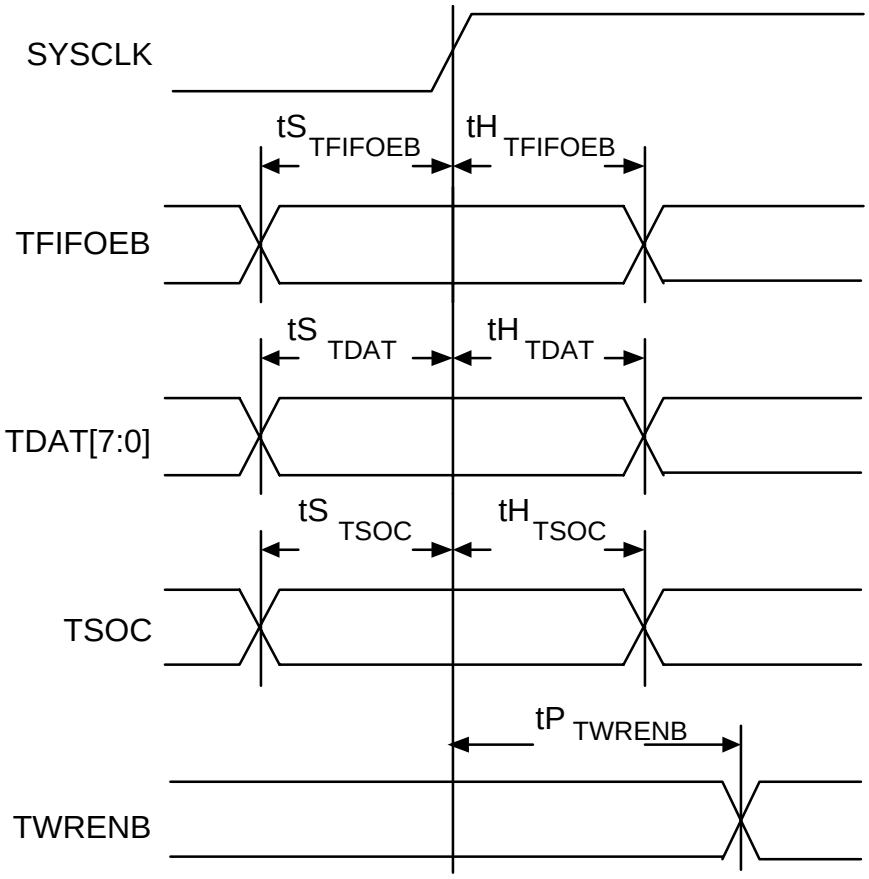
18.1.1.7 Fig. 18.7 Receive Multipurpose Port (RXPHYBP=1) Timing



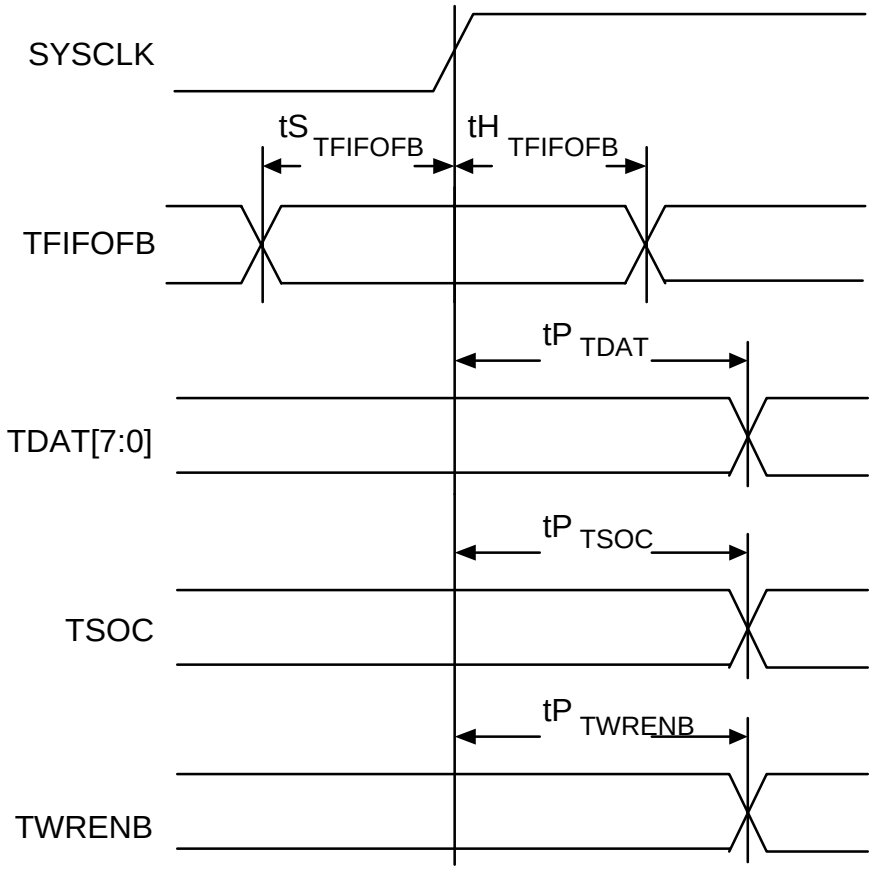
Transmit Multipurpose Port (Fig. 18.8 and Fig. 18.9)

Symbol	Description	Min	Max	Units
$tS_{TFIFOFB}$	TFIFOEB/TFIFOFB Set-up time to SYSCLK	10		ns
$tH_{TFIFOFB}$	TFIFOEB/TFIFOFB Hold time to SYSCLK	1		ns
tS_{TDAT}	TDAT[7:0] Set-up time to SYSCLK	10		ns
tH_{TDAT}	TDAT[7:0] Hold time to SYSCLK	1		ns
tP_{TDAT}	SYSCLK to TDAT Valid	2	26	ns
tS_{TSOC}	TSOC Set-up time to SYSCLK	10		ns
tH_{TSOC}	TSOC Hold time to SYSCLK	1		ns
tP_{TSOC}	SYSCLK to TSOC Valid	2	26	ns
tP_{TWRENB}	SYSCLK to TWRENB Valid	2	26	ns

18.1.1.8 Fig. 18.8 Transmit Multipurpose Port (TXPHYBP=0) Timing



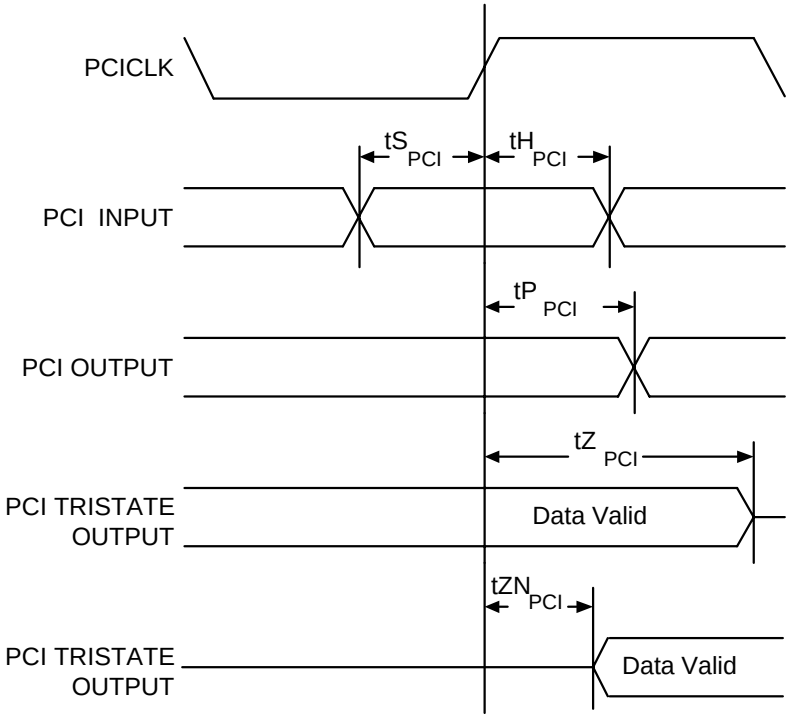
18.1.1.9 Fig. 18.9 Transmit Multipurpose Port (TXPHYBP=1) Timing



PCI Interface (Fig. 18.10)

Symbol	Description	Min	Typical	Max	Units
	PCICLK Frequency			33	MHz
	PCICLK Duty Cycle	40		60	%
tS_{PCI}	All PCI Input and Bidirectional Set-up time to PCICLK	7			ns
tH_{PCI}	All PCI Output and Bidirectional Hold time to PCICLK		0		ns
tP_{PCI}	PCICLK to all PCI Outputs Valid	2		11	ns
tP_{PCI}	PCICLK to PCI PCIINTB, PERRB, STOPB, CBEB, AD Outputs Valid		10		ns
tZ_{PCI}	All PCI Output PCICLK to Tri-state			28	ns
tZN_{PCI}	All PCI Output Tri-state from PCICLK to active	2			ns

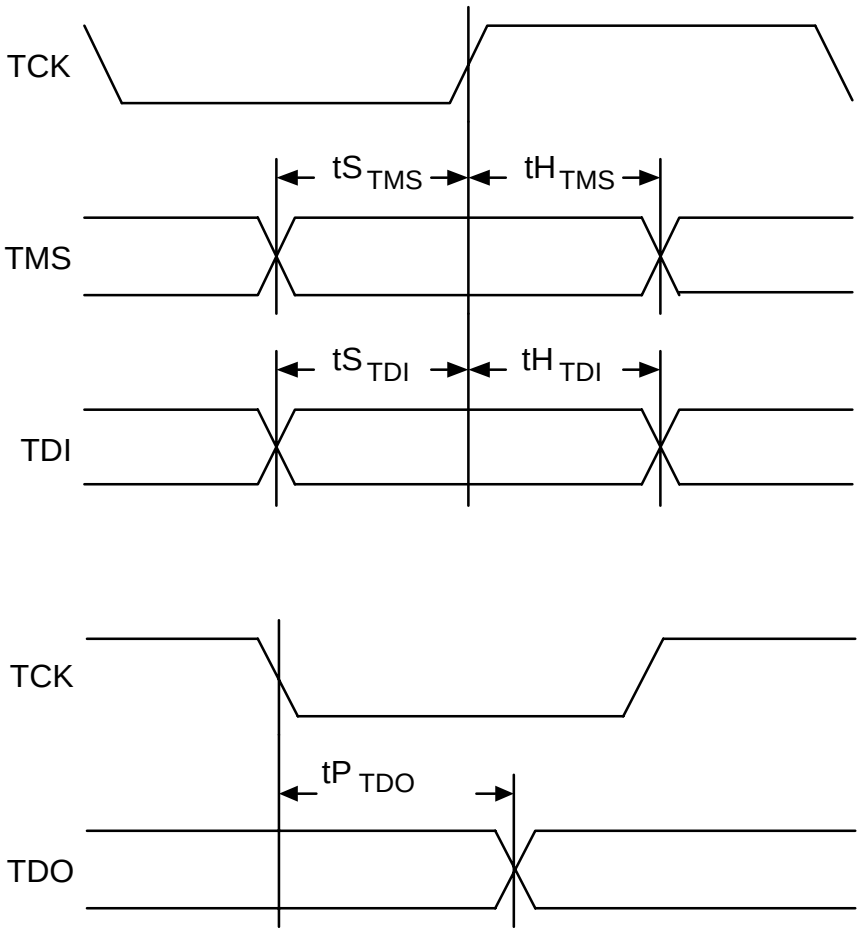
18.1.1.10 Fig. 18.10 PCI Interface Timing



JTAG Port Interface (Fig. 18.11)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

18.1.1.11 Fig. 18.11 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. When a set-up time is specified between a PECL input and a PECL clock, the set-up time is the time in nanoseconds from the crossing point of the differential input to the crossing point of the differential clock.

4. When a hold time is specified between a PECL input and a PECL clock, the hold time is the time in nanoseconds from the crossing point of the differential clock to the crossing point of the differential input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs, except for TXD+/- , TDAT, RDAT, and all PCI Bus outputs. Maximum and minimum output propagation delays for TXD+/- , TDAT and RDAT are specified with a 30 pF load. For PCI Bus outputs, maximum output propagation delays are measured with a 50 pF load while minimum output propagation delays are measured with a 0 pF load.

3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pf to GND.

4. Differential output propagation delay time is the time in nanoseconds from the crossing point of the reference signal to the crossing point of the output.

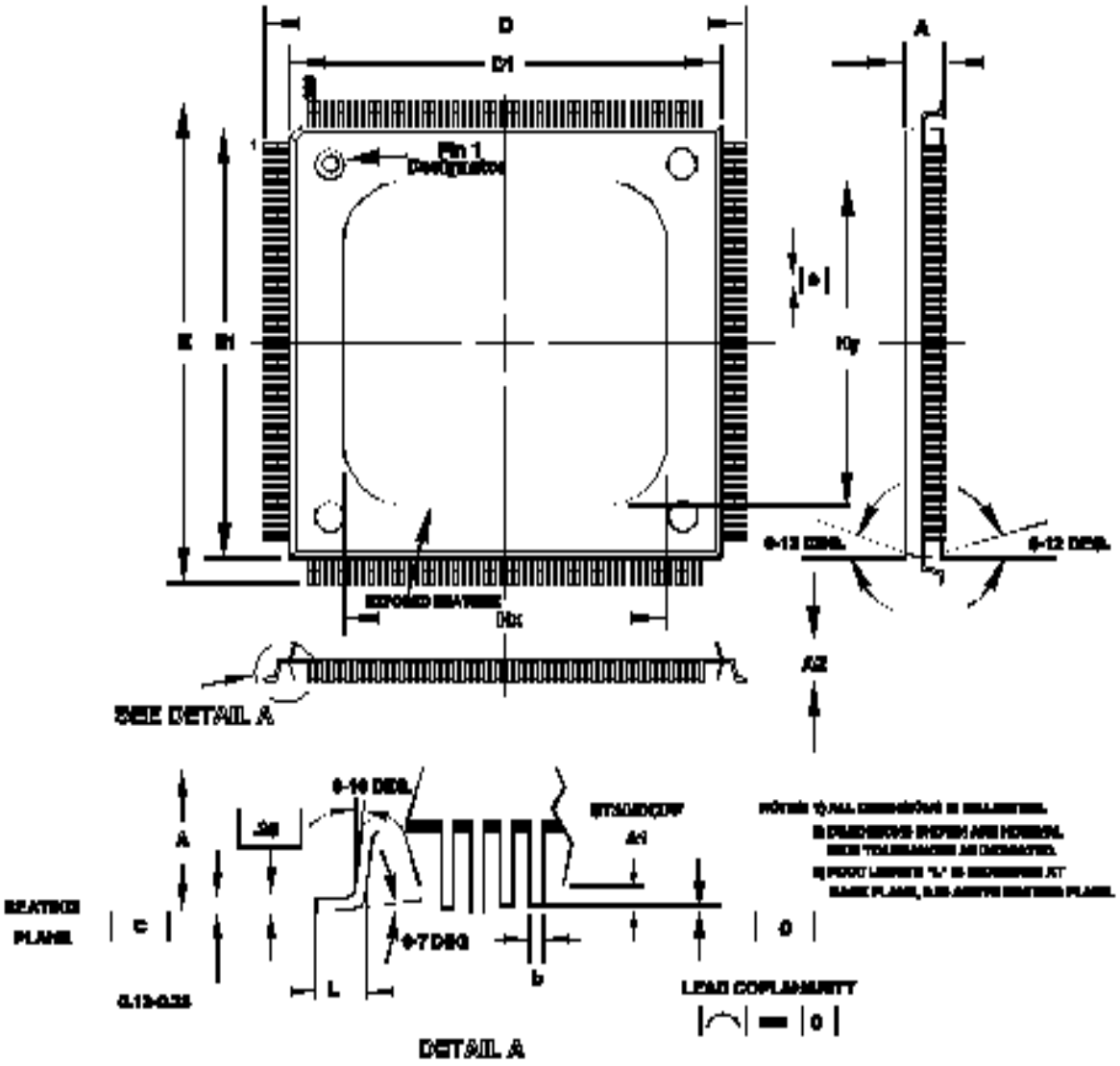
19 ORDERING AND THERMAL INFORMATION

PART NO.	DESCRIPTION
PM7375-SC	208 Slugged Plastic Quad Flat Pack (PQFP)

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM7375-SC	0°C to 70°C	24 °C/W	8 °C/W

20 MECHANICAL INFORMATION

20.1.1.1 Fig. 20.1 208 Pin Slugged Plastic Quad Flat Pack



Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc	Hx	Hy
Min.													
Nom.													
Max.													

NOTES

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