Features

- High Performance, Low Power AVR®32 UC 32-Bit Microcontroller
  - Compact Single-cycle RISC Instruction Set Including DSP Instruction Set
  - Read-Modify-Write Instructions and Atomic Bit Manipulation
  - Performing 1.38 DMIPS / MHz
    - Up to 75 DMIPS Running at 60 MHz from Flash
    - Up to 45 DMIPS Running at 33 MHz from Fash
  - Memory Protection Unit
- Multi-hierarchy Bus System
  - High-Performance Data Transfers on Separate Buses for IIncreased Performance
  - 7 Peripheral DMA Channels Improves Speed for Peripheral Communication
- Internal High-Speed Flash
  - 256K Bytes, 128K Bytes, 64K Bytes Versions
  - Single Cycle Access up to 30 MHz
  - Prefetch Buffer Optimizing Instruction Execution at Maximum Speed
  - 4ms Page Programming Time and 8ms Full-Chip Erase Time
  - 100,000 Write Cycles, 15-year Data Retention Capability
  - Flash Security Locks and User Defined Configuration Area
- Internal High-Speed SRAM, Single-Cycle Access at Full Speed
  - 32K Bytes (256KB and 128KB Flash), 16K Bytes (64KB Flash)
- Interrupt Controller
  - Autovectored Low Latency Interrupt Service with Programmable Priority
- System Functions
  - Power and Clock Manager Including Internal RC Clock and One 32KHz Oscillator
  - Two Multipurpose Oscillators and Two Phase-Lock-Loop (PLL) allowing Independant CPU Frequency from USB Frequency
  - Watchdog Timer, Real-Time Clock Timer
- Universal Serial Bus (USB)
  - Device 2.0 Full/Low Speed and On-The-Go (OTG)
  - Flexible End-Point Configuration and Management with Dedicated DMA Channels
  - On-chip Transceivers Including Pull-Ups
  - USB Wake Up from Sleep Functionality
- One Three-Channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, PWM, Capture and Various Counting Capabilities
- One 7-Channel 16-bit Pulse Width Modulation Controller (PWM)
- Three Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Independant Baudrate Generator, Support for SPI, IrDA and ISO7816 interfaces
  - Support for Hardware Handshaking, RS485 Interfaces and Modem Line
- One Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals
- One Synchronous Serial Protocol Controller
  - Supports I2S and Generic Frame-Based Protocols
- One Master/Slave Two-Wire Interface (TWI), 400kbit/s I2C-compatible
- One 8-channel 10-bit Analog-To-Digital Converter
- On-Chip Debug System (JTAG interface)
  - Nexus Class 2+, Runtime Control, Non-Intrusive Data and Program Trace
- 64-pin TQFP/QFN (44 GPIO pins), 48-pin TQFP/QFN (28 GPIO pins)
- 5V Input Tolerant I/Os, including 4 high-drive pins.
- Single 3.3V Power Supply or Dual 1.8V-3.3V Power Supply

AVR®32 32-Bit Microcontroller

AT32UC3B0256
AT32UC3B0128
AT32UC3B064
AT32UC3B1256
AT32UC3B1128
AT32UC3B164

Preliminary

Summary

32059GS–AVR32–04/08

1. Description

The AT32UC3B is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 60 MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems.

Higher computation capability is achieved using a rich set of DSP instructions.

The AT32UC3B incorporates on-chip Flash and SRAM memories for secure and fast access.

The Peripheral Direct Memory Access controller enables data transfers between peripherals and memories without processor involvement. PDC drastically reduces processing overhead when transferring continuous and large data streams between modules within the MCU.

The Power Manager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The Timer/Counter includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

The PWM modules provides seven independent channels with many configuration options including polarity, edge alignment and waveform non overlap control. One PWM channel can trigger ADC conversions for more accurate close loop control implementations.

The AT32UC3B also features many communication interfaces for communication intensive applications. In addition to standard serial interfaces like UART, SPI or TWI, other interfaces like flexible Synchronous Serial Controller and USB are available.

The Synchronous Serial Controller provides easy access to serial communication protocols and audio standards like I2S, UART or SPI.

The Full-Speed USB 2.0 Device interface supports several USB Classes at the same time thanks to the rich End-Point configuration. The On-The-GO (OTG) Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor.

AT32UC3B integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control. The Nanotrace interface enables trace feature for JTAG-based debuggers.

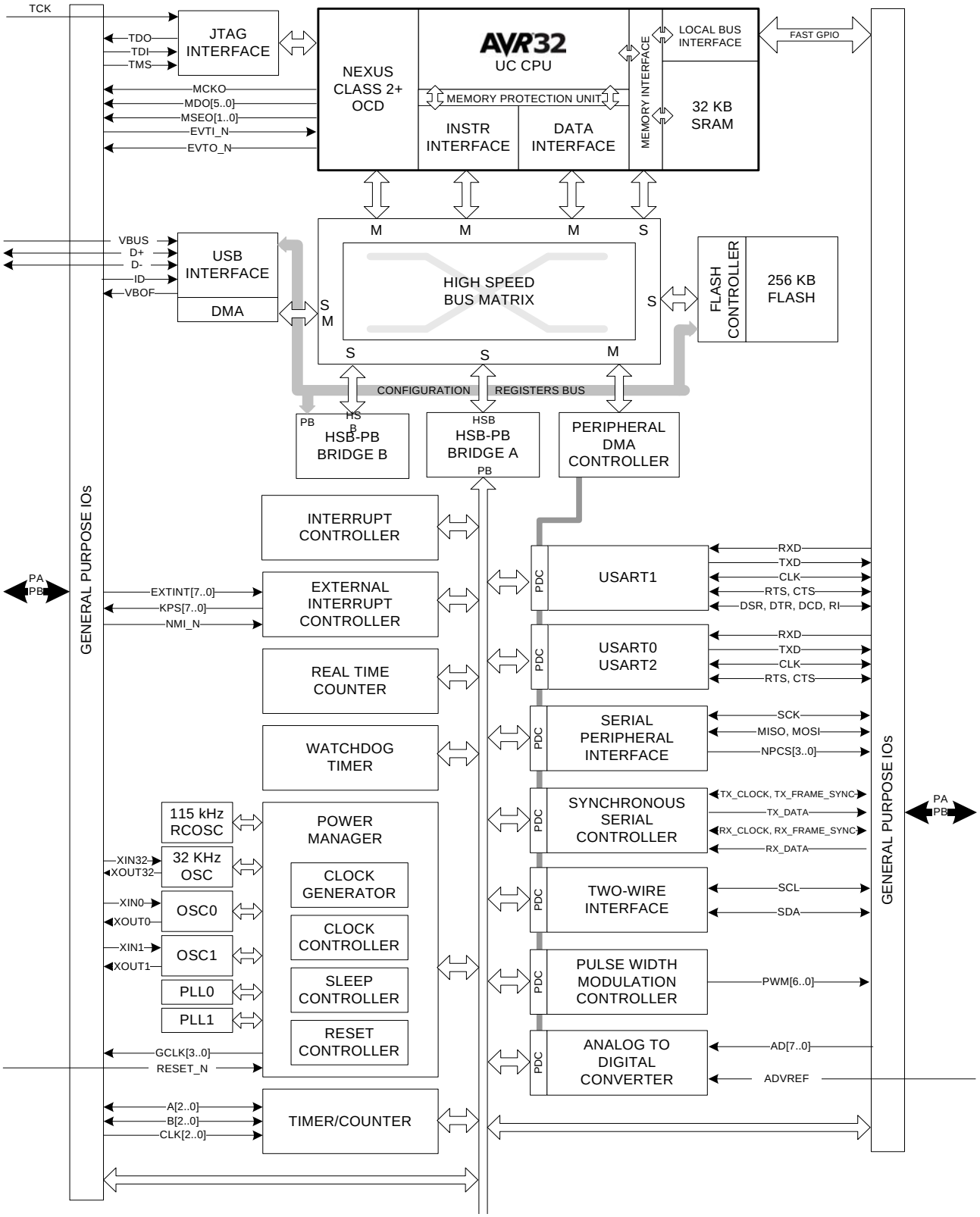
2. Configuration Summary

The table below lists all AT32UC3B memory and package configurations:

Device	Flash	SRAM	USART	SSC	ADC	OSC	USB Configuration	Package
AT32UC3B0256	256 Kbytes	32 Kbytes	3	1	8	2	Mini-Host + Device	64 lead TQFP/QFN
AT32UC3B0128	128 Kbytes	32 Kbytes	3	1	8	2	Mini-Host + Device	64 lead TQFP/QFN
AT32UC3B064	64 Kbytes	16 Kbytes	3	1	8	2	Mini-Host + Device	64 lead TQFP/QFN
AT32UC3B1256	256 Kbytes	32 Kbytes	2	0	6	1	Device	48 lead TQFP/QFN
AT32UC3B1128	128 Kbytes	16 Kbytes	2	0	6	1	Device	48 lead TQFP/QFN
AT32UC3B164	64 Kbytes	16 Kbytes	2	0	6	1	Device	48 lead TQFP/QFN

3. Blockdiagram

Figure 3-1. Block diagram



3.1 Processor and architecture

3.1.1 AVR32UC CPU

- 32-bit load/store AVR32A RISC architecture.
  - 15 general-purpose 32-bit registers.
  - 32-bit Stack Pointer, Program Counter and Link Register reside in register file.
  - Fully orthogonal instruction set.
  - Privileged and unprivileged modes enabling efficient and secure Operating Systems.
  - Innovative instruction set together with variable instruction length ensuring industry leading code density.
  - DSP extention with saturating arithmetic, and a wide variety of multiply instructions.
- 3 stage pipeline allows one instruction per clock cycle for most instructions.
  - Byte, half-word, word and double word memory access.
  - Multiple interrupt priority levels.
- MPU allows for operating systems with memory protection.

3.1.2 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 2+
  - Low-cost NanoTrace supported.
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

3.1.3 Peripheral DMA Controller (PDCA)

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- 7 channels that can be dynamically attributed to
  - all USARTs
  - the Serial Synchronous Controller
  - the Serial Peripheral Interface
  - the ADC
  - the TWI Interface

3.1.4 Bus system

- High Speed Bus (HSB) matrixs
  - Handles Requests from
    Masters: the CPU (instruction and Data Fetch), PDCA, USBB, CPU SAB,
    Slaves: the internal Flash, internal SRAM, Peripheral Bus A, Peripheral Bus B, USBB.
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
  - One Address Decoder Provided per Master
  - Peripheral Bus A able to run on at divided bus speeds compared to the High Speed Bus
  - All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager.

4. Package and Pinout

The device pins are multiplexed with peripheral functions as described in ”Peripheral Multiplexing on I/O lines” on page 24.

Figure 4-1. QFP64 Pinout

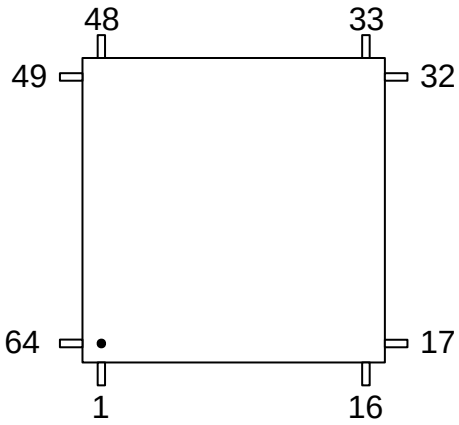


Table 4-1. QFP64 Package Pinout

1	GND	**17**	GND	**33**	PA13	**49**	GND
2	TCK	**18**	ADVREF	**34**	PA14	**50**	DP
3	TDI	**19**	VDDANA	**35**	PA15	**51**	DM
4	TDO	**20**	VDDOUT	**36**	PA16	**52**	VBUS
5	TMS	**21**	VDDIN	**37**	PA17	**53**	VDDPLL
6	PB00	**22**	VDDCORE	**38**	PB06	**54**	PB08
7	PB01	**23**	GND	**39**	PA18	**55**	PB09
8	VDDCORE	**24**	PB02	**40**	PA19	**56**	VDDCORE
9	PA03	**25**	PB03	**41**	PA28	**57**	PB10
10	PA04	**26**	PB04	**42**	PA29	**58**	PB11
11	PA05	**27**	PB05	**43**	PB07	**59**	PA24
12	PA06	**28**	PA09	**44**	PA20	**60**	PA25
13	PA07	**29**	PA10	**45**	PA21	**61**	PA26
14	PA08	**30**	PA11	**46**	PA22	**62**	PA27
15	PA30	**31**	PA12	**47**	PA23	**63**	RESET_N
16	PA31	**32**	VDDIO	**48**	VDDIO	**64**	VDDIO

Figure 4-2. QFP48 Pinout

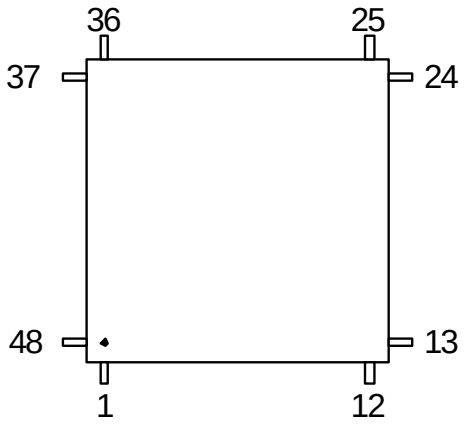


Table 4-2. QFP48 Package Pinout

1	GND	**13**	GND	**25**	PA13	**37**	GND
2	TCK	**14**	ADVREF	**26**	PA14	**38**	DP
3	TDI	**15**	VDDANA	**27**	PA15	**39**	DM
4	TDO	**16**	VDDOUT	**28**	PA16	**40**	VBUS
5	TMS	**17**	VDDIN	**29**	PA17	**41**	VDDPLL
6	VDDCORE	**18**	VDDCORE	**30**	PA18	**42**	VDDCORE
7	PA03	**19**	GND	**31**	PA19	**43**	PA24
8	PA04	**20**	PA09	**32**	PA20	**44**	PA25
9	PA05	**21**	PA10	**33**	PA21	**45**	PA26
10	PA06	**22**	PA11	**34**	PA22	**46**	PA27
11	PA07	**23**	PA12	**35**	PA23	**47**	RESET_N
12	PA08	**24**	VDDIO	**36**	VDDIO	**48**	VDDIO

5. Signals Description

The following table gives details on the signal name classified by peripheral

The signals are multiplexed with GPIO pins as described in ”Peripheral Multiplexing on I/O lines” on page 24.

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDPLL	PLL Power Supply	Power Input		1.65V to 1.95 V
VDDCORE	Core Power Supply	Power Input		1.65V to 1.95 V
VDDIO	I/O Power Supply	Power Input		3.0V to 3.6V
VDDANA	Analog Power Supply	Power Input		3.0V to 3.6V
VDDIN	Voltage Regulator Input Supply	Power Input		3.0V to 3.6V
VDDOUT	Voltage Regulator Output	Power Output		1.65V to 1.95 V
GNDANA	Analog Ground	Ground		
GND	Ground	Ground		
Clocks, Oscillators, and PLL’s				
XIN0, XIN1, XIN32	Crystal 0, 1, 32 Input	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32 Output	Analog		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO0 - MDO5	Trace Data Output	Output		

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
MSEO0 - MSEO1	Trace Frame Control	Output		
EVTI_N	Event In	Output	Low	
EVTO_N	Event Out	Output	Low	
Power Manager - PM				
GCLK0 - GCLK2	Generic Clock Pins	Output		
RESET_N	Reset Pin	Input	Low	
External Interrupt Module - EIM				
EXTINT0 - EXTINT7	External Interrupt Pins	Input		
KPS0 - KPS7	Keypad Scan Pins	Output		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
General Purpose I/O pin- GPIOA, GPIOB				
PA0 - PA31	Parallel I/O Controller GPIOA	I/O		
PB0 - PB11	Parallel I/O Controller GPIOB	I/O		
Serial Peripheral Interface - SPI0				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS0 - NPCS3	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Synchronous Serial Controller - SSC				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
Timer/Counter - TIMER				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
DCD	Data Carrier Detect			Only USART1
DSR	Data Set Ready			Only USART1
DTR	Data Terminal Ready			Only USART1
RI	Ring Indicator			Only USART1
RTS	Request To Send	Output		
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
Analog to Digital Converter - ADC				
AD0 - AD7	Analog input pins	Analog input		
ADVREF	Analog positive reference voltage input	Analog input		2.6 to 3.6V
Pulse Width Modulator - PWM				
PWM0 - PWM6	PWM Output Pins	Output		
Universal Serial Bus Device - USB				
DDM	USB Device Port Data -	Analog		

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
DDP	USB Device Port Data +	Analog		
VBUS	USB VBUS Monitor and OTG Negociation	Analog Input		
USBID	ID Pin of the USB Bus	Input		
USB_VBOF	USB VBUS On/off: bus power control port	output		

6. Power Considerations

6.1 Power Supplies

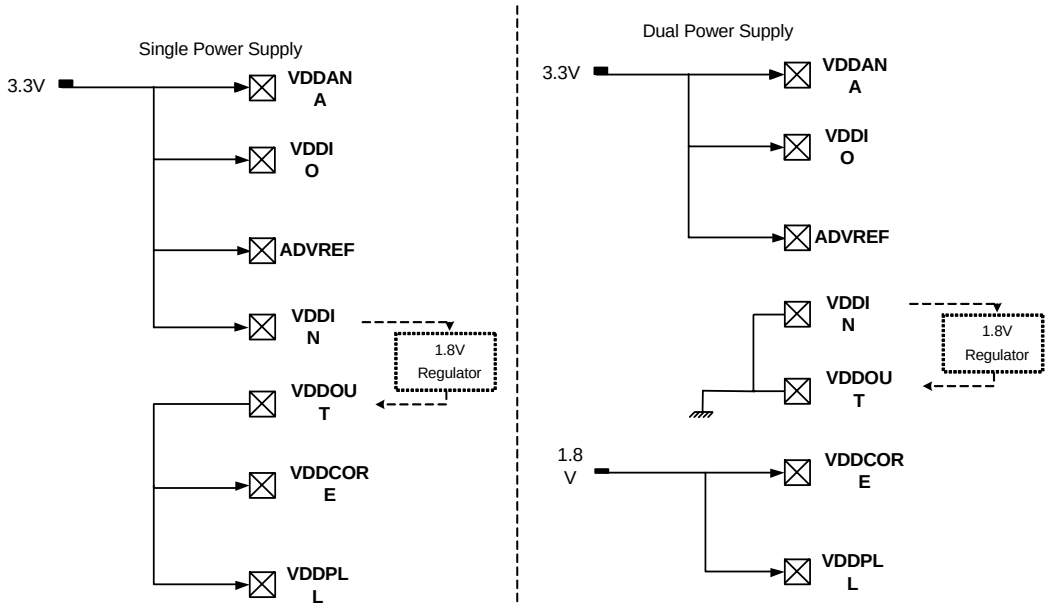
The AT32UC3B has several types of power supply pins:

- **VDDIO: Powers I/O lines. Voltage is 3.3V nominal.**
- **VDDANA: Powers the ADC Voltage is 3.3V nominal.**
- **VDDIN: Input voltage for the voltage regulator. Voltage is 3.3V nominal.**
- **VDDCORE: Powers the core, memories, and peripherals. Voltage is 1.8V nominal.**
- **VDDPLL: Powers the PLL. Voltage is 1.8V nominal.**

The ground pins GND are common to VDDCORE, VDDIO and VDDPLL. The ground pin for VDDANA is GNDANA.

Refer to "Electrical Characteristics" on page 30 for power consumption on the various supply pins.

The main requirement for power supplies connection is to respect a star topology for all electrical connection.



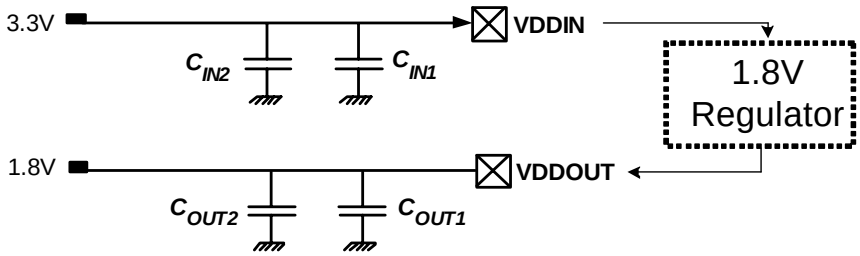
6.2 Voltage Regulator

6.2.1 Single Power Supply

The AT32UC3B embeds a voltage regulator that converts from 3.3V to 1.8V. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDOUT that should be externally connected to the 1.8V domains.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. Two input decoupling capacitors must be placed close to the chip.

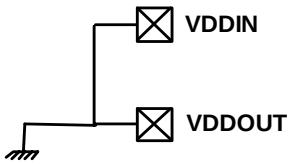
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel between VDDOUT and GND as close to the chip as possible



Refer to Section 11.3 on page 32 for decoupling capacitors values and regulator characteristics.

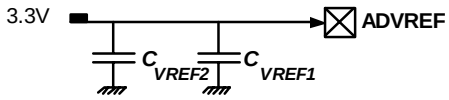
6.2.2 Dual Power Supply

In case of dual power supply, VDDIN and VDDOUT should be connected to ground to prevent from leakage current.



6.3 Analog-to-Digital Converter (A.D.C) reference.

The ADC reference (ADVREF) must be provided from an external source. Two decoupling capacitors must be used to insure proper decoupling.



Refer to Section 11.4 on page 32 for decoupling capacitors values and electrical characteristics.

In case ADC is not used, the ADVREF pin should be connected to GND to avoid extra consumption.

7. I/O Line Considerations

7.1 JTAG pins

TMS and TDI pins have pull-up resistors. TDO pin is an output, driven at up to VDDIO, and has no pull-up resistor. These 3 pins can be used as GPIO-pins. At reset state, these pins are in GPIO mode.

TCK pin cannot be used as GPIO pin. JTAG interface is enabled when TCK pin is tied low.

7.2 RESET_N pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

7.3 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as PIO pins.

7.4 GPIO pins

All the I/O lines integrate a pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up resistors disabled, except when indicated otherwise in the column “Reset State” of the GPIO Controller multiplexing tables.

7.5 High drive pins

The four pins PA20, PA21, PA22, PA23 have high drive output capabilities. Refer to Figure 11. on page 30 for electrical characteristics.

8. Memories

8.1 Embedded Memories

- **Internal High-Speed Flash**
  - **256 KBytes (AT32UC3B0256, AT32UC3B1256)**
  - **128 KBytes (AT32UC3B0128, AT32UC3B1128)**
  - **64 KBytes (AT32UC3B064, AT32UC3B164)**
    - **0 Wait State Access at up to 30 MHz in Worst Case Conditions**
    - **1 Wait State Access at up to 60 MHz in Worst Case Conditions**
    - **Pipelined Flash Architecture, allowing burst reads from sequential Flash locations, hiding penalty of 1 wait state access**
    - **Pipelined Flash Architecture typically reduces the cycle penalty of 1 wait state operation to only 8% compared to 0 wait state operation**
    - **100 000 Write Cycles, 15-year Data Retention Capability**
    - **4 ms Page Programming Time, 8 ms Chip Erase Time**
    - **Sector Lock Capabilities, Bootloader Protection, Security Bit**
    - **32 Fuses, Erased During Chip Erase**
    - **User Page For Data To Be Preserved During Chip Erase**
- **Internal High-Speed SRAM, Single-cycle access at full speed**
  - **32KBytes (AT32UC3B0256, AT32UC3B0128, AT32UC3B1256 and AT32UC3B1128)**
  - **16KBytes (AT32UC3B064 and AT32UC3B164)**

8.2 Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot. Note that AVR32 UC CPU uses unsegmented translation, as described in the AVR32 Architecture Manual. The 32-bit physical address space is mapped as follows:

Table 8-1. AT32UC3B Physical Memory Map

Device	Start Address	Size					
		AT32UC3B0256	AT32UC3B1256	AT32UC3B0128	AT32UC3B1128	AT32UC3B064	AT32UC3B164
Embedded SRAM	0x0000_0000	32 Kbytes	32 Kbytes	32 Kbytes	32 Kbytes	16 Kbytes	16 Kbytes
Embedded Flash	0x8000_0000	256 Kbytes	256 Kbytes	128 Kbytes	128 Kbytes	64 Kbytes	64 Kbytes
USB Configuration	0xD000_0000	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes
HSB-PB Bridge A	0xFFFE_0000	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes
HSB-PB Bridge B	0xFFFF_0000	64 Kbytes	64 Kbytes	64 kBytes	64 kBytes	64 Kbytes	64 Kbytes

Table 8-2. Flash Memory Parameters

Part Number	Flash Size (*FLASH_PW*)	Number of pages (*FLASH_P*)	Page size (*FLASH_W*)	General Purpose Fuse bits (*FLASH_L*)
AT32UC3B0256	256 Kbytes	512	128 words	32 fuses
AT32UC3B1256	256 Kbytes	512	128 words	32 fuses

Table 8-2. Flash Memory Parameters

AT32UC3B0128	128 Kbytes	256	128 words	32 fuses
AT32UC3B1128	128 Kbytes	256	128 words	32 fuses
AT32UC3B064	64 Kbytes	128	128 words	32 fuses
AT32UC3B164	64 Kbytes	128	128 words	32 fuses

8.3 Bus Matrix Connections

Accesses to unused areas returns an error result to the master requesting such an access.

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, HMATRIX MCFG0 register is associated with the CPU Data master interface.

Table 8-3. High Speed Bus masters

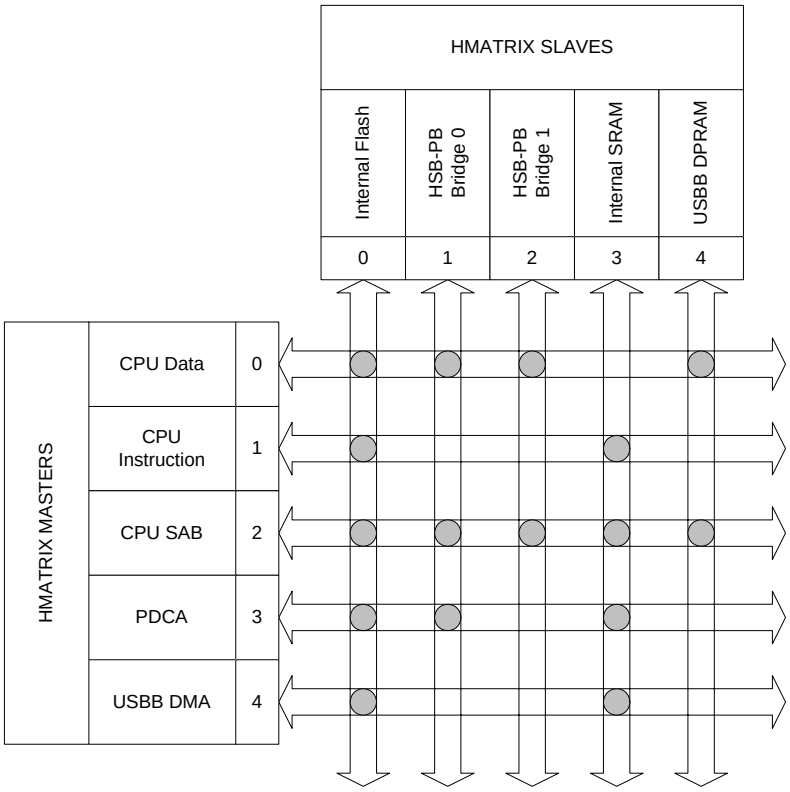
Master 0	CPU Data
Master 1	CPU Instruction
Master 2	CPU SAB
Master 3	PDCA
Master 4	USBB DMA

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with the Internal SRAM Slave Interface.

Table 8-4. High Speed Bus slaves

Slave 0	Internal Flash
Slave 1	HSB-PB Bridge 0
Slave 2	HSB-PB Bridge 1
Slave 3	Internal SRAM
Slave 4	USBB DPRAM

Figure 8-1. HMatrix Master / Slave Connections



9. Peripherals

9.1 Peripheral Address Map

Table 9-1. Peripheral Address Mapping

Address		Peripheral Name	Bus
0xFFFE0000	USBB	USB 2.0 OTG - USBB	PBB
0xFFFE1000	HMATRIX	HMATRIX Configuration Interface - HMATRIX	PBB
0xFFFE1400	FLASHC	Flash controller - FLASHC	PBB
0xFFFF0000	PDCA	Peripheral Direct Memory Access - PDCA	PBA
0xFFFF0800	INTC	Interrupt controller - INTC	PBA
0xFFFF0C00	PM	Power Manager - PM	PBA
0xFFFF0D00	RTC	Real Time Counter - RTC	PBA
0xFFFF0D30	WDT	Watchdog Timer - WDT	PBA
0xFFFF0D80	EIC	External Interrupt Controller - EIC	PBA
0xFFFF1000	GPIO	General Purpose Input/Output - GPIO	PBA
0xFFFF1400	USART0	Universal Synchronous Asynchronous Receiver Transmitter - USART0	PBA
0xFFFF1800	USART1	Universal Synchronous Asynchronous Receiver Transmitter - USART1	PBA
0xFFFF1C00	USART2	Universal Synchronous Asynchronous Receiver Transmitter - USART2	PBA
0xFFFF2400	SPI	Serial Peripheral Interface - SPI	PBA
0xFFFF2C00	TWI	Two-wire Interface - TWI	PBA
0xFFFF3000	PWM	Pulse Width Modulation Controller - PWM	PBA
0xFFFF3400	SSC	Synchronous Serial Controller - SSC	PBA

Table 9-1. Peripheral Address Mapping

0xFFFF3800	TC	Timer/Counter - TC	PBA
0xFFFF3C00	ADC	Analog to Digital Converter - ADC	PBA

9.2 CPU Local Bus Mapping

Some of the registers in the GPIO module are mapped onto the CPU local bus, in addition to being mapped on the Peripheral Bus. These registers can therefore be reached both by accesses on the Peripheral Bus, and by accesses on the local bus.

Mapping these registers on the local bus allows cycle-deterministic toggling of GPIO pins since the CPU and GPIO are the only modules connected to this bus. Also, since the local bus runs at CPU speed, one write or read operation can be performed per clock cycle to the local bus-mapped GPIO registers.

The following GPIO registers are mapped on the local bus:

Table 9-2. Local bus mapped GPIO registers

Port	Register	Mode	Local Bus Address	Access
0	Output Driver Enable Register (ODER)	WRITE	0x4000_0040	Write-only
		SET	0x4000_0044	Write-only
		CLEAR	0x4000_0048	Write-only
		TOGGLE	0x4000_004C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0050	Write-only
		SET	0x4000_0054	Write-only
		CLEAR	0x4000_0058	Write-only
		TOGGLE	0x4000_005C	Write-only
	Pin Value Register (PVR)	-	0x4000_0060	Read-only
1	Output Driver Enable Register (ODER)	WRITE	0x4000_0140	Write-only
		SET	0x4000_0144	Write-only
		CLEAR	0x4000_0148	Write-only
		TOGGLE	0x4000_014C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0150	Write-only
		SET	0x4000_0154	Write-only
		CLEAR	0x4000_0158	Write-only
		TOGGLE	0x4000_015C	Write-only
	Pin Value Register (PVR)	-	0x4000_0160	Read-only

9.3 Interrupt Request Signal Map

The various modules may output Interrupt request signals. These signals are routed to the Interrupt Controller (INTC), described in a later chapter. The Interrupt Controller supports up to 64

groups of interrupt requests. Each group can have up to 32 interrupt request signals. All interrupt signals in the same group share the same autovector address and priority level. Refer to the documentation for the individual submodules for a description of the semantics of the different interrupt requests.

The interrupt request signals are connected to the INTC as follows.

Table 9-3. Interrupt Request Signal Map

Group	Line	Module	Signal
0	0	AVR32 UC CPU with optional MPU and optional OCD	SYSBLOCK COMPARE
1	0	External Interrupt Controller	EIC 0
	1	External Interrupt Controller	EIC 1
	2	External Interrupt Controller	EIC 2
	3	External Interrupt Controller	EIC 3
	4	External Interrupt Controller	EIC 4
	5	External Interrupt Controller	EIC 5
	6	External Interrupt Controller	EIC 6
	7	External Interrupt Controller	EIC 7
	8	Real Time Counter	RTC
	9	Power Manager	PM
	10	Frequency Meter	FREQM
2	0	General Purpose Input/Output Controller	GPIO 0
	1	General Purpose Input/Output Controller	GPIO 1
	2	General Purpose Input/Output Controller	GPIO 2
	3	General Purpose Input/Output Controller	GPIO 3
	4	General Purpose Input/Output Controller	GPIO 4
	5	General Purpose Input/Output Controller	GPIO 5
3	0	Peripheral DMA Controller	PDCA 0
	1	Peripheral DMA Controller	PDCA 1
	2	Peripheral DMA Controller	PDCA 2
	3	Peripheral DMA Controller	PDCA 3
	4	Peripheral DMA Controller	PDCA 4
	5	Peripheral DMA Controller	PDCA 5
	6	Peripheral DMA Controller	PDCA 6
4	0	Flash Controller	FLASHC
5	0	Universal Synchronous/Asynchronous Receiver/Transmitter	USART0
6	0	Universal Synchronous/Asynchronous Receiver/Transmitter	USART1

Table 9-3. Interrupt Request Signal Map

7	0	Universal Synchronous/Asynchronous Receiver/Transmitter	USART2
9	0	Serial Peripheral Interface	SPI
11	0	Two-wire Interface	TWI
12	0	Pulse Width Modulation Controller	PWM
13	0	Synchronous Serial Controller	SSC
14	0	Timer/Counter	TC0
	1	Timer/Counter	TC1
	2	Timer/Counter	TC2
15	0	Analog to Digital Converter	ADC
17	0	USB 2.0 OTG Interface	USBB

9.4 Clock Connections

9.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 9-4. Timer/Counter clock connections

Source	Name	Connection
Internal	TIMER_CLOCK1	32 KHz Oscillator
	TIMER_CLOCK2	PBA Clock / 2
	TIMER_CLOCK3	PBA Clock / 8
	TIMER_CLOCK4	PBA Clock / 32
	TIMER_CLOCK5	PBA Clock / 128
External	XC0	See Section 9.8
	XC1	
	XC2	

9.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 9-5. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	PBA Clock / 8
1			
2			

9.4.3 SPIs

SPI can be connected to an internally divided clock:

Table 9-6. SPI clock connections

SPI	Source	Name	Connection
0	Internal	CLK_DIV	PBA clock or PBA clock / 32

9.5 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the PIO configuration. Two different OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the AVR32 UCTechnical Reference Manual.

Table 9-7. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1
EVTI_N	PB05	PA14
MDO[5]	PB04	PA08
MDO[4]	PB03	PA07
MDO[3]	PB02	PA06
MDO[2]	PB01	PA05
MDO[1]	PB00	PA04
MDO[0]	PA31	PA03
EVTO_N	PA15	PA15
MCKO	PA30	PA13
MSEO[1]	PB06	PA09
MSEO[0]	PB07	PA10

9.6 DMA handshake signals

The PDCA and the peripheral modules communicate through a set of handshake signals. The following table defines the valid settings for the Peripheral Identifier (PID) in the PDCA Peripheral Select Register (PSR).

Table 9-8. PDCA Handshake Signals

PID Value	Peripheral module & direction
0	ADC
1	SSC - RX
2	USART0 - RX
3	USART1 - RX
4	USART2 - RX

Table 9-8. PDCA Handshake Signals

PID Value	Peripheral module & direction
5	TWI - RX
6	SPI0 - RX
7	SSC - TX
8	USART0 - TX
9	USART1 - TX
10	USART2 - TX
11	TWI - TX
12	SPI0 - TX

9.7 High Drive Current GPIO

Ones of GPIOs can be used to drive twice current than other GPIO capability (see Electrical Characteristics chapter). The list of those GPIOs is shown in Table 9-9.

Table 9-9. High Drive Current GPIO

GPIO Name
GPIO/0/P21
GPIO/0/P22
GPIO/0/P23
GPIO/0/P24

9.8 Peripheral Multiplexing on I/O lines

Each GPIO line can be assigned to one of 3 peripheral functions; A, B or C. The following table define how the I/O lines on the peripherals A, B and C are multiplexed by the GPIO.

Table 9-10. GPIO Controller Function Multiplexing

QFP48	QFP64	PIN	GPIO Pin	Function A	Function B	Function C
7	9	PA03	GPIO 3	ADC - AD[0]	PM - GCLK[0]	USBB - USB_ID
8	10	PA04	GPIO 4	ADC - AD[1]	PM - GCLK[1]	USBB - USB_VBOF
9	11	PA05	GPIO 5	EIC - EXTINT[0]	ADC - AD[2]	USART1 - DCD
10	12	PA06	GPIO 6	EIC - EXTINT[1]	ADC - AD[3]	USART1 - DSR
11	13	PA07	GPIO 7	PWM - PWM[0]	ADC - AD[4]	USART1 - DTR
12	14	PA08	GPIO 8	PWM - PWM[1]	ADC - AD[5]	USART1 - RI
20	28	PA09	GPIO 9	TWI - SCL	SPI - NPCS[2]	USART1 - CTS
21	29	PA10	GPIO 10	TWI - SDA	SPI - NPCS[3]	USART1 - RTS
22	30	PA11	GPIO 11	USART0 - RTS	TC - A2	PWM - PWM[0]
23	31	PA12	GPIO 12	USART0 - CTS	TC - B2	PWM - PWM[1]
25	33	PA13	GPIO 13	NMI	PWM - PWM[2]	USART0 - CLK

Table 9-10. GPIO Controller Function Multiplexing

26	34	PA14	GPIO 14	SPI - MOSI	PWM - PWM[3]	EIC - EXTINT[2]
27	35	PA15	GPIO 15	SPI - SCK	PWM - PWM[4]	USART2 - CLK
28	36	PA16	GPIO 16	SPI - NPCS[0]	TC - CLK1	
29	37	PA17	GPIO 17	SPI - NPCS[1]	TC - CLK2	SPI - SCK
30	39	PA18	GPIO 18	USART0 - RXD	PWM - PWM[5]	SPI - MISO
31	40	PA19	GPIO 19	USART0 - TXD	PWM - PWM[6]	SPI - MOSI
32	44	PA20	GPIO 20	USART1 - CLK	TC - CLK0	USART2 - RXD
33	45	PA21	GPIO 21	PWM - PWM[2]	TC - A1	USART2 - TXD
34	46	PA22	GPIO 22	PWM - PWM[6]	TC - B1	ADC - TRIGGER
35	47	PA23	GPIO 23	USART1 - TXD	SPI - NPCS[1]	EIC - EXTINT[3]
43	59	PA24	GPIO 24	USART1 - RXD	SPI - NPCS[0]	EIC - EXTINT[4]
44	60	PA25	GPIO 25	SPI - MISO	PWM - PWM[3]	EIC - EXTINT[5]
45	61	PA26	GPIO 26	USBB - USB_ID	USART2 - TXD	TC - A0
46	62	PA27	GPIO 27	USBB - USB_VBOF	USART2 - RXD	TC - B0
	41	PA28	GPIO 28	USART0 - CLK	PWM - PWM[4]	SPI - MISO
	42	PA29	GPIO 29	TC - CLK0	TC - CLK1	SPI - MOSI
	15	PA30	GPIO 30	ADC - AD[6]	EIC - SCAN[0]	PM - GCLK[2]
	16	PA31	GPIO 31	ADC - AD[7]	EIC - SCAN[1]	
	6	PB00	GPIO 32	TC - A0	EIC - SCAN[2]	USART2 - CTS
	7	PB01	GPIO 33	TC - B0	EIC - SCAN[3]	USART2 - RTS
	24	PB02	GPIO 34	EIC - EXTINT[6]	TC - A1	USART1 - TXD
	25	PB03	GPIO 35	EIC - EXTINT[7]	TC - B1	USART1 - RXD
	26	PB04	GPIO 36	USART1 - CTS	SPI - NPCS[3]	TC - CLK2
	27	PB05	GPIO 37	USART1 - RTS	SPI - NPCS[2]	PWM - PWM[5]
	38	PB06	GPIO 38	SSC - RX_CLOCK	USART1 - DCD	EIC - SCAN[4]
	43	PB07	GPIO 39	SSC - RX_DATA	USART1 - DSR	EIC - SCAN[5]
	54	PB08	GPIO 40	SSC - RX_FRAME_SYNC	USART1 - DTR	EIC - SCAN[6]
	55	PB09	GPIO 41	SSC - TX_CLOCK	USART1 - RI	EIC - SCAN[7]
	57	PB10	GPIO 42	SSC - TX_DATA	TC - A2	USART0 - RXD
	58	PB11	GPIO 43	SSC - TX_FRAME_SYNC	TC - B2	USART0 - TXD
3	3	TDI	GPIO 0			
4	4	TDO	GPIO 1			
5	5	TMS	GPIO 2			

9.9 Oscillator Pinout

The oscillators are not mapped to the normal A,B or C functions and their muxings are controlled by registers in the Power Manager (PM). Please refer to the power manager chapter for more information about this.

Table 9-11. Oscillator pinout

QFP48 pin	QFP64 pin	Pad	Oscillator pin
30	39	PA18	xin0
	41	PA28	xin1
22	30	PA11	xin32
31	40	PA19	xout0
	42	PA29	xout1
23	31	PA12	xout32

9.10 USART Configuration

Table 9-12. USART Configuration

	SPI	RS485	ISO7816	IrDA	Modem	Manchester Encoding
USART0	Yes	No	No	No	No	No
USART1	Yes	Yes	Yes	Yes	Yes	Yes
USART2	Yes	No	No	No	No	No

9.11 GPIO

The GPIO open drain feature (GPIO ODMER register (Open Drain Mode Enable Register)) is not available for all GPIO pins.

9.12 Peripheral Overview

9.12.1 USB Controller

- **USB 2.0 Compliant, Full-/Low-Speed (FS/LS) and On-The-Go (OTG), 12 Mbit/s**
- **7 Pipes/Endpoints**
- **960 bytes of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints**
- **Up to 2 Memory Banks per Pipe/Endpoint (Not for Control Pipe/Endpoint)**
- **Flexible Pipe/Endpoint Configuration and Management with Dedicated DMA Channels**
- **On-Chip Transceivers Including Pull-Ups**
- **System wake-up on USB line activity**

9.12.2 Serial Peripheral Interface

- **Supports communication with serial external devices**
  - **Four chip selects with external decoder support allow communication with up to 15 peripherals**
  - **Serial memories, such as DataFlash and 3-wire EEPROMs**
  - **Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors**
  - **External co-processors**
- **Master or slave serial peripheral bus interface**
  - **8- to 16-bit programmable data length per chip select**

  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to Peripheral Bus A (PBA) max frequency
  - The chip select line may be left active to speed up transfers on the same device

9.12.3 Two-wire Interface

- High speed up to 400kbit/s
- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

9.12.4 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency PBA/4
- Supports Connection of Two Peripheral DMA Controller Channels (PDC)
  - Offers Buffer Transfer without Processor Intervention

9.12.5 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

9.12.6 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

9.12.7 Pulse Width Modulation Controller

- 7 channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

10. Boot Sequence

This chapter summarizes the boot sequence of the AT32UC3B. The behaviour after power-up is controlled by the Power Manager. For specific details, refer to Section 13. ”Power Manager (PM)” on page 45.

10.1 Starting of clocks

After power-up, the device will be held in a reset state by the Power-On Reset circuitry, until the power has stabilized throughout the device. Once the power has stabilized, the device will use the internal RC Oscillator as clock source.

On system start-up, the PLLs are disabled. All clocks to all modules are running. No clocks have a divided frequency, all parts of the system recieves a clock with the same frequency as the internal RC Oscillator.

10.2 Fetching of initial instructions

After reset has been released, the AVR32 UC CPU starts fetching instructions from the reset address, which is 0x8000_0000. This address points to the first address in the internal Flash.

The code read from the internal Flash is free to configure the system to use for example the PLLs, to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-60°C to +150°C
Voltage on GPIO Pins with respect to Ground	-0.3 to 5V
Maximum Voltage on RESET_N Pin	3.3V
Maximum Operating Voltage (VDDCORE, VDDPLL)	1.95V
Maximum Operating Voltage (VDDIO)	3.6V
Total DC Output Current on all I/O Pin for 48-pin package	200 mA
Total DC Output Current on all I/O Pin for 64-pin package	265 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up to T_J = 100°C.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$V_{VDDCORE}$	DC Supply Core			1.65		1.95	V
V_{VDDPLL}	DC Supply PLL			1.65		1.95	V
V_{VDDIO}	DC Supply Peripheral I/Os			3.0		3.6	V
V_{REF}	Analog reference voltage			2.6		3.6	V
V_{IL}	Input Low-level Voltage			-0.3		+0.8	V
V_{IH}	Input High-level Voltage	All I/O pins except TDI, TDO, TMS, PA11, PA12, PA18, PA19, PA28, PA29.		2.0		5.5	V
		TDI, TDO, TMS, PA11, PA12, PA18, PA19, PA28, PA29 pins		2.0		3.6	V
V_{OL}	Output Low-level Voltage					0.4	V
V_{OH}	Output High-level Voltage	V_{VDDIO}= V_{VDDIOM} or V_{VDDIOP}		V_{VDDIO}-0.4			
I_{LEAK}	Input Leakage Current	Pullup resistors disabled				1	µA
C_{IN}	Input Capacitance					TBD	pF
R_{PULLUP}	Pull-up Resistance				TBD		
I_O	I/O Output Current	All I/O pins except PA21, PA22, PA23, PA24			4		mA
		PA21, PA22, PA23, PA24			8		mA
I_{SC}	Static Current	On $V_{VDDCORE}$ = 1.8V, device in static mode	T_A =25°C		6		µA
		All inputs driven including JTAG; RESET_N=1	T_A =85°C		25		µA
I_{SCR}	Static Current of internal regulator	Low Power mode (stop, deep stop or static	T_A =25°C		10		µA

11.3 Regulator characteristics

11.3.1 Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{VDDIN}	Supply voltage (input)		2.7	3.3	3.6	V
V_{VDDOUT}	Supply voltage (output)		1.81	1.85	1.89	V
I_{OUT}	Maximum DC output current with $V_{VDDIN = 3.3V}$				100	mA
	Maximum DC output current with $V_{VDDIN = 2.7V}$				90	mA

11.3.2 Decoupling requirements

Symbol	Parameter	Condition	Typ.	Techno.	Units
C_{IN1}	Input Regulator Capacitor 1		1	NPO	nF
C_{IN2}	Input Regulator Capacitor 2		4.7	X7R	uF
C_{OUT1}	Output Regulator Capacitor 1		470	NPO	pF
C_{OUT2}	Output Regulator Capacitor 2		2.2	X7R	uF

11.4 Analog characteristics

11.4.1 Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{ADVREF}	Analog voltage reference (input)		2.6		3.6	V

11.4.2 Decoupling requirements

Symbol	Parameter	Condition	Typ.	Techno.	Units
C_{VREF1}	Voltage reference Capacitor 1		10	-	nF
C_{VREF2}	Voltage reference Capacitor 2		1	-	uF

11.4.3 BOD

Table 11-1. BODLEVEL Values

BODLEVEL Value	Typ.	Units.
000000b	1.58	V
010111b	1.62	V
011111b	1.67	V
100111b	1.77	V
111111b	1.92	V

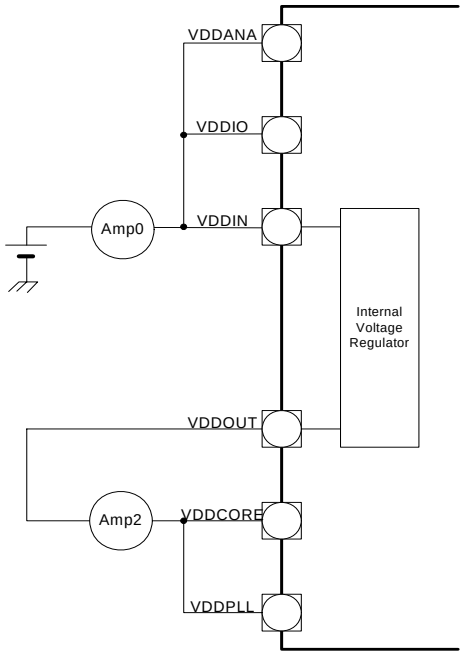
The values in Table 11-1 describes the values of the BODLEVEL in the flash General Purpose Fuse register.

11.5 Power Consumption

The values in Table 11-2 and Table 11-3 on page 34 are measured values of power consumption with operating conditions as follows:

- V_{DDIO} = 3.3V
- V_{DDCORE} = V_{DDPLL} = 1.8V
- T_A = 25°C, T_A = 85°C
- I/Os are inactive

Figure 11-1. Measure schematic



These figures represent the power consumption measured on the power supplies.

Table 11-2. Power Consumption for Different Modes[1]

Mode	Conditions		Consumption Typ.	Unit
Active	CPU running from flash. CPU clocked from PLL0 at f MHz Voltage regulator is on. XIN0 : external clock. [1] XIN1 stopped. XIN32 stopped PLL0 running All peripheral clocks activated. GPIOs on internal pull-up. JTAG unconnected with ext pull-up.	f = 12 MHz	5.5	mA
		f = 24 MHz	10	mA
		f = 36MHz	14.5	mA
		f = 50 MHz	19.5	mA
		f = 60 MHz	23.5	mA
Static	Typ : Ta = 25 °C CPU is in static mode GPIOs on internal pull-up. All peripheral clocks de-activated. DM and DP pins connected to ground. XIN0,Xin1 and XIN2 are stopped	on Amp0	15.5	uA
		on Amp1	6	uA

1. Core frequency is generated from XIN0 using the PLL so that 140 MHz < fpll0 < 160 MHz and 10 MHz < fxin0 < 12MHz.

Table 11-3. Power Consumption by Peripheral in Active Mode

Peripheral	Consumption	Unit
INTC	20	µA/MHz
GPIO	27	
PDCA	27	
USART	35	
USB	30	
ADC	18	
TWI	14	
PWM	26	
SPI	11	
SSC	35	
TC	26	

11.6 Clock Characteristics

These parameters are given in the following conditions:

- V_{DDCORE} = 1.8V
- Ambient Temperature = 25°C

11.6.1 CPU/HSB Clock Characteristics

Table 11-4. Core Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPCPU})$	CPU Clock Frequency			60	MHz
t_{CPCPU}	CPU Clock Period		16.6		ns

11.6.2 PBA Clock Characteristics

Table 11-5. PBA Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPPBA})$	PBA Clock Frequency			60	MHz
t_{CPPBA}	PBA Clock Period		16.6		ns

11.6.3 PBB Clock Characteristics

Table 11-6. PBB Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPPBB})$	PBB Clock Frequency			60	MHz
t_{CPPBB}	PBB Clock Period		16.6		ns

11.6.4 XIN Clock Characteristics

Table 11-7. XIN Clock Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPXIN})$	XIN Clock Frequency	External Clock		50	MHz
		Crystal	3	20	MHz
t_{CHXIN}	XIN Clock High Half-period		$0.4 \times t_{CPXIN}$	$0.6 \times t_{CPXIN}$	
t_{CLXIN}	XIN Clock Low Half-period		$0.4 \times t_{CPXIN}$	$0.6 \times t_{CPXIN}$	
C_{IN}	XIN Input Capacitance		12		pF
R_{IN}	XIN Pulldown Resistor			TBD	kΩ

11.6.5 RESET_N Characteristics

Table 11-8. RESET_N Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
t_{RESET}	RESET_N minimum pulse length		10		ns

11.7 Crystal Oscillator Characteristis

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C and worst case of power supply, unless otherwise specified.

11.7.1 32 KHz Oscillator Characteristics

Table 11-9. 32 KHz Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CP32KHz})$	Crystal Oscillator Frequency				32 768	Hz
	Duty Cycle		40	50	60	%
C_L	Equivalent Load Capacitance		6		12.5	pF
t_{ST}	Startup Time	C_L = 6pF(1) C_L = 12.5pF(1)			600 1200	ms
I_{OSC}	Current Consumption	Active mode			1.8	µA
		Standby mode			0.1	µA

Note: 1. C_L is the equivalent load capacitance.

11.7.2 Main Oscillators Characteristics

Table 11-10. Main Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency		3		16	MHz
C_{L1}, C_{L2}	Internal Load Capacitance (C_{L1} = C_{L2})			12		pF
C_L	Equivalent Load Capacitance			6		pF
	Duty Cycle		40	50	60	%
t_{ST}	Startup Time	@3MHz @8MHz @16MHz @20MHz			14.5 4 1.4 1	ms
I_{OSC}	Current Consumption	Active mode @3 MHz Active mode @8 MHz Active mode @16 MHz Active mode @20 MHz		150 150 300 400		µA
		Standby mode @TBD V		1		µA

11.7.3 PLL Characteristics

Table 11-11. Phase Lock Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		80		240	MHz
F_{IN}	Input Frequency		4		32	MHz
I_{PLL}	Current Consumption	Active mode F_{VCO}@96MHz Active mode F_{VCO}@128MHz Active mode F_{VCO}@160MHz		320 410 450		µA
		Standby mode		5		µA

11.8 ADC Characteristics

Table 11-12. Channel Conversion Time and ADC Clock

Parameter	Conditions	Min	Typ	Max	Units
ADC Clock Frequency	10-bit resolution mode			5	MHz
ADC Clock Frequency	8-bit resolution mode			8	MHz
Startup Time	Return from Idle Mode			20	µs
Track and Hold Acquisition Time		600			ns
Conversion Time	ADC Clock = 5 MHz			2	µs
Conversion Time	ADC Clock = 8 MHz			1.25	µs
Throughput Rate	ADC Clock = 5 MHz			384(1)	kSPS
Throughput Rate	ADC Clock = 8 MHz			533(2)	kSPS

Notes: 1. Corresponds to 13 clock cycles at 5 MHz: 3 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.
2. Corresponds to 15 clock cycles at 8 MHz: 5 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.

Table 11-13. External Voltage Reference Input

Parameter	Conditions	Min	Typ	Max	Units
ADVREF Input Voltage Range		2.6		VDDANA	V
ADVREF Average Current	On 13 samples with ADC Clock = 5 MHz		200	250	µA
Current Consumption on VDDANA				TBD	mA

Table 11-14. Analog Inputs

Parameter	Min	Typ	Max	Units
Input Voltage Range	0		V_{ADVREF}	
Input Leakage Current		TBD		µA
Input Capacitance			TBD	pF

Table 11-15. Transfer Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Resolution			10		Bit
Absolute Accuracy	f=5MHz			0.8	LSB
Integral Non-linearity	f=5MHz		0.35	0.5	LSB
Differential Non-linearity	f=5MHz		0.3	0.5	LSB
Offset Error	f=5MHz	-0.5		0.5	LSB
Gain Error	f=5MHz	-0.5		0.5	LSB

11.9 JTAG/ICE Timings

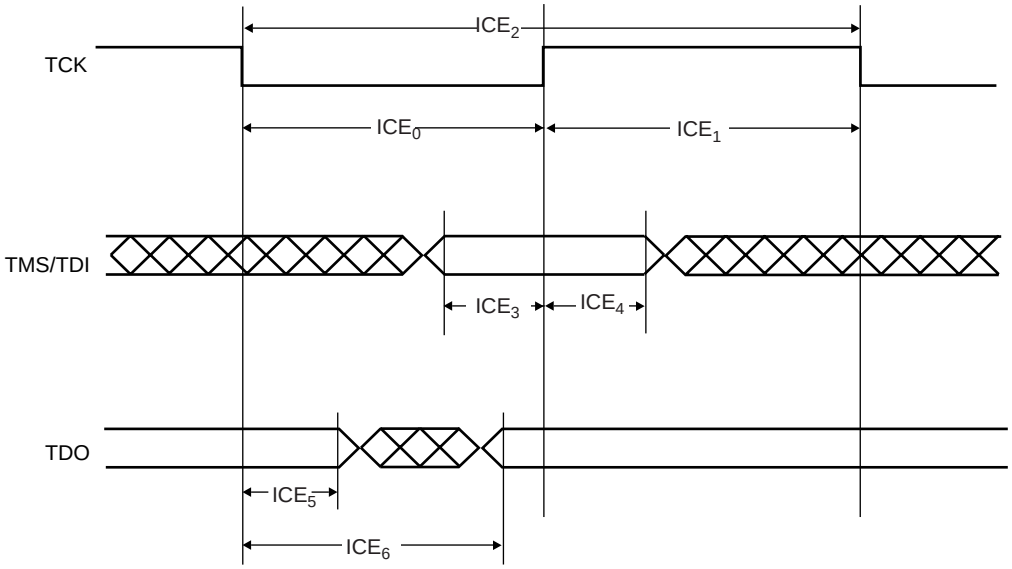
11.9.1 ICE Interface Signals

Table 11-16. ICE Interface Timing Specification

Symbol	Parameter	Conditions	Min	Max	Units
ICE_0	TCK Low Half-period	(1)			ns
ICE_1	TCK High Half-period	(1)			ns
ICE_2	TCK Period	(1)			ns
ICE_3	TDI, TMS, Setup before TCK High	(1)			ns
ICE_4	TDI, TMS, Hold after TCK High	(1)			ns
ICE_5	TDO Hold Time	(1)			ns
ICE_6	TCK Low to TDO Valid	(1)			ns

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF

Figure 11-2. ICE Interface Signals



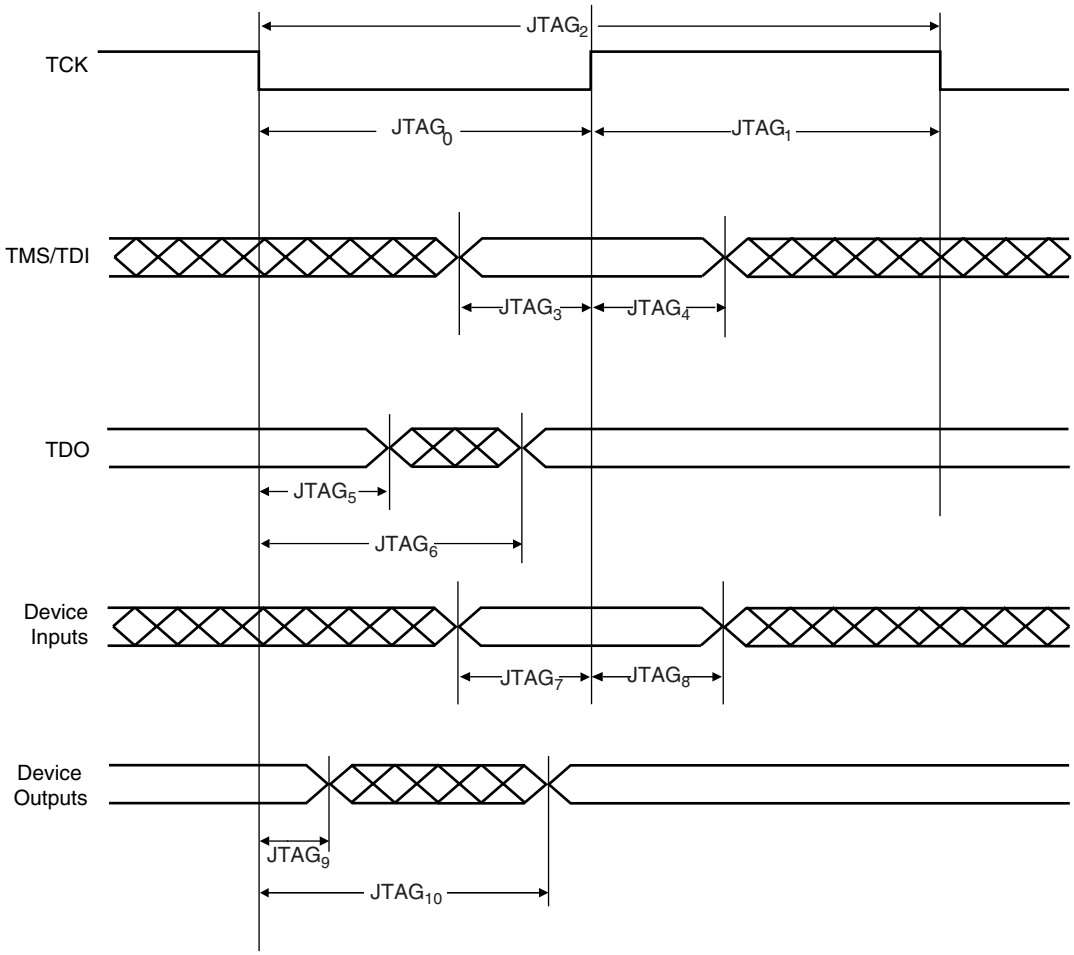
11.9.2 JTAG Interface Signals

Table 11-17. JTAG Interface Timing specification

Symbol	Parameter	Conditions	Min	Max	Units
$JTAG_0$	TCK Low Half-period	(1)	6		ns
$JTAG_1$	TCK High Half-period	(1)	3		ns
$JTAG_2$	TCK Period	(1)	9		ns
$JTAG_3$	TDI, TMS Setup before TCK High	(1)	1		ns
$JTAG_4$	TDI, TMS Hold after TCK High	(1)	0		ns
$JTAG_5$	TDO Hold Time	(1)	4		ns
$JTAG_6$	TCK Low to TDO Valid	(1)		6	ns
$JTAG_7$	Device Inputs Setup Time	(1)			ns
$JTAG_8$	Device Inputs Hold Time	(1)			ns
$JTAG_9$	Device Outputs Hold Time	(1)			ns
$JTAG_{10}$	TCK to Device Outputs Valid	(1)			ns

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF

Figure 11-3. JTAG Interface Signals



11.10 SPI Characteristics

Figure 11-4. SPI Master mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)

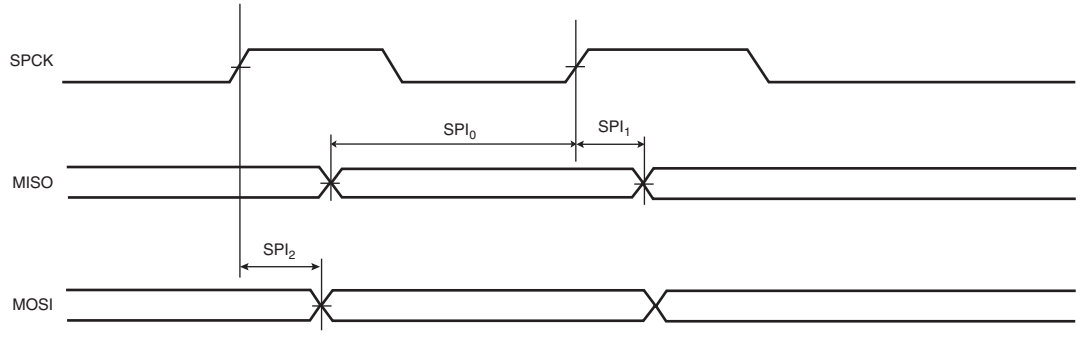


Figure 11-5. SPI Master mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

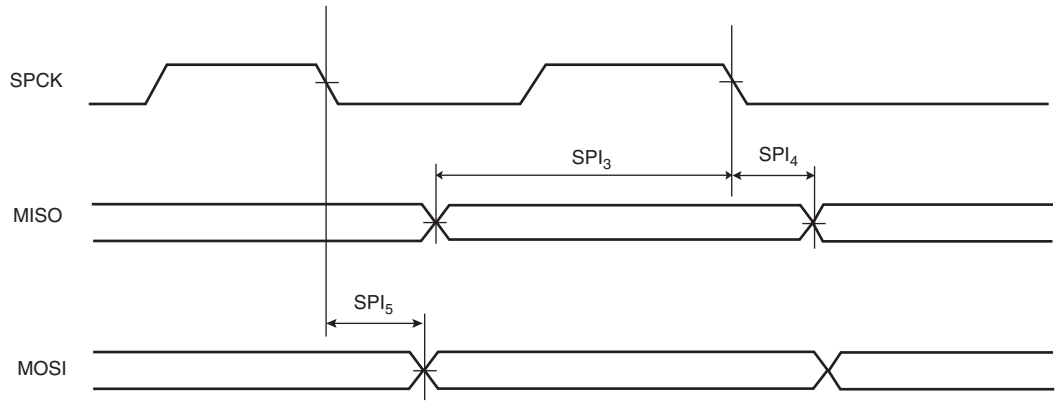


Figure 11-6. SPI Slave mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

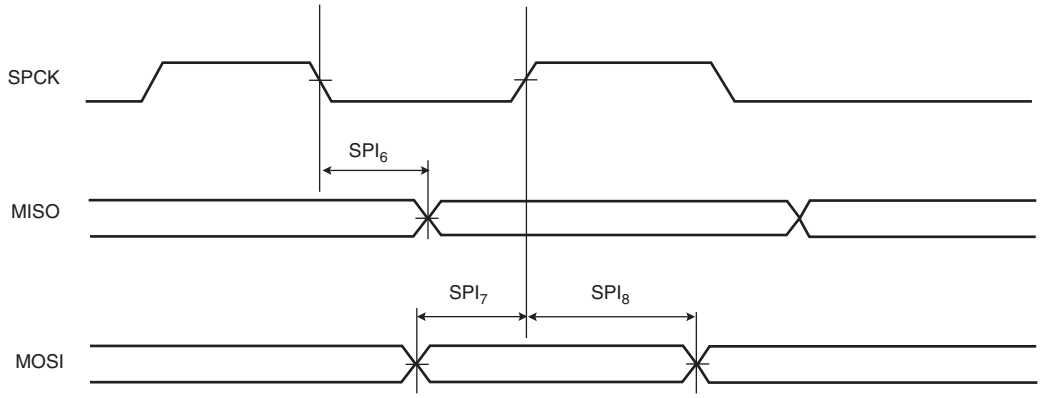


Figure 11-7. SPI Slave mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)

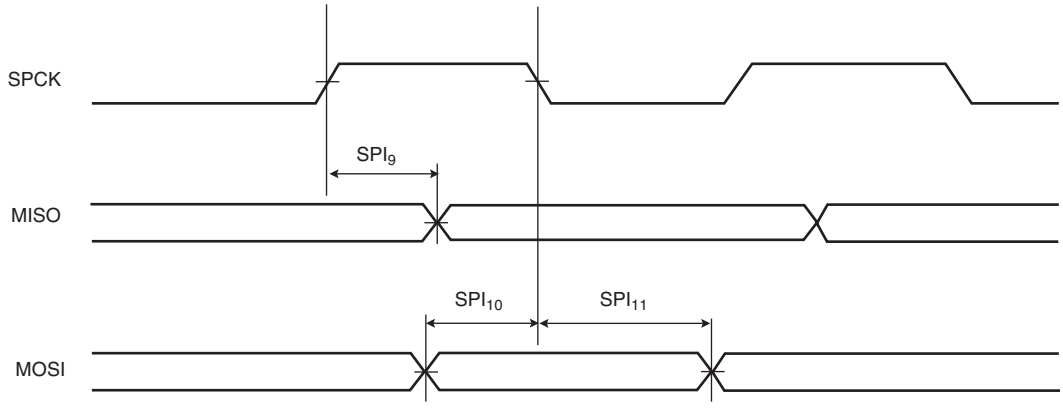


Table 11-18. SPI Timings

Symbol	Parameter	Conditions	Min	Max	Units
SPI_0	MISO Setup time before SPCK rises (master)	3.3V domain(1)	22 + (t_{CPMCK})/2(2)		ns
SPI_1	MISO Hold time after SPCK rises (master)	3.3V domain(1)	0		ns
SPI_2	SPCK rising to MOSI Delay (master)	3.3V domain(1)		7	ns
SPI_3	MISO Setup time before SPCK falls (master)	3.3V domain(1)	22 + (t_{CPMCK})/2(2)		ns
SPI_4	MISO Hold time after SPCK falls (master)	3.3V domain (1)	0		ns
SPI_5	SPCK falling to MOSI Delay (master)	3.3V domain (1)		7	ns
SPI_6	SPCK falling to MISO Delay (slave)	3.3V domain (1)		26.5	ns
SPI_7	MOSI Setup time before SPCK rises (slave)	3.3V domain (1)	0		ns
SPI_8	MOSI Hold time after SPCK rises (slave)	3.3V domain (1)	1.5		ns
SPI_9	SPCK rising to MISO Delay (slave)	3.3V domain (1)		27	ns
SPI_{10}	MOSI Setup time before SPCK falls (slave)	3.3V domain (1)	0		ns
SPI_{11}	MOSI Hold time after SPCK falls (slave)	3.3V domain (1)	1		ns

Notes: 1. 3.3V domain: V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40 pF.
2. t_{CPMCK}: Master Clock period in ns.

11.11 Flash Characteristics

The following table gives the device maximum operating frequency depending on the field FWS of the Flash FSR register. This field defines the number of wait states required to access the Flash Memory.

Table 11-19. Flash Wait States

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	33
1	2 cycles	60

12. Mechanical Characteristics

12.1 Thermal Considerations

12.1.1 Thermal Data

Table 12-1 summarizes the thermal resistance data depending on the package.

Table 12-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP64	TBD	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP64	TBD	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP48	TBD	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP48	TBD	

12.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

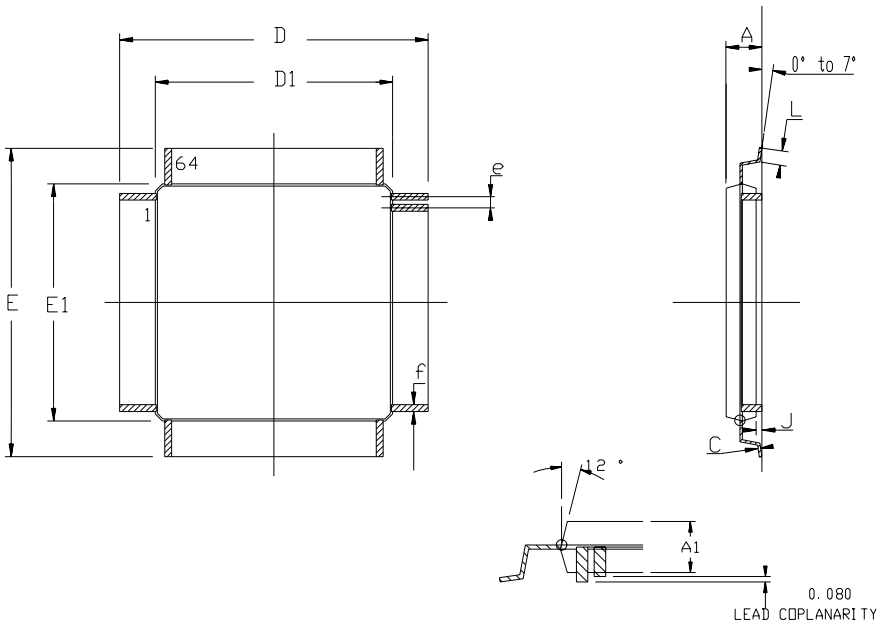
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 12-1 on page 45.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 12-1 on page 45.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section "Power Consumption" on page 33.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

12.2 Package Drawings

Figure 12-1. TQFP-64 package drawing



	MM		INCH	
	Min	Max	Min	Max
A	----	1.20	----	.047
A1	0.95	1.05	.037	.041
C	0.09	0.20	.004	.008
D	12.00 BSC		.472 BSC	
D1	10.00 BSC		.394 BSC	
E	12.00 BSC		.472 BSC	
E1	10.00 BSC		.394 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.17	0.27	.007	.011

Table 12-2. Device and Package Maximum Weight

TBD	mg

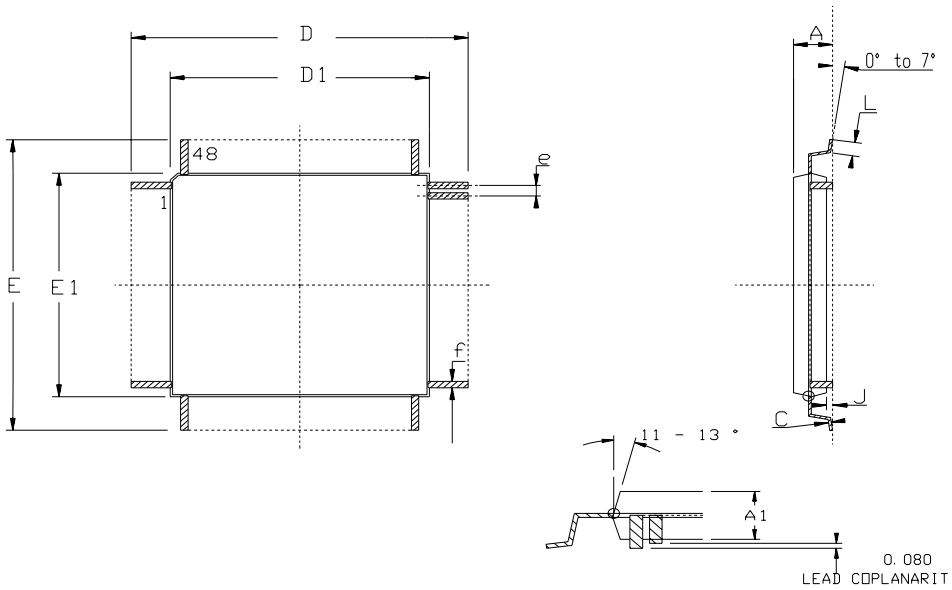
Table 12-3. Package Characteristics

Moisture Sensitivity Level	TBD

Table 12-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 12-2. TQFP-48 package drawing



	MM		INCH	
	Min	Max	Min	Max
A	----	1.20	----	.047
A1	0.95	1.05	.037	.041
C	0.09	0.20	.004	.008
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.17	0.27	.0067	.0106

Table 12-5. Device and Package Maximum Weight

TBD	mg

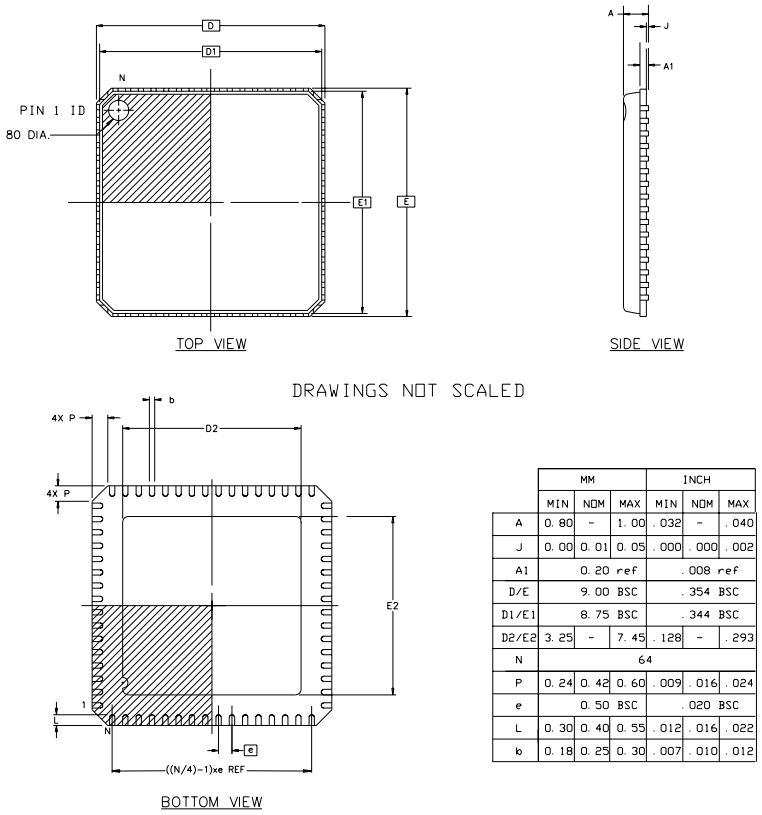
Table 12-6. Package Characteristics

Moisture Sensitivity Level	TBD

Table 12-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 12-3. QFN-64 package drawing



	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	-	1.00	.032	-	.040
J	0.00	0.01	0.05	.000	.000	.002
A1		0.20 ref			.008 ref	
D/E		9.00 BSC			.354 BSC	
D1/E1		8.75 BSC			.344 BSC	
D2/E2	3.25	-	7.45	.128	-	.293
N		64				
P	0.24	0.42	0.60	.009	.016	.024
e		0.50 BSC			.020 BSC	
L	0.30	0.40	0.55	.012	.016	.022
b	0.18	0.25	0.30	.007	.010	.012

Table 12-8. Device and Package Maximum Weight

TBD	mg

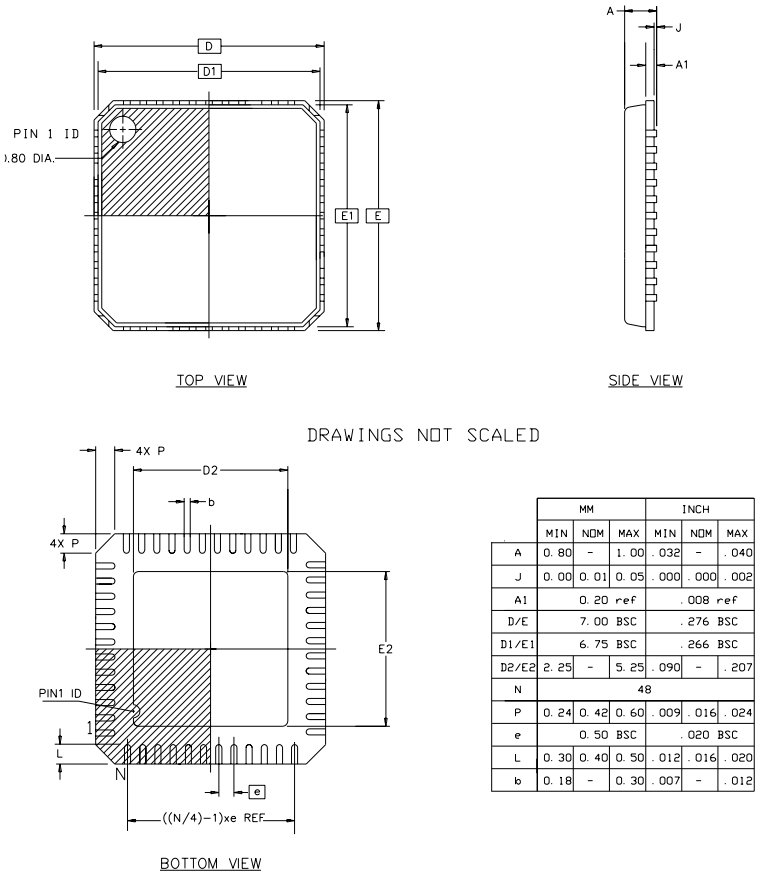
Table 12-9. Package Characteristics

Moisture Sensitivity Level	TBD

Table 12-10. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	E3

Figure 12-4. QFN-48 package drawing



	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	-	1.00	.032	-	.040
J	0.00	0.01	0.05	.000	.000	.002
A1		0.20 ref			.008 ref	
D/E		7.00 BSC			.276 BSC	
D1/E1		6.75 BSC			.266 BSC	
D2/E2	2.25	-	5.25	.090	-	.207
N		48				
P	0.24	0.42	0.60	.009	.016	.024
e		0.50 BSC			.020 BSC	
L	0.30	0.40	0.50	.012	.016	.020
b	0.18	-	0.30	.007	-	.012

Table 12-11. Device and Package Maximum Weight

TBD	mg

Table 12-12. Package Characteristics

Moisture Sensitivity Level	TBD

Table 12-13. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	E3

12.3 Soldering Profile

Table 12-14 gives the recommended soldering profile from J-STD-20.

Table 12-14. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	TBD
Preheat Temperature 175°C ±25°C	TBD
Temperature Maintained Above 217°C	TBD
Time within 5°C of Actual Peak Temperature	TBD
Peak Temperature Range	TBD
Ramp-down Rate	TBD
Time 25°C to Peak Temperature	TBD

Note: It is recommended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.

13. Ordering Information

Device	Ordering Code	Package	Conditioning	Temperature Operating Range
AT32UC3B0256	AT32UC3B0256-A2UT	TQFP 64	Tray	Industrial (-40°C to 85°C)
	AT32UC3B0256-Z2UT	QFN 64	Tray	Industrial (-40°C to 85°C)
AT32UC3B0128	AT32UC3B0128-A2UT	TQFP 64	Tray	Industrial (-40°C to 85°C)
	AT32UC3B0128-Z2UT	QFN 64	Tray	Industrial (-40°C to 85°C)
AT32UC3B064	AT32UC3B064-A2UT	TQFP 64	Tray	Industrial (-40°C to 85°C)
	AT32UC3B064-Z2UT	QFN 64	Tray	Industrial (-40°C to 85°C)
AT32UC3B1256	AT32UC3B1256-AUT	TQFP 48	Tray	Industrial (-40°C to 85°C)
	AT32UC3B1256-Z1UT	QFN 48	Tray	Industrial (-40°C to 85°C)
AT32UC3B1128	AT32UC3B1128-AUT	TQFP 48	Tray	Industrial (-40°C to 85°C)
	AT32UC3B1128-Z1UT	QFN 48	Tray	Industrial (-40°C to 85°C)
AT32UC3B164	AT32UC3B164-AUT	TQFP 48	Tray	Industrial (-40°C to 85°C)
	AT32UC3B164-Z1UT	QFN 48	Tray	Industrial (-40°C to 85°C)

14. Errata

All industrial parts labelled with -UES (for engineering samples) are revision B parts.

14.1 Rev. F

14.1.1 PWM

1. **PWM channel interrupt enabling triggers an interrupt**
   When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

   Fix/Workaround
   When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

2. **PWN counter restarts at 0x0001**
   The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.
   Fix/Workaround
   - The first period is 0x0000, 0x0001, ..., period
   - Consecutive periods are 0x0001, 0x0002, ..., period

3. **PWM update period to a 0 value does not work**
   It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

   Fix/Workaround
   Do not update the PWM_CUPD register with a value equal to 0.

14.1.2 SPI

1. **SPI Slave / PDCA transfer: no TX UNDERRUN flag**
   There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

   Fix/Workaround
   For PDCA transfer: none.

2. **SPI FDIV option does not work**
   Selecting clock signal using FDIV = 1 does not work as specified.

   Fix/Workaround
   Do not set FDIV = .1

3. **SPI disable does not work in SLAVE mode.**
   Fix/Workaround
   Read the last received data, then perform a Software Reset.

4. **SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0**
   When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an aditional pulse will be generated on SCK.

Fix/workaround

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

5. **SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**

   In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

   Fix/Workaround

   1. Set slave mode, set required CPOL/CPHA.
   2. Enable SPI.
   3. Set the polarity CPOL of the line in the opposite value of the required one.
   4. Set the polarity CPOL to the required one.
   5. Read the RXHOLDING register.

   Transfers can now befin and RXREADY will now behave as expected.

14.1.3 Power Manager

1. **If the BOD level is higher than VDDCORE, the part is constantly resetted**

   If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

   Fix/Workaround

   Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

14.1.4 ADC

1. **Sleep Mode activation needs addtionnal A to D conversion**

   If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

   Fix/Workaround

   Activate the sleep mode in the mode register and then perform an AD conversion.

14.2 Rev. B

14.2.1 Processor and Architecture

1. **Local Busto fast GPIO not available on silicon Rev B**
   Local bus is only available for silicon RevE and later.

   Fix/Workaround
   Do not use if silicon revison older than F.

2. **Memory Protection Unit (MPU) is non functional.**
   Fix/Workaround
   Do not use the MPU.

3. **Bus error should be masked in Debug mode**
   If a bus error occurs during debug mode, the processor will not respond to debug commands through the DINST register.

   Fix/Workaround
   A reset of the device will make the CPU respond to debug commands again.

4. **Read Modify Write (RMW) instructions on data outside the internal RAM does not work.**
   Read Modify Write (RMW) instructions on data outside the internal RAM does not work.

   Fix/Workaround
   Do not perform RMW instructions on data outside the internal RAM.

5. **Need two NOPs instruction after instructions masking interrupts**
   The instructions following in the pipeline the instruction masking the interrupt through SR may behave abnormally.

   Fix/Workaround
   Place two NOPs instructions after each SSRF or MTSR instruction setting IxM or GM in SR

6. **Clock connection table on Rev B**
   Here is the table of Rev B

Figure 14-1. Timer/Counter clock connections on RevB

Source	Name	Connection
Internal	TIMER_CLOCK1	32KHz Oscillator
	TIMER_CLOCK2	PBA Clock / 4
	TIMER_CLOCK3	PBA Clock / 8
	TIMER_CLOCK4	PBA Clock / 16
	TIMER_CLOCK5	PBA Clock / 32
External	XC0	
	XC1	
	XC2	

7. **Spurious interrupt may corrupt core SR mode to exception**
   If the rules listed in the chapter `Masking interrupt requests in peripheral modules' of the AVR32UC Technical Reference Manual are not followed, a spurious interrupt may occur. An interrupt context will be pushed onto the stack while the core SR mode will indicate an exception. A RETE instruction would then corrupt the stack..

   Fix/Workaround
   Follow the rules of the AVR32UC Technical Reference Manual. To increase software robustness, if an exception mode is detected at the beginning of an interrupt handler, change the stack interrupt context to an exception context and issue a RETE instruction.

8. **CPU cannot operate on a divided slow clock (internal RC oscillator)**
   Fix/Workaround
   Do not run the CPU on a divided slow clock.

14.2.2 PWM

1. **PWM counter restarts at 0x0001**
   The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

   Fix/Workaround
   - The first period is 0x0000, 0x0001, ..., period

   - Consecutive periods are 0x0001, 0x0002, ..., period

2. **PWM channel interrupt enabling triggers an interrupt**
   When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

   Fix/Workaround
   When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

3. **PWM update period to a 0 value does not work**
   It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

   Fix/Workaround
   Do not update the PWM_CUPD register with a value equal to 0.

4. **PWM channel status may be wrong if disabled before a period has elapsed**
   Before a PWM period has elapsed, the read channel status may be wrong. The CHIDx-bit for a PWM channel in the PWM Enable Register will read '1' for one full PWM period even if the channel was disabled before the period elapsed. It will then read '0' as expected.

   Fix/Workaround
   Reading the PWM channel status of a disabled channel is only correct after a PWM period has elapsed.

5. **The following alternate C functions PWM[4] on PA16 and PWM[6] on PA31 are not available on Rev B.**
   Fix/Workaround

Do not use these PWM alternate functions on these pins.

14.2.3 SPI

1. **SPI FDIV option does not work**
   Selecting clock signal using FDIV = 1 does not work as specified.

   Fix/Workaround
   Do not set FDIV = 1.

2. **SPI Slave / PDCA transfer: no TX UNDERRUN flag**
   There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

   Fix/Workaround
   For PDCA transfer: none.

3. **SPI Bad serial clock generation on 2nd chip select when SCBR=1, CPOL=1 and CNCPHA=0**
   When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.

   Fix/Workaround
   When multiple CS are in use, if one of the baudrate equals to 1, the other must also equal 1 if CPOL=1 and CPHA=0.

4. **SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**
   In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

   Fix/Workaround
   1. Set slave mode, set required CPOL/CPHA.
   2. Enable SPI.
   3. Set the polarity CPOL of the line in the opposite value of the required one.
   4. Set the polarity CPOL to the required one.
   5. Read the RXHOLDING register.

   Transfers can now befin and RXREADY will now behave as expected.

5. **SPI CSNAAT bit 2 in register CSR0...CSR3 is not available.**
   Fix/Workaround
   Do not use this bit.

6. **SPI disable does not work in SLAVE mode.**
   Fix/Workaround
   Read the last received data, then perform a Software Reset.

7. **SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0**
   When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an aditional pulse will be generated on SCK.
   Fix/workaround

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

14.2.4 Power Manager

1. **PLL Lock control does not work**
   PLL lock Control does not work.

   Fix/Workaround
   In PLL Control register, the bit 7 should be set in order to prevent unexpected behaviour.

2. **Wrong reset causes when BOD is activated**
   Setting the BOD enable fuse will cause the Reset Cause Register to list BOD reset as the reset source even though the part was reset by another source.

   Fix/Workaround
   Do not set the BOD enable fuse, but activate the BOD as soon as your program starts.

3. **System Timer mask (Bit 16) of the PM CPUMASK register is not available.**
   Fix/Workaround
   Do not use this bit.

14.2.5 SSC

1. **SSC does not trigger RF when data is low**
   The SSC cannot transmit or receive data when CKS = CKDIV and CKO = none, in TCMR or RCMR respectively.

   Fix/Workaround
   Set CKO to a value that is not "none" and bypass the output of the TK/RK pin with the GPIO.

14.2.6 USB

1. **USB No end of host reset signaled upon disconnection**
   In host mode, in case of an unexpected device disconnection whereas a usb reset is being sent by the usb controller, the UHCON.RESET bit may not been cleared by the hardware at the end of the reset.

   Fix/Workaround
   A software workaround consists in testing (by polling or interrupt) the disconnection (UHINT.DDISCI == 1) while waiting for the end of reset (UHCON.RESET == 0) to avoid being stuck.

2. **USBFSM and UHADDR1/2/3 registers are not available.**
   Do not use USBFSM register.

   Fix/Workaround
   Do not use USBFSM register and use HCON[6:0] field instead for all the pipes.

14.2.7 Cycle counter

1. **CPU Cycle Counter does not reset the COUNT system register on COMPARE match.**
   The device revision B does not reset the COUNT system register on COMPARE match. In this revision, the COUNT register is clocked by the CPU clock, so when the CPU clock stops, so does incrementing of COUNT**.**
   Fix/Workaround
   None.

14.2.8 ADC

1. **ADC possible miss on DRDY when disabling a channel**
   The ADC does not work properly when more than one channel is enabled.

   Fix/Workaround
   Do not use the ADC with more than one channel enabled at a time.

2. **ADC OVRE flag sometimes not reset on Status Register read**
   The OVRE flag does not clear properly if read simultaneously to an end of conversion.

   Fix/Workaround
   None.

3. **Sleep Mode activation needs addtionnal A to D conversion**
   If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

   Fix/Workaround
   Activate the sleep mode in the mode register and then perform an AD conversion.

14.2.9 USART

1. **USART Manchester Encoder Not Working**
   Manchester encoding/decoding is not working.

   Fix/Workaround
   Do not use manchester encoding.

2. **USART RXBREAK problem when no timeguard**
   In asynchronous mode the RXBREAK flag is not correctly handled when the timeguard is 0 and the break character is located just after the stop bit.

   Fix/Workaround
   If the NBSTOP is 1, timeguard should be different from 0.

3. **USART Handshaking: 2 characters sent / CTS rises when TX**
   If CTS switches from 0 to 1 during the TX of a character, if the Holding register is not empty, the TXHOLDING is also transmitted.

   Fix/Workaround
   None.

4. **USART PDC and TIMEGUARD not supported in MANCHESTER**
   Manchester encoding/decoding is not working.

   Fix/Workaround
   Do not use manchester encoding.

5. **USART SPI mode is non functional on this revision**
   Fix/Workaround
   Do not use the USART SPI mode.

14.2.10 HMATRIX

1. **HMatrix fixed priority arbitration does not work**
   Fixed priority arbitration does not work.

   Fix/Workaround
   Use Round-Robin arbitration instead.

14.2.11 Clock caracteristic

1. **PBA max frequency**
   The Peripheral bus A (PBA) max frequency is 30MHz instead of 60MHz.

   Fix/Workaround
   Do not set the PBA maximum frequency higher than 30MHz.

14.2.12 FLASHC

1. **The address of Flash General Purpose Fuse Register Low (FGPFRLO) is 0xFFFE140C on revB instead of 0xFFFE1410.**
   Fix/Workaround
   None.

2. **The command Quick Page Read User Page(QPRUP) is not functional.**
   Fix/Workaround
   None.

3. **PAGEN Semantic Field for Program GP Fuse Byte is WriteData[7:0], ByteAddress[1:0] on revision B instead of WriteData[7:0], ByteAddress[2:0].**
   Fix/Workaround
   None.

14.2.13 RTC

1. **Writes to control (CTRL), top (TOP) and value (VAL) in the RTC are discarded if the RTC peripheral bus clock (PBA) is divided by a factor of four or more relative to the HSB clock.**
   Fix/Workaround
   Do not write to the RTC registers using the peripheral bus clock (PBA) divided by a factor of four or more relative to the HSB clock.

2. **The RTC CLKEN bit (bit number 16) of CTRL register is not available..**
   Fix/Workaround

Do not use the CLKEN bit of the RTC on Rev B.

14.2.14 OCD

1. **Stalled memory access instruction writeback fails if followed by a HW breakpoint.**
   Consider the following assembly code sequence:
   A
   B
   If a hardware breakpoint is placed on instruction B, and instruction A is a memory access instruction, register file updates from instruction A can be discarded.
   Fix/Workaround
   Do not place hardware breakpoints, use software breakpoints instead.
   Alternatively, place a hardware breakpoint on the instruction before the memory access instruction and then single step over the memory access instruction.

15. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

15.1 Rev. G – 04/08

1. Open Drain Mode removed from ”General-Purpose Input/Output Controller (GPIO)” on page 151.

15.2 Rev. F – 4/08

1. Updated ”Errata” on page 788.

15.3 Rev. E – 12/07

1. Updated ”Memory protection” on page 18.

15.4 Rev. D – 11/07

1. Updated ”The AVR32UC CPU” on page 16.
2. Updated ”Electrical Characteristics” on page 30.

15.5 Rev. C – 10/07

1. Updated ”Features” on page 1.
2. Updated block diagram with local bus Figure 3-1 on page 4.
3. Add schematic for HMatrix master/slave connection Figure 9-1 on page 29.
4. Updated ”Peripherals” on page 32 with local bus.
5. Added SPI feature ”Universial Synchronous/Asynchronous Receiver/Transmitter (USART)” on page 298.
6. Updated ”USB On-The-Go Interface (USBB)” on page 367.
7. Updated ADC trigger selection in ”Analog-to-Digital Converter (ADC)” on page 568.
8. Updated ”JTAG and Boundary Scan” on page 594 with programming procedure.
9. Add description for silicon revision D page 52.
10. Add ABDAC Chapter

15.6 Rev. B – 07/07

1. Updated registered trademarks
2. Updated address page.

15.7 Rev. A – 05/07

1. Initial revision.

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