Micropower Long Range Timer

GENERAL DESCRIPTION

The XR-2243 is a monolithic Timer/Controller capable of producing ultra-long time delays from micro-seconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 11-bit binary counter and a control flop-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 1024 RC. If the two circuits are cascaded, a total time delay of $(1024)^2$ or 1,048,576 RC is obtained.

The XR-2243 long range timer was designed for low power operation. Its supply current requires less than 100 μA in standby or reset mode. Normal operation requires less than 1mA.

The timing cycle is initiated by applying a positive going pulse to the trigger input, Pin 6. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications, the output terminal (Pin 3) is connected to the reset terminal, Pin 5. In this manner, after 1024 clock pulses are counted, this output goes to "high" state and resets the circuit, thus completing the timing cycle. Therefore, after triggering, the output at Pin 3 will produce a total timing pulse of 1024 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

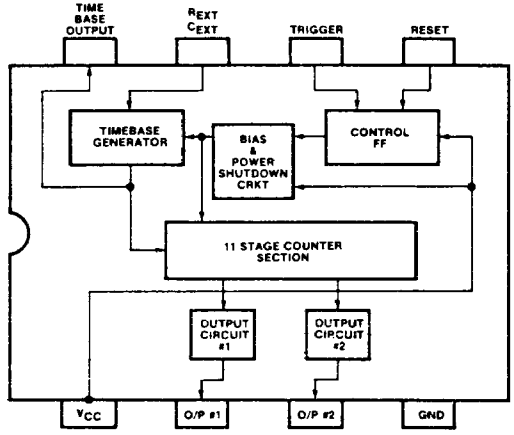
APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator
Battery Powered Applications

FEATURES

High Output Current Sink Capability
Timing from Micro-seconds to Days
Wide Supply Range: 2.7V to 15V
TTL and HCMOS Compatible Outputs

FUNCTIONAL BLOCK DIAGRAM



High Accuracy: 0.5%
Excellent Supply Rejection
Monostable and Astable Operation
Micro Power Consumption-Standby Operation
Low Power Consumption-Normal Operation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 Volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2243C	0°C to +70°C
Storage	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2243CN	Ceramic	0°C to +70°C
XR-2243CP	Plastic	0°C to +70°C

PRINCIPLES OF OPERATION

The ultra-long time delay micropower timer, in simplest block diagram terms, consists of a timing section followed by a counter section and a control flip-flop.

The main functional portion of the circuit is the time base section. It is a relaxation oscillator whose period

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, $R = 22\ k\Omega$, $C = 0.047\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2243C MIN	XR-2243C TYP	XR-2243C MAX	UNIT	CONDITIONS
Supply Voltage	2.7		15	V	
Supply Current		45	95	μA	$V_{CC} = 2.7V\ V_{TR} = 0V\ V_{RS} = 5V$
Standby		80	135	μA	$V_{CC} = 5V$
		250	415	μA	$V_{CC} = 15V$
Operating		900	1000	μA	$V_{CC} = 5V\ V_{TR} = 5V\ V_{RS} = 0V$
		750	900	μA	$V_{CC} = 2.7V$
		1250	1500	μA	$V_{CC} = 15V$
Time Base Section					
Timing Accuracy[1]		0.5	3	%	
Temperature Drift		80	125	ppm/°C	$V_{CC} = 2.7V\ V_{TR} = 5V\ V_{RS} = 0V$
		150	225	ppm/°C	$V_{CC} = 5V$
		300	650	ppm/°C	$V_{CC} = 15V\ 0°C \le T_A \le 70°C$
Supply Drift		0.30	1.0	%/V	$V_{CC} = 8V$
Maximum Frequency	25	35		kHz	
Recommended Range of Timing Components					
Timing Resistor, R	0.005		10	MΩ	
Timing Capacitor, C	0.005		1000	μF	**Low Leakage Capacitor**
Trigger/Reset Controls					
Trigger					Measures at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0	V	
Trigger Current		22	30	μA	$V_{RS} = 0,\ V_{TR} = 2V$
Impedance		25		kΩ	
Response Time[2]		**20**		**μS**	**Nominal**
Reset					
Reset Threshold		1.4	2.0	V	
Reset Current		22	30	μA	$V_{TR} = 0,\ V_{RS} = 2V$
Impedance		25		kΩ	
Response Time		**20**		**μS**	**Nominal**
Counter Section					See Figure 4, $V^+ = 5V$
Max. Toggle Rate	100	250		kHz	$V_{RS} = 0,\ V_{TR} = 5V$ Measured at Pin 8
Input:					
Impedance		15		kΩ	
Threshold		1.4		V	**$2.7V \le V_{CC} \le 15V$**
Output:					
Sink Current		10		mA	$V_{OL} \le 0.4V$
Leakage Current		0.01		μA	$V_{OH} \le 15V$

1. Timing error solely introduced by XR-2243.
2. Minimum time between reset and trigger is dependent upon timing capacitor values.

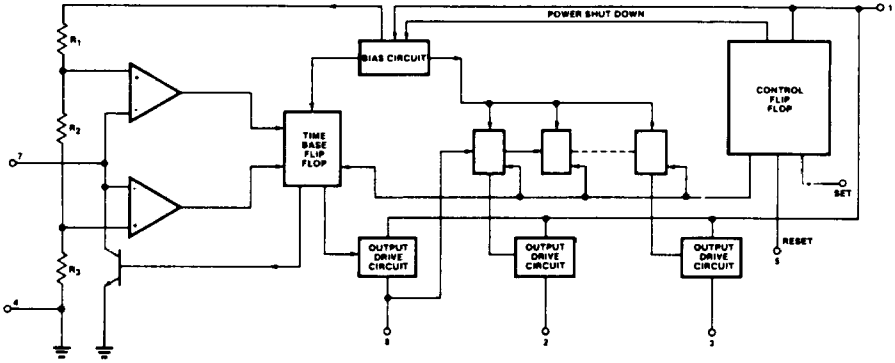


Figure 1. Simplified Circuit Schematic

of oscillation is determined by the external R and C values. The timing section is followed by an I^2L counter, which consists of eleven binary stages, with high current drive capability output stages from the first and the last. A third subsection of the circuit is the control logic circuit consisting of a flip-flop that is set and reset by Pins 6 and 5, respectively. This section controls the resetting of all counter stages, and starting the timing circuit upon application of a positive-going trigger pulse. The control logic also activates the power shut down circuit when a reset pulse is received, or when the timing cycle is completed. The power shut down circuit turns off the bias line to the time base and I^2L counters to reduce the standby power.

CONTROL FLIP-FLOP

The logic flip-flop circuit controls the time/counter, as well as the internal power, to reduce standby current consumption to approximately 100μA. Upon command, by a positive-going trigger pulse applied to Pin 6, the control logic circuit will first establish the upper and lower threshold voltages and then setup all internal current sources, biasing the time base and counter sections.

The circuit will automatically reset itself when power is first applied. Once triggered, the circuit is immune to additional trigger pulses until it is reset. A reset pin terminates the timing cycle by resetting the internal logic and shuts off the internal bias circuitry.

TIME BASE OSCILLATOR

The time base oscillator is a simple exponential ramp type timer circuit. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, the discharge transistor is "off", and the external capacitor, C, is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_{th-}, the upper comparator changes state, resets the flip-flop and turns the discharge transistor "off". Then, C charges toward V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_{th+}, the comparator changes state, sets the flip-flop again, and discharges C back to the lower threshold level, V_{th-}. In this manner, the circuit continues to oscillate with the voltage level across C exponentially rising to V_{th+}, then rapidly decaying to V_{th-} and then repeating this cycle until the timing period ends.

COUNTER SECTION (Pin 8)

The counter consists of eleven stages connected in a "ripple counter" configuration. The operating injector currents are set from a bus of 1.2 volts. This current is supply independent. Pin 8, which is time based o/p, is also the counter section input.

I^2L counters are D-type flip-flops with their $\overline{Q}$ output internally connected to their D input; basically, they form a divide by 2 block. With eleven stages, one could create delays of 1024 RC in a monostable mode of operation. The counters change state on the falling edge of the clock pulses.

When the trigger pulse is applied, the internal power line which is supplying voltage for I^2L circuitry (I^2L_{VCC}) is set up first, a Schmitt trigger circuit with a built in delay ensures the application of an internal set pulse, right after the power for the I^2 section is made available. The counters are all set to "1" and are ready to count with the incoming falling edges of clock impulses.

OUTPUT SECTIONS (Pins 2 and 3)

The output sections are designed such that they can handle 10mA load currents @ V_{OL} = 300mV. Both of the transistors in this section are operating in a non-saturated mode because of the clamping action. This ensures faster operation and also decreases the need **of high base drive at full load operation. The two outputs of the XR-2243 contain 1KΩ pull up resistors.**

The timing cycle for the circuit is initiated by applying a positive-going trigger to the set, or trigger pin, (Pin 6) of the device. The trigger pulse actuates the time base oscillator, enables the counter section, and sets the outputs to "low" state. The time base oscillator generates timing pulses with its period, T = 1RC. These timing or clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to the reset pin (Pin 5).

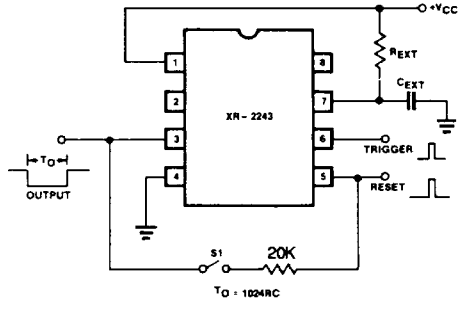


Figure 2. Typical Operation Diagram

ASTABLE AND MONOSTABLE MODE

Figure 2 shows the basic connection diagram for astable and monostable modes. When switch S_1 is open, the circuit is in its astable mode of operation. Upon the application of a trigger pulse, the time base oscillator resumes the timing cycles. Until the application of a reset pulse, the circuit will keep on working while generating a square wave at the last stage output, whose frequency is 1/2048 of the time base oscillator frequency. When switch S_1 is closed, the circuit is in its monostable mode of operation, with the last stage being connected to the reset input via an external resistor. This way, when a trigger pulse is applied, and the time base resumes its timing cycle, the last stage output will go low with the first pulse generated by the time

base generator, and will stay low for 1024 pulses. With the arrival of the 1024th pulse, the last output will go to a high state since it is coupled to the reset input (see Figure 3). When this stage goes high, the timing cycle is completed.

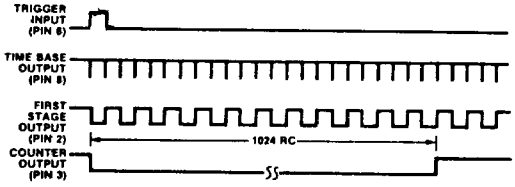


Figure 3. Timing Diagram of Output Waveforms

CASCADED MODE

The cascaded mode of operation allows the generation of ultra-long time delays. When several XR-2243 circuits are cascaded, such that their counter sections are connected in series, the total count available increases geometrically rather than arithmetically. Since one XR-2243 is capable of generating a total of 1024 RC time delay, where R and C are the external timing components, then when two such timers are cascaded, they will produce $(1024)^2$ RC and three will produce $(1024)^3$ RC time delay, and so on. Thus, one can easily achieve time delays in the range of days, months, or years, simply by cascading two or three such counter/timer circuits.

Figure 4 shows the basic connection for cascaded operation. Unit 2's time base is disabled by grounding Pin 7 to ground via 1 kΩ resistor. The last stage output of Unit 1 is connected to the input of the counter section of Unit 2. When the circuit is triggered, Unit 1 will resume generating a frequency whose period $T = R_{ext}C_{ext}$. The output of Unit 1 will change state every 1024 pulses. Since these pulses are supplied to Unit 2, the circuit will stop the timing cycle after 1024 pulses are generated by Unit 1. Therefore, a time delay of $(1024)^2$ RC is generated.

SEQUENTIAL TIMING APPLICATIONS

Figure 5 shows the basic connections for sequential timing applications. In this mode of operation, Unit 2's trigger input is connected to Unit 1's last output, while each unit's reset input is connected to their last output via external resistors. This way, Unit 1 will generate a time delay $1024\ R_1C_1$ upon the application of a trigger pulse. Once $1024\ R_1C_1$ seconds have elapsed, Unit 2 will be triggered, generating in its turn a delay equal to $1024\ R_2C_2$ seconds; therefore, resulting in an overall time delay of $1024\ R_1C_1 + 1024\ R_2C_2$.

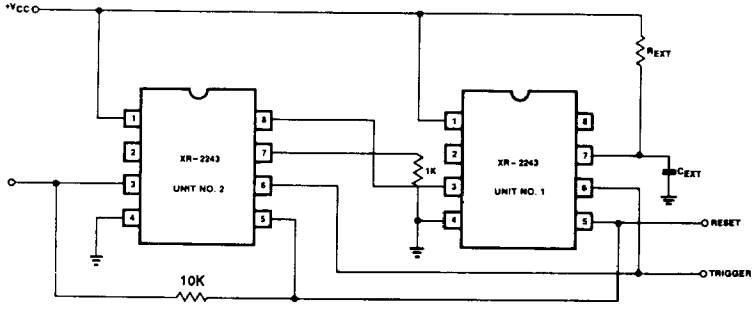


Figure 4. Cascaded Operation of Two XR-2243 Timer Circuits

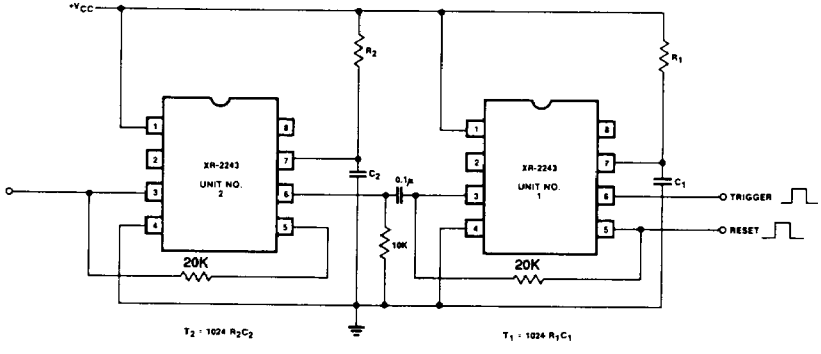


Figure 5. Sequential Timing Using XR-2243 Timer Circuits

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

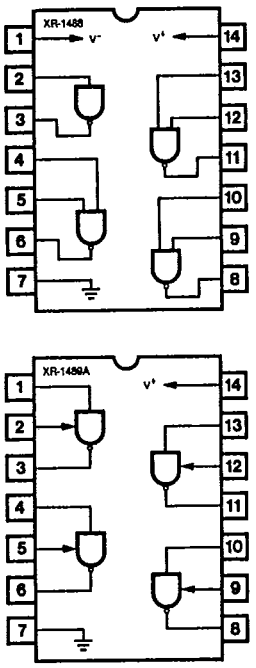
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.