27.0-31.0 GHz GaAs MMIC Power Amplifier

January 2010 - Rev 25-Jan-10

XP1027-BD

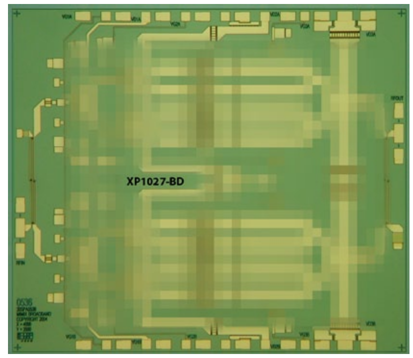
Features

- Ka-Band 4 W Power Amplifier
- Balanced Design Provides Good Input/Output Match
- 21.0 dB Small Signal Gain
- +35.5 dBm Saturated Output Power
- +43.0 dBm Output Third Order Intercept (OIP3)
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

General Description

Mimix Broadband's three stage 27.0-31.0 GHz GaAs MMIC power amplifier has a small signal gain of 21.0 dB with +35.5 dBm saturated output power. The device also includes Lange couplers to achieve good input/output return loss. This MMIC uses Mimix Broadband's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings

Supply Voltage (Vd)	+6.0 VDC[2]
Supply Current (Id1,2,3)	325,825,1575 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (Pin)	+25 dBm
Storage Temperature (Tstg)	-65 to +165 ºC
Operating Temperature (Ta)	-55 to +85 ºC
Channel Temperature (Tch)[1]	175 ºC

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.
(2) Under pulsed bias conditions, under CW Psat conditions further reduction in max supply voltage (~0.5V) is recommended.

Electrical Characteristics (Ambient Temperature T = 25 ºC)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	27.0	-	31.0
Input Return Loss (S11)	dB	-	20.0	-
Output Return Loss (S22)	dB	-	20.0	-
Small Signal Gain (S21)[2]	dB	-	21.0	-
Gain Flatness (ΔS21)	dB	-	+/-1.0	-
Reverse Isolation (S12)	dB	-	50.0	-
Output Power for 1dB Compression (P1dB)	dBm	-	+34.5	-
Output Third Order Intercept Point (OIP3)	dBm	-	+43.0	-
Saturated Output Power (Psat)[2]	dBm	-	+35.5	-
Drain Bias Voltage (Vd1,2,3)	VDC	-	+5.5	+5.8
Gate Bias Voltage (Vg1,2,3)	VDC	-1.0	-0.7	0.0
Supply Current (Id1) (Vd=5.5V, Vg=-0.7V Typical)	mA	-	250	300
Supply Current (Id2) (Vd=5.5V, Vg=-0.7V Typical)	mA	-	625	750
Supply Current (Id3) (Vd=5.5V, Vg=-0.7V Typical)	mA	-	1185	1435

(2) Measured on wafer pulsed.

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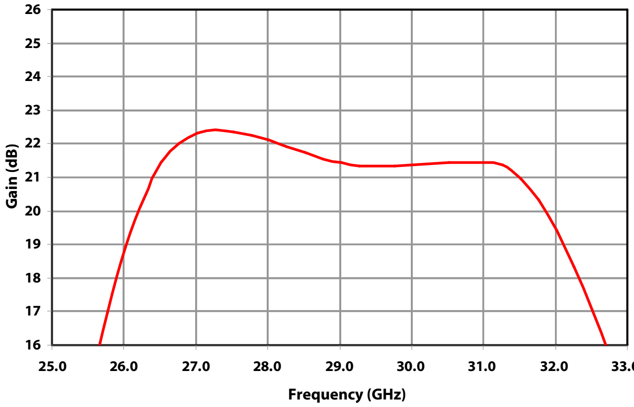
Power Amplifier Measurements (On-Wafer[1])

XP1027-BD Vd=5.0 V, Vg=-0.7 V, Id1=221 mA Id2=551 mA, Id3=1045 mA



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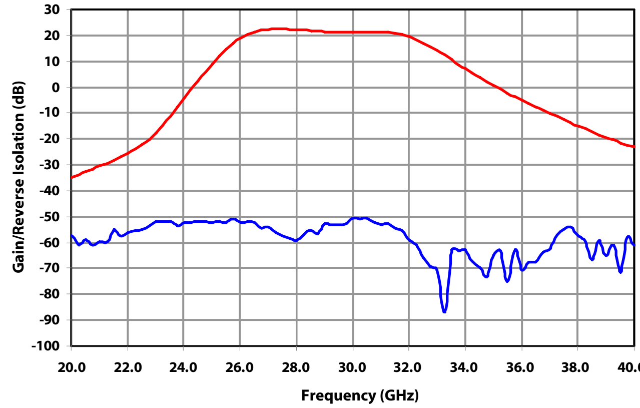

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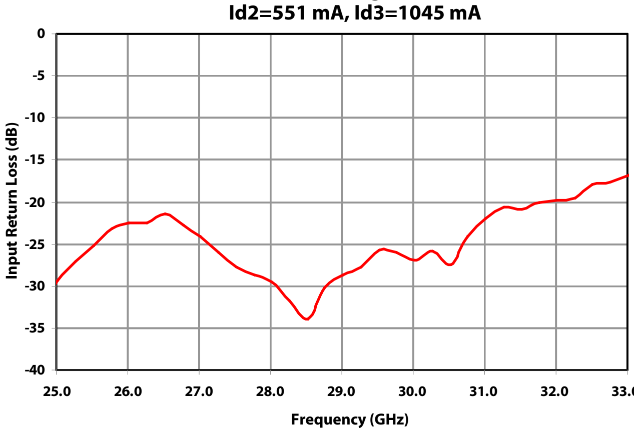

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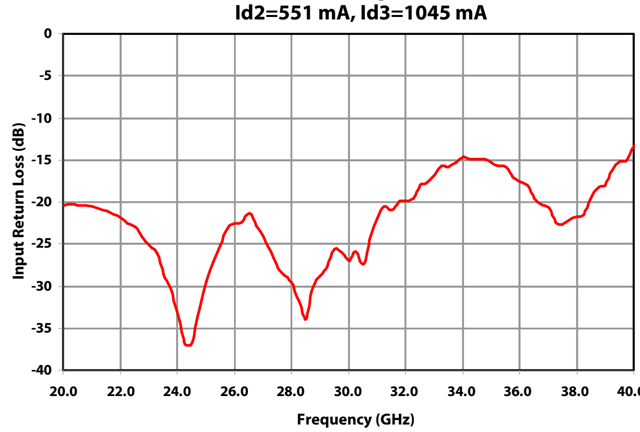

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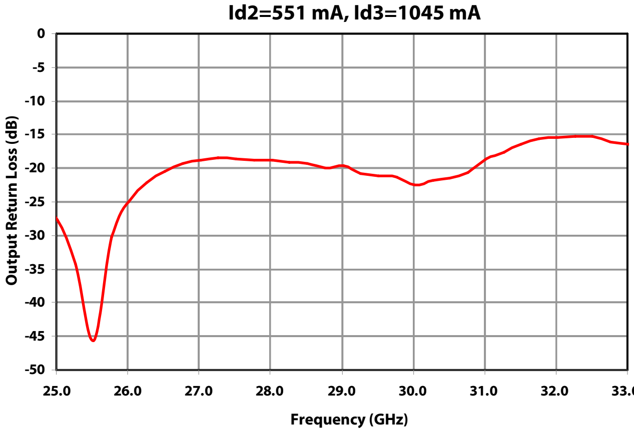

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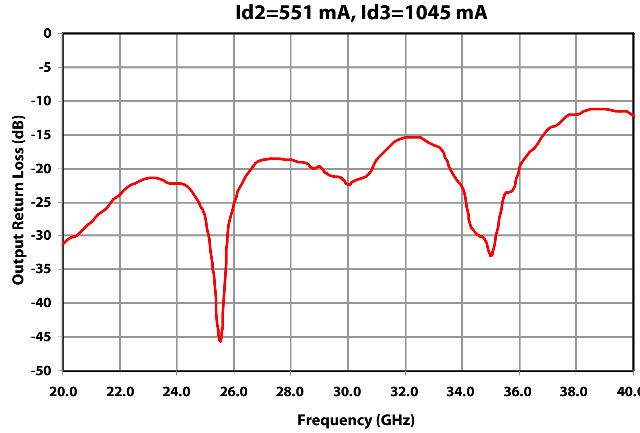
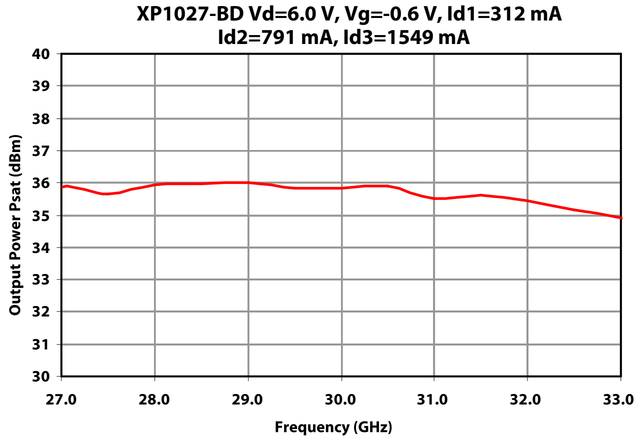
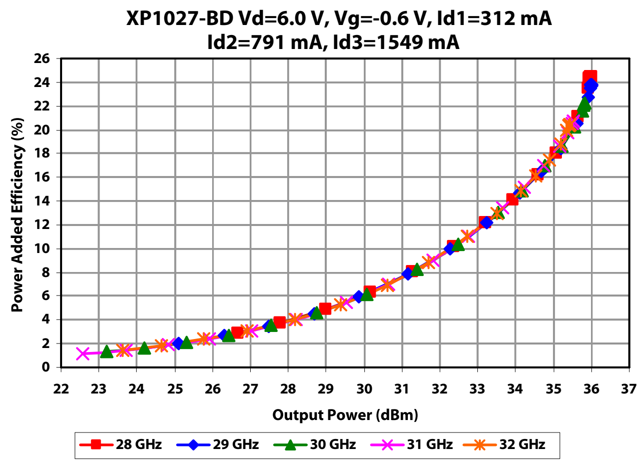
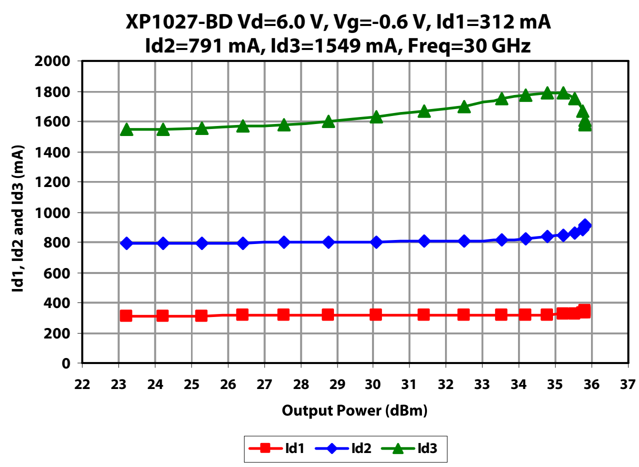


Note [1] Measurements – On-Wafer S-Parameters have been taken using reduced bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance Mimix T-pad transition and tuned output matching network is recommended. For additional information see the Mimix "T-Pad Transition" application note. Contact technical sales for output matching network information.

Power Amplifier Measurements (On-Wafer[1]) (cont.)

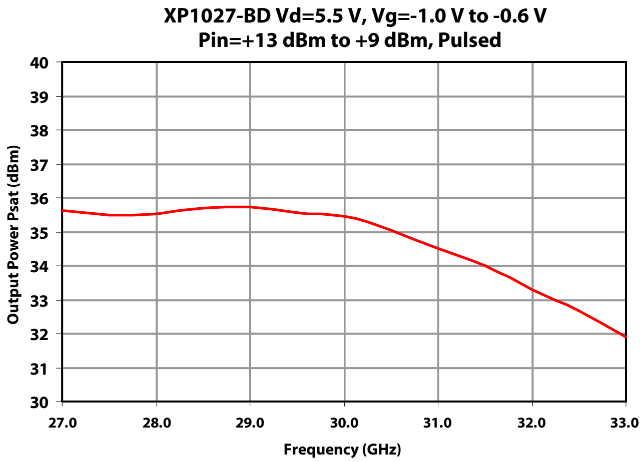


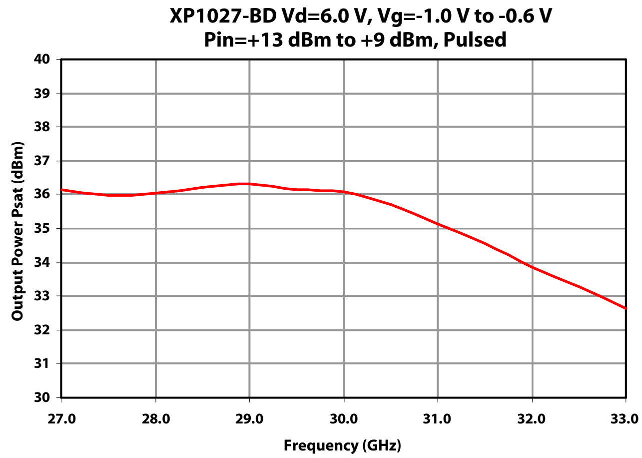


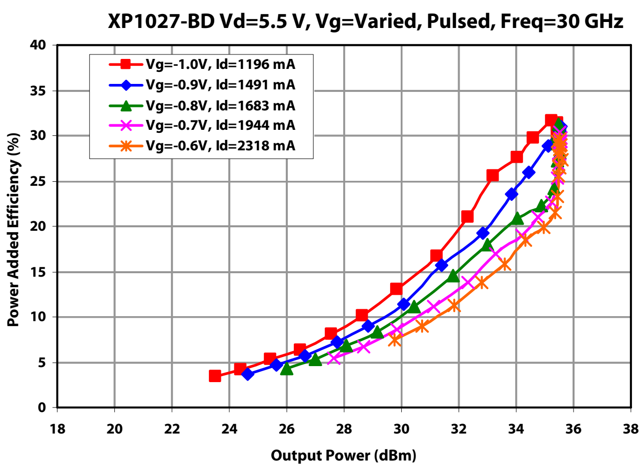


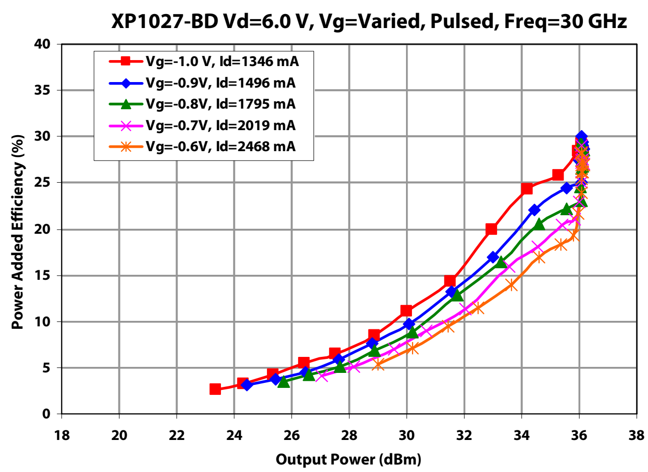
Note [1] Measurements – On-Wafer Output Power data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance Mimix T-pad transition and tuned output matching network is recommended. For additional information see the Mimix "T-Pad Transition" application note. Contact technical sales for output matching network information.

Power Amplifier Measurements (On-Wafer[1]) (cont.)



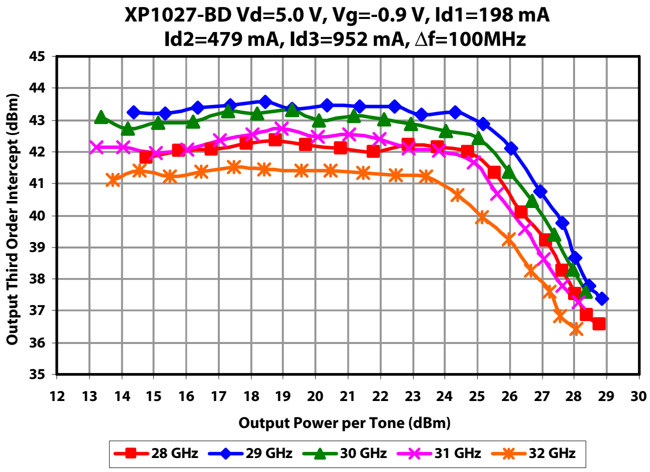


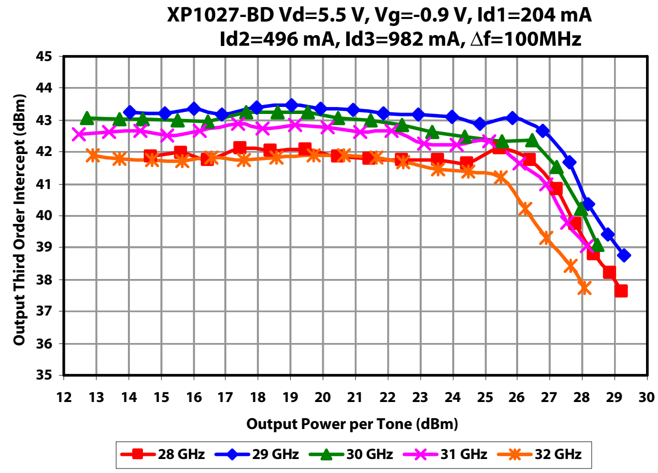


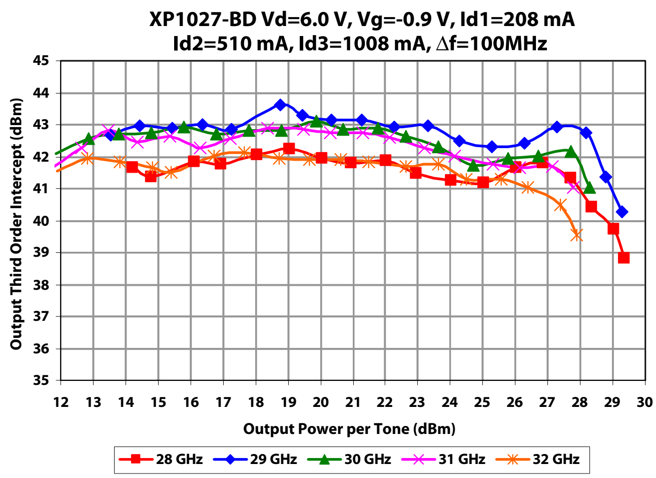


Note [1] Measurements – On-Wafer Output Power data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance Mimix T-pad transition and tuned output matching network is recommended. For additional information see the Mimix "T-Pad Transition" application note. Contact technical sales for output matching network information.

Power Amplifier Measurements (On-Wafer[1]) (cont.)



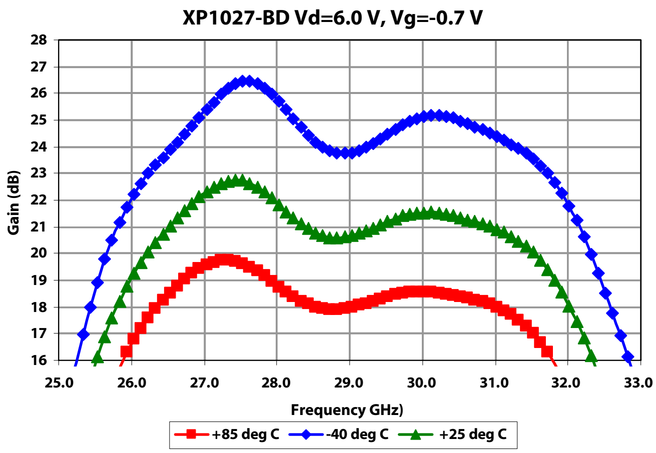


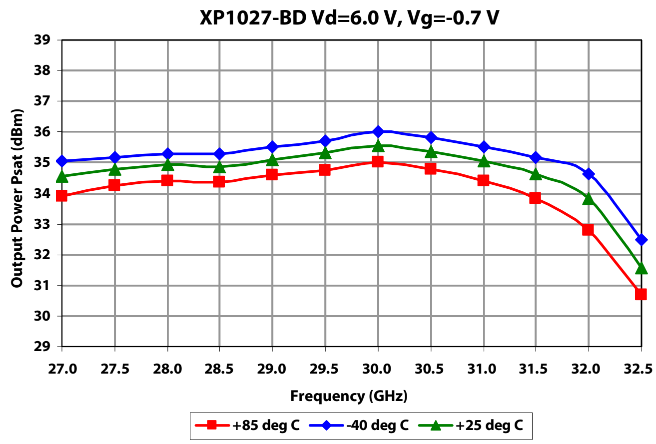


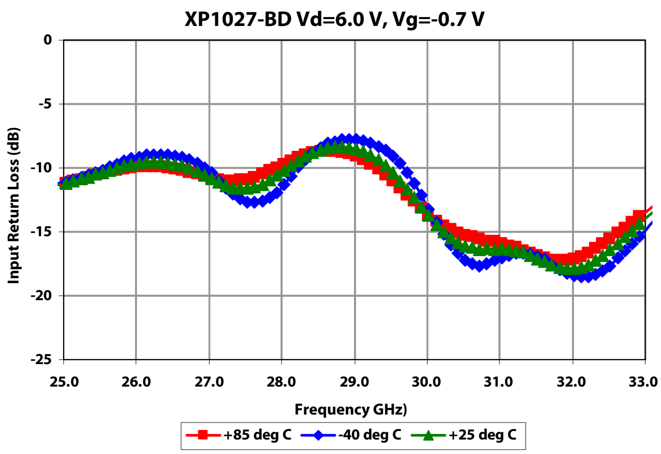
Additional Data – The XP1027 device consists of a balanced XP1026 pair. See the XP1026 data sheet for additional data concerning OIP3 control and optimization.

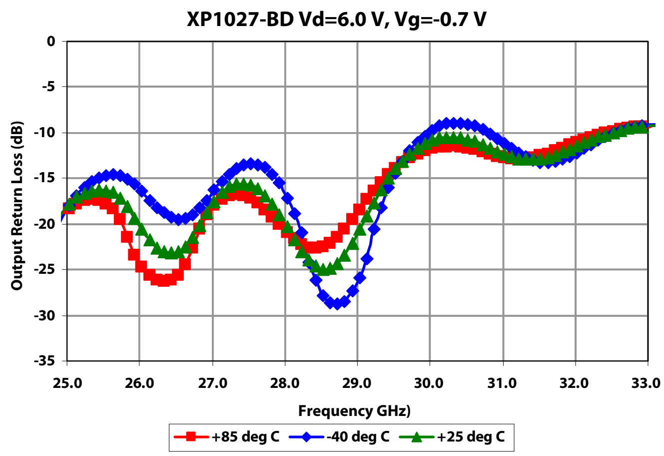
Note [1] Measurements – On-Wafer Output Power data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance Mimix T-pad transition and tuned output matching network is recommended. For additional information see the Mimix "T-Pad Transition" application note. Contact technical sales for output matching network information.

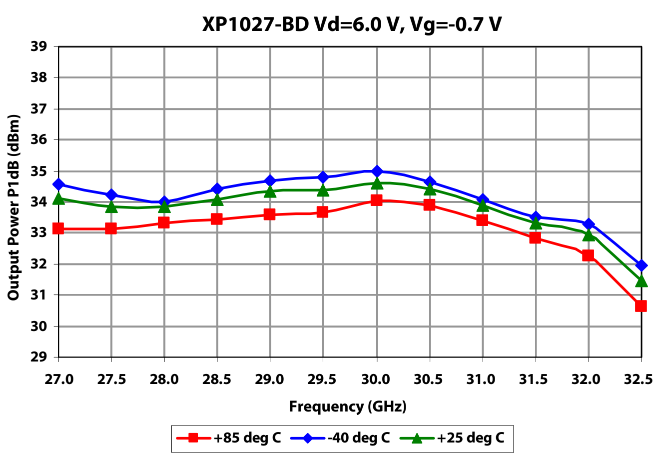
Power Amplifier Measurements (Text Fixture[1])

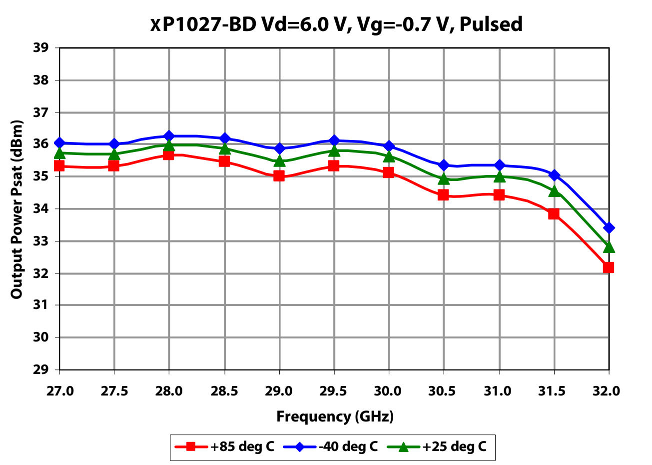












Note [1] Measurements – Test Fixture data includes all bond wire parasitics, uncompensated RF In/Out Mimix T-Pad transitions and RF ceramic circuit losses. For Gain and Output Power curves RF In/Out circuit losses have been removed.

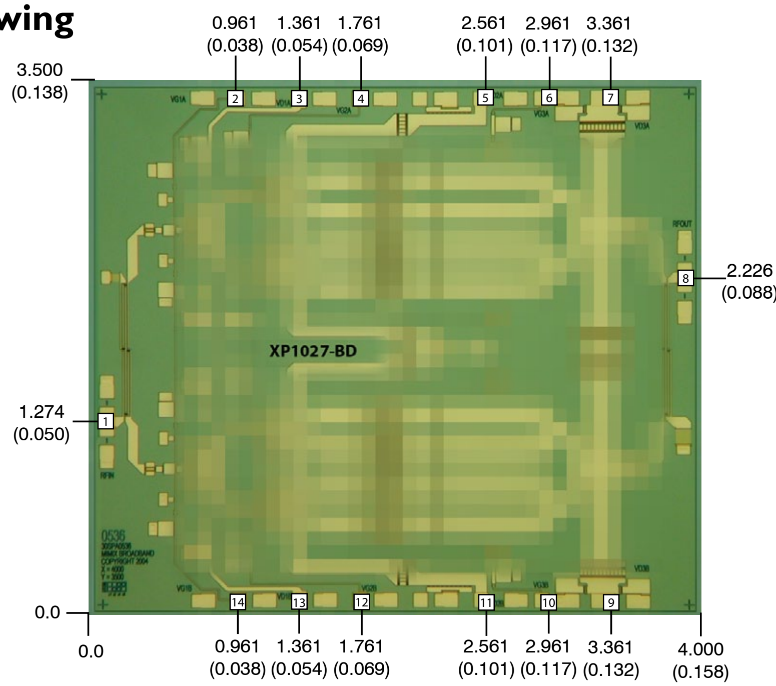
S-Parameters (On-Wafer[1])

Typcial S-Parameter Data for XP1027-BD
Vd=5.0 V, Id=1817 mA

Frequency (GHz)	S11 (Mag)	S11 (Ang)	S21 (Mag)	S21 (Ang)	S12 (Mag)	S12 (Ang)	S22 (Mag)	S22 (Ang)
20.0	0.095	-161.19	0.018	141.50	0.0014	24.88	0.028	33.51
21.0	0.094	-176.82	0.030	145.61	0.0010	17.35	0.040	-2.58
22.0	0.081	167.19	0.053	145.02	0.0016	21.04	0.063	-39.25
23.0	0.056	150.22	0.133	149.82	0.0026	1.17	0.085	-71.83
24.0	0.021	156.80	0.609	127.34	0.0024	-30.49	0.077	-103.77
25.0	0.034	-112.97	2.829	60.25	0.0025	-64.53	0.041	-158.29
26.0	0.075	-132.74	8.859	-42.86	0.0025	-101.60	0.056	-35.72
27.0	0.063	-172.62	13.061	-157.41	0.0020	-133.14	0.115	-81.64
28.0	0.033	-154.36	12.733	107.23	0.0011	-154.87	0.115	-101.71
29.0	0.037	-96.19	11.810	25.72	0.0023	-162.26	0.104	-112.08
30.0	0.045	-117.39	11.733	-52.07	0.0029	161.25	0.075	-109.13
31.0	0.080	-80.63	11.822	-136.80	0.0022	89.92	0.118	-95.89
32.0	0.102	-90.30	9.329	125.72	0.0011	21.55	0.169	-115.52
33.0	0.144	-99.69	5.029	35.62	0.0003	165.09	0.150	-140.18
34.0	0.186	-116.62	2.256	-35.68	0.0007	11.33	0.070	-154.59
35.0	0.172	-135.02	1.078	-91.79	0.0006	-10.99	0.022	-60.02
36.0	0.132	-147.33	0.569	-143.33	0.0003	151.55	0.100	-66.42
37.0	0.093	-137.42	0.314	168.21	0.0008	161.82	0.194	-78.20
38.0	0.082	-98.95	0.177	122.89	0.0013	29.32	0.249	-89.91
39.0	0.125	-83.78	0.106	81.94	0.0006	-45.43	0.278	-105.81
40.0	0.213	-91.17	0.070	41.66	0.0009	41.42	0.244	-124.19

Note [1] S-Parameters – On-Wafer S-Parameters have been taken using reduced bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge.

Mechanical Drawing

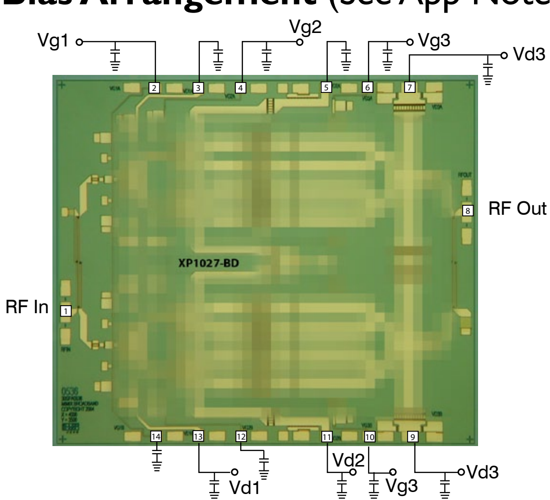


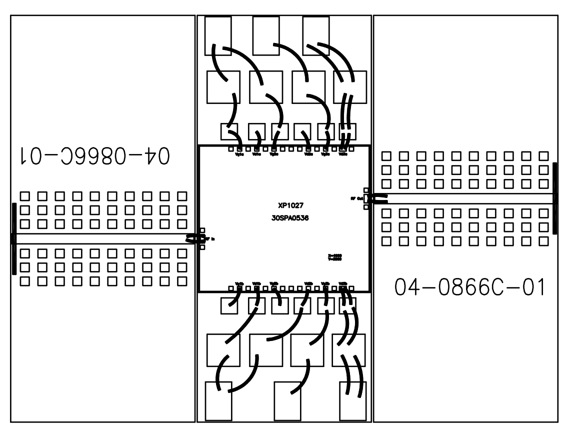
(Note: Engineering designator is 30SPA0536)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
Most DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF and Vd3 Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 8.68 mg.

Bond Pad #1 (RF In)	Bond Pad #5 (Vd2A)	Bond Pad #9 (Vd3B)	Bond Pad #13 (Vd1B)
Bond Pad #2 (Vg1A)	Bond Pad #6 (Vg3A)	Bond Pad #10 (Vg3B)	Bond Pad #14 (Vg1B)
Bond Pad #3 (Vd1A)	Bond Pad #7 (Vd3A)	Bond Pad #11 Vd2B)	
Bond Pad #4 (Vg2A)	Bond Pad #8 (RF Out)	Bond Pad #12 (Vg2B)	

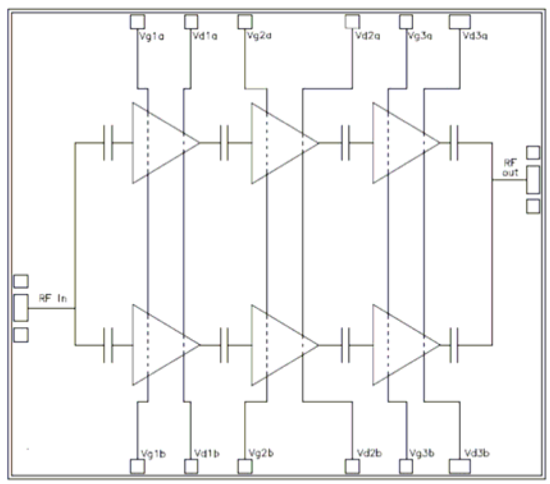
Bias Arrangement (See App Notes [1], [2] and [3])





Layout for reference only – It is recommended to bias output stage from both sides.

App Note [1] Biasing - It is recommended to separately bias each amplifier stage Vd1 through Vd3 at Vd(1,2,3)=5.5V with Id1=250mA, Id2=625mA and Id3=1185mA. Separate biasing is recommended if the amplifier is to be used in a linear application or at high levels of saturation, where gate rectification will alter the effective gate control voltage. For non-critical applications it is possible to parallel all stages and adjust the common gate voltage for a total drain current Id(total)=2060mA.



[Linear Applications] - For applications where the amplifier is being used in linear operation, where best IM3 (Third-Order Intermod) performance is required at more than 5dB below P1dB, it is also recommended to use active gate biasing to keep the drain currents constant as the RF power and temperature vary; this gives the best performance and most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate voltage of the pHEMT is controlled to maintain correct drain current compensating for changes over temperature.

[Saturated Applications] - For applications where the amplifier RF output power is saturated, the optimum drain current will vary with RF drive and each amplifier stage is best operated at a constant gate voltage. Significant gate currents will flow at saturation and bias circuitry must allow for drain current growth under this condition to achieve best RF output power and power added efficiency. Additionally, if the input RF power level will vary significantly, a more negative gate voltage will result in less die heating at lower RF input drive levels where the absence of RF cooling becomes significant. Note under this bias condition, gain will then vary with RF drive

NOTE! - For any application it is highly recommended to bias the output amplifier stage from both sides for best RF and thermal performance.

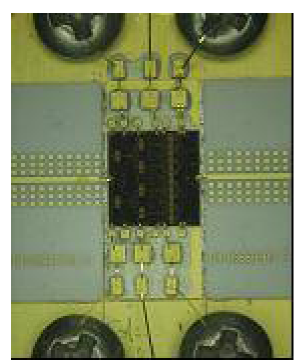
CAUTION! - Also, make sure to properly sequence the applied voltages to ensure negative gate bias (Vg1,2,3) is available before applying the positive drain supply (Vd1,2,3). Additionally, it is recommended that the device gates are protected with Silicon diodes to limit the applied voltage.

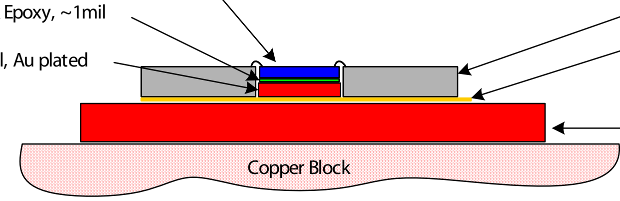
App Note [2] Bias Arrangement
[For Individual Stage Bias] (recommended for linear/saturated applications) - Each DC pad (Vd1,2,3 and Vg1,2,3) needs to have DC bypass capacitance (100-200 pF) as close to the device as possible. Additional DC bypass capacitance (1 nF and 3.3 uF) is also recommended. All DC pads have been tied together on chip and device can be biased from either side.

[For Parallel Stage Bias] (general applications) - The same as Individual Stage Bias but all the drain or gate pad DC bypass capacitors (100-200 pF) are tied together at one point after bypass capacitance. Additional DC bypass capacitance (1 nF and 3.3 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads. All DC pads have been tied together on chip and can be biased from either side.

NOTE! In either arrangement, for most stable performance all unused DC pads must also be bypassed with at least 100-200 pf capacitance.

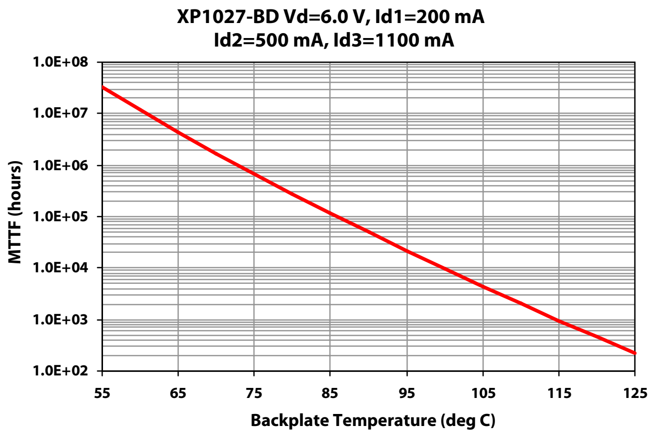
App Note [3] Material Stack-Up – In addition to the practical aspects of bias and bias arrangement, device base material stack-up also must be considered for best thermal performance. A well thought out thermal path solution will improve overall device reliability, RF performance and power added efficiency. The photo shows a typical high power amplifier carrier assembly. The material stack-up for this carrier is shown below. This stack-up is highly recommended for most reliable performance however, other materials (i.e. eutectic solder vs epoxy, copper tungsten/copper moly rib, etc.) can be considered/possibly used but only after careful review of material thermal properties, material availability and end application performance requirements.

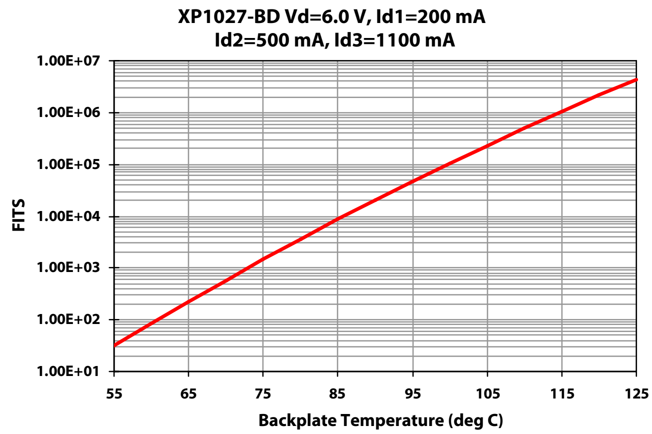


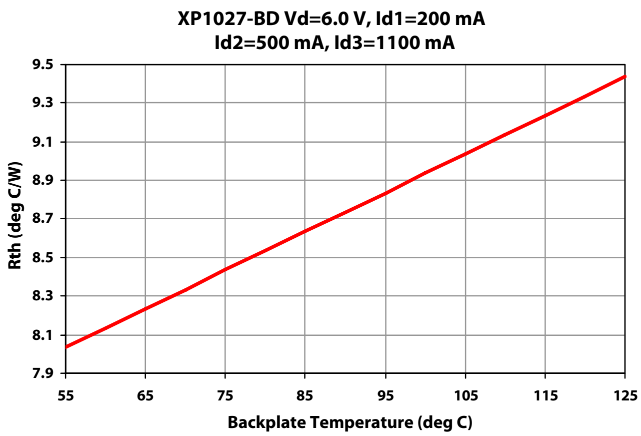


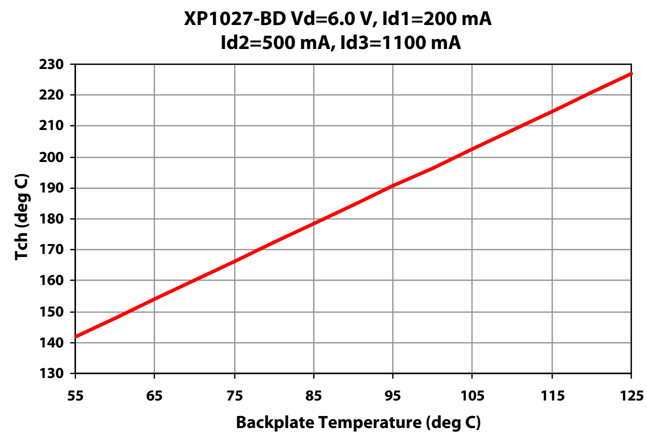
MTTF Graphs

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at Mimix Broadband. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of die placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.









Handling and Assembly Information

CAUTION! - Mimix Broadband MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- *Do not ingest.*
- *Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.*
- *Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.*

Life Support Policy - Mimix Broadband's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of Mimix Broadband. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from Mimix Broadband are 0.100 mm (0.004") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxy is Die Mat DM6030HK or an epoxy with >52 W/m ºK thermal conductivity cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the Mimix "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001[2] thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280 ºC (Note: Gold Germanium should be avoided). The work station temperature should be 310 ºC +/- 10 ºC. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Ordering Information

Part Number for Ordering	Description
XP1027-BD-000V	RoHS compliant die packed in vacuum release gel packs
XP1027-BD-EV1	XP1027-BD evaluation module

Caution: ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling this device.