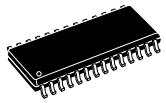
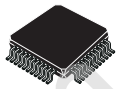
STA015
STA015B STA015T

MPEG 2.5 LAYER III AUDIO DECODER WITH ADPCM CAPABILITY

- SINGLE CHIP MPEG2 LAYER 3 DECODER SUPPORTING:
  - All features specified for Layer III in ISO/IEC 11172-3 (MPEG 1 Audio)
  - All features specified for Layer III in ISO/IEC 13818-3.2 (MPEG 2 Audio)
  - Lower sampling frequencies syntax extension, (not specified by ISO) called MPEG 2.5
- DECODES LAYER III STEREO CHANNELS, DUAL CHANNEL, SINGLE CHANNEL (MONO)
- SUPPORTING ALL THE MPEG 1 & 2 SAMPLING FREQUENCIES AND THE EXTENSION TO MPEG 2.5: 48, 44.1, 32, 24, 22.05, 16, 12, 11. 025, 8 KHz
- ACCEPTS MPEG 2.5 LAYER III ELEMENTARY COMPRESSED BITSTREAM WITH DATA RATE FROM 8 Kbit/s UP TO 320 Kbit/s
- ADPCM CODEC CAPABILITIES:
  - sample frequency from 8 kHz to 32 kHz
  - sample size from 8 bits to 32 bits
  - encoding algorithm: DVI, ITU-G726 pack (G723-24, G721,G723-40)
  - Tone control and fast-forward capability
- EASY PROGRAMMABLE GPSO INTERFACE FOR ENCODED DATA UP TO 5Mbit/s (TQFP44 & LFBGA 64)
- DIGITAL VOLUME CONTROL
- DIGITAL BASS & TREBLE CONTROL
- BYPASS MODE FOR EXTERNAL AUDIO SOURCE
- SERIAL BITSTREAM INPUT INTERFACE
- EASY PROGRAMMABLE ADC INPUT INTERFACE
- ANCILLARY DATA EXTRACTION VIA I^2C INTERFACE.
- SERIAL PCM OUTPUT INTERFACE (I^2S AND OTHER FORMATS)
- PLL FOR INTERNAL CLOCK AND FOR OUTPUT PCM CLOCK GENERATION
- CRC CHECK AND SYNCHRONISATION ERROR DETECTION WITH SOFTWARE INDICATORS
- I^2C CONTROL BUS
- LOW POWER 2.4V CMOS TECHNOLOGY
- WIDE RANGE OF EXTERNAL CRYSTALS FREQUENCIES SUPPORTED



SO28



TQFP44

LFBGA64

ORDERING NUMBER: STA015$ (SO28)
STA015T$ (TQFP44)
STA015B$ (LFBGA 8x8)

APPLICATIONS

- PC SOUND CARDS
- MULTIMEDIA PLAYERS
- VOICE RECORDERS

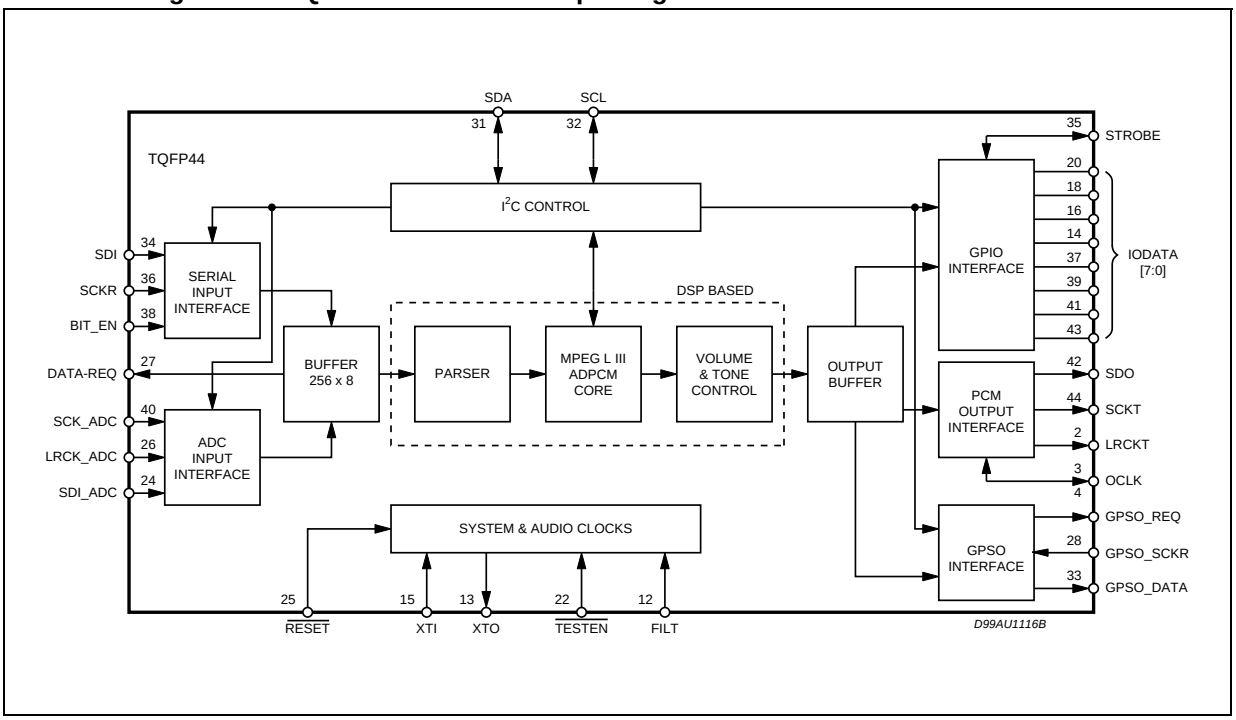
DESCRIPTION

The STA015 is a fully integrated high flexibility MPEG Layer III Audio Decoder, capable of decoding Layer III compressed elementary streams, as specified in MPEG 1 and MPEG 2 ISO standards. The device decodes also elementary streams compressed by using low sampling rates, as specified by MPEG 2.5. STA015 receives the input data through a Serial input Interface. The decoded signal is a stereo, mono, or dual channel digital output that can be sent directly to a D/A converter, by the PCM Output Interface.

This interface is software programmable to adapt the STA015 digital output to the most common DACs architectures used on the market. The functional STA015 chip partitioning is described in Fig.1a and Fig.1b.

Figure 1.

1a. Block Diagram for TQFP44 and LFBGA64 package.



1b. BLOCK DIAGRAM for SO28 package

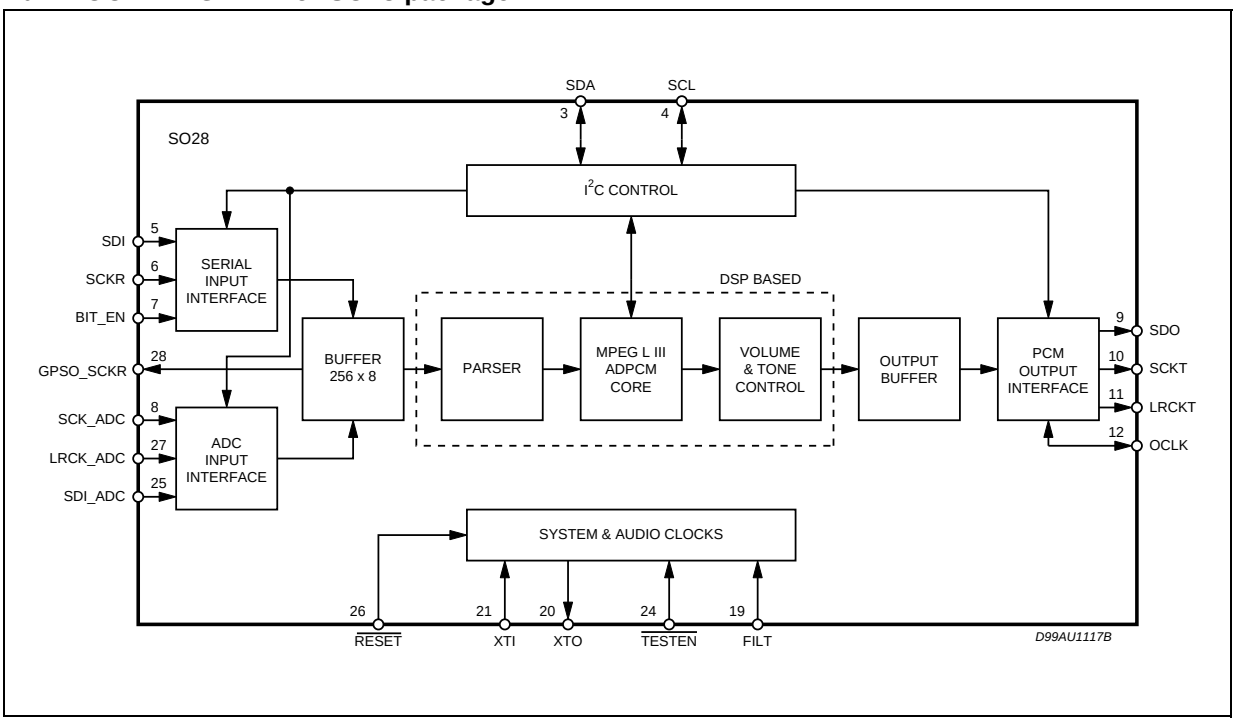
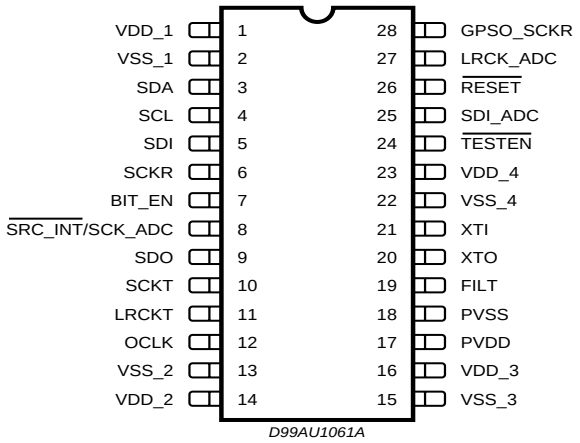
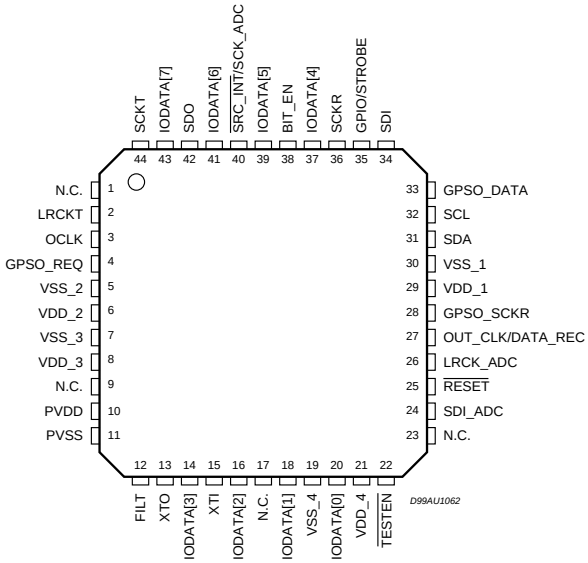
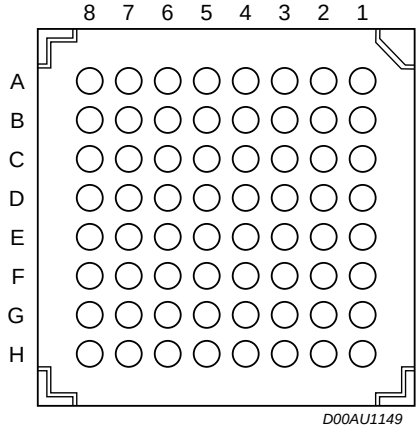


Figure 2. Pin Connection







A1 = SDI
B2 = SCKR
D4 = BIT_EN
D1 = SRC_INT
E2 = SDO
F2 = SCKT
H1 = LRCKT
H3 = OCLK
F3 = VSS_2
E4 = VDD_2
G4 = VSS_3
G5 = VDD_3
F5 = PVDD
G6 = PVSS
G7 = FILT
G8 = XTO
F7 = XTI
E7 = VSS_4
C8 = VDD_4
D7 = TESTEN
A7 = SDI_ADC
B6 = RESET
A5 = LRCK_ADC
C5 = OUT_CLK/DATA_REQ
B5 = VDD_1
B4 = VSS_1
A4 = SDA
B3 = SCL
C2 = GPIO_STROBE
C3 = IODATA [4]
E3 = IODATA [5]
D2 = IODATA [6]
F1 = IODATA [7]
G3 = GPSO_REQ
F8 = IODATA [3]
F6 = IODATA [2]
E6 = IODATA [1]
C7 = IODATA [0]
C6 = GPSO_SCKR
A2 = GPSO_DATA

LFBGA64

1.0 OVERVIEW

1.1 MP3 decoder engine

The MP3 decoder engine is able to decode any Layer III compliant bitstream: MPEG1, MPEG2 and MPEG2.5 streams are supported. Besides audio data decoding the MP3 engine also performs ANCILLARY data extraction: these data can be retrieved via I^2C bus by the application microcontroller in order to implement specific functions.

Decoded audio data goes through a software volume control and a two-band equalizer blocks before feeding the output I2S interface. This results in no need for an external audio processor.

MP3 bitstream is sent to the decoder using a simple serial input interface (see pins SDI, SCKR, BIT_EN and DATA_REQ), supporting input rate up to 20 Mbit/s. Received data are stored in a 256 bytes long input buffer which provides a feedback line (see DATA_REQ pin) to the bitstream source (tipically an MCU).

1.2 ADPCM encoder/decoder engine

This device also embeds a multistandard ADPCM encoder/decoder supporting different sample rates (from 8 KHz up to 32 KHz) and different sample sizes (from 8 bit to 32 bits).

During encoding process two different interfaces can be used to feed data: the serial input interface (same interface used also to feed MP3 bitstream) or the ADC input interface, which provides a seamless connection with an external A/D converter. The currently used interface is selected via I^2C bus.

Also to retrieve encoded data two different interfaces are available: the I^2C bus or the faster GPSO output interface. GPSO interface is able to output data with a bitrate up to 5 Mbit/s and its control pins (GPSO_SCKR, GPSO_DATA and GPSO_REQ) can be configured in order to easily fit the target application.

1.3 BYPASS functional mode

In order to allow using the device to post-process auxiliary audio sources a special BYPASS mode is available. When the device is configured in BYPASS mode the embedded DSP will process digital audio data coming through the ADC input interface and will output the resulting data to the external DAC.

Available processings include volume and a tone ontrols.

THERMAL DATA

Symbol	Parameter	Value	Unit
Rth j-amb	Thermal resistance Junction to Ambient	85	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	-0.3 to 4	V
Vi	Voltage on Input pins	-0.3 to V_{DD} +0.3	V
V_O	Voltage on output pins	-0.3 to V_{DD} +0.3	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_{oper}	Operative ambient temp	-20 to +85	°C

PIN DESCRIPTION

SO28	TQFP44	LFBGA64	Pin Name	Type	Function	PAD Description
1	29	B5	VDD_1		Supply Voltage	
2	30	B4	VSS_1		Ground	
3	31	A4	SDA	I/O	i^2C Serial Data + Acknowledge	CMOS Input Pad Buffer CMOS 4mA Output Drive
4	32	B3	SCL	I	I^2C Serial Clock	CMOS Input Pad Buffer
5	34	A1	SDI	I	Receiver Serial Data	CMOS Input Pad Buffer
6	36	B2	SCKR	I	Receiver Serial Clock	CMOS Input Pad Buffer
7	38	D4	BIT_EN	I	Bit Enable	CMOS Input Pad Buffer with pull up
8	40	D1	$\overline{\text{SRC\_INT}}$/ $\overline{\text{SCK\_ADC}}$	I	Interrupt Line/ADC Serial Clock	CMOS Input Pad Buffer
9	42	E2	SDO	O	Transmitter Serial Data (PCM Data)	CMOS 4mA Output Drive
10	44	F2	SCKT	O	Transmitter Serial Clock	CMOS 4mA Output Drive
11	2	H1	LRCKT	O	Transmitter Left/Right Clock	CMOS 4mA Output Drive
12	3	H3	OCLK	I/O	Oversampling Clock for DAC	CMOS Input Pad Buffer CMOS 4mA Output Drive
13	5	F3	VSS_2		Ground	
14	6	E4	VDD_2		Supply Voltage	
15	7	G4	VSS_3		Ground	
16	8	G5	VDD_3		Supply Voltage	
17	10	F5	PVDD		PLL Power	
18	11	G6	PVSS		PLL Ground	
19	12	G7	FILT	O	PLL Filter Ext. Capacitor Conn.	
20	13	G8	XTO	O	Crystal Output	CMOS 4mA Output Drive
21	15	F7	XTI	I	Crystal Input (Clock Input)	Specific Level Input Pad (see paragraph 2.1)
22	19	E7	VSS_4		Ground	
23	21	C8	VDD_4		Supply Voltage	
24	22	D7	$\overline{\text{TESTEN}}$	I	Test Enable	CMOS Input Pad Buffer with pull up
25	24	A7	$\overline{\text{SDI\_ADC}}$	I	ADC Data Input	CMOS Input Pad Buffer
26	25	B6	$\overline{\text{RESET}}$	I	System Reset	CMOS Input Pad Buffer with pull up
27	26	A5	LRCK_ADC	I	ADC left/Right Clock	CMOS Output Pad Buffer
28	27	C5	IN_CLK/ DATA_REQ	O	Buffered Output Clock/ Data Request Signal	CMOS 4mA Output Drive
	20	C7	IODATA[0]	I/O	GPIO Data Line	CMOS 4mA Schmitt Trigger Bidir Pad Buffer
	18	E6	IODATA[1]	I/O	GPIO Data Line	
	16	F6	IODATA[2]	I/O	GPIO Data Line	
	14	F8	IODATA[3]	I/O	GPIO Data Line	
	37	C3	IODATA[4]	I/O	GPIO Data Line	
	39	E3	IODATA[5]	I/O	GPIO Data Line	
	41	D2	IODATA[6]	I/O	GPIO Data Line	
	43	F1	IODATA[7]	I/O	GPIO Data Line	
	35	C2	GPIO_STROBE	I/O	GPIO Strobe Signal	
	4	G3	GPSO_REQ	O	GPSO Request Signal	CMOS Output Pad Buffer
	28	C6	GPSO_SCKR	I	GPSO Serial Clock	CMOS Input Pad Buffer
	33	A2	GPSO_DATA	O	GPSO Serial Data	CMOS Output Pad Buffer

Note: In functional mode $\overline{\text{TESTEN}}$ must be connected to VDD,

ELECTRICAL CHARACTERISTICS: V_{DD} = 3.3V ±0.3V; Tamb = 0 to 70°C; Rg = 50Ω unless otherwise specified

DC OPERATING CONDITIONS

Symbol	Parameter	Value
V_{DD}	Power Supply Voltage	2.4 to 3.6V
T_j	Operating Junction Temperature	-20 to 125°C

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{IL}	Low Level Input Current Without pull-up device	Vi = 0V	-10		10	µA	1
I_{IH}	High Level Input Current Without pull-up device	Vi = V_{DD}	-10		10	µA	1
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	2

Notes: 1. The leakage currents are generally very small, < 1nA. The value given here is a maximum that can occur after an electrostatic stress on the pin.
2. Human Body Model.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{IL}	Low Level Input Voltage				0.2*V_{DD}	V	
V_{IH}	High Level Input Voltage		0.8*V_{DD}			V	
V_{ol}	Low Level Output Voltage	I_{ol} = Xma			0.4V	V	1, 2
V_{oh}	High Level Output Voltage		0.85*V_{DD}			V	1, 2

Notes: 1. Takes into account 200mV voltage drop in both supply lines.
2. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{pu}	Pull-up current	Vi = 0V; pin numbers 7, 24 and 26;	-25	-66	-125	µA	1
R_{pu}	Equivalent Pull-up Resistance			50		kΩ	

Notes: 1. Min. condition: V_{DD} = 2.7V, 125°C Min process
Max. condition: V_{DD} = 3.6V, -20°C Max.

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ	Max	Unit	Note
P_D	Power Dissipation @ V_{DD} = 2.4V	Sampling_freq ≤24 kHz		76		mW	
		Sampling_freq ≤32 kHz		79		mW	
		Sampling_freq ≤48 kHz		85		mW	

Figure 3. Test Circuit

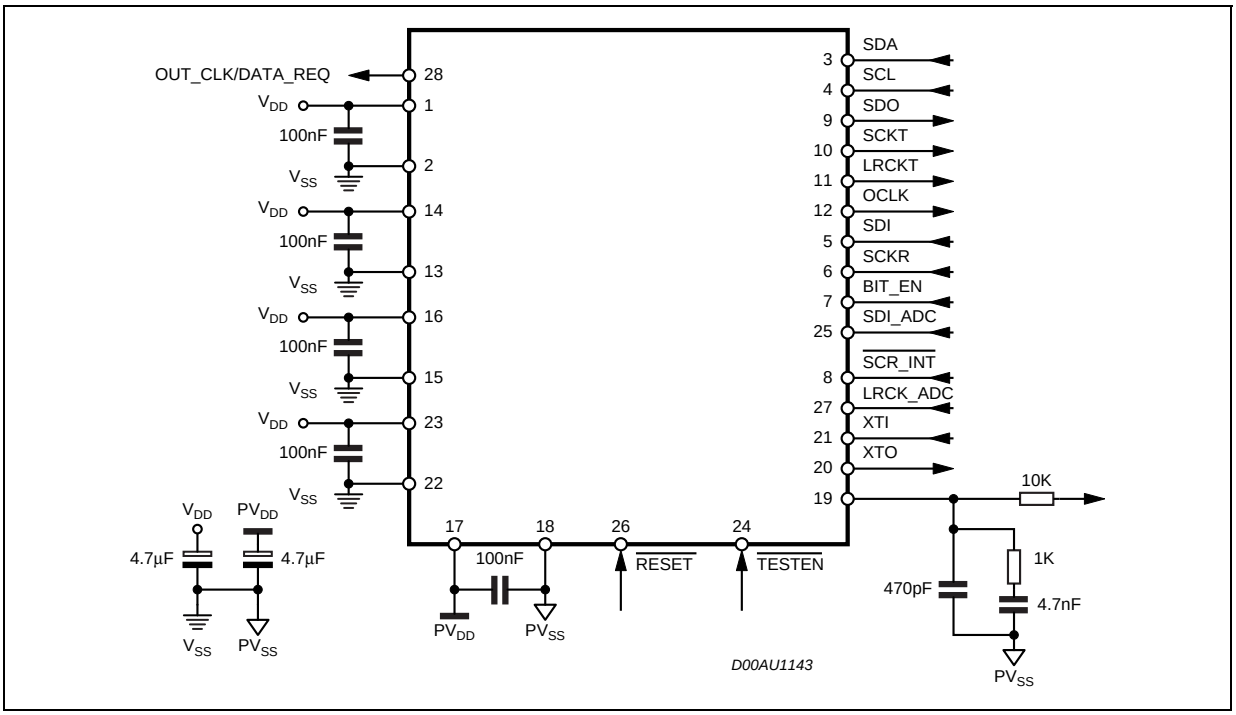
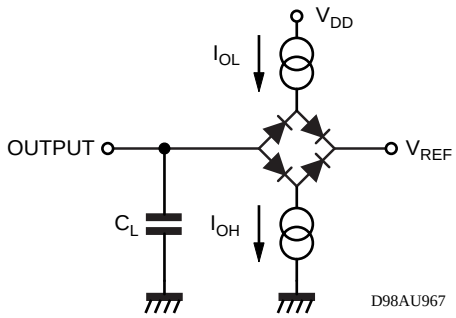


Figure 4. Test Load Circuit



Test Load

Output	I_{OL}	I_{OH}	C_L	V_{REF}
SDA	1mA		100pF	3.6V
Other Outputs	100µA	100µA	100pF	1.5V

2.0 FUNCTIONAL DESCRIPTION

2.1 Clock Signal

The STA015 input clock is derivated from an external source or from a industry standard crystal oscillator, generating input frequencies of 10, 14.31818 or 14.7456 MHz.

Other frequencies may be supported upon request to STMicroelectronics. Each frequency is supported by downloading a specific configuration file, provided by STM XTI is an input Pad with specific levels.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				V_{DD}-1.8	V
V_{IH}	High Level Input Voltage		V_{DD}-0.8			V

CMOS compatibility

The XTI pad low and high levels are CMOS compatible; XTI pad noise margin is better than typical CMOS pads.

TTL compatibility

The XTI pad low level is compatible with TTL while the high level is not compatible (for example if V_{DD} = 3V TTL min high level = 2.0V while XTI min high level = 2.2V)

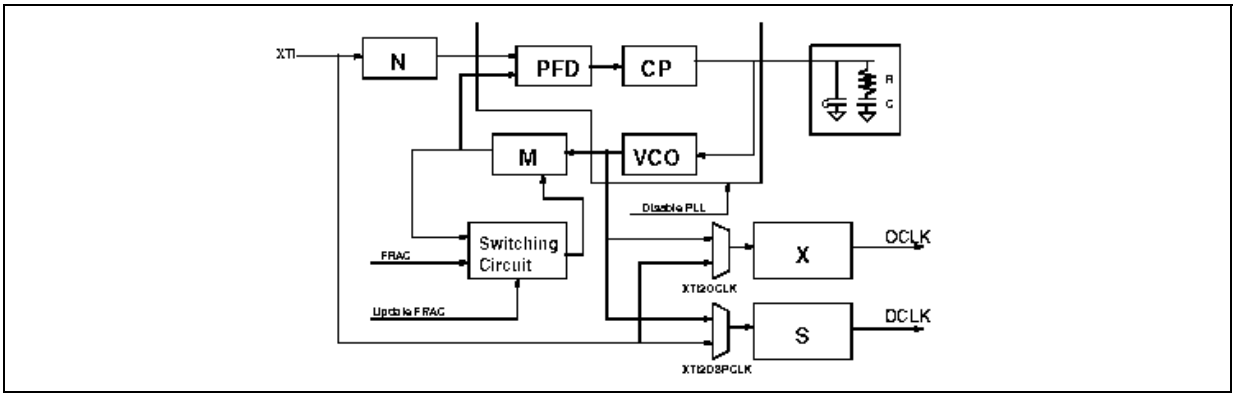
2.2 PLL & Clock Generator System

When STA015 receives the input clock, as described in Section 2.1, and a valid layer III input bit stream, the internal PLL locks, providing to the DSP Core the master clock (DCLK), and to the Audio Output Interface the nominal frequencies of the incoming compressed bit stream. The STA015 PLL block diagram is described in Figure 5.

The audio sample rates are obtained dividing the oversampling clock (OCLK) by software programmable factors. The operation is done by STA015 embedded software and it is transparent to the user.

The STA015 PLL can drive directly most of the ommercial DACs families, providing an over sampling clock, OCLK, obtained dividing the VCO frequency with a software programmable dividers.

Figure 5. PLL and Clocks Generation System



2.3 STA015 Operational Modes

The device can be configured in 4 different operational modes. To select one specific mode a dedicated CHIP_MODE registers is available. For proper operation the following steps must be issued to switch between different modes:

– issue a software reset (SOFT_RESET register)

– select the desired mode (CHIP_MODE register)

– run the device (RUN register)

Hereby is a short description of each available mode

- **ADPCM Encoder**
  This mode can be used to encode the incoming bitstream with 4 different compression algorithms. Moreover different sample frequencies and word size are supported. For a detailed escription of this features refer to the related registers.
- **ADPCM Decoder**
  This mode can be used when an ADPCM compressed bitstream must be decoded. The input interface handling and control flow is the same as in the MP3 Mode.
- **BYPASS mode**
  Using this mode it's possible to use the embedded post-processing controls (volume and tone controls) to process an incoming uncompressed stereo audio stream. In this configuration ADC input is the only

supported interface. This could be useful, for instance, to process audio data coming from an external tuner or some other auxiliary source.

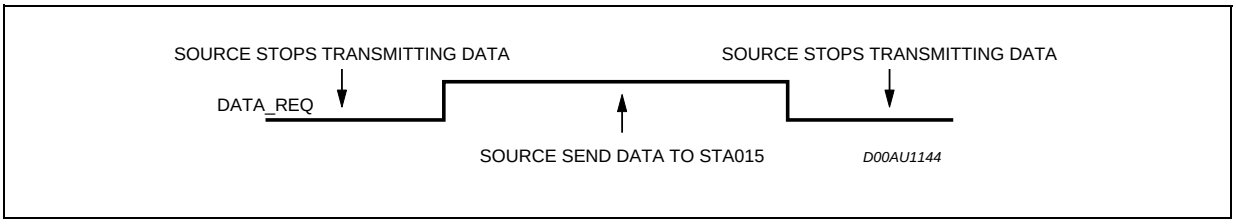
- **MP3 mode**
  In MP3 Mode (default mode) STA015 decodes the incoming bitstream, acting as a master of the data communication from the source to itself. This control is done by a specific buffer management, controlled by STA015 embedded oftware.
  The data coming from the serial interface are stored in the input buffer, a 256 bytes long FIFO.
  The feedback line DATA_REQ actually is the result of the h/w comparison between the writing address of the FIFO and the constant value 252. This means that if the buffer is filled up with more than 252 bytes the DATA_REQ line goes low, requesting MCU to stop transmission: the maximum time to stop transmitting is given by the time required to transmit 4 bytes (this time, in turn, depends on the bitstream speed used to send MP3 data).
  The input interface can receive data with a speed up to 20Mbit/s. The speed at which the FIFO is emptied is equal to the MP3 nominal bitrate. Provided the FIFO is filled up with 252 bytes the time required to empty it (in worst condition, which is 320kbit/s mpeg stream) is about 6ms. So if no more data is received in this time the buffer will be emptied and this will badly affect the output audio.

In this mode the fractional part of the PLL is disabled and the audio clocks are generated at nominal rates. Fig. 6 describes the default DATA_REQ signal behaviour. Programming STA015 it is possible to invert the polarity of the DATA_REQ line (register REQ_POL).

In order to allow proper operation of the device in broadcast applications a special BRAODCAST MP3 decoding mode is available. When configured in BROADCAST mode the device will operate as a slave decoder and no more feedback will be generated to the data source.

The output PCM clock will be automatically adjusted by the embedded DSP in order to follow the incoming bitstream rate and to avoid input buffer underrun/overrun. A special configuration file must be used to enable this operational mode: the file must be downloaded via I^2C link after device power-on. Please contact your local ST branch to have more information about.

Figure 6. DATA_REQ control line



2.4 STA015 Decoding States

There are three different decoder states: **Idle, Init,** and **Decode**. Commands to change the decoding states are described in the STA015 I^2C registers description.

Idle Mode

IIn this mode (entered after a S/W or H/W reset) the decoder is waiting for the RUN command. This mode should be used to initialize the configuration registers of the device. The DAC connected to STA015 can be initialized during this mode (set MUTE to 1).

MUTE to 1).

PLAY	MUTE	Clock State	PCM Output
X	0	Not Running	0
X	1	Running	0

Init Mode

"PLAY" and "MUTE" changes are ignored in this mode. The internal state of the decoder will be updated only when the decoder changes from the state "init" to the state "decode". The "init" phase ends when the first decoded samples are at the output stage of the device.

Decode Mode

This mode is completely described by the following table:

PLAY	MUTE	Clock State	PCM Output	Decoding
0	0	Not Running	0	No
0	1	Running	0	No
1	0	Running	Decoded Samples	Yes
1	1	Running	0	Yes

Figure 7. MPEG Decoder Interface

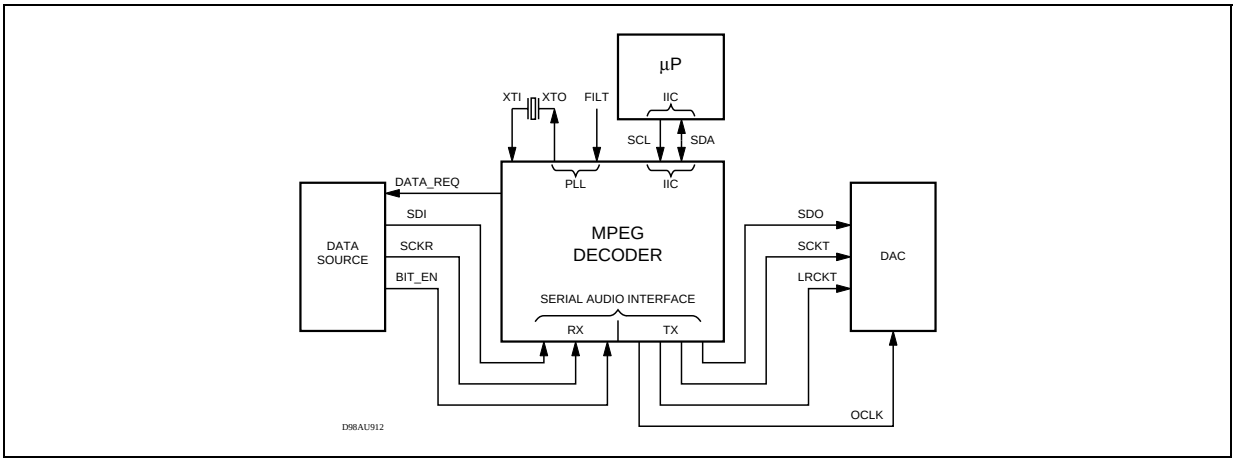
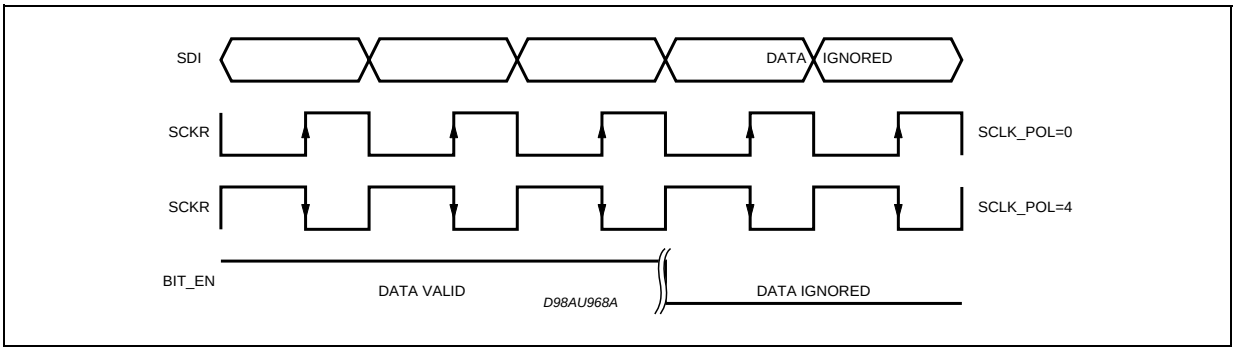


Figure 8. Serial Input Interface Clocks



3.0 INTERFACE DESCRIPTION

3.1 Serial Input Interface

STA015 receives the input data (MSB first) through the Serial Input Interface (Fig.7). It is a serial communication interface connected to the SDI (Serial Data Input) and SCKR (Receiver Serial Clock).

The interface can be configured to receive data sampled on both rising and falling edge of the SCKR clock. The BIT_EN pin, when set to low, forces the bitstream input interface to ignore the incoming data. For

proper operation BIT_EN line should be toggled only when SCKR is stable low (for both SCLK_POL configuration). The possible configurations are described in Fig. 8.

3.2 GPSO Output Interface

In order to retrieve ADPCM encoded data a General Purpose Serial Output interface is available (in TQFP44 and LFBGA64 packages only). The maximum frequency for GPSO_SCKR clock is the DSP system clock frequency divided by 3 (i.e. 8.192 MHz @ 24.58MHz). The interface is based on a simple and configurable 3-lines protocol, as described by figure 10.

3.3 PCM Output Interface

The decoded audio data are output in serial PCM format. The interface consists of the following signals:

SDO PCM Serial Data Output

SCKT PCM Serial Clock Output

LRCLK Left/Right Channel Selection Clock

The output samples precision is selectable from 16 to 24 bits/word, by setting the output precision with PCMCONF (16, 18, 20 and 24 bits mode) register. Data can be output either with the most significant bit first (MS) or least significant bit first LS), selected by writing into a flag of the PCMCONF register.

Figure 9 gives a description of the several STA015 PCM Output Formats. The sample rates set decoded by STA015 is described in Table 1.

To enable the GPSO interface bit GEN of GPSO_ENABLE register must be set. Using the GPSO_CONF register the protocol can be configured in order to provide outcoming data on rising/ falling edge of GPSO_SCKR input clock; the GPSO_REQ request signal polarity (usually connected to an MCU interrupt line) can be configured as well.

Figure 9. PCM Output Formats

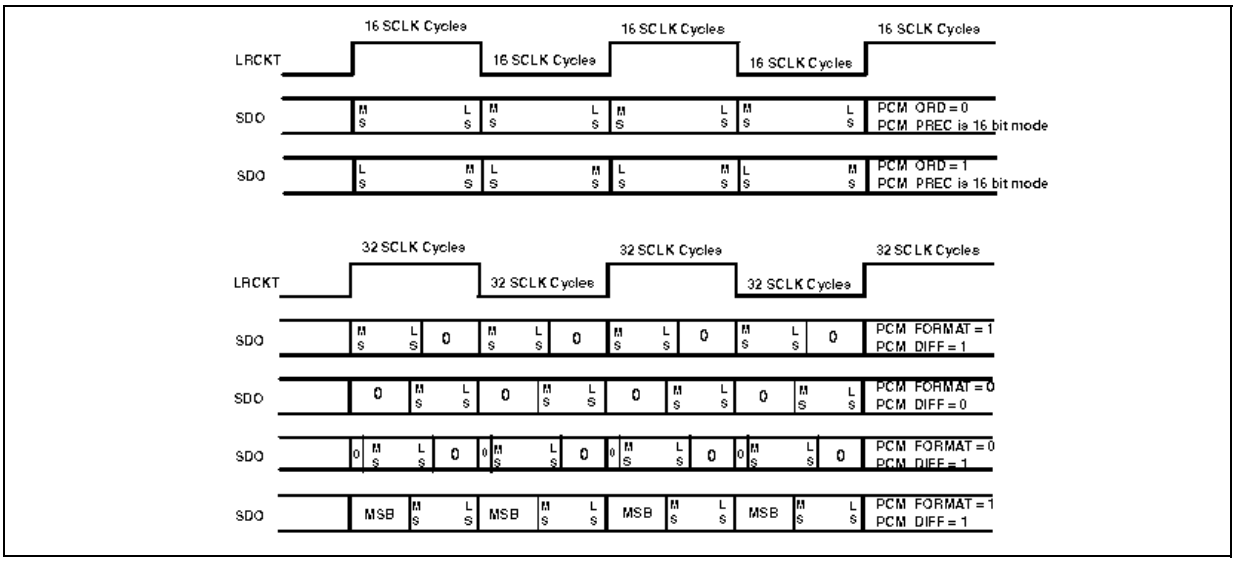


Table 1. MPEG Sampling Rates (KHz)

MPEG 1	MPEG 2	MPEG 2.5
48	24	12
44.1	22.05	11.025
32	16	8

3.4 ADC Inteface

Beside the serial input interface based on SDI and SCKR lines a 3 wire flexible and user configurable input interface is also available, suitable to interface with most A/D converters. To configure this interface 4 specific I^2C registers are available (ADC_ENABLE, ADC_CONF, ADC_WLEN and ADC_WPOS). Refer to registers description for more details.

3.5 General Purpose I/O Interface

A new general purpose I/O interface has been added to this device (TQFP44 and LFBGA64 only). Actually only the strobe line is used in ADPCM encoding mode to provide an interrupt; other pins are reserved for future use. The related configuration register is GPIO_CONF. See the following summary for related pin usage:

Name	Description	Dir
I/ODATA [0] ..... I/ODATA [7]	GPIO data line	I/O ..... I/O
GPIO_STROBE	GPIO strobe line	I/O

4.0 ADPCM ENCODING: OVERVIEW

According to the previously described interfaces there are 4 ways to manage ADPCM data stream while encoding. Input interface can be either the serial receiver block (SDI + SCKR + DATA_REQ lines) or the ADC specific interface.

Output interfaces can be either the I2C bus (with or without interrupt line) or the GPSO high-speed serial interface (GPSO_REQ + GPSO_ DATA + GPSO_SCKR lines). This result in the following 4 methods to handle encoding flow:

INPUT (data to encode)	Output (encoded data)	Available on package
ADC I/F (SDI_ADC + LRCK_ADC + SCK_ADC)	GPSO I/F (GPSO_REQ + GPSO_DATA + GPSO_SCKR)	TQFP44/LFBGA64
ADC I/F (SDI_ADC + LRCK_ADC + SCK_ADC)	I^2C + Interrupt (SCL + SDA +DATA_REQ)	SO28/TQFP44 LFBGA64
SERIAL I/F (SCKR + SDI + DATA_REQ)	GPSO I/F (GPSO_REQ + GPSO_DATA + GPSO_SCKR)	TQFP44/LFBGA64
SERIAL I/F (SCKR + SDI + DATA_REQ) (*)	I^2C (polling) (SCL + SDA)	SO28/TQFP44 LFBGA64

(*) STA013 Compatible mode

Figure 10.

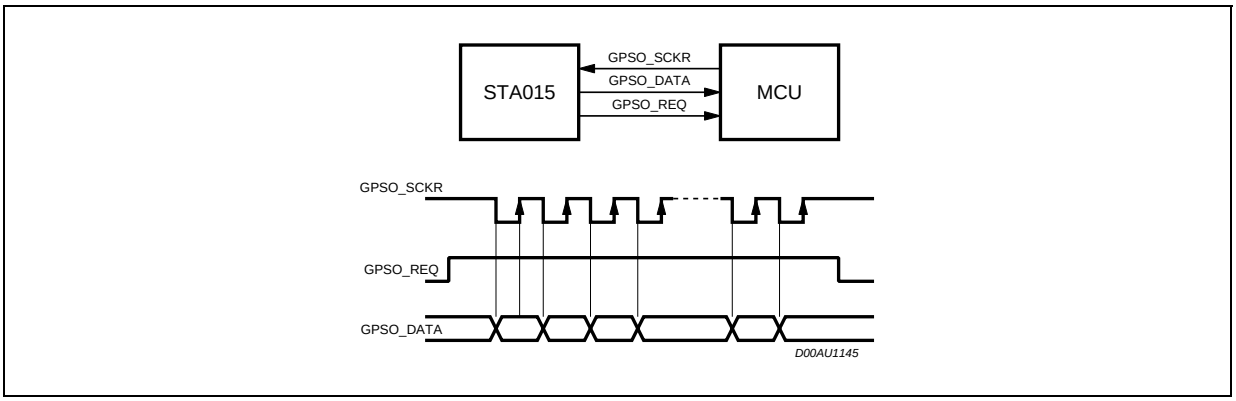
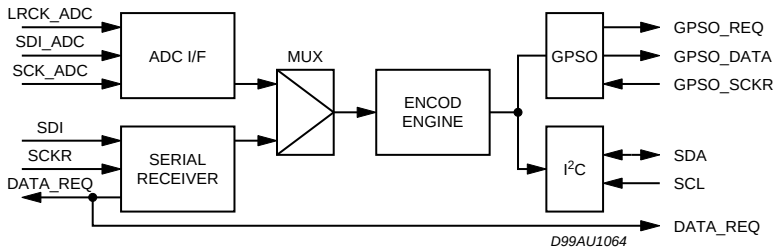
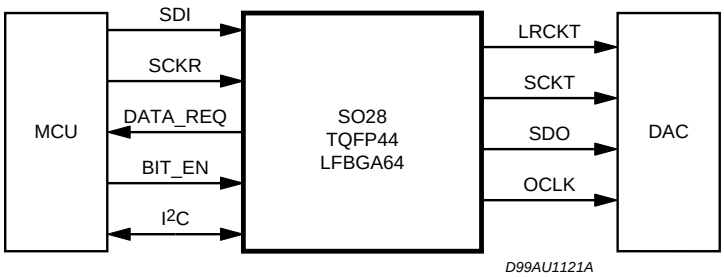


Figure 11.



The following 4 figures (fig. 12, 13, 14, 15) show the available connection diagrams as far as ADPCM encoding function. As shown in the figures some configuration is not available in SO28 package.

Figure 12. Input from BITSTREAM, Output from I^2C



STA013 compatible mode

Figure 13. Input from ADC, Output from I^2C +IRQ

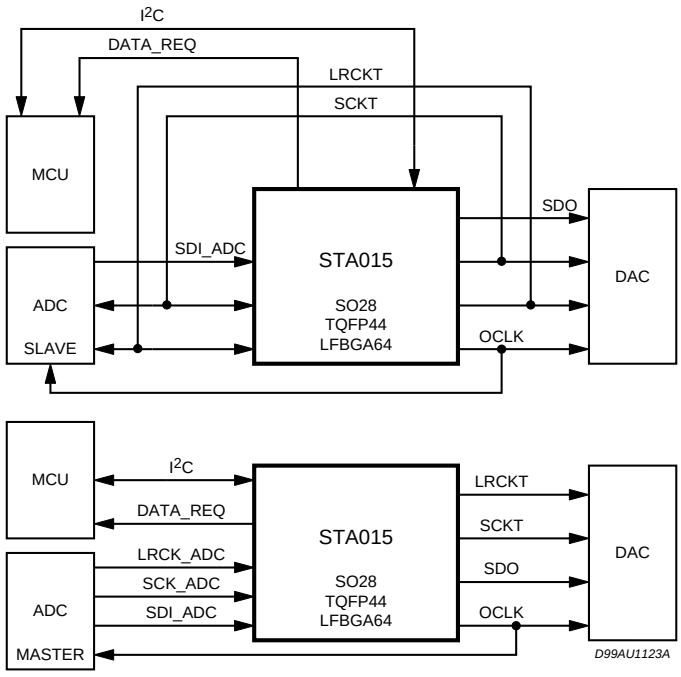


Figure 14. Input from BITSTREAM, Output from GPSO

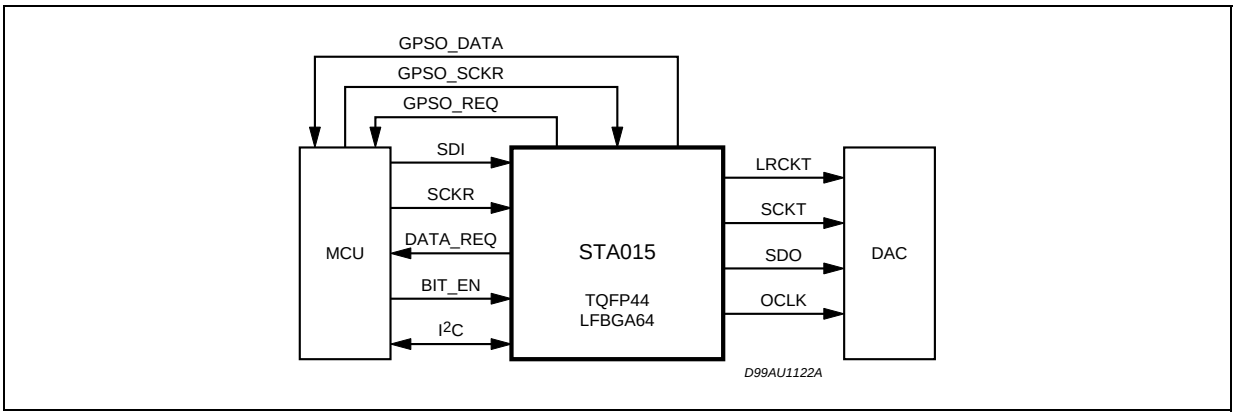
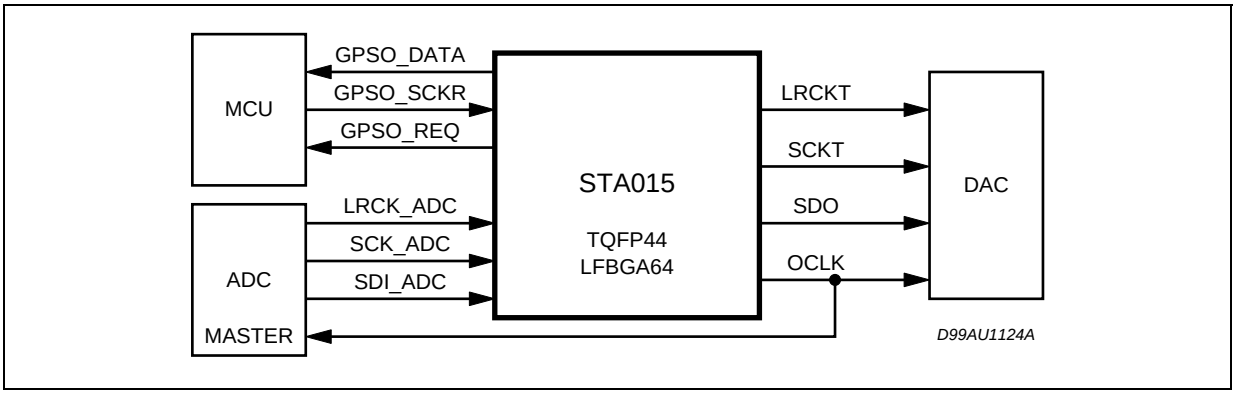


Figure 15. Input from ADC, Output from GPSO



5.0 I²C BUS SPECIFICATION

The STA015 supports the I²C protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the others as the slave. The master always starts the transfer and provides the serial clock for synchronisation. The STA015 is always a slave device in all its communications.

5.1 COMMUNICATION PROTOCOL

3.1.0 - Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high are used to identify START or STOP condition.

5.1.1 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.2 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communications between STA015 and the bus master.

5.1.3 Acknowledge bit

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, releases the SDA bus after sending 8 bit of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of 8 bits of data.

5.1.4 Data input

During the data input the STA015 samples the SDA signal on the rising edge of the clock SCL. For correct device operation the SDA signal has to be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 DEVICE ADDRESSING

To start communication between the master and the STA015, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode. The 7 most significant bits are the device address identifier, corresponding to the I^2C bus definition. For the STA015 these are fixed as 1000011.

The 8th bit (LSB) is the read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA015 identifies on the bus the device address and, if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The following byte after the device identification byte is the internal space address.

5.3 WRITE OPERATION (see fig. 16)

Following a START condition the master sends a device select code with the RW bit set to 0. The STA015 acknowledges this and waits for the byte of internal address.

After receiving the internal bytes address the STA015 again responds with an acknowledge.

5.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by STA015. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multibyte write

The multibyte write mode can start from any internal address. The transfer is terminated by the master generating a STOP condition.

Figure 16. Write Mode Sequence

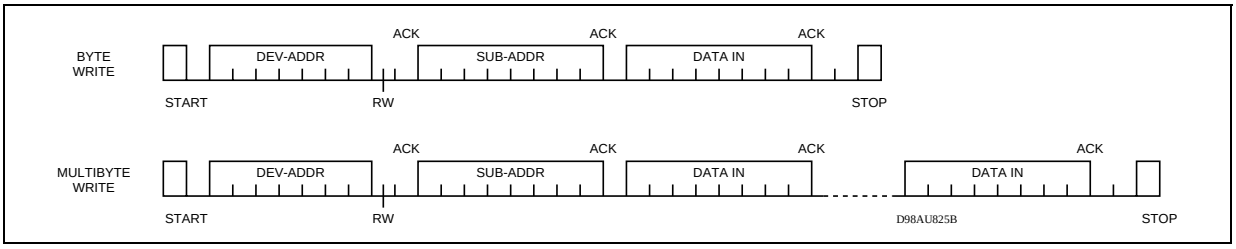
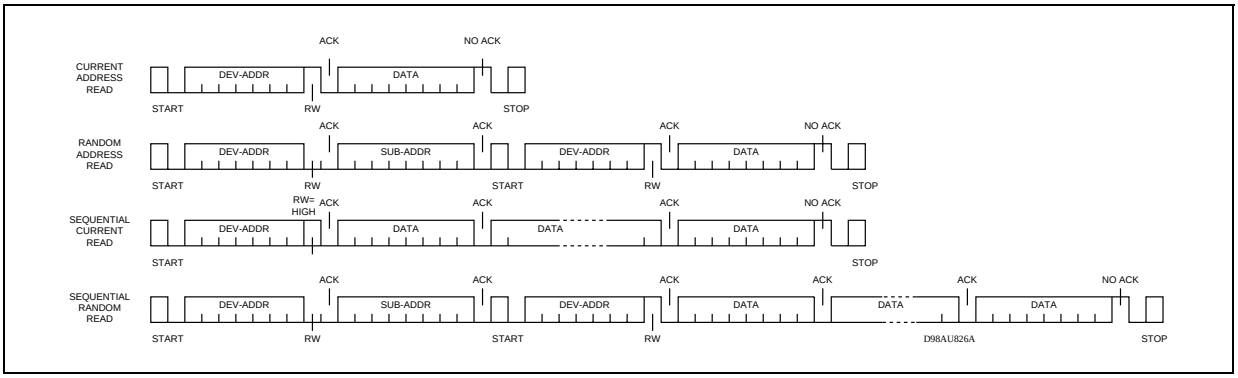


Figure 17. Read Mode Sequence



5.4 READ OPERATION (see Fig. 17)

5.4.1 Current byte address read

The STA015 has an internal byte address counter. Each time a byte is written or read, this counter is incremented. For the current byte address read mode, following a START condition the master sends the device address with the RW bit set to 1.

The STA015 acknowledges this and outputs the byte addressed by the internal byte address counter. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

5.4.2 Sequential address read

This mode can be initiated with either a current address read or a random address read. However in this case the master does acknowledge the data byte output and the STA015 continues to output the next byte in sequence. To terminate the streams of bytes the master does not acknowledge the last received byte, but terminates the transfer with a STOP condition. The output data stream is from consecutive byte addresses, with the internal byte address counter automatically incremented after one byte output.

6.0 I^2C REGISTERS

The following table gives a description of the MPEG Source Decoder (STA015) register list.

The first column (HEX_COD) is the hexadecimal code for the sub-address.

The second column (DEC_COD) is the decimal code.

The third column (DESCRIPTION) is the description of the information contained in the register.

The fourth column (RESET) inidicate the reset value if any. When no reset value is specifyed, the default is "undefined".

The fifth column (R/W) is the flag to distinguish register "read only" and "read and write", and the useful size of the register itself. Each register is 8 bit wide. The master shall operate reading or writing on 8 bits only.

I^2C REGISTERS

HEX_COD	DEC_COD	DESCRIPTION	RESET	R/W
$00	0	VERSION		R (8)
$01	1	IDENT	0xAC	R (8)
$05	5	PLLCTL [7:0]	0xA1	R/W (8)
$06	6	PLLCTL [20:16] (MF[4:0]=M)	0x0C	R/W (8)
$07	7	PLLCTL [15:12] (IDF[3:0]=N)	0x00	R/W (8)
$0C	12	REQ_POL	0x01	R/W (8)
$0D	13	SCLK_POL	0x04	R/W (8)
$0F	15	ERROR_CODE	0x00	R (8)
$10	16	SOFT_RESET	0x00	W (8)
$13	19	PLAY	0x01	R/W(8)
$14	20	MUTE	0x00	R/W(8)
$16	22	CMD_INTERRUPT	0x00	R/W(8)
$18	24	DATA_REQ_ENABLE	0x00	R/W(8)
$40 - $51	64 - 81	ADPCM_DATA_1 to ADPCM_DATA_18	0x00	R (8)
$40	64	SYNCSTATUS	0x00	R (8)
$41	65	ANCCOUNT_L	0x00	R (8)
$42	66	ANCCOUNT_H	0x00	R (8)
$43	67	HEAD_H[23:16]	0x00	R(8)
$44	68	HEAD_M[15:8]	0x00	R(8)

I²C REGISTERS

$45	69	HEAD_L[7:0]	0x00	R(8)
$46	70	DLA	0x00	R/W (8)
$47	71	DLB	0xFF	R/W (8)
$48	72	DRA	0x00	R/W (8)
$49	73	DRB	0xFF	R/W (8)
$4D	77	CHIP_MODE	0x00	R/W (2)
$4E	78	CRCR	0x00	R/W (1)
$50	80	MFSDF_441	0x00	R/W (8)
$51	81	PLLFRAC_441_L	0x00	R/W (8)
$52	82	ADPCM_DATA_READY	0x00	R/W (1)
$52	82	PLLFRAC_441_H	0x00	R/W (8)
$53	83	ADPCM_SAMPLE_FREQ	0x00	R/W (4)
$54	84	PCM DIVIDER	0x03	R/W (8)
$55	85	PCMCONF	0x21	R/W (8)
$56	86	PCMCROSS	0x00	R/W (8)
$61	97	MFSDF (X)	0x07	R/W (8)
$63	99	DAC_CLK_MODE	0x00	R/W (8)
$64	100	PLLFRAC_L	0x46	R/W (8)
$65	101	PLLFRAC_H	0x5B	R/W (8)
$67	103	FRAME_CNT_L	0x00	R (8)
$68	104	FRAME_CNT_M	0x00	R (8)
$69	105	FRAME_CNT_H	0x00	R (8)
$6A	106	AVERAGE_BITRATE	0x00	R (8)
$71	113	SOFTVERSION		R (8)
$72	114	RUN	0x00	R/W (8)
$77	119	TREBLE_FREQUENCY_LOW	0x00	R/W (8)
$78	120	TREBLE_FREQUENCY_HIGH	0x00	R/W (8)
$79	121	BASS_FREQUENCY_LOW	0x00	R/W (8)
$7A	122	BASS_FREQUENCY_HIGH	0x00	R/W (8)
$7B	123	TREBLE_ENHANCE	0x00	R/W (8)
$7C	124	BASS_ENHANCE	0x00	R/W (8)
$7D	125	TONE_ATTEN	0x00	R/W (8)
$7E - B5	126 - 181	ANC_DATA_1 to ANC_DATA_56	0x00	R (8)
$B6	182	ISR	0x00	R/W (1)
$B8	184	ADPCM_CONFIG	0x00	R/W (2)
$B9	185	GPSO_ENABLE	0x00	R/W (1)
$BA	186	GPSO_CONF	0x00	R/W (2)
$BB	187	ADC_ENABLE	0x00	R/W (1)
$BC	188	ADC_CONF	0x00	R/W (5)
$BD	189	ADPCM_FRAME_SIZE	0x00	R/W (8)
$BE	190	ADPCM_INT_CFG	0x00	R/W (8)
$BF	191	GPIO_CONF	0x00	R/W (2)
$C0	192	ADC_ WLEN	0x0F	R/W (5)
$C1	193	ADC_ WPOS	0x00	R/W (5)
$C2	194	ADPCM_SKIP_FRAME	0x00	R/W (8)

Notes: 1. The HEX_COD is the hexadecimal adress that the microcontroller has to generate to access the information.
2. RESERVED: register used for production test only, or for future use.

6.1 STA015 REGISTERS DESCRIPTION

The STA015 device includes 128 I^2C registers. In this document, only the user-oriented registers are described. The undocumented registers are reserved. These registers must never be accessed (in Read or in Write mode). The Read-Only registers must never be written.

The following table describes the meaning of the abbreviations used in the I^2C registers description:

Symbol	Comment
NA	Not Applicable
UND	Undefined
NC	No Charge
RO	Read Only
WO	Write Only
R/W	Read and Write
R/WS	Read, Write in specific mode

VERSION

Address: 0x00 (00)

Type: RO

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
V8	V7	V6	V5	V4	V3	V2	V1

The VERSION register is read-only and it is used to identify the IC on the application board.

IDENT

Address: 0x01

Type: RO

Software Reset: 0xAC

Hardware Reset: 0xAC

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
1	0	1	0	1	1	0	0

IDENT is a read-only register and is used to identify the IC on an application board. IDENT always has the value "0xAC"

PLLCTL

Address: 0x05

Type: R/W

Software Reset: 0x21

Hardware Reset: 0x21

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
XTO_BUF	XTODIS	OCLKEN	SYS2OCLK	PPLDIS	XTI2DSPCLK	XTI2OCLK	UPD_FRAC

UPD_FRAC: when is set to 1, update FRAC in the switching circuit. It is set to 1 after autoboot.

XTI2OCLK: when is set to 1, use the XTI as input of the divider X instead of VCO output. It is set to 0 on HW reset.

XTI2DSPCLK: when is to 1, set use the XTI as input of the divider S instead of VCO output. It is set to 0 on HW reset.

PLLDIS: when set to 1, the VCO output is disabled. It is set to 0 on HW reset.

SYS2OCLK: when is set to 1, the OCLK frequency is equal to the system frequency. It is useful for testing. It is set to 0 on HW reset.

OCLKEN: when is set to 1, the OCLK pad is enable as output pad. It is set to 1 on HW reset.

XTODIS: when is set to 1, the XTO pad is disable. It is set to 0 on HW reset.

XTO_BUF: when this bit is set, the pin nr. 28 (OUT_CLOCK/DATA_REQ) is enabled. It is set to 0 after autoboot.

PLLCTL (M)

Address: 0x06 (06)

Type: R/W

Software Reset: 0x0C

Hardware Reset: 0x0C

PLLCTL (N)

Address: 0x07 (07)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

The M and N registers are used to configure the STA015 PLL by DSP embedded software.

M and N registers are R/W type but they are completely controlled, on STA015, by DSP software.

REQ_POL

Address: 0x0C (12)

Type: R/W

Software Reset: 0x01

Hardware Reset: 0x00

The REQ_POL registers is used to program the polarity of the DATA_REQ line.

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	1

Default polarity (the source sends data when the DATA_REQ line is high)

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	1	0	1

Inverted polarity (the source sends data when the ATA_REQ line is low)

SCKL_POL

Address: 0x0D (13)

Type: R/W

Software Reset: 0x04

Hardware Reset: 0x04

MSB							LSB	
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	
X	X	X	X	X	0	0	0	(1)
					1	0	0	(2)

X = don't care

SCKL_POL is used to select the working polarity of the Input Serial Clock (SCKR).

(1) If SCKL_POL is set to 0x00, the data (SDI) are sent with the falling edge of SCKR and sampled on the rising edge.

(2) If SCKL_POL is set to 0x04, the data (SDI) are sent with the rising edge of SCKR and sampled on the falling edge.

ERROR_CODE

Address: 0x0F (15)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	EC5	EC4	EC3	EC2	EC1	EC0

X = don't care

ERROR_CODE register contains the last error occourred if any. The codes can be as follows:

CODE	Description
0x00	No error since the last SW or HW Reset
0x01	CRC Failure
0x02	DATA not available
0x04	Ancillary data not read
0x10	Audio synch word not found
0x2X	MPEG Header error
0x3X	MPEG Decoding errors

SOFT_RESET

Address: 0x10 (16)

Type: WO

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	X	X	X	X	0
							1

X = don't care; 0 = normal operation; 1 = reset

When this register is written, a soft reset occours. The STA015 core command register and the interrupt register are cleared. The decoder goes in to idle mode.

PLAY

Address: 0x13 (19)

Type: R/W

Software Reset: 0x01

Hardware Reset: 0x01

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	X	X	X	X	0
							1

X = don't care; 0 = normal operation; 1 = play

The PLAY command is handled according to the state of the decoder, as described in section 2.5. PLAY only becomes active when the decoder is in DECODE mode.

MUTE

Address: 0x14

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	X	X	X	X	0
							1

X = don't care; 0 = normal operation; 1 = mute The MUTE command is handled according to the state of the decoder, as described in section 2.5. MUTE sets the clock running.

CMD_INTERRUPT

Address: 0x16 (22)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	0
							1

X = don't care;

0 = normal operation;

1 = write into I^2C/Ancillary Data

The INTERRUPT is used to give STA015 the command to write into the I^2C/Ancillary Data Buffer (Registers: 0x7E ... 0xB5). Every time the Master has to extract the new buffer content it writes into this register, setting it to a non-zero value.

DATA_REQ_ENABLE

Address: 0x18 (24)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
X	X	X	X	X	0	X	X	buffered output clock
X	X	X	X	X	1	X	X	request signal

The DATA_REQ_ENABLE register is used to configure Pin n. 28 working as buffered output clock or data request signal, used for multimedia mode.

The buffered Output Clock has the same frequency than the input clock (XTI)

SYNCSTATUS

Address: 0x40 (64)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
X	X	X	X	X	X	SS1	SS0	
						0	0	Research of sync word
						0	1	Wait for Confirmation
						1	0	Synchronised

ADPCM_DATA BUFFER

Address: 0x40 - 0x51 (64 - 81)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
ENCODED DATA N to N+18							

ANCCOUNT_L

Address: 0x41 (65)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0

ANCCOUNT_H

Address: 0x42 (66)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

ANCCOUNT_H

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
AC15	AC14	AC13	AC12	AC11	AC10	AC9	AC8

ANCCOUNT registers are logically concatenated and indicate the number of Ancillary Data bits available at every correctly decoded MPEG frame.

HEAD_H[23:16]

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	H20	H19	H18	H17	H16

x = don’t care

HEAD_M[15:8]

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
H15	H14	H13	H12	H11	H10	H9	H8

HEAD_L[7:0]

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
H7	H6	H5	H4	H3	H2	H1	H0

Address: 0x43, 0x44, 0x45 (67, 68, 69)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

Head[1:0] emphasis

Head[2] original/copy

Head[3] copyrightHead

[5:4] mode extension

Head[7:6] mode

Head[8] private bit

Head[9] padding bit

Head[11:10] sampling frequency index

Head[15:12] bitrate index

Head[16] protection bit

Head[18:17] layer

Head[19] ID

Head[20] ID_ex

The HEAD registers can be viewed as logically concatenated to store the MPEG Layer III Header content. The set of three registers is updated every time the synchronisation to the new MPEG frame is achieved The meaning of the flags are shown in the following tables:

MPEG IDs

IDex	ID	
0	0	MPEG 2.5
0	1	reserved
1	0	MPEG 2
1	1	MPEG 1

Layer

in Layer III these two flags must be set always to "01".

Protection_bit

It equals "1" if no redundancy has been added and "0" if redundancy has been added.

Bitrate_index

indicates the bitrate (Kbit/sec) depending on the MPEG ID.

bitrate index	ID = 1	ID = 0
'0000'	free	free
'0001'	32	8
'0010'	40	16
'0011'	48	24
'0100'	56	32
'0101'	64	40
'0110'	80	48
'0111'	96	56
'1000'	112	64
'1001'	128	80
'1010'	160	96
'1011'	192	112
'1100'	224	128
'1101'	256	144
'1110'	320	160
'1111'	forbidden	forbidden

Sampling Frequency

indicates the sampling frequency of the encoded audio signal (KHz) depending on the MPEG ID

Sampling Frequency	MPEG1	MPEG2	MPEG2.5
'00'	44.1	22.05	11.03
'01'	48	24	12
'10'	32	16	8
'11'	reserved	reserved	reserved

Padding bit

if this bit equals '1', the frame contains an additional slot to adjust the mean bitrate to the sampling frequency, otherwise this bit is set to '0'.

Private bit

Bit for private use. This bit will not be used in the future by ISO/IEC.

Mode

Indicates the mode according to the following table. The joint stereo mode is intensity_stereo and/or ms_stereo.

mode	mode specified
'00'	stereo
'01'	joint stereo (intensity_stereo and/or ms_stereo)
'10'	dual_channel
'11'	single_channel (mono)

Mode extension

These bits are used in joint stereo mode. They indicates which type of joint stereo coding method is applied. The frequency ranges, over which the intensity_stereo and ms_stereo modes are applied, are implicit in the algorithm.

Copyright

If this bit is equal to '0', there is no copyright on the bitstream, '1' means copyright protected.

Original/Copy

This bit equals '0' if the bitstream is a copy, '1' if it is original.

Emphasis

Indicates the type of de-emphasis that shall be used.

emphasis	emphasis specified
'00'	none
'01'	50/15 microseconds
'10'	reserved
'11'	CCITT J, 17

DLA

Address: 0x46 (70)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

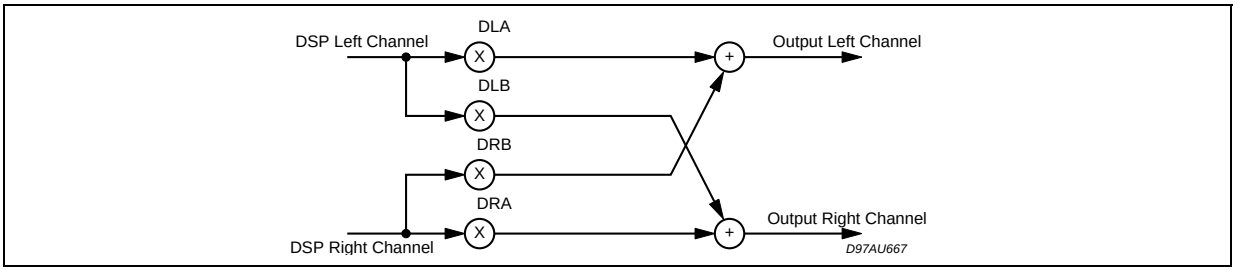
MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
DLA7	DLA6	DLA5	DLA4	DLA3	DLA2	DLA1	DLA0	OUTPUT ATTENUATION
0	0	0	0	0	0	0	0	NO ATTENUATION
0	0	0	0	0	0	0	1	-1dB
0	0	0	0	0	0	1	0	-2dB
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	0	0	-96dB

DLA register is used to attenuate the level of audio output at the Left Channel using the butterfly shown in Fig. 18. When the register is set to 255 (0xFF), the maximum attenuation is achieved.

A decimal unit correspond to an attenuation step of 1 dB.

Figure 18. Volume Control and Output Setup



DLB

Address: 0x47 (71)

Type: R/W

Software Reset: 0xFF

Hardware Reset: 0xFF

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
DLB7	DLB6	DLB5	DLB4	DLB3	DLB2	DLB1	DLB0	OUTPUT ATTENUATION
0	0	0	0	0	0	0	0	NO ATTENUATION
0	0	0	0	0	0	0	1	-1dB
0	0	0	0	0	0	1	0	-2dB
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	0	0	-96dB

DLB register is used to re-direct the Left Channel on the Right, or to mix both the Channels. Default value is 0x00, corresponding at the maximum attenuation in the re-direction channel.

DRA

Address: 0x48 (72)

Type: R/W

Software Reset: 0X00

Hardware Reset: 0X00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
DRA7	DRA6	DRA5	DRA4	DRA3	DRA2	DRA1	DRA0	OUTPUT ATTENUATION
0	0	0	0	0	0	0	0	NO ATTENUATION
0	0	0	0	0	0	0	1	-1dB
0	0	0	0	0	0	1	0	-2dB
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	0	0	-96dB

DRA register is used to attenuate the level of audio output at the Right Channel using the butterfly shown in Fig. 11. When the register is set to255 (0xFF), the maximum attenuation is achieved.

A decimal unit correspond to an attenuation stepof 1 dB.

DRB

Address: 0x49 (73)

Type: R/W

Software Reset: 0xFF

Hardware Reset: 0xFF

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
DRB7	DRB6	DRB5	DRB4	DRB3	DRB2	DRB1	DRB0	OUTPUT ATTENUATION
0	0	0	0	0	0	0	0	NO ATTENUATION
0	0	0	0	0	0	0	1	-1dB
0	0	0	0	0	0	1	0	-2dB
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	0	0	-96dB

DRB register is used to re-direct the Right Channel on the Left, or to mix both the Channels. Default value is 0x00, corresponding at the maximum attenuation in the re-direction channel.

CHIP_MODE

Address: 0x4D (77)

Type: R/W

Hardware Reset: 0x00

Using this register it's possible to select which operation will be performed by the DSP.

Possible values are:

0x00 - MP3 decoding

0x01 - Reserved

0x02 - ADPCM Encoder

0x03 - ADPCM Decoder

0x04 - BYPASS mode

The DSP will check for the value of this register right after the RUN command has been issued (refer to RUN register). After that no more checks will be performed: therefore a SOFT_RESET must be generated in order to change the device mode.

CRCR

Address: 0x4E (78)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	CRCEN

The CRC register is used to enable/disable the CRC check. If CRC_EN bit is cleared, the CRC value encoded in the bitstream is checked against the hardware one. If a discrepance occurs, the current frame is skipped and the decoder is muted. The ERROR_CODE register is affected with the value 0x01.

If CRC_EN bit is set, the result of the CRC check is ignored, but the ERROR_CODE register is nevertheless affected with the value 0x01 if a discrepance has occurred.

MFSDF_441

Address: 0x50 (80)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	M4	M3	M2	M1	M0

This register contains the value for the PLL X driver for the 44.1KHz reference frequency.

The VCO output frequency, when decoding 44.1KHz bitstream, is divided by (MFSDF_441 +1)

PLLFRAC_441_L

Address: 0x51 (81)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

ADPCM_DATA_READY

Address: 0x52 (82)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	ADR

ADR: Adpcm Data Ready

This bit signal ADPCM encoded data are ready to be retrieved.

PLLFRAC_441_H

Address: 0x52 (82)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PF15	PF14	PF13	PF12	PF11	PF10	PF19	PF8

The registers are considered logically concatenated and contain the fractional values for the PLL, for 44.1KHz reference frequency.

(see also PLLFRAC_L and PLLFRAC_H registers)

ADPCM_SAMPLE_FREQ

Address: 0x53 (83)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	ADPCM_SF				

ADPCM_SF: Adpcm Sample Frequency

0x02	8KHz
0x0A	16KHz
0x0E	32KHz

PCMDIVIDER

Address: 0x54 (84)

Type: RW

Software Reset: 0x01

Hardware Reset: 0x01

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PCMDIVIDER is used to set the frequency ratio between the OCLK (Oversampling Clock for DACs), and the SCKT (Serial Audio Transmitter Clock).

The relation is the following:

$$SCKT\_freq = \frac{OCLK\_freq}{2(1 + PCM\_DIV)}$$

The Oversampling Factor (O_FAC) is related to OCLK and SCKT by the following expression:

1) OCLK_freq = O_FAC * LRCKT_ Freq (DAC relation)

2) OCLK_ Freq = 2 * (1+PCM_DIV) * 32* LRCKT_Freq (when 16 bit PCM mode is used)

3) OCLK_ Freq = 2 * (1+PCM_DIV) * 64* LRCKT_Freq (when 32 bit PCM mode is used)

4) PCM_DIV = (O_FAC/64) - 1 in 16 bit mode
5) PCM_DIV = (O_FAC/128) - 1 in 32 bit mode
Example for setting:

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description	
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0		
0	0	0	0	0	1	1	1	16 bit mode	512 x Fs
0	0	0	0	0	1	0	1	16 bit mode	384 x Fs
0	0	0	0	0	0	1	1	16 bit mode	256 x Fs
0	0	0	0	0	0	1	1	32 bit mode	512 x Fs
0	0	0	0	0	0	1	0	32 bit mode	384 x Fs
0	0	0	0	0	0	0	1	32 bit mode	256 x Fs

for 16 bit PCM Mode

O_FAC = 512 ; PCM_DIV = 7

O_FAC = 256 ; PCM_DIV = 3

O_FAC = 384 ; PCM_DIV = 5

for 32 bit PCM Mode

O_FAC = 512 ; PCM_DIV = 3

O_FAC = 256 ; PCM_DIV = 1

O_FAC = 384 ; PCM_DIV = 2

PCMCONF

Address: 0x55 (85)

Type: R/W

Software Reset: 0x21

Hardware Reset: 0x21

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
X	ORD	DIF	INV	FOR	SCL	PREC (1)	PREC (1)	
X	1							PCM order the LS bit is transmitted First
X	0							PCM order the MS bit is transmitted First
X		0						The word is right aligned
X		1						The word is left aligned
X			0					LRCKT Polarity compliant to I^2S format
X			1					LRCKT Polarity inverted
X				0				I^2S format
X				1				Different formats
X					1			Data are sent on the rising edge of SCKT
X					0			Data are sent on the falling edge of SCKT
X						0	0	16 bit mode (16 slots transmitted)
X						0	1	18 bit mode (32 slots transmitted)
X						1	0	20 bit mode (32 slots transmitted)
X						1	1	24 bit mode (32slots transmitted)

PCMCONF is used to set the PCM Output Interface configuration:

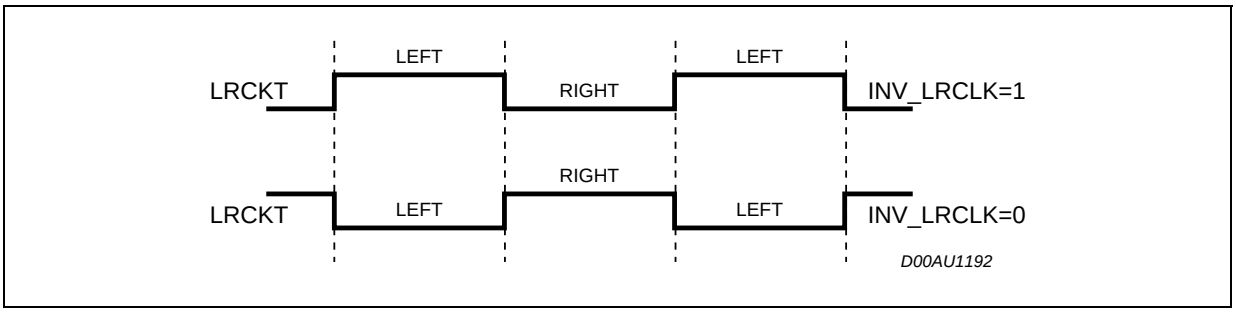
ORD: PCM order. If this bit is set to'1', the LS Bit is transmitted first, otherwise MS Bit is transmiited first.

DIF: PCM_DIFF. It is used to select the position of the valid data into the transmitted word. This setting is significant only in 18/20/24 bit/word mode.If it is set to '0' the word is right-padded, otherwise it is left-padded.

INV (fig.13): It is used to select the LRCKT clock polarity. If it is set to '1' the polarity is compliant to I^2S format (low -> left , high -> right), otherwise the LRCKT is inverted.

The default value is '0'. (if I^2S have to be selected, must be set to '1' in the TA013 configuration phase).

Figure 19. LRCKT Polarity Selection



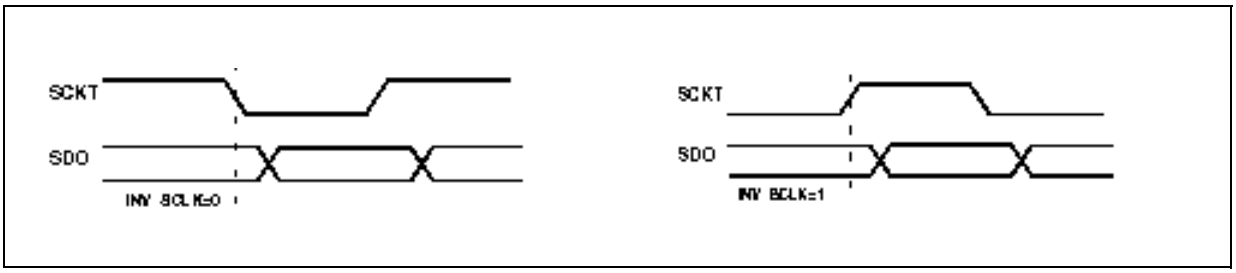
FOR: FORMAT is used to select the PCM Output Interface format.

After hw and sw reset the value is set to 0 corresponding to I^2S format.

SCL (fig.14): used to select the Transmitter Serial Clock polarity. If set to '1' the data are sent on the falling edge and sampled on the rising. This last option is the most commonly used by the commercial DACs.

The default configuration for this flag is '0'.

Figure 20. SCKT Polarity Selection



PREC [1:0]: PCM PRECISION

It is used to select the PCM samples precision, as follows:

'00': 16 bit mode (16 slots transmitted)

'01': 18 bit mode (32 slots transmitted)

'10': 20 bit mode (32 slots transmitted)

'11': 24 bit mode (32 slots transmitted)

The PCM samples precision in STA015 can be 16 or 18-20-24 bits.

When STA015 operates in 16 (18-20-24) bits mode, the number of bits transmitted during a LRCLT period is 32 (64).

PCMCROSS

Address: 0x56 (86)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0	Description
X	X	X	X	X	X	0	0	Left channel is mapped on the left output. Right channel is mapped on the Right output
X	X	X	X	X	X	0	1	Left channel is duplicated on both Output channels.
X	X	X	X	X	X	1	0	Right channel is duplicated on both Output channels
X	X	X	X	X	X	1	1	Right and Left channels are toggled

The default configuration for this register is ’0x00’.

MFSDF (X)

Address: 0x61 (97)

Type: R/W

Software Reset: 0x07

Hardware Reset: 0x07

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	M4	M3	M2	M1	M0

The register contains the values for PLL X divider (see Fig. 7).

The value is changed by the internal STA015 Core, to set the clocks frequencies, according to the incoming bitstream. This value can be even set by the user to select the PCM interface configuration.

The VCO output frequency is divided by (X+1). This register is a reference for 32KHz and 48KHz input bitstream.

DAC_CLK_MODE (99)

Address: 0x63

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	MODE

This register is used to select the operating mode for OCLK clock signal. If it is set to “1”, the OCLK frequency is fixed, and it is mantained to the value fixed by the user even if the sampling frequency of the incoming bitstream changes. It the MODE flag is set to f0f, the OCLK frequency changes, and can be set to (512, 384, 256) * Fs. The default configuration for this mode is 256 * Fs. When this mode is selected,

the default OCLK frequency is 12.288 MHz.

PLLFRAC_L ([7:0])

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

PLLFRAC_H ([15:8])

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8

Address: 0x64 - 0x65 (100 - 101)

Type: R/W

Software Reset: 0x46 | 0x5B

Hardware Reset: 0xNA | 0x5B

The registers are considered logically concatenated and contain the fractional values for the PLL, used to select the internal configuration. After Reset, the values are NA, and the operational setting are done when the MPEG synchronisation is achieved.

The following formula describes the relationships among all the STA015 fractional PLL parameters:

$$OCLK\_Freq = \left[\frac{1}{X+1}\right] \cdot \left[\frac{MCLK\_Freq}{N+1}\right] \cdot \left[M + 1 + \frac{FRAC}{65536}\right]$$

where:

FRAC=256 x FRAC_H + FRAC_L (decimal)

These registers are a reference for 48 / 24 / 12 / 32 / 16 / 8KHz audio.

FRAME_CNT_L

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0

FRAME_CNT_M

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8

FRAME_CNT_H

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
FC23	FC22	FC21	FC20	FC19	FC18	FC17	FC16

Address: 0x67, 0x68, 0x69 (103 - 104 - 105)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

The three registers are considered logically concatenated and compose the Global Frame Counter as described in the table.

It is updated at every decoded MPEG Frame. The registers are reset on both hardware and software reset.

AVERAGE_BITRATE

Address: 0x6A (106)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0

AVERAGE_BITRATE is a read-only register and it contains the average bitrate of the incoming bitstream divided by two.

The value is rounded with an accuracy of 1 Kbit/sec.

SOFTVERSION

Address: 0x71 (113)

Type: RO

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
SV7	SV6	SV5	SV4	SV3	SV2	SV1	SV0

After the STA015 boot, this register contains the version code of the embedded software.

RUN

Address: 0x72 (114)

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	RUN

Setting this register to 1, STA015 leaves the idle state, starting the decoding process.

The Microcontroller is allowed to set the RUN flag, once all the control registers have been initialized.

TREBLE_FREQUENCY_LOW

Address: 0x77 (119)

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
TF7	TF6	TF5	TF4	TF3	TF2	TF1	TF0

TREBLE_FREQUENCY_HIGH

Address: 0x78

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
TF15	TF14	TF13	TF12	TF11	TF10	TF9	TF8

The registers TREBLE_FREQUENCY-HIGH and TREBLE_FREQUENCY-LOW, logically concatenated as a 16 bit wide register, are used to select the frequency, in Hz, where the selected frequency is +12dB respect to the stop band. By setting these registers, the following rule must be kept:

Treble_Freq < Fs/2

BASS_FREQUENCY_LOW

Address: 0x79 (121)

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

BASS_FREQUENCY_HIGH

Address: 0x7A (122)

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
BF15	BF14	BF13	BF12	BF11	BF10	BF9	BF8

The registers BASS_FREQUENCY_HIGH and BASS_FREQUENCY_LOW, logically concatenated as a 16 bit wide register, are used to select the frequency, in Hz, where the selected frequency is -12dB respect to the pass-band. By setting the BASS_FREQUENCY registers, the following rules must be kept:

Bass_Freq <= Treble_Freq

Bass_Freq > 0

(suggested range: 20 Hz < Bass_Freq < 750 Hz)

Example:

Bass = 200Hz

Treble = 3kHz

TFS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0

BFS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

TREBLE_ENHANCE

Address: 0x7B (123)

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0

Signed number (2 complement)

This register is used to select the enhancement or attenuation STA015 has to perform on Treble Frequency range at the digital signal.

A decrement (increment) of a decimal unit corresponds to a step of attenuation (enhancement) of 1.5dB.

The allowed Attenuation/Enhancement range is [-18dB, +18dB].

MSB							LSB	ENHANCE/ATTENUATION
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	**1.5dB step**
0	0	0	0	1	1	0	0	+18
0	0	0	0	1	0	1	1	+16.5
0	0	0	0	1	0	1	0	+15
0	0	0	0	1	0	0	1	+13.5
							:	
							:	
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	-1
							:	
							:	
1	1	1	1	0	1	1	1	+13.5
1	1	1	1	0	1	1	0	-15
1	1	1	1	0	1	0	0	-16.5
1	1	1	1	0	1	0	0	-18

BASS_ENHANCE

Address: 0x7C (1240

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0

Signed number (2 complement)

This register is used to select the enhancement or attenuation STA015 has to perform on Bass Frequency range at the digital signal. A decrement (increment) of a decimal unit corresponds to a step of attenuation (enhancement) of 1.5dB.

The allowed Attenuation/Enhancement range is [-18dB, +18dB].

MSB **LSB** **ENHANCE/ATTENUATION**

b7	b6	b5	b4	b3	b2	b1	b0	1.5dB step
0	0	0	0	1	1	0	0	+18
0	0	0	0	1	0	1	1	+16.5
0	0	0	0	1	0	1	0	+15
0	0	0	0	1	0	0	1	+13.5
							:	
							:	
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	-1
							:	
							:	
1	1	1	1	0	1	1	1	+13.5
1	1	1	1	0	1	1	0	-15
1	1	1	1	0	1	0	0	-16.5
1	1	1	1	0	1	0	0	-18

TONE_ATTEN

Address: 0x7D (125)

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

In the digital output audio, the full signal is achieved with 0 dB of attenuation. For this reason, before applying Bass & Treble Control, the user has to set the TONE_ATTEN register to the maximum value of en-

hancement is going to perform.

For example, in case of a 0 dB signal (max. level) only attenuation would be possible. If enhancement is desired, the signal has to be attenuated accordingly before in order to reserve a margin in dB.

An increment of a decimal unit corresponds to a Tone Attenuation step of 1.5dB.

MSB							LSB	ATTENUATION
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	**1.5dB step**
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	-1.5dB
0	0	0	0	1	0	1	0	3dB
0	0	0	0	0	0	1	1	4.5dB
							:	
							:	
0	0	0	0	1	0	1	0	-15
0	0	0	0	1	0	1	1	-16.5
0	0	0	0	1	1	0	0	-18

ANCILLARY DATA BUFFER

Address: 0x7E - 0xB5 (126 - 181)

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

The STA015 contains 56 consecutive 8-bit registers corresponding to the maximum number of ancillary data that may be contained in MPEG frame.

The ANCCOUNT_L and ANCOUNT_H registers contain the number of ancillary data bits available within the current MPEG frame.

To perform ancillary data reading a status register (0xB6 - INTERRUPT_STATUS_REGISTER) is available: bit 0 of this register should be polled by the microcontroller in order to understand when new data are available.

0x7E	ANC_DATA_1
.....	.....
.....	.....
.....	.....
0xB5	ANC_DATA_56

0xB6	ISR

ISR

Address: 0xB6 (182)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	X	X	X	X	0
							1

X = don't care;

0 = no ancillary data

1 = Ancillary Data Available

The ISR is used by the microcontroller to understand when a new ancillary data block is available. After all ancillary data has been retrieved this bit must be cleared.

ADPCM_CONFIG

Address: 0xB8 (184)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB							LSB
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
X	X	X	X	AA1	AA0	ASM_EN	AFM_EN

This register controls ADPCM engine and how data must be compressed.

AFM_EN ADPCM Frame Mode Enable

0 = no frames (raw format)

1 = select the framed output format for ADPCM encoded data

ASM_EN: ADPCM Stereo Mode Enable

0 = Disable stereo mode

1 = Enable stereo mode

AA0,AA1: ADPCM Algorithm selection The ADPCM encoding/decoding algorithm can be selected according to the following table:

AA1	AA0	
0	0	DVI algorithm
0	1	G723-24 algorithm (24kbp/s)
1	0	G721 algorithm (32kbp/s)
1	1	G723-40 algorithm (40kbp/s)

The above bitrates refers to an 8 KHz 16 bits mono input stream.

Please note that 32KHz stereo mode is only available (both in encoding and decoding) with DVI algorithm

GPSO_ENABLE

Address: 0xB9 (185)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	GEN

This register enable/disable the GPSO interface.

Setting the GEN bit will enable the serial interface for ADPCM data retrieving. Reset GEN bit to disable GPSO interface.

GPSO_CONF

Address: 0xBA (186)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	GRP	GSP

GSP: GPSO clock polarity sing this bit the GPSO_SCKR polarity can be controlled. Clearing GSP bit data on GPSO_DATA line will be provided on the rising edge of GPSO_SCKR (sampling on falling edge). Setting GSP bit data are provided on falling edge of GPSO_SCKR (sampling on rising edge)

GRP: GPSO Request Polarity This bit is used to determine the polarity of GPSO_REQ signal. If GRP bit is cleared data are valid on GPSO_REQ signal high. If this bit is set data are valid on GPSO_REQ signal low

ADC_ENABLE

Address: 0xBB (187)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	ADCEN

This register controls if the ADPCM data to be encoded comes from A/D interface or from MP3 bitstream input interface.

If ADCEN bit is set data to be encoded comes from ADC interface, otherwise data comes from MP3 stream interface

ADC_CONF

Address: 0xBC (188)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	ALRCS	ALRCP	ASCP	ADC	AIIS

Using this register the ADC input interface can be configured as follow:

AIIS: ADC I^2S mode
0 = sample word must be aligned with LRCK (no I^2S mode)
1 = sample word not aligned with LRCK (I^2S compliant mode)

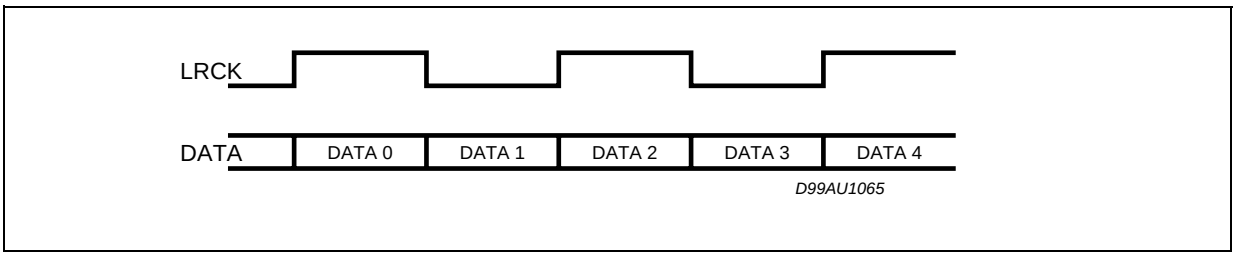
ADC: ADC Data Config.
0 = sample word is LSB first
1 = sample word is MSB first

ASCP: ADC Serial Clock Polarity
0 = Data is sampled on rising edge
1 = Data is sampled an falling edge

ALRCP: ADC Left/Right Clock Polarity

ALRCS: ADC Left/Right Clock Start value. This two bits permit to determine Left/Right clock usage according to the following table:

ALRCP	ALRCS	LEFT/RIGHT COUPLE	
0	0	(Data1, Data2)	(Data3, Data4)
1	0	(0, 1)	(2, 3)
0	1	(0, 1)	(2, 3)
1	1	(1, 2)	(3, 4)



ADPCM_FRAME_SIZE

Address: 0xBD (189)

Type: R/W

Software Reset: 0x13

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
AFS7	AFS6	AFS5	AFS4	AFS3	AFS2	AFS1	AFS0

The ADPCM frame size may be adjusted to match a trade-off between the bitrate overhead and the frame length. The frame size (in bytes) is calculated as follow:

FRAME size = (ADPCM_FRAME_SIZE * 90) +108

The frame starts with a 12 bytes header:

– 6 bytes for DVI algorithm

– 96 bytes for G726 pack algorithms

ADPCM_INT_CFG

Address: 0xBE (190)

Type: R/W

Software Reset: 0x0B

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
INTL6	INTL5	INTL4	INTL3	INTL2	INTL1	INTL0	X

Using this register the ADPCM interrupt capability can be properly configured. INTL0 - INTL6 Interrupt Length he interrupt length can be programmed, using this bits, from 0 up to 128 system clock cycles

GPIO_CONF

Address: 0xBF (191)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	GOSP	GISP

This register controls how data are strobed on the GPIO interface.

GISP: GPIO Strobe Polarity in INPUT mode

0 = data strobed an falling edge

1 = data strobed on rising edge

GOSP: GPIO Strobe Polarity in OUTPUT mode

0 = non inverted

1 = inverted

ADC_WLEN

Address: 0xC0 (192)

Type: R/W

Software Reset: 0x0F

Hardware Reset: 0x0F

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	AWL4	AWL3	AWL2	AWL1	AWL0

To select ADC word length AWL4 through AWL0 bits can be used.

This 5 bit value must contain the size of the significant data bits minus one.

ADC_WPOS

Address: 0xC1 (193)

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB **LSB**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	AWP4	AWP3	AWP2	AWP1	AWP0

These bits specify the position of the sample word referred to the LRCK slot boundary.

Bit AWP0 thru AWP4 must be programmed with the number of bits to ignore after the sample word.

ADPCM_SKIP_FRAME

Address: 0xC2 (194)

Type: R/W

Software Reset:0x00

Hardware Reset: 0x00

MSB **LSB**

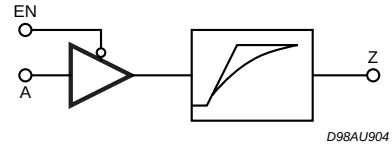
b7	b6	b5	b4	b3	b2	b1	b0
ASF7	ASF6	ASF5	ASF4	ASF3	ASF2	ASF1	ASF0

This register is useful when decoding ADPCM frame-based streams in order to skip the specified number of frames.

The content of the register will automatically be decremented on each new frame and the skip process will continue until the content reaches zero.

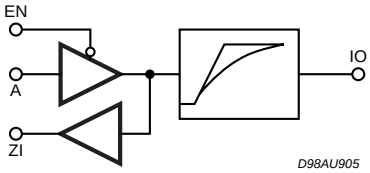
6.2 I/O CELL DESCRIPTION (pinout relative to TQFP44 package)

1) CMOS Tristate Output Pad Buffer, 4mA, with Slew Rate Control / Pin numbers 2, 4, 13, 27, 33, 42, 44



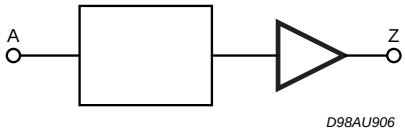
OUTPUT PIN	MAX LOAD
Z	100pF

2) CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control / Pin numbers 3, 31



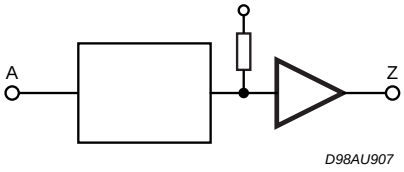
INPUT PIN	CAPACITANCE	OUTPUT PIN	MAX LOAD
IO	5pF	IO	100pF

3) CMOS Inpud Pad Buffer / Pin numbers 24, 26, 32, 34, 36, 40



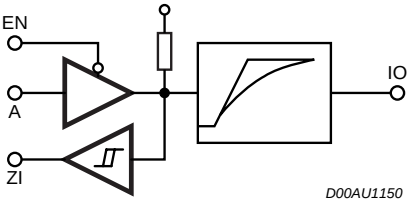
INPUT PIN	CAPACITANCE
A	3.5pF

4) CMOS Inpud Pad Buffer with Active Pull-Up / Pin numbers 22, 25, 28, 38



INPUT PIN	CAPACITANCE
A	3.5pF

5) CMOS Schmitt Trigger Bidir Pad Buffer with active Pull-up, 4mA, with slew rate control/
Pin numbers 14, 16, 18, 20, 35, 37, 39, 41, 43

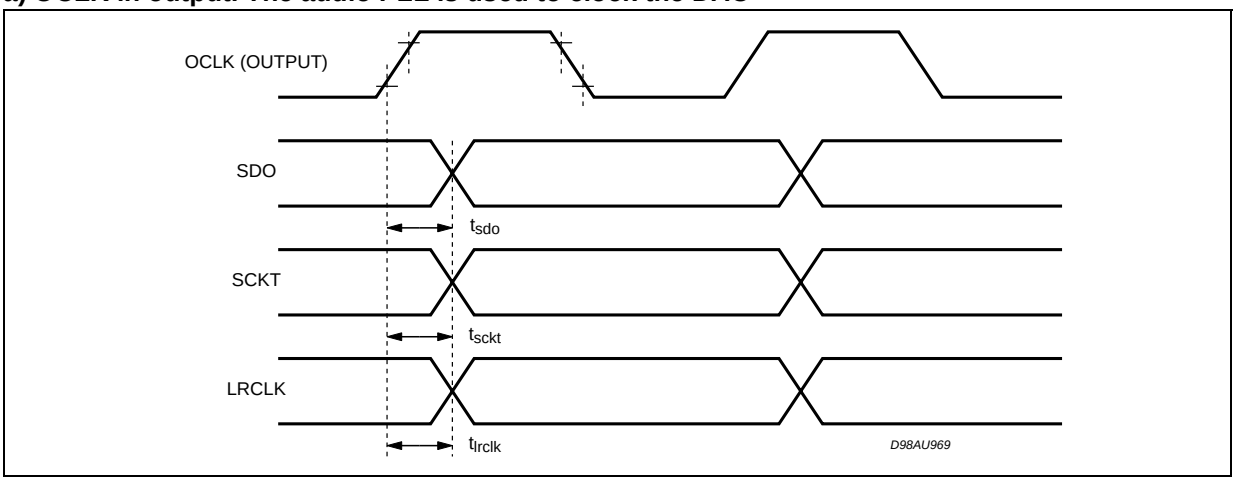


INPUT PIN	CAPACITANCE	OUTPUT PIN	MAX LOAD
IO	5pF	IO	100pF

6.3 TIMING DIAGRAMS

6.3.1 Audio DAC Interface

a) OCLK in output. The audio PLL is used to clock the DAC



tsdo = 3.5 + pad_timing (Cload_SDO) - pad_timing (Cload_ OCLK)

tsckt = 4 + pad_timing (Cload_SCKT) - pad_timing (Cload_ OCLK)

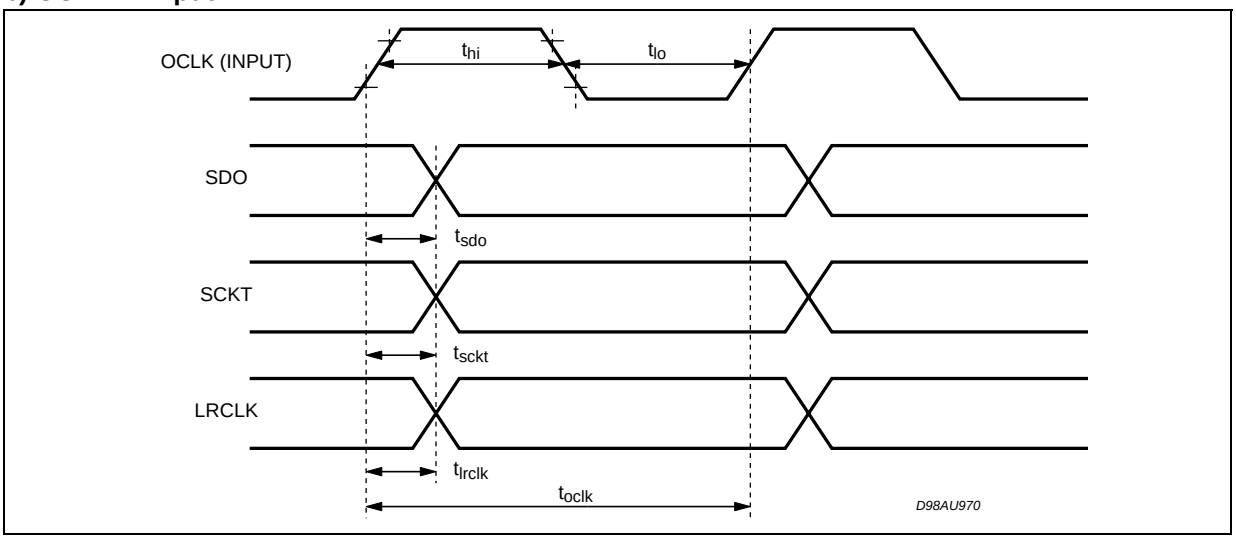
tlrckt = 3.5 + pad_timing (Cload_LRCCKT) - pad_timing (Cload_ OCLK)

Pad-timing versus load

Load (pF)	Pad_timing
25	2.90ns
50	3.82ns
75	4.68ns
100	5.52ns

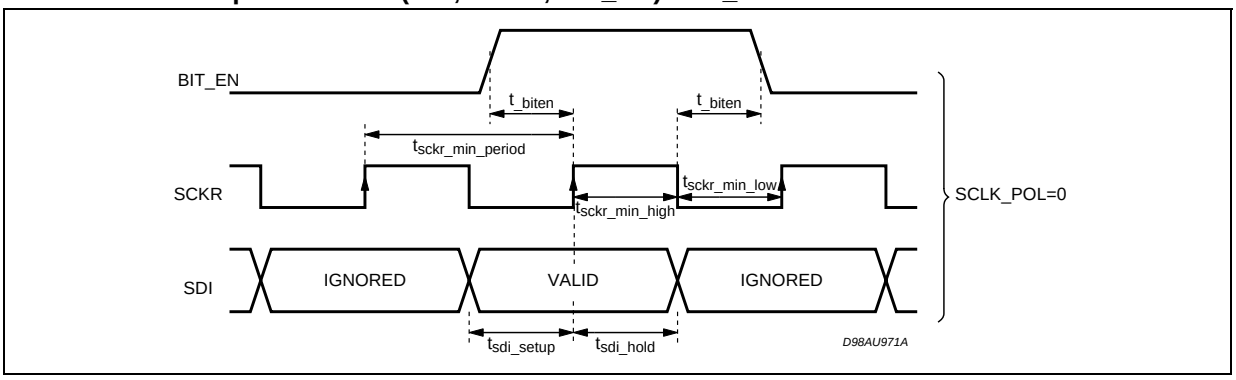
Cload_XXX is the load in pF on the XXX output. pad_timing (Cload_XXX) is the propagation delay added to the XXX pad due to the load.

b) OCLK in input.

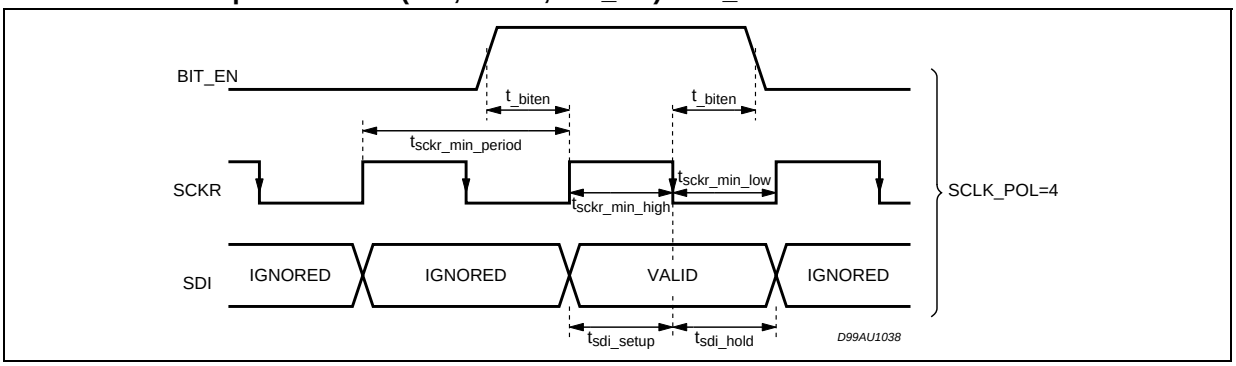


Thi min = 3ns
Tlo min = 3ns
Toclk min = 25ns
tsdo = 5.5 + pad_timing (Cload_SDO) ns
tsckt = 6 + pad_timing (Cload_SCKT) ns
tlrckt = 5.5 + pad_timing (Cload_LRCKT) ns

6.3.2 Bitstream input interface (SDI, SCKR, BIT_EN) SCL_POL = 0



6.3.3 Bitstream input interface (SDI, SCKR, BIT_EN) SCL_POL = 1

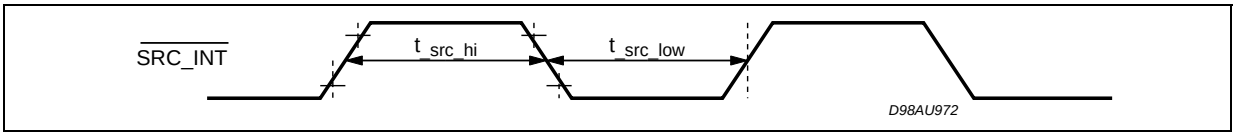


tsdi_setup_min = 2ns
tsdi_hold_min = 3ns
tsckr_min_hi = 10ns
tsckr_min_low = 10ns
tsckr_min_lperiod = 50ns
t_biten (min) = 2ns

6.3.4 SRC_INT

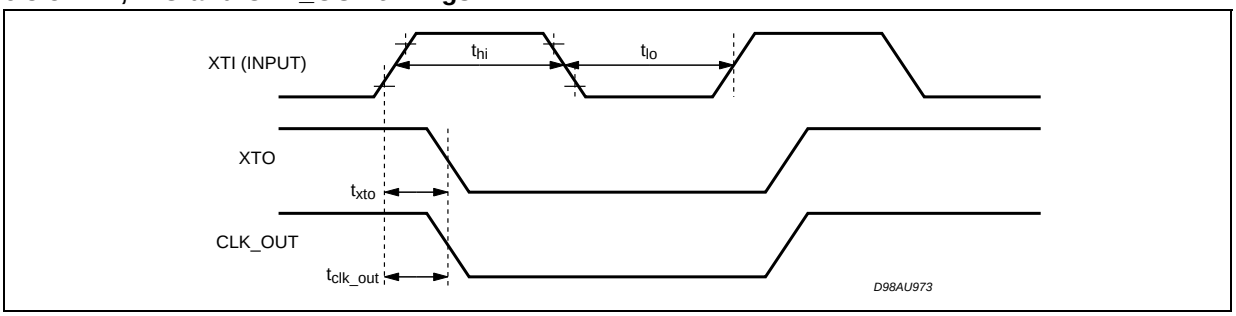
This is an asynchronous input used in "broadcast' mode.

SRC_INT is active low



t_src_low min duration is 50ns (1DSP clock period)
t_src_high min duration is 50ns (1DSP clock period)

6.3.5 XTI,XTO and CLK_OUT timings



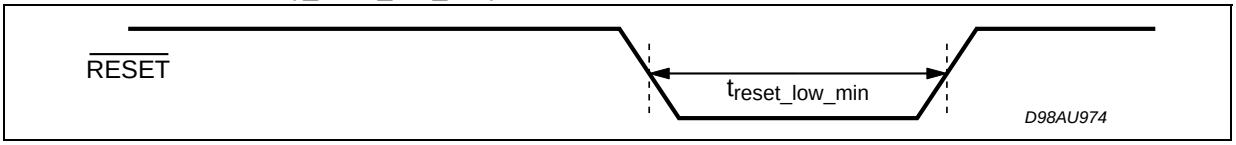
txto = 1.40 + pad_timing (Cload_XTO) ns

tclk_out = 4 + pad_timing (Cload_CLK_OUT) ns

Note: In "multimedia" mode, the CLK_OUT pad is DATA_REQ. In that case, no timing is given between the XTI input and this pad.

6.3.6 $\overline{\text{RESET}}$

The Reset min duration (t_reset_low_min) is 100ns



6.4 CONFIGURATION FLOW EXAMPLE

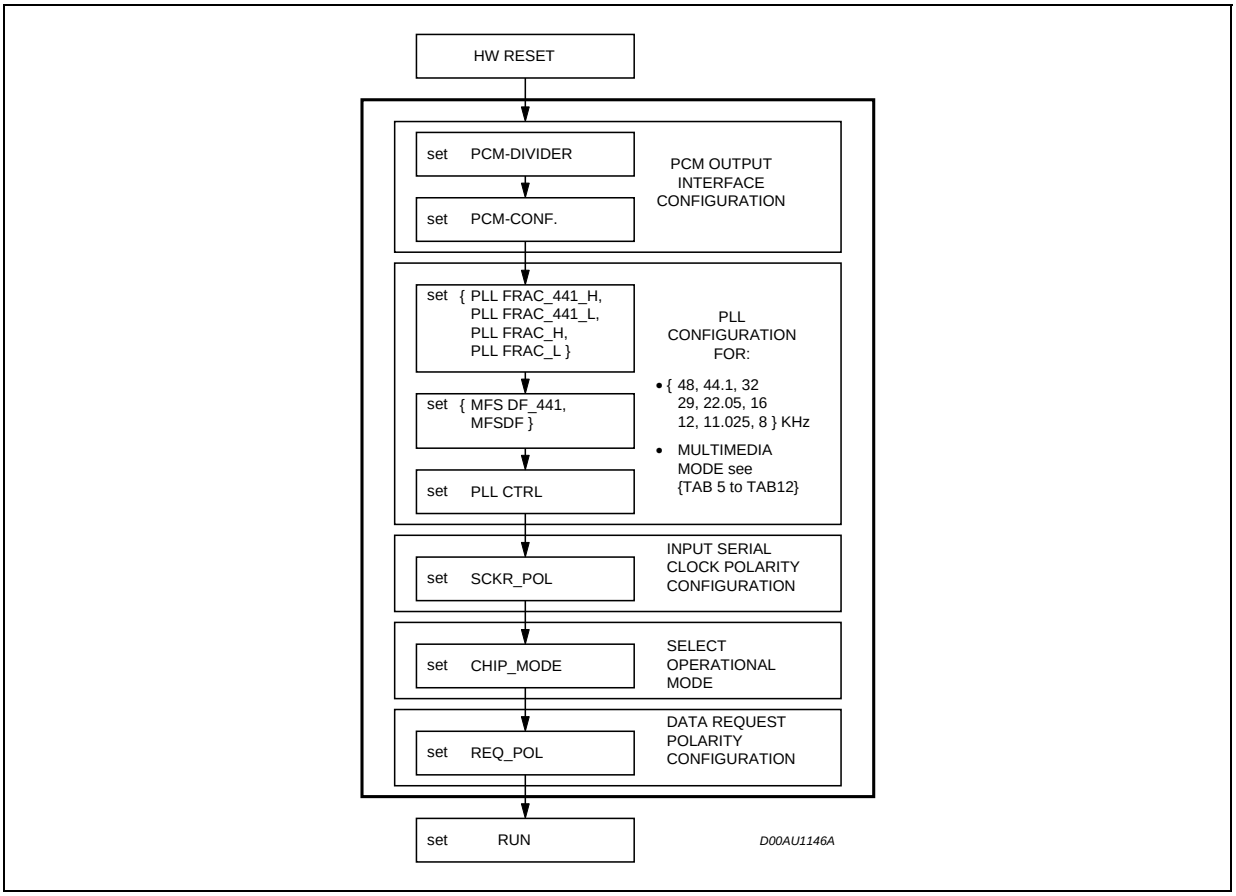


Table 2.

PLL Configuration Sequence For
10MHz Input Clock
256 Oversapling Clock

REGISTER ADDRESS	NAME	VALUE
6	reserved	18
11	reserved	3
97	MFSDF (x)	15
80	MFSDF-441	16
101	PLLFRAC-H	169
82	PLLFRAC-441-H	49
100	PLLFRAC-L	42
81	PLLFRAC-441-L	60
5	PLLCTRL	161

Table 3.

PLL Configuration Sequence For
10MHz Input Clock
384 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	17
11	reserved	3
97	MFSDF (x)	9
80	MFSDF-441	10
101	PLLFRAC-H	110
82	PLLFRAC-441-H	160
100	PLLFRAC-L	152
81	PLLFRAC-441-L	186
5	PLLCTRL	161

Table 4.

PLL Configuration Sequence For
14.31818MHz Input Clock
256 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	12
11	reserved	3
97	MFSDF (x)	15
80	MFSDF-441	16
101	PLLFRAC-H	187
82	PLLFRAC-441-H	103
100	PLLFRAC-L	58
81	PLLFRAC-441-L	119
5	PLLCTRL	161

Table 5.

PLL Configuration Sequence For
14.31818MHz Input Clock
384 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	11
11	reserved	3
97	MFSDF (x)	6
80	MFSDF-441	7
101	PLLFRAC-H	3
82	PLLFRAC-441-H	157
100	PLLFRAC-L	211
81	PLLFRAC-441-L	157
5	PLLCTRL	161

Table 6.

PLL Configuration Sequence For
14.31818MHz Input Clock
512 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	11
11	reserved	3
97	MFSDF (x)	6
80	MFSDF-441	7
101	PLLFRAC-H	3
82	PLLFRAC-441-H	157
100	PLLFRAC-L	211
81	PLLFRAC-441-L	157
5	PLLCTRL	161

Table 7.

PLL Configuration Sequence For
14.7456MHz Input Clock
256 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	12
11	reserved	3
97	MFSDF (x)	15
80	MFSDF-441	16
101	PLLFRAC-H	85
82	PLLFRAC-441-H	4
100	PLLFRAC-L	85
81	PLLFRAC-441-L	0
5	PLLCTRL	161

Table 8.

PLL Configuration Sequence For
14.7456MHz Input Clock
384 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	10
11	reserved	3
97	MFSDF (x)	8
80	MFSDF-441	9
101	PLLFRAC-H	64
82	PLLFRAC-441-H	124
100	PLLFRAC-L	0
81	PLLFRAC-441-L	0
5	PLLCTRL	161

Table 9.

PLL Configuration Sequence For
14.7456MHz Input Clock
512 Oversapling Rathio

REGISTER ADDRESS	NAME	VALUE
6	reserved	9
11	reserved	2
97	MFSDF (x)	5
80	MFSDF-441	6
101	PLLFRAC-H	0
82	PLLFRAC-441-H	184
100	PLLFRAC-L	0
81	PLLFRAC-441-L	0
5	PLLCTRL	161

6.5 STA015 CONFIGURATION FILE FORMAT

The STA015 Configuration File is an ASCII format. An example of the file format is the following:

58 1

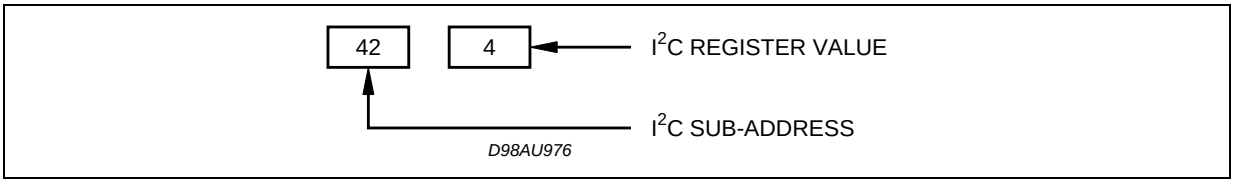
42 4

128 15

.....

It is a sequence of rows and each one can be interpreted as an I^2C command. The first part of the row is the I^2C address (register) and the second one is the I^2C data (value). To download the STA015 configuration file into the device, a sequence of write operation to STA015 I^2C interface must be performed.

The following program describes the I^2C routine to be implemented for the configuration driver:



STA015 Configuration Code (pseudo code)

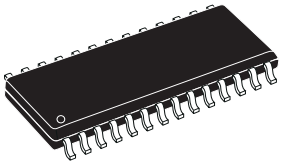
```
download cfg - file
{
fopen (cfg_file);
fp:=1;                          /*set file pointer to first row */
do {
    I2C_start_cond;             /* generate I2C start condition for STA015 device address  */
    I2C_write_dev_addr;         /* write STA015 device address                             */
    I2C_write_subaddress (fp);  /* write subaddress                                        */
    I2C_write_data (fp);        /* write data                                              */
    I2C_stop_cond;              /* generate I2C stop condition                             */
    fp++;                       /* update pointer to new file row                          */
    }
while (!EDF)                    /* repeat until End of File                                */
}                               /* End routine                                             */
```

Note: 1. STA015 is a device based on an integrated DSP core. Some of the I^2C registers default values are loaded after an internal DSP boot operation. The bootstrap time is 60 micro second. Only after this time lenght, the data in the register can be considered stable .

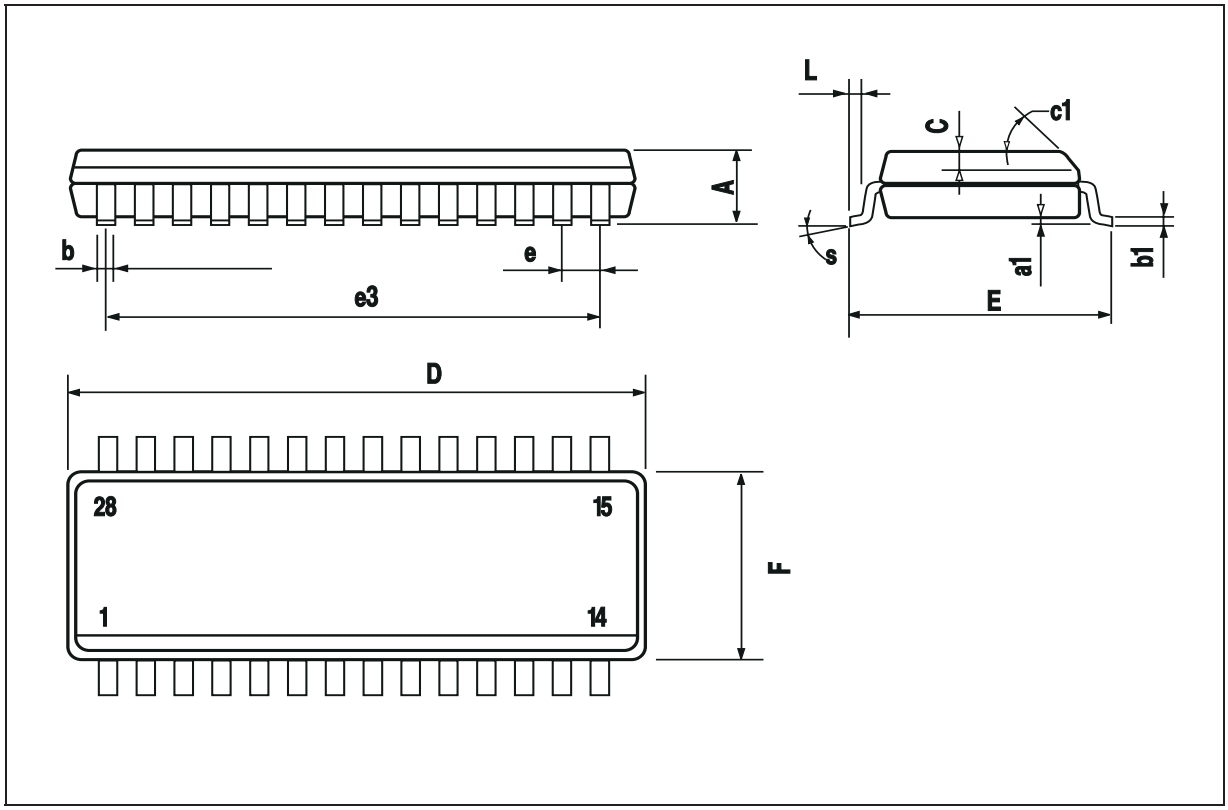
2. Refer also to the application note AN1250

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA

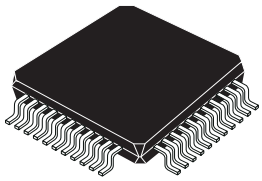


SO28

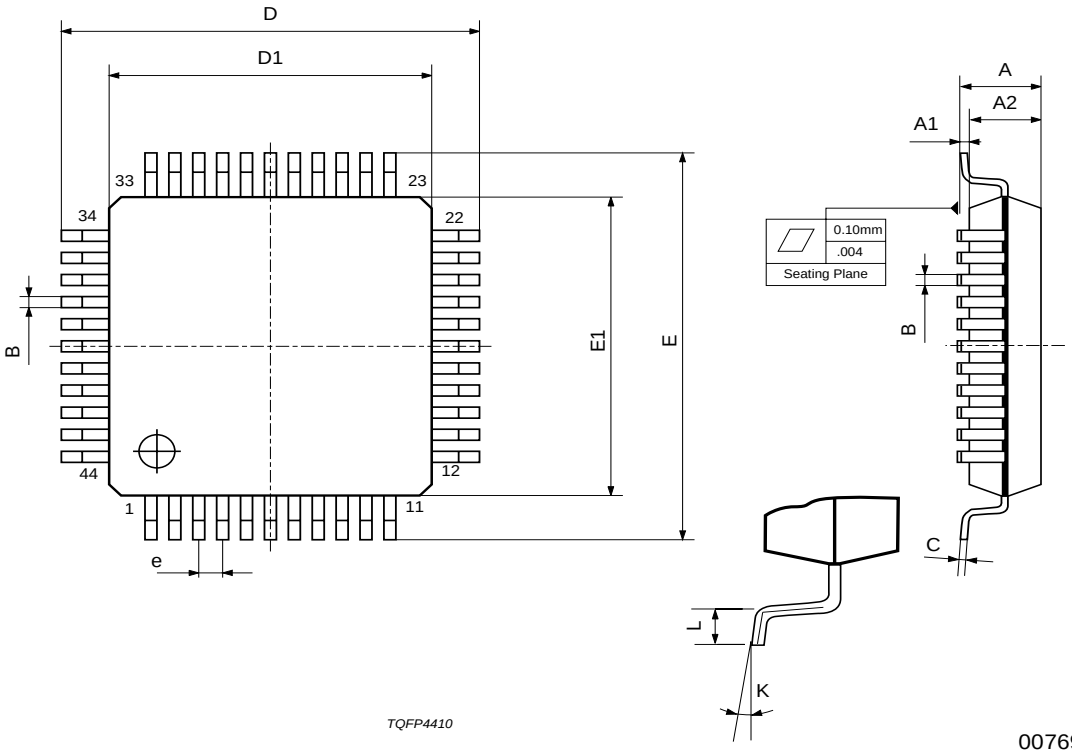


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA

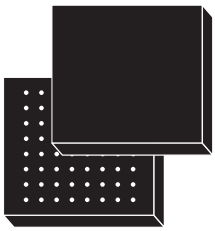


TQFP44 (10 x 10 x 1.4mm)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.700			0.067
A1	0.350	0.400	0.450	0.014	0.016	0.018
A2		1.100			0.043	
b		0.500			0.20	
D		8.000			0.315	
D1		5.600			0.220	
e		0.800			0.031	
E		8.000			0.315	
E1		5.600			0.220	
f		1.200			0.047	

OUTLINE AND MECHANICAL DATA



Body: 8 x 8 x 1.7mm

LFBGA64