

HWCAT**CSC1004**

1. General Description

The CSC1004 is a timing controller IC to control AV type TFT LCD modules, which built in horizontal frequency driver and phase comparator circuit for PLL circuit.

Also this IC can support external clock mode that it doesn't need PLL circuit.

This IC generates all kind of control timing signals to the LCD source drivers and gate drivers.

This IC provides 16:9 aspect ratio TFT LCD modules and it also provides different display mode.

2. Features

- Support multiple resolution mode
- Support Standard NTSC/PAL video system
- Line Inversion Driving method
- Provide timing scan for Left/Right and Up/Down shift control
- Support 3 shift clock
- Provide multi display mode (960*234, 1200*234, 1440*234 mode, 1920*234 mode)
- Support composite sync input mode and separate sync input mode
- Support external clock input mode (960*234, 1200*234, 1440*234, 1920*234 mode)
- 64 pin QFP (0.5mm pitch)
- Dual power supplies: +5.0v/+3.3v
- 0.35u CMOS process, 3.3V for core and 3.3V/5V for IO PAD

3. Pin assignment

pin No.	pin	I/O	Remark	pin No.	pin	I/O	Remark
1	ivsync	I	schimtt	33	ires1	I	pull_down
2	iviy	I	schimtt	34	iz_sel	I	Pull_down
3	ifrst	I	schimtt	35	itst1	I	AC/DC test
4	icsy	I	schimtt	36	ooe3	O	3mA
5	icomps	I	pull_up	37	ooe2	O	3mA
6	ickc	I	pull_up	38	ooe1	O	3mA
7	iomclk	I/O	Bi dir.(3mA)	39	VSS		
8	opsi	O	3mA	40	ostv2	O	3_state(1mA)
9	opsc	O	3mA	41	ostv1	O	3_state(1mA)
10	opols	O	3mA	42	ocpv	O	3mA
11	opolc	O	3mA	43	HVDD		5.0V/3.3V
12	oblk	O	3mA	44	iosci	I	xin (25Mhz)
13	onpo	O	3mA	45	oosco	O	xout(25Mhz)
14	iohsy	I/O	Bi dir.(3mA)	46	VSS		
15	iovsy	I/O	Bi dir(3mA).	47	opda	O	3_state(3mA)
16	HVDD		5.0V/3.3V	48	osrst	O	1mA
17	imode1	I	pull_down	49	ocph1	O	6mA
18	imode2	I	pull_down	50	ocph2	O	6mA
19	imode3	I	pull_down	51	ocph3	O	6mA
20	ivpos1	I	pull_up	52	osth1	O	3_state(3mA)
21	ivpos2	I	pull_up	53	osth2	O	3_state(3mA)
22	VSS			54	og2h	O	3mA
23	ihpos1	I	pull_up	55	LVDD		3.3V
24	ihpos2	I	pull_up	56	ooeh	O	3mA
25	iarea_sel	I	pull_up	57	ocpo	O	3mA
26	iimode	I	pull_up	58	VSS		
27	icpo_sel	I	pull_up	59	icpi	I	
28	icph_sel	I	pull_up	60	iq2h_sel	I	pull_up
29	iodd_sel	I	pull_up	61	ioeh_sel	I	pull_up
30	LVDD		3.3V	62	ilnr	I	pull_up
31	ires3	I	pull_down	63	iund	I	pull_up
32	ires2	I	pull_down	64	innp	I	pull_up

4. Pin Description

No.	Symbol	I/O	Description	Remark																																		
1	ivsync	I	vertical sync signal in composite sync mode (low active)																																			
2	iviy	I	vertical sync signal in separate sync mode(low active)																																			
3	ifrst	I	reset pin in ASIC 1) ifrst = "H" : Normal state 2) ifrst = "L" : Reset state																																			
4	icsy	I	select composite signal/horizontal signal 1) icomps = "H" : icsy is composite sync signal (high active) 2) icomps = "L" : icsy is horizontal sync signal(low active)																																			
5	icomps	I	select composite sync mode/separate sync mode 1) icomps = "H" : composite sync mode 2) icomps = "L" : separate sync mode	Note1)																																		
6	iclkc	I	select PLL mode/external clock mode 1) iclkc = "H" : PLL mode 2) iclkc = "L" : external clock mode	Note1)																																		
7	iomclk	I/O	input clock signal (external clock mode) 1) iclkc = "H" : This signal will be ground 2) iclkc = "L" : This signal will be external input terminal																																			
8	opsl	O	control decoder chip pin																																			
9	opsc	O	control DC-DC chip pin																																			
10	opols	O	polarity alternating signal for video																																			
11	opolc	O	polarity alternating signal for Vcom																																			
12	oblk	O	blanking control pin 1) oblk = "H" : blanking display (black) 2) oblk = "L" : normal display																																			
13	onpo	O	auto detect pin for NTSC/PAL 1) onpo = "H" : NTSC 2) onpo = "L" : PAL	Note2)																																		
14	iohsy	I/O	input/output horizontal sync. signal (low active) 1) iclkc = "H" : This signal outputs horizontal sync. signal 2) iclkc = "L" : This signal will be external horizontal sync. Input.																																			
15	iovsy	I/O	input/output vertical sync. signal (low active) 1) iclkc = "H" : This signal outputs vertical sync. signal 2) iclkc = "L" : This signal will be external vertical sync. Input.																																			
16	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)																																		
17	imode1	I	select display mode (1920,1440, 1200, 960 mode only)	Note4)																																		
18	imode2	I																																				
19	imode3	I																																				
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>imode1</th> <th>imode2</th> <th>imode3</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>Full mode</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>Normal center mode</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>Normal wide mode</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>Zoom1 mode</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>Zoom2 mode</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>Normal left mode</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>Normal right mode</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>Zoom3 mode</td> </tr> </tbody> </table>					imode1	imode2	imode3	Description	L	L	L	Full mode	H	L	L	Normal center mode	L	H	L	Normal wide mode	H	H	L	Zoom1 mode	L	L	H	Zoom2 mode	H	L	H	Normal left mode	L	H	H	Normal right mode	H	H
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L	H	H	Normal right mode																																			
H	H	H	Zoom3 mode																																			

No.	Symbol	I/O	Description	Remark																																				
20	ivpos1	I	select vertical start line <table border="1"> <thead> <tr> <th>ivpos2</th> <th>ivpos1</th> <th>NTSC</th> <th>PAL</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>20</td> <td>26</td> </tr> <tr> <td>L</td> <td>H</td> <td>21</td> <td>28</td> </tr> <tr> <td>H</td> <td>L</td> <td>22</td> <td>30</td> </tr> <tr> <td>H</td> <td>H</td> <td>23</td> <td>31</td> </tr> </tbody> </table>	ivpos2	ivpos1	NTSC	PAL	L	L	20	26	L	H	21	28	H	L	22	30	H	H	23	31	Note1)																
ivpos2	ivpos1	NTSC		PAL																																				
L	L	20	26																																					
L	H	21	28																																					
H	L	22	30																																					
H	H	23	31																																					
21	ivpos2	I																																						
22	VSS	-	Ground																																					
23	ihpos1	I	select horizontal start point (iclkc = "L" only, ext clock mode) <table border="1"> <thead> <tr> <th>ivpos2</th> <th>ivpos1</th> <th>1440</th> <th>1200</th> <th>960</th> <th>1920</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>100</td> <td>85</td> <td>67</td> <td>134</td> </tr> <tr> <td>L</td> <td>H</td> <td>101</td> <td>86</td> <td>68</td> <td>135</td> </tr> <tr> <td>H</td> <td>L</td> <td>102</td> <td>87</td> <td>69</td> <td>136</td> </tr> <tr> <td>H</td> <td>H</td> <td>103</td> <td>88</td> <td>70</td> <td>137</td> </tr> </tbody> </table>	ivpos2	ivpos1	1440	1200	960	1920	L	L	100	85	67	134	L	H	101	86	68	135	H	L	102	87	69	136	H	H	103	88	70	137	Note1)						
ivpos2	ivpos1	1440		1200	960	1920																																		
L	L	100		85	67	134																																		
L	H	101		86	68	135																																		
H	L	102	87	69	136																																			
H	H	103	88	70	137																																			
24	ihpos2	I		Note5)																																				
25	iarea_sel	I	select display range 1) iarea_sel = "H" : The display range is 50.01us (NTSC) 2) iarea_sel = "L" : The display range is 48.00us (NTSC)	Note1)																																				
26	iimode	I	select simultaneous mode/sequential mode 1) iimode = "H" : simultaneous mode (stripe arrangement) 2) iimode = "L" : sequential mode (delta arrangement)	Note1)																																				
27	icpo_sel	I	select horizontal position adjust (iclkc = "H" only) 1) icpo_sel = "H" : hor. Position adjustment is normal 2) icpo_sel = "L" : hor. position adjustment is more wide	Note1)																																				
28	icph_sel	I	select ocph1,2,3 phase (delta arrangement module only) 1) icph_sel = "H" : PVI's arrangement 2) icph_sel = "L" : another company's arrangement	Note1) Note6)																																				
29	iodd_sel	I	select falling edge of iovsy's position (NTSC, composite sync only) 1) iodd_sel = "H" : iovsy's phase difference is 1.5H (even field) 2) iodd_sel = "L" : iovsy's phase difference is 0.5H (even field)	Note1)																																				
30	LVDD	-	low voltage power (3.3V only)																																					
31	ires3	I	select resolution mode <table border="1"> <thead> <tr> <th>ires1</th> <th>ires2</th> <th>ires3</th> <th>resolution mode</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>1200 * 234</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>-</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>1920 * 234</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>240 * 234</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>480 * 234</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>960 * 234 (S)</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>960 * 234 (D)</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>1440 * 234</td> </tr> </tbody> </table>	ires1	ires2	ires3	resolution mode	L	L	L	1200 * 234	H	L	L	-	L	H	L	1920 * 234	H	H	L	240 * 234	L	L	H	480 * 234	H	L	H	960 * 234 (S)	L	H	H	960 * 234 (D)	H	H	H	1440 * 234	Note4)
ires1	ires2	ires3		resolution mode																																				
L	L	L		1200 * 234																																				
H	L	L		-																																				
L	H	L	1920 * 234																																					
H	H	L	240 * 234																																					
L	L	H	480 * 234																																					
H	L	H	960 * 234 (S)																																					
L	H	H	960 * 234 (D)																																					
H	H	H	1440 * 234																																					
32	ires2	I																																						
33	ires1	I																																						
34	iz_sel	I	select falling edge of iovsy's position (PAL mode only) 1) iz_sel = "H" : iovsy's phase difference is 0.5H (even field) 2) iz_sel = "L" : iovsy's phase difference is 1.5H (even field)	Note4)																																				

No.	Symbol	I/O	Description	Remark
35	istt1	I	select AC/DC test 1) istt1 = "H" : AC/DC test mode 2) istt1 = "L" : normal mode	
36	ooe3	O	output enable control signal for gate driver	note7)
37	ooe2	O	ooe1,2,3 = "H" : gate output => Vee	
38	ooe1	O	1) ooe1 controls 1 4 7 10 --- 238 lines 2) ooe2 controls 2 5 8 11 --- 239 lines 3) ooe3 controls 3 6 9 12 --- 240 lines	
39	VSS	-	Ground	
40	ostv2	O	gate driver start pulse 1) iund = "H" : ostv2 is in high impedance state 2) iund = "L" : ostv2 is output pin of start pulse	note7)
41	ostv1	O	gate driver start pulse 1) iund = "H" : ostv1 is output pin of start pulse 2) iund = "L" : ostv1 is in high impedance state	note7)
42	ocpv	O	gate driver shift clock	
43	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)
44	iosci	I	input for clock oscillator circuit	
45	oosco	O	output for clock oscillator circuit	
46	VSS	-	Ground	
47	opda	O	output for phase comparative signal for PLL circuit	
48	osrst	O	reset source driver IC (active high)	
49	ocph1	O	source driver shift clock #1	
50	ocph2	O	source driver shift clock #2 1) iimode = "H" : ocph2 is always high signal (stripe arrangement) 2) iimode = "L" : ocph2 is shift clock (delta arrangement)	
51	ocph3	O	source driver shift clock #3 1) iimode = "H" : ocph3 is always low signal (stripe arrangement) 2) iimode = "L" : ocph3 is shift clock (delta arrangement)	
52	osth1	O	source driver start pulse 1) ilnr = "H" : osth1 is output pin of start pulse 2) ilnr = "L" : osth1 is in high impedance state	Note8)
53	osth2	O	source driver start pulse 1) ilnr = "H" : osth2 is in high impedance state 2) ilnr = "L" : osth2 is output pin of start pulse	Note8)
54	oq2h	O	pin of RGB output data order on no rotation mode 1) iimode = "H" : no use (low) 2) iimode = "L" : use (delta arrangement)	
55	LVDD	-	low voltage power (3.3V only)	
56	ooeh	O	output enable control signal for source driver 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	
57	ocpo	O	output for horizontal position adjustment	
58	VSS	-	Ground	
59	icpi	I	input for horizontal position adjustment	

No.	Symbol	I/O	Description	Remark
60	iq2h_sel	I	select oe's control in zoom mode 1) iq2h_sel = "H" : 3 oe (oe1,oe2,oe3) control 2) iq2h_sel = "L" : 1 oe control	Note1) note6)
61	ioeh_sel	I	select perioty of ooeh 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	Note1)
62	ilnr	I	select left/right direction 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1) Note8)
63	iund	I	select up/down direction 1) iund = "H" : normal scan 2) iund = "L" : reverse scan	Note1) Note7)
64	innp	I	select NTSC/PAL 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1)

Note1) Those pins are Normally pull-up

Note2) If use auto detection, this pin must connect innp

Note3) If you want to use 5V's I/O signal, It must connect 5V's Voltage,
otherwise, if you want to use 3.3V's I/O signal, it must connect 3.3V's voltage

Note4) Those pins are Normally pull-down

Note5) This count means No.of input clock from the falling edge of iohsy

Note6) If you use another company's TFT LCD module, please contact PVI.

Note7) iund controls up/down direction

1) iund = "H" : ostv1 → G1(oe1) → G2(oe2) → G3(oe3) → G4(oe1) →
G5(oe1) → — → G238(oe1) → G239(oe2) → G240(oe3)
→ ostv2

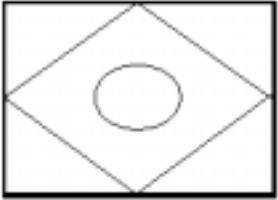
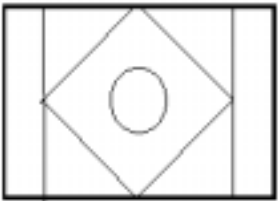
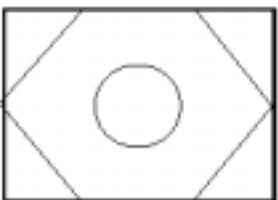
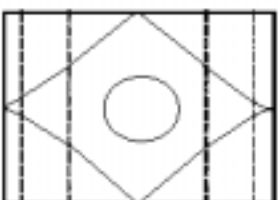

2) iund = "L" : ostv1 ← G1(oe1) ← G2(oe2) ← G3(oe3) ← G4(oe1) ←
G5(oe1) ← — ← G238(oe1) ← G239(oe2) ← G240(oe3)
← ostv2

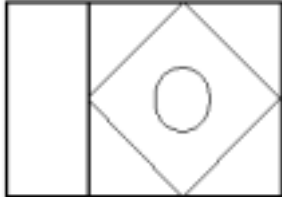
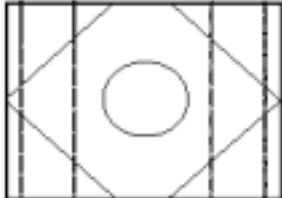
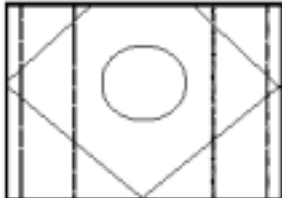
Note8) ilnr controls left/right direction

1) ilnr = "H" : osth1 → ---- → osth2

2) ilnr = "L" : osth1 ← ---- ← osth2

5. Display mode (1200, 1440, 1920, 960 mode only)

Display mode	Display characteristics (4:3 aspect-ratio input)	imd 1	imd 2	imd 3	Note
Full		Lo	Lo	Lo	Input video signals are displayed in full screen (To display 4:3 signal on 16:9 screen)
Normal Center		Hi	Lo	Lo	Input video signals are displayed in the center screen (4:3 aspect ratio)
Zoom 1		Hi	Hi	Lo	Input video signal of central 176 lines are displayed in full screen (Vertically extension)
Wide		Lo	Hi	Lo	Input video signals are displayed in full screen (Horizontal modification)
Normal Left		Hi	Lo	Hi	Input video signals are displayed in the left screen (4:3 aspect ratio)

Display mode	Display characteristics (4:3 aspect-ratio input)	in d 1	in d 2	in d 3	Note
Normal Right		Lo	Hi	Hi	Input video signals are displayed in the right screen (4:3 aspect ratio)
Zoom 2		Lo	Lo	Hi	Input video signal of central 204 lines are displayed in full screen (Vertically extension and horizon. Modifi.)
Zoom 3		Hi	Hi	Hi	Same as Zoom 2 mode. Vertically offset centered

6. Electrical Characteristics**6.1 Absolute Maximum Ratings**

Parameter	Symbol	Rating	Units
Power supply voltage	HVDD	-0.3 to 7.0	V
	LVDD	-0.3 to 4.0	V
Input voltage	V _I	-0.3 to HVDD+0.5	V
Output voltage	V _{OUT}	-0.3 to HVDD+0.5	V
Storage temperature	T _{stg}	-65 to 150	°C

6.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	HVDD 1	4.5	5.0	5.5	V
	HVDD 2	3.0	3.3	3.6	V
	LVDD	3.0	3.3	3.6	V
Input voltage	V _I	VSS	0	HVDD	V
Operating temperature	T _{opr}	-40	-	85	°C

6.3 General DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Remark
Input low current	I _L	V _I = 0 V	-1	-	1	µA	
Input high current	I _H	V _I = HVDD	-1	-	1	µA	
Tristate leakage current	I _Z		-10	-	10	µA	
Logic input low voltage	V _{IL}	HVDD=MIN	-	-	1.0	V	
Schmitt input low voltage	V _{SL}	HVDD=MIN	0.8	-	3.1	V	
Logic input high voltage	V _{IH}	HVDD=MAX	3.5	-	-	V	
Schmitt input high voltage	V _{SH}	HVDD=MAX	2.0	-	4.0	V	
Output low voltage	V _{OL}	HVDD=MIN	HVDD-0.4	-	-	V	
Output high voltage	V _{OH}	HVDD=MIN	-	-	VDD+0.4	V	
Input pullup/down resistor	R _I	V _L = 0V or V _H = HVDD	-	60	-	Ω	

6.4 Current consumption

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Remark
Current consumption	I _B	HVDD=3.3V	-	8.5	15	mA	

7. Timing conditions

7-1) 1200 * 234 mode (6.5")

a. Input signal characteristics

Paramet	Symbo	Min.	Typ.	Max.	Unit	Remar
iosci	t _{OSC}	81	83	85	ns	
icsy	T _H	61.	63.	65.	us	
icsy pulse	t _{CSYN}	4	4.7	5.4	us	
icsy rising	T _r	-	-	700	ns	
icsy falling	T _f	-	-	300	ns	
ivsync pulse	t _{VS}	1	3	5	t _i	
ivsync rising	T _r	-	-	700	ns	
ivsync falling	T _f	-	-	1.5	us	
Horizontal lines per		256	262.	268	line	Note

Note 1 : Please don't use odd horizontal lines to drive LCD panel for both simult

b. Output signal characteristics

Paramet	Symbo	Min.	Typ.	Max.	Unit	Remar
rising	t _r	-	-	10	ns	
falling	t _f	-	-	10	ns	
clock pulse	t _{CPH}	-	1.5	-	t _{OSC}	
clock pulse	t _{CPH}	30	33(67)	70	%	
osth setup	t _{STH}	-	t _{CPH} /2	-	ns	
osth pulse	t _{STH}	-	1	-	t _{CPH}	
iohsy pulse	t _{HSY}	-	4.6	-	us	
ooeh pulse	t _{OEH}	-	2.8	-	us	
sample & hold disable	t _{DS1}	-	5.5	-	us	
ooe1(2)(3) pulse	t _{OEV}	-	16	-	us	
ocpv pulse	t _{CPV}	-	t _i /2	-	us	
ocpo - ooe1 time	t _i	-	7.4	-	us	
ocpv - opda time	t _i	-	6.1	-	us	
ooe1 - opda time	t _i	-	14.2	-	us	
ocpo - opda time	t _i	-	7.7	-	us	
iohsy - oosi time	t _i	-	4.8	-	us	
opsi pulse	t _{OPW}	-	4.6	-	us	
ostv1(2) setup	t _{STV}	-	t _i /2	-	us	
ostv1(2) pulse	t _{STV}	-	1	-	t _i	
iovsy - ostv1(2) time	t _{VS(2)}	-	18(27)	-	t _i	Note1

Note1) Values in brackets correspond to

7-2) 1440 * 234 mode (6.2",7", 8.4")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
oscl period	t _{osc}	64.5	69.5	74.5	ns	
icsy period	T _H	61.5	63.5	65.5	us	
icsy pulse width	t _{csyn}	4	4.7	5.4	us	
icsy rising time	T _r	-	-	700	ns	
icsy falling time	T _f	-	-	300	ns	
vsync pulse width	t _{vsy}	1	3	5	t _H	
vsync rising time	T _r	-	-	700	ns	
vsync falling time	T _f	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t _r	-	-	10	ns	
falling time	t _f	-	-	10	ns	
clock pulse width	t _{CPH}	-	1.5	-	t _{osc}	
clock pulse duty	t _{CPH}	30	33(67)	70	%	
osth setup time	t _{stH}	-	t _{CPH} /2	-	ns	
osth pulse width	t _{stH}	-	1	-	t _{CPH}	
lohsy pulse width	t _{loSY}	-	4.65	-	us	
ooeh pulse width	t _{oeh}	-	3.46	-	us	
sample & hold disable time	t _{sd1}	-	5.52	-	us	
ooe1(2)(3) pulse width	t _{oeV}	-	16	-	us	
ocpv pulse width	t _{cpV}	-	t/2	-	us	
ocpo - ooeh time diff.	t _t	-	-2.8	-	us	
ocpv - opda time diff.	t _t	-	8.56	-	us	
ooe1 - opda time diff.	t _t	-	16.64	-	us	
ocpo - opda time diff.	t _t	-	-1.8	-	us	
lohsy - opsi time diff.	t _t	-	4.8	-	us	
opsi pulse width	t _{psw}	-	4.48	-	us	
ostv1(2) setup time	t _{stV}	-	t/2	-	us	
ostv1(2) pulse width	t _{stV}	-	1	-	t _H	
lovsy - ostv1(2) time diff.	t _{vs(12)}	-	18(27)	-	t _H	Note1)

Note1) Values in brackets correspond to PAL mode

7-3) 960 * 234 mode (Stripe mode, 3.6", 4.5", 5", 6.4")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
hosc period	t _{OSC}	100.2	104.2	108.2	ns	
hcsy period	T _H	61.5	63.5	65.5	us	
hcsy pulse width	t _{CSYN}	4	4.7	5.4	us	
hcsy rising time	T _{cr}	-	-	700	ns	
hcsy falling time	T _{cf}	-	-	300	ns	
hvsync pulse width	t _{VS}	1	3	5	t _H	
hvsync rising time	T _{vr}	-	-	700	ns	
hvsync falling time	T _{vf}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t _r	-	-	10	ns	
falling time	t _f	-	-	10	ns	
clock pulse width	t _{CPH}	-	1.5	-	t _{OSC}	
clock pulse duty	t _{CPW}	30	33(67)	70	%	
osth setup time	t _{SOH}	-	t _{CPH} /2	-	ns	
osth pulse width	t _{STH}	-	1	-	t _{CPH}	
ohsy pulse width	t _{OSY}	-	4.76	-	us	
oeh pulse width	t _{OEH}	-	3.52	-	us	
sample & hold disable tin	t _{SDI}	-	5.82	-	us	
oe1(2)(3) pulse width	t _{OE1}	-	17.2	-	us	
ocpv pulse width	t _{OPV}	-	t ₂	-	us	
ocpo - oeh time diff.	t ₁	-	4.4	-	us	
ocpv - opda time diff.	t ₂	-	8.56	-	us	
oe1 - opda time diff.	t ₃	-	16.6	-	us	
ocpo - opda time diff.	t ₄	-	5.5	-	us	
ohsy - opsi time diff.	t ₅	-	4.88	-	us	
opsi pulse width	t _{OSW}	-	4.8	-	us	
ostv1(2) setup time	t _{SOV}	-	t ₂	-	us	
ostv1(2) pulse width	t _{STV}	-	1	-	t _H	
ovsy - ostv1(2) time diff.	t _{OS1(2)}	-	18(27)	-	t _H	Note1)

Note1) Values in brackets correspond to PAL mode

7-4) 480 * 234 mode (2.5", 3.5")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
hsync period	t_{hs}	100.2	104.2	109.2	ns	
hsync period	T_H	61.5	63.5	65.5	us	
hsync pulse width	t_{HWH}	4	4.7	5.4	us	
hsync rising time	T_{er}	-	-	700	ns	
hsync falling time	T_{ef}	-	-	300	ns	
hsync pulse width	t_{Hw}	1	3	5	us	
hsync rising time	T_{er}	-	-	700	ns	
hsync falling time	T_{ef}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
clock pulse width	t_{clk}	-	3	-	us	
clock pulse duty	t_{clk}	30	33	40	%	
osth setup time	t_{os}	-	$t_{clk}/2$	-	ns	
osth pulse width	t_{os}	-	1	-	us	
bhsy pulse width	t_{bhsy}	-	4.76	-	us	
ooeh pulse width	t_{ooeh}	-	3.52	-	us	
sample & hold disable time	t_{shd}	-	5.82	-	us	
ooel (2) (3) pulse width	t_{ooel}	-	17.2	-	us	
ocpv pulse width	t_{ocpv}	-	$t_r/2$	-	us	
ocpv - ooeh time diff.	t_d	-	4.4	-	us	
ocpv - opda time diff.	t_d	-	8.56	-	us	
ooel - opda time diff.	t_d	-	16.6	-	us	
ocpv - opda time diff.	t_d	-	5.5	-	us	
bhsy - opsi time diff.	t_d	-	4.88	-	us	
opsi pulse width	t_{psi}	-	4.8	-	us	
ostv1 (2) setup time	t_{osv}	-	$t_r/2$	-	us	
ostv1 (2) pulse width	t_{osv}	-	1	-	us	
bvsv - ostv1 (2) time diff.	t_{osv1}	-	18 (27)	-	us	Note1)

Note1) Values in brackets correspond to PAL mode

7-5) 1920 * 234 mode (9")

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	tosc	50.1	52.1	54.1	ns	
icsy period	T _H	61.5	63.5	65.5	us	
icsy pulse width	t _{CSYN}	4	4.7	5.4	us	
icsy rising time	T _r	-	-	700	ns	
icsy falling time	T _f	-	-	300	ns	
ivsync pulse width	t _{IVS}	1	3	5	t _H	
ivsync rising time	T _r	-	-	700	ns	
ivsync falling time	T _f	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t _r	-	-	10	ns	
falling time	t _f	-	-	10	ns	
clock pulse width	t _{CPH}	-	1.5	-	t _{osc}	
clock pulse duty	t _{DWH}	30	33(67)	70	%	
osth setup time	t _{SUH}	-	t _{CPH} /2	-	ns	
osth pulse width	t _{TPH}	-	1	-	t _{CPH}	
iohsy pulse width	t _{HSY}	-	4.6	-	us	
ooeh pulse width	t _{OEH}	-	3.6	-	us	
sample & hold disable time	t _{DIS1}	-	5.26	-	us	
ooe1(2)(3) pulse width	t _{DEV}	-	16	-	us	
ocpv pulse width	t _{CPV}	-	t _r /2	-	us	
ocpv - ooeh time diff.	t ₁	-	4.08	-	us	
ocpv - opda time diff.	t ₂	-	8.72	-	us	
ooe1 - opda time diff.	t ₃	-	16.8	-	us	
ocpv - opda time diff.	t ₄	-	5	-	us	
iohsy - opsi time diff.	t ₅	-	3.3	-	us	
opsi pulse width	t _{PSW}	-	4.64	-	us	
ostv1(2) setup time	t _{SUV}	-	t _r /2	-	us	
ostv1(2) pulse width	t _{STV}	-	1	-	t _H	
iovsy - ostv1(2) time diff.	t _{VS1(2)}	-	18(27)	-	t _H	Note1)

Note1) Values in brackets correspond to PAL mode

7-6) 960 * 234 mode (Delta mode, 3.5")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
hsciperiod	t_{sc}	50.1	52.1	54.1	ns	
hscy period	T_H	61.5	63.5	65.5	us	
hscy pulse width	t_{HWH}	4	4.7	5.4	us	
hscy rising time	T_{cr}	-	-	700	ns	
hscy falling time	T_{cf}	-	-	300	ns	
hsync pulse width	t_{SY}	1	3	5	ts	
hsync rising time	T_{rE}	-	-	700	ns	
hsync falling time	T_{fE}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
cbck pulse width	t_{WH}	-	3	-	tscc	
cbck pulse duty	t_{WH}	30	33 (67)	70	%	
osth setup time	t_{WH}	-	$t_{WH}/2$	-	ns	
osth pulse width	t_{WH}	-	1	-	tswh	
ohsy pulse width	t_{HY}	-	4.6	-	us	
ooeh pulse width	t_{OH}	-	3.6	-	us	
sample & hold disable time	t_{SH}	-	5.26	-	us	
ooel (2) (3) pulse width	t_{HY}	-	16	-	us	
ocpv pulse width	t_{HY}	-	$t_r/2$	-	us	
ocpo - ooeh time diff.	t_r	-	4.08	-	us	
ocpv - opda time diff.	t_r	-	8.72	-	us	
ooel - opda time diff.	t_r	-	16.8	-	us	
ocpo - opda time diff.	t_r	-	5	-	us	
ohsy - opsit time diff.	t_r	-	3.3	-	us	
opsi pulse width	t_{WH}	-	4.64	-	us	
ostvl (2) setup time	t_{HY}	-	$t_r/2$	-	us	
ostvl (2) pulse width	t_{HY}	-	1	-	ts	
ovsy - ostvl (2) time diff.	$t_{SH(2)}$	-	18 (27)	-	ts	Note1)

Note1) Values in brackets correspond to PAL mode

8. Display Position

8-1. Horizontal position

Items	Symbol	Conditions	NTSC	PAL	unit	Remark
Horizontal Start Position	HPOS	-	11.78	11.89	us	*)
Horizontal display Area	HDIS	-	50.01	50.36	us	**)

*) Sampling start based on the csy's rising edge

**) Horizontal display position is changed by delay

8-2. Vertical position

Items	Symbol	Conditions	Display mode					unit	Remark
			Full Normal	Wide	Zoom1	Zoom2	Zoom3		
Vertical Start Position	VPOS	NTSC	Odd	25	25	55	41	56	Line *)
			Even	288	288	318	304	318	
		PAL	Odd	31	31	65	51	68	Line
			Even	343	343	377	363	380	
Vertical display Position	VDIS	NTSC	234	234	176	204	204	Line	
		PAL	273	273	199	234	234	Line	

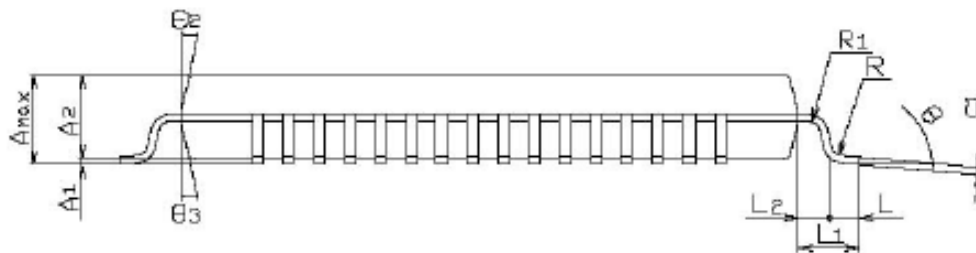
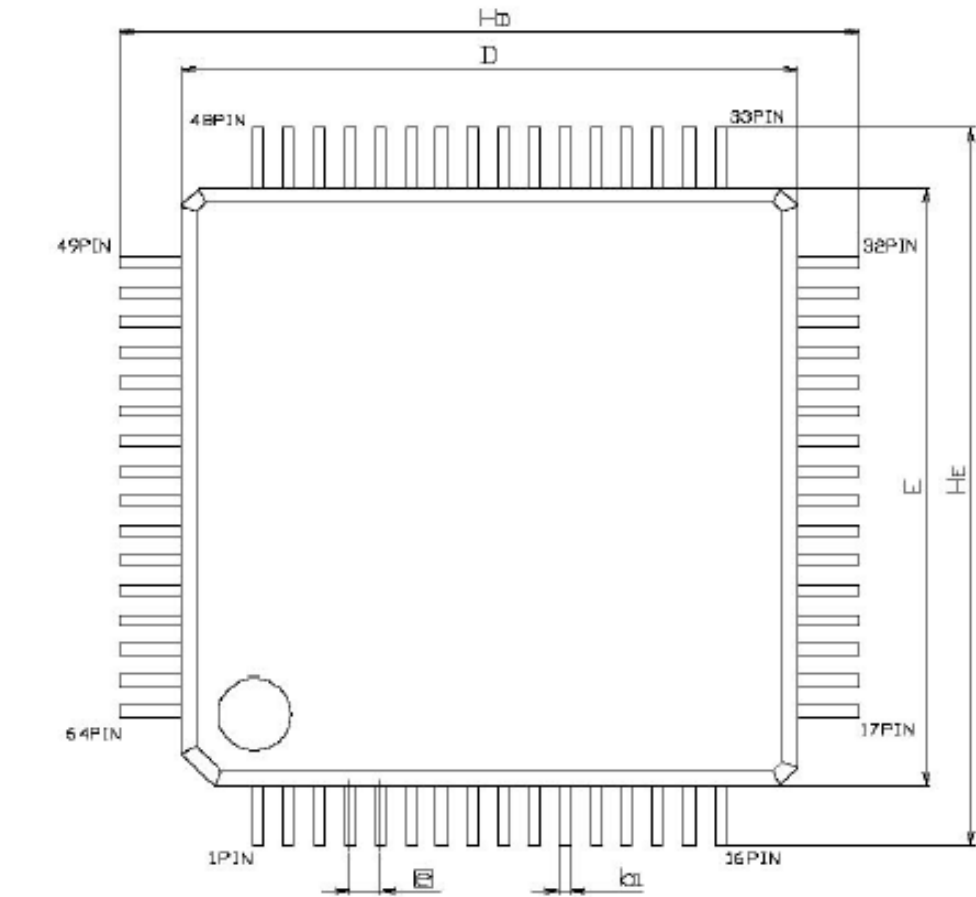
*) Sampling start line number base on Line no

9. Reliability test items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 150 < 240h	
2	Low temperature storage	Ta = -60 < 240h	
3	High temperature operation	Ta = 85 < 240h	
4	Low temperature operation	Ta = -40 < 240h	
5	High temperature and High humidity	Ta = 80 < , 95%RH 240h	operation
6	Heat shock	-30 < , .. < , .. < 200cycle 30min, 5mun, 30min	non- operation
7	Electrostatic discharge	< 200V, 200pF(0?) once for each terminal	non- operation

Note : Ta = Ambient temperature

10. Package information



Symbol	Dimension in Millimeters		
	Min	Nom	Max
* E	9.9	10	10.1
* D	9.9	10	10.1
Amax			1.7
A1		0.1	
A2	1.3	1.4	1.5
B3		0.5	
* k1	0.13	0.18	0.26
* k2	0.1	0.125	0.175
B	0*		10*
L	0.3	0.5	0.7
L1		1	
L2		0.5	
HE	11.6	12	12.4
Hb	11.6	12	12.4
R1		12*	
R		12*	
B		0.2	
L		0.2	

*E,D Excluding the tie bar cutting stub
 k1 Lead width of base metal.
 d Lead thickness of base metal.

A. The timing Diagram

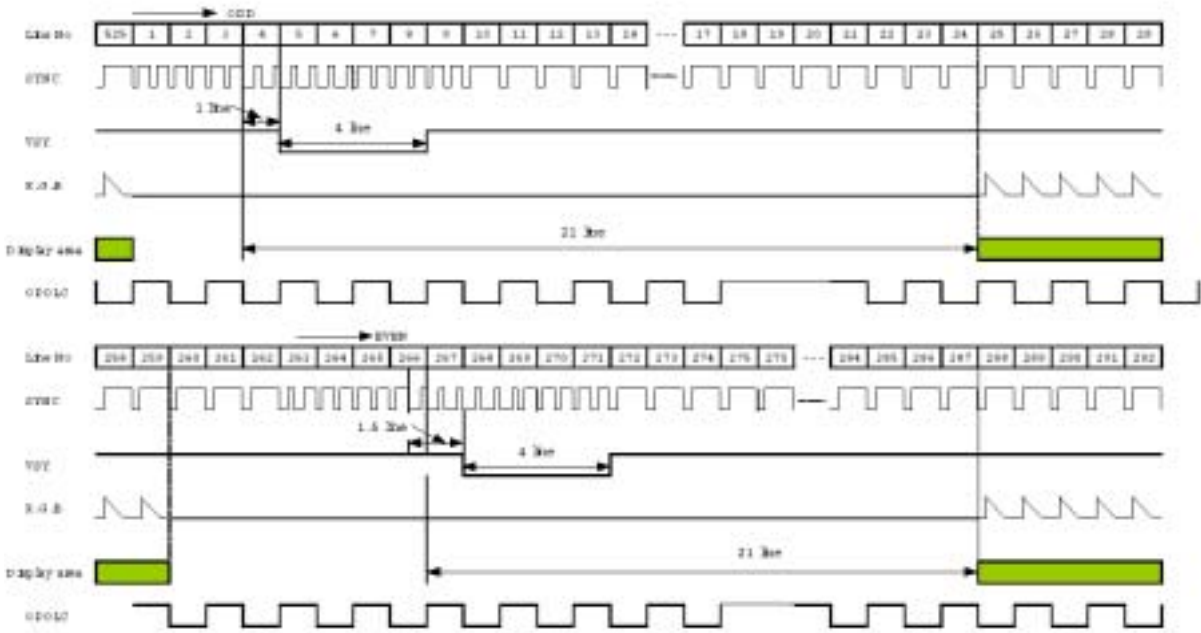


Fig.1. NTSC Vertical(budd_sel= "High")

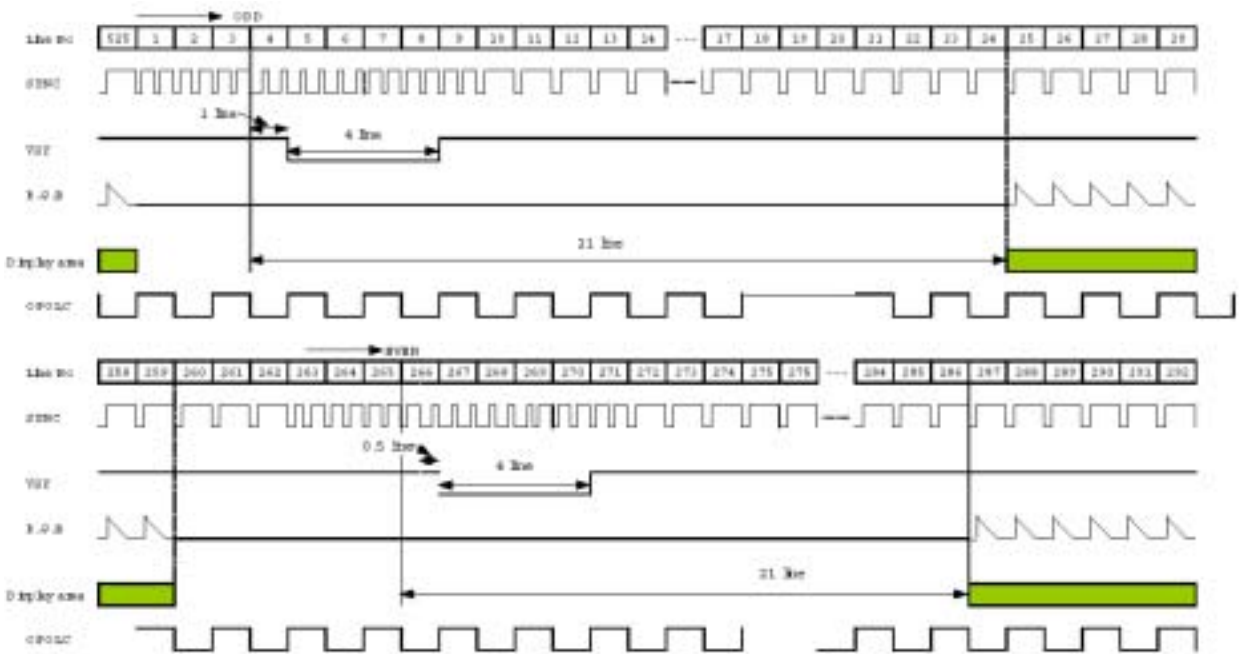


Fig.2. NTSC Vertical(budd_sel= "Low")

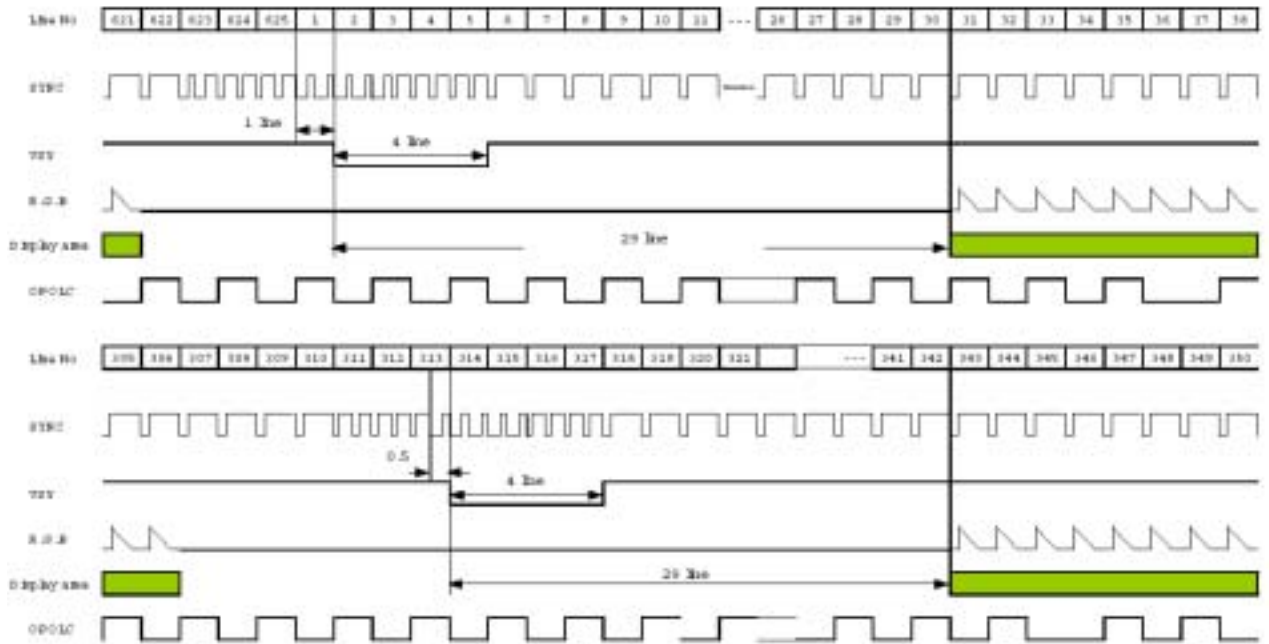


Fig.3. PAL Vertical (M_sel= "H")

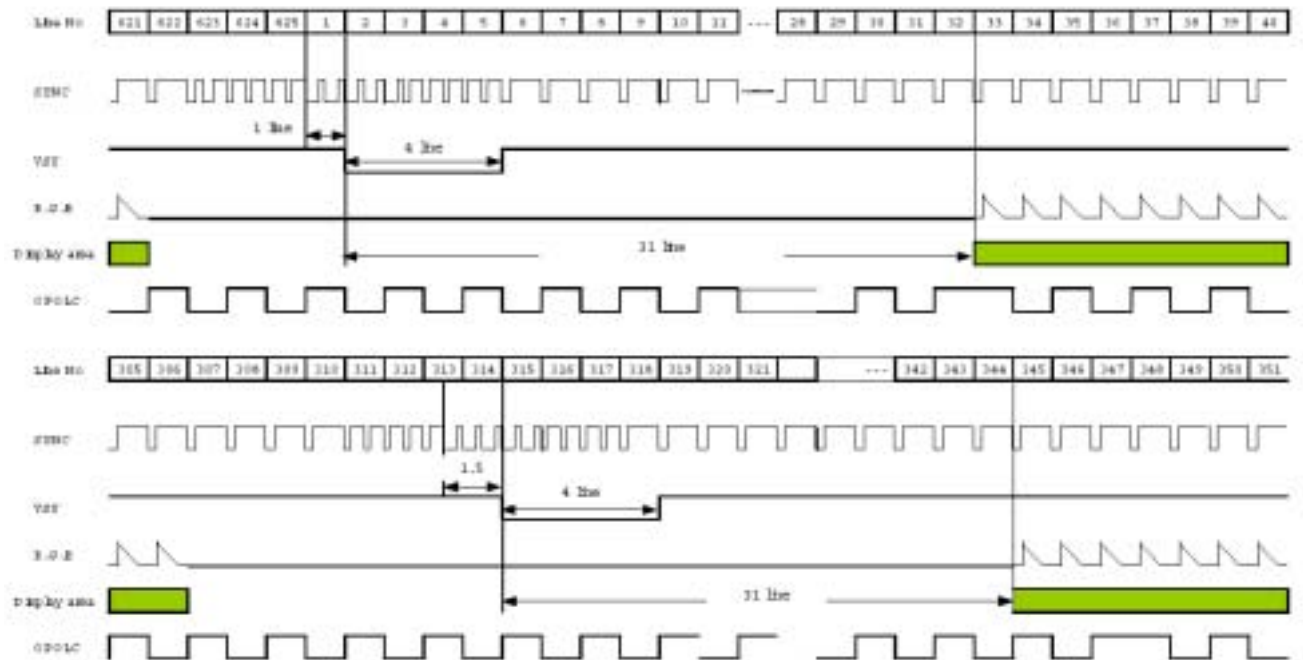
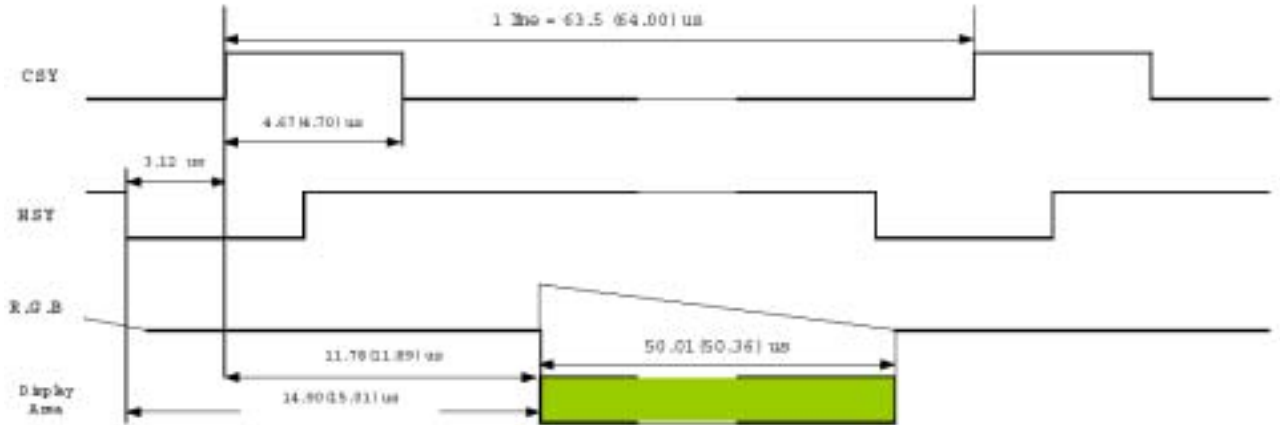


Fig.4. PAL Vertical (M_sel= "L")



- *) Values in brackets correspond to PAL mode
- **) $f_H = 15.734$ (15.625) kHz
- ***) Horizontal display position is changed by delay time (control cp4 cpo)

Fig.5. Horizontal (NTSC/PAL)

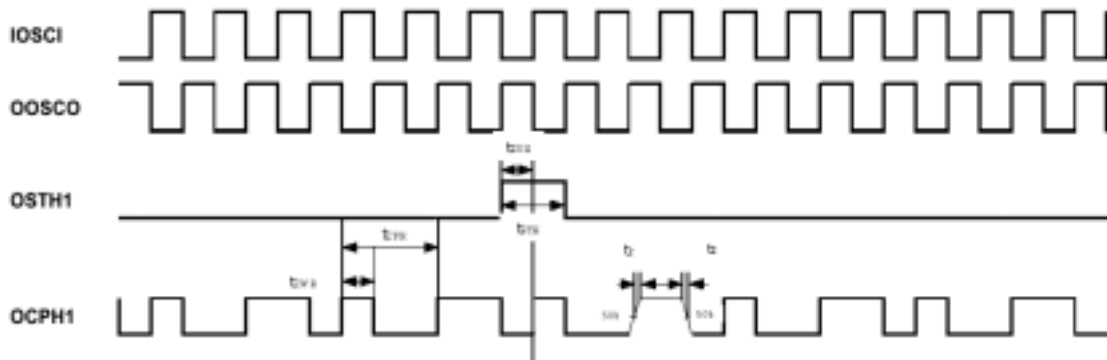


Fig.6 Sampling clock timing (1920,1440,1200,960*234 mode)

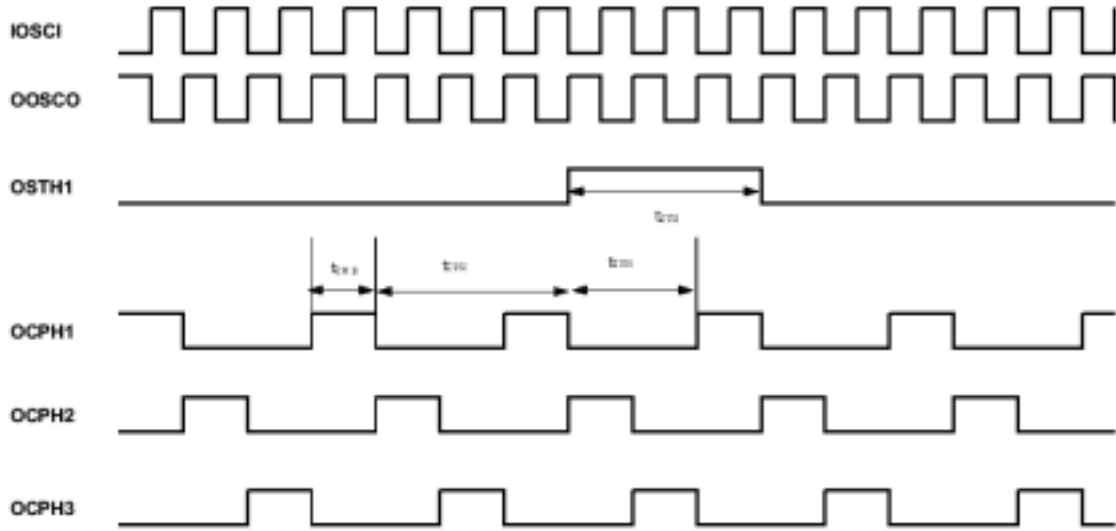


FIG.7 Sampling clock timing (960,480*234mode Delta mode)

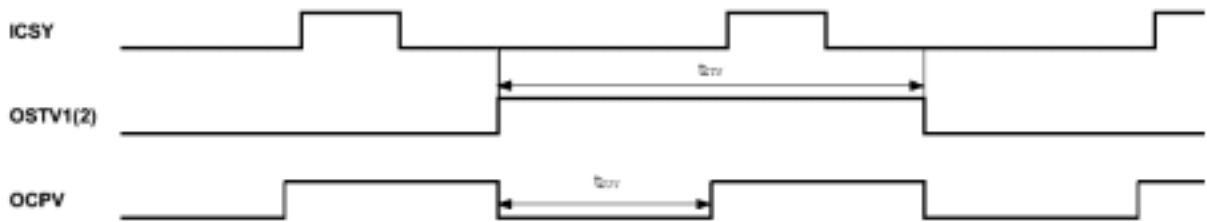


FIG.8 Vertical shift clock timing



FIG.9 Horizontal Timing

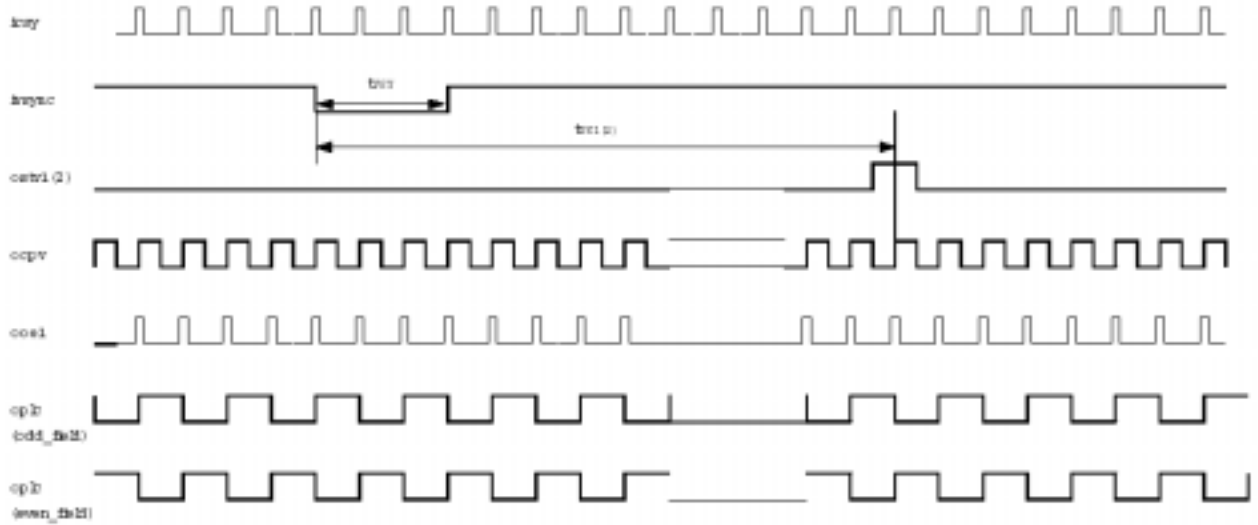


FIG.10 Vertical Timing

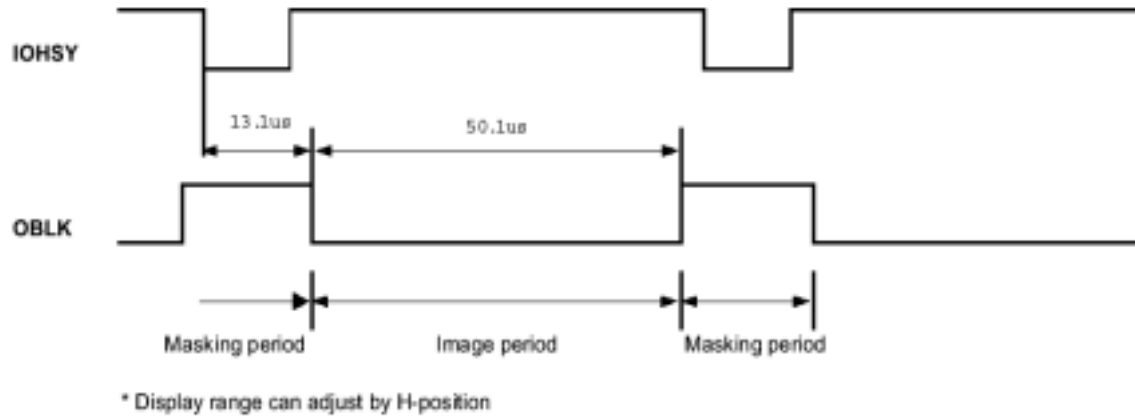


FIG.11 Input/output signal waveforms(Normal center, Normal left, Normal right mode)

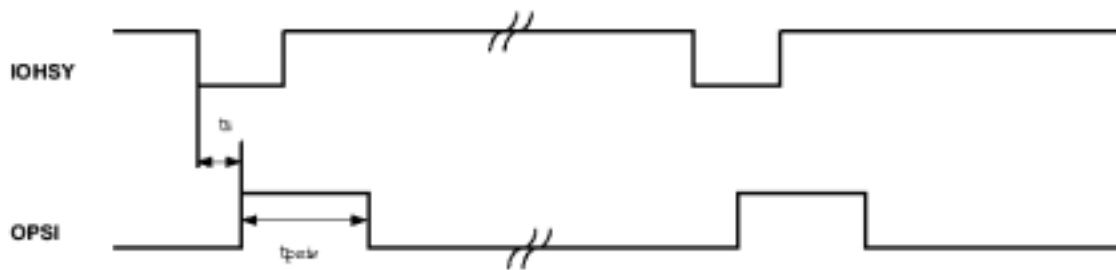
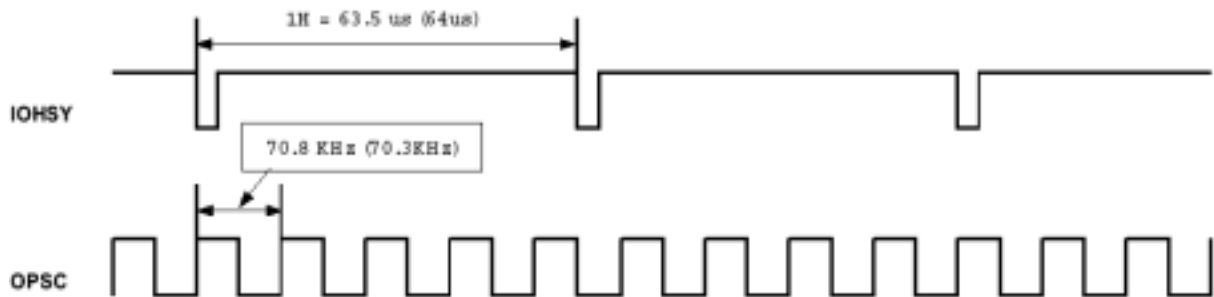


FIG.12 OPSI timing



Note1) Values in brackets correspond to PAL mode

FIG.13 OPSC dimming timing