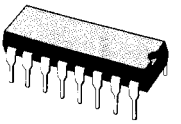
2 x 8 CROSSPOINT MATRIX

- VERY LOW ON RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE ISOLATION
- SERIAL SWITCH ADDRESSING, μ-PROCESSOR COMPATIBLE



(Plastic)
(Ceramic Frit-seal)
(Ceramic Metal-seal)

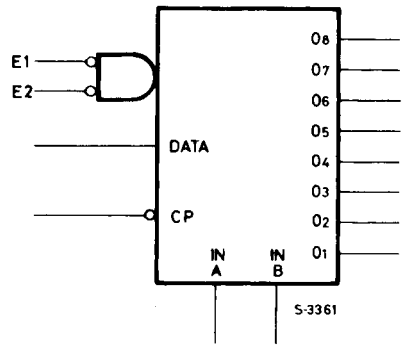
ORDER CODES : M089 B1
M089 F1
M089 D1

DESCRIPTION

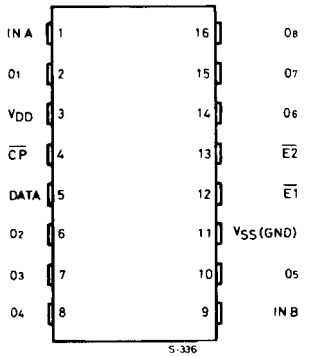
The M089 is a 2 x 8 crosspoint matrix consisting of 16 N-channel MOS transistors.

The device has been specially designed to provide switches with low cross-talk, high off-state isolation (both better than - 90dB) and low on-resistance.

LOGIC DIAGRAM



PIN CONFIGURATION

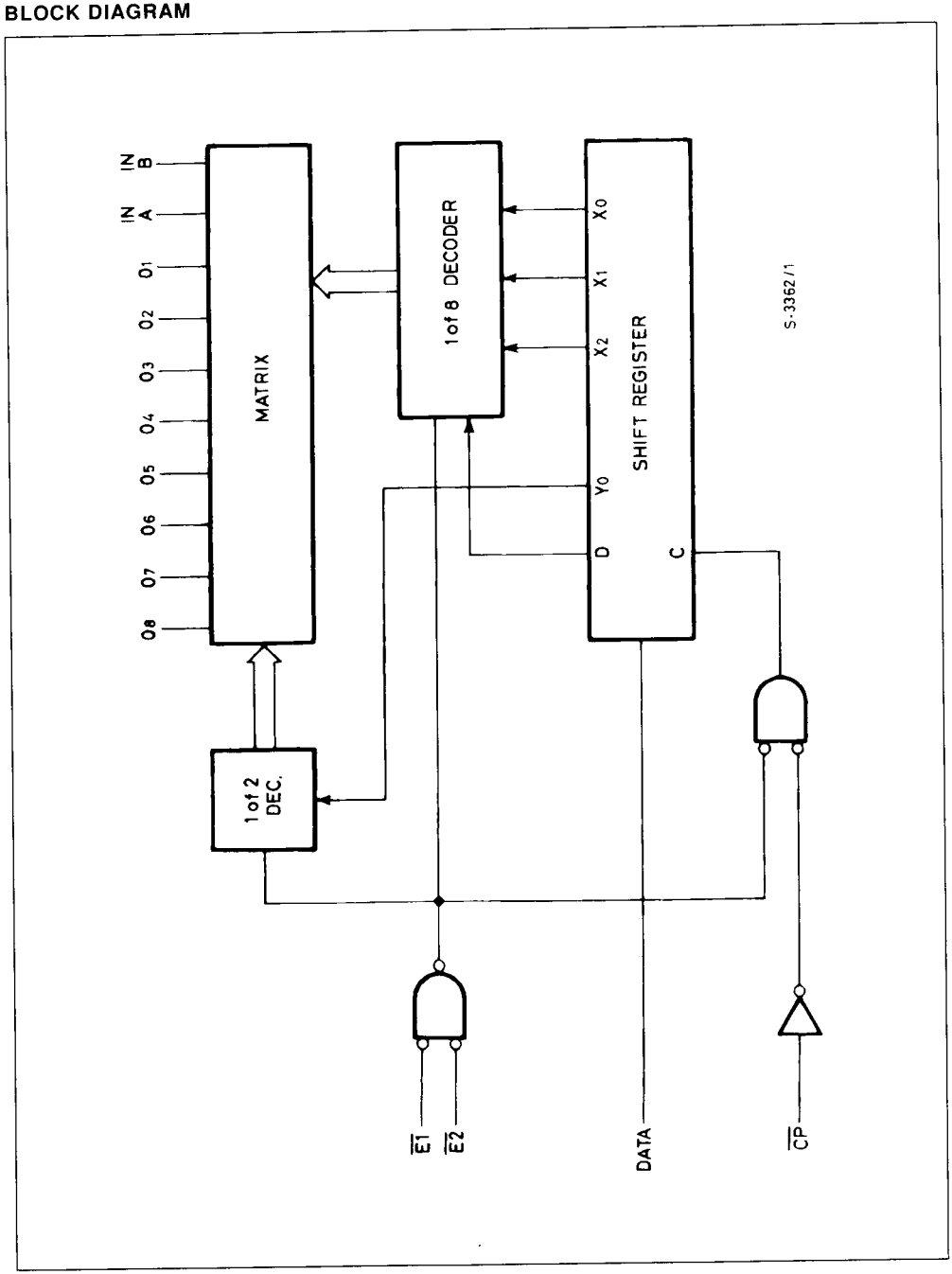


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.5 to 17	V
V_I	Input Voltage Pins 4, 5, 12, 13	– 0.5 to 17	V
V_{IN}-V_{OUT}	Differential Voltage Across any Disconnected Switch	10	V
P_{tot}	Total Power Dissipation	640	mW
T_{op}	Operating Temperature Range : for Plastic for Ceramic	0 to 70 – 40 to 70	°C °C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the opera-tional sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The M089 is capable of forming any combination of switch conditions in an 8 x 2 matrix. Each switch is individually set and a latch maintains it in its set condition.

The switch address and control bits are loaded serially into an internal shift register (5 bits), when inputs E_1, and E_2 are low. The address bits consist of : 3 input selection bits (X_0-X_2) and a single output selection bit (Y_0). A fifth (control) bit (D) defines whether the chosen switch is to be opened or closed.

D	Y_0	X_2	X_1	X_0

M089 Shift Register Bit Allocation

Data bits are clocked into the shift register on the high to low transition of the clock input (CP). If more than 5 clock transmission are applied during loading of the shift register the last 5 data bits are loaded into it. The status of the switch addressed changes on the low to high transition of one or both enable inputs.

ENABLE INPUTS TRUTH TABLE

$\overline{E}_1$	$\overline{E}_2$	Function
		Data Load
L	L	Addressed Switch Changed
⌐	L	
L	⌐	
⌐	⌐	

DATA BIT TRUTH TABLE

Data	Switch Status after Enable Transition
L	Disconnect
H	Connect

DATA BITS TRUTH TABLE FOR SWITCH SELECTION

	O_1 Y_0 X_2 X_1 X_0	O_2	O_3	O_4	O_5	O_6	O_7	O_8
IN A	1111	1011	1101	1001	1110	1010	1100	1000
IN B	0111	0011	0101	0001	0110	0010	0100	0000

For example to address the switch connecting IN A to O_5 the shift register must be loaded with the code :

	D Y_0 X_2 X_1 X_0
to Connect	11110
to Disconnect	01110

ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C for M089 B1 ; – 40 to 70°C for M089 F1, D1 ; V_{DD} = 14V to 16V unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
R_{ON}*	ON-resistance		T_{amb} = 25°C $V_{i(A, B)}$ = 3.5V V_{DD} = 14V $I_{D(min)}$ = 10mA		10	15	Ω
ΔR_{ON}	ON-resistance Variation in any Package		T_{amb} = 25°C V_i = 3.5V V_{DD} = 14V I_D = 10mA			± 2	%
I_{DD}	Supply Current					7	mA
I_{LI}	Input Leakage	Pins 4, 5, 12, 13	V_i = 5V			1	µA
		Pins 1, 9	V_{iA}, V_{iB} = 4.5V V_{O1}, V_{O8} = 1.5V			0.2	µA
			V_{iA}, V_{iB} = 6V V_{O1}, V_{O8} = 1.5V			1	µA
I_{LO}	Output Leakage	Pins 2, 6, 7, 8, 10, 14, 15, 16	V_{O1}, V_{O8} = 4.5V V_{iA}, V_{iB} = 1.5V			0.2	µA
			V_{O1}, V_{O8} = 6V V_{iA}, V_{iB} = 1.5V			1	µA
V_{low}	Logic 0 Input Level		All Inputs	– 0.3		0.8	V
V_{high}	Logic 1 Input Level		All Inputs	4.5		V_{DD}	V
CT	Cross-talk Attenuation		See fig. 4	90	95		dB
I_O	Off Isolation		See fig. 5	90	95		dB
f_{CL}	Maximum Clock Input Frequency		See fig. 6			1	MHz
T_{LG}	Lag Time			100			ns
T_{LD1}	Lead Time			400			ns
T_{LD2}				150			
T_{WR}	Write Time					3	µs
t_W	Clock Pulse Width			0.4		100	µs

* See figure 1 and 2 for R_{ON} variation with temperature and V_{BIAS}.

Figure 1 : R_{ON} derating vs. temperature typ.

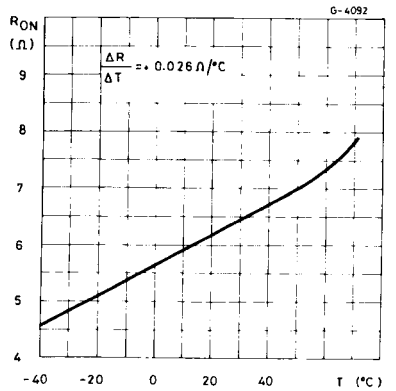
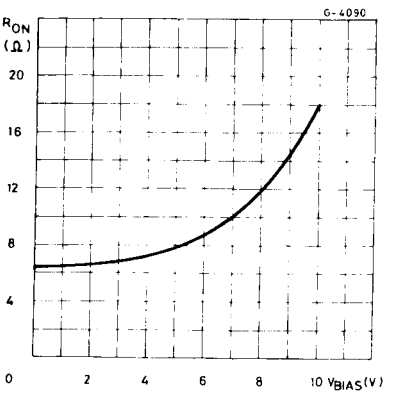


Figure 2 : R_{ON} derating vs. V_{BIAS}.



TEST CIRCUITS

Figure 3 : R_{ON} measurement.

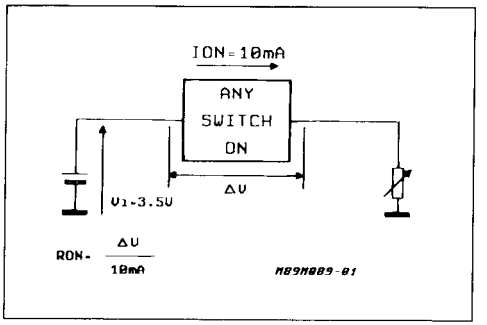


Figure 4 : Crosstalk Measurements.

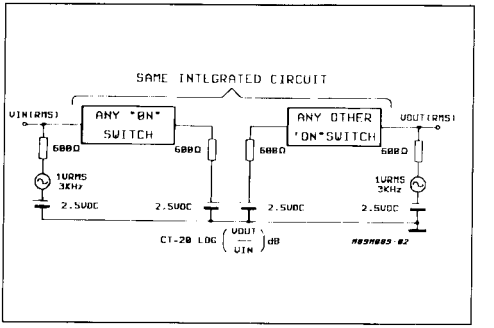
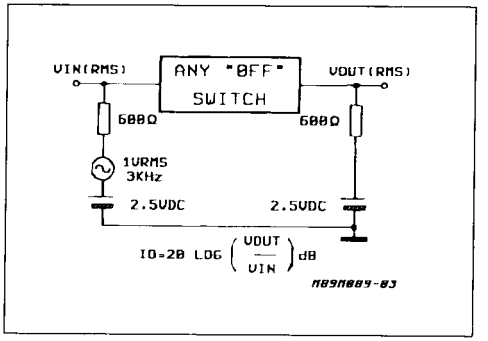
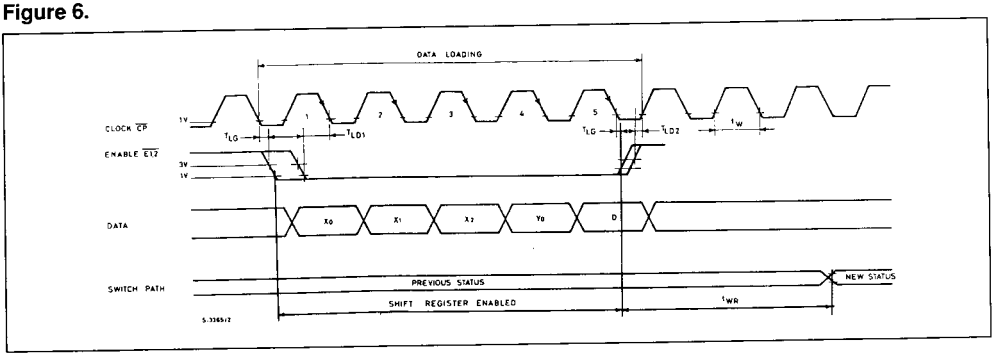


Figure 5 : Off Isolation Measurement.



TIMING DIAGRAM

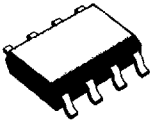
Figure 6.

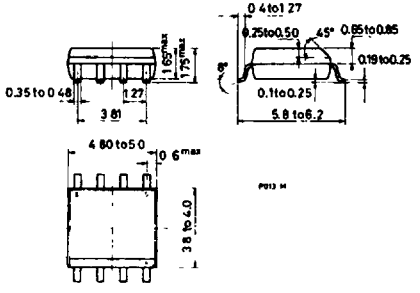


T-90-20

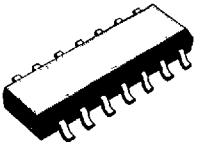
S G S-THOMSON

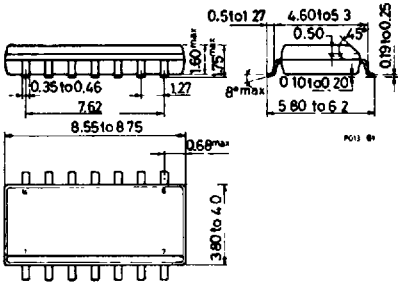
SO-8J



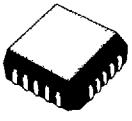


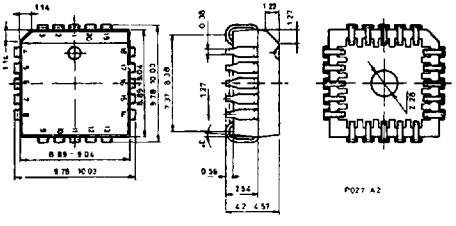
SO-14J



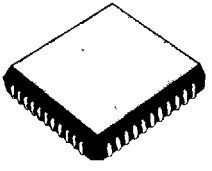


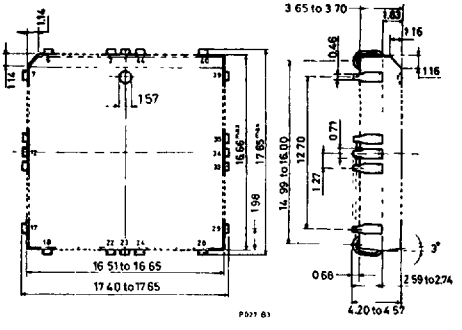
PLCC20



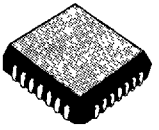


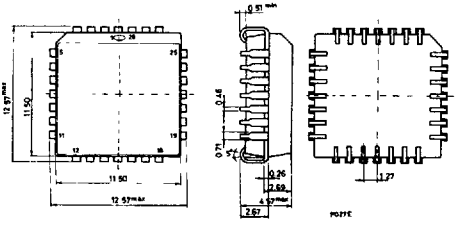
PLCC44



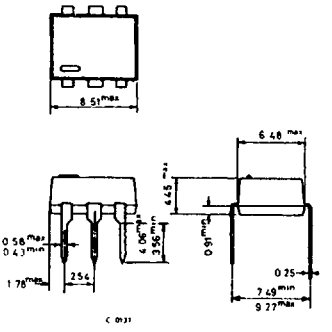


PLCC-28 Plastic Chip Carrier

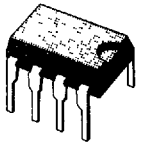


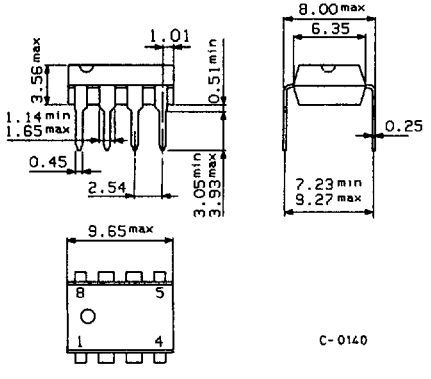


DIP-6

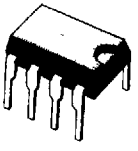


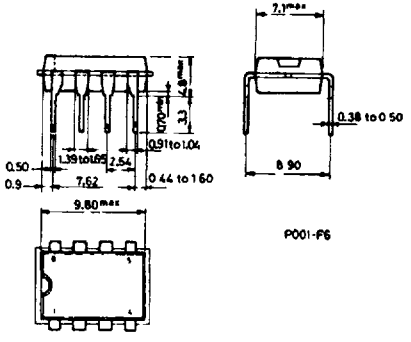
Minidip A Plastic



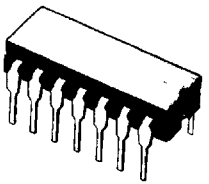


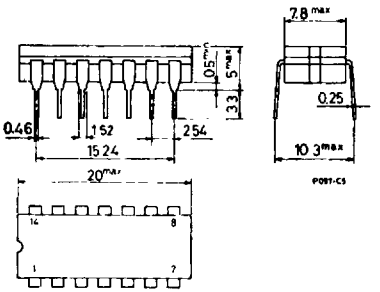
8 lead Plastic Minidip



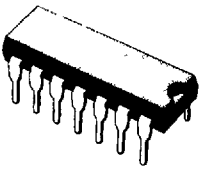


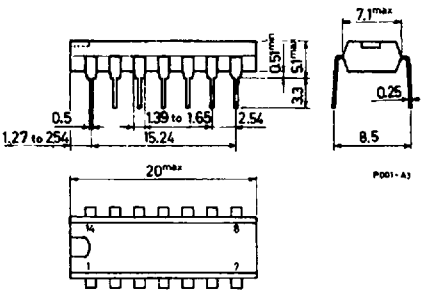
14 lead Ceramic Dip



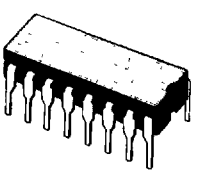


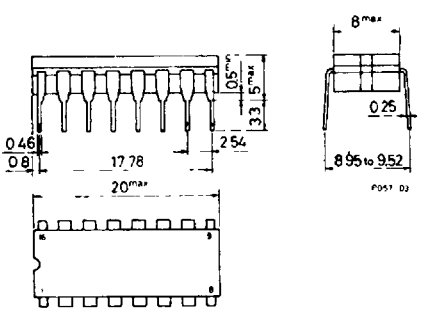
14 lead Plastic Dip



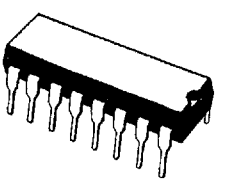


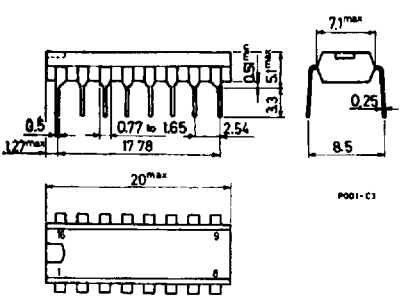
16 lead Ceramic Dip



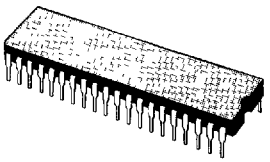


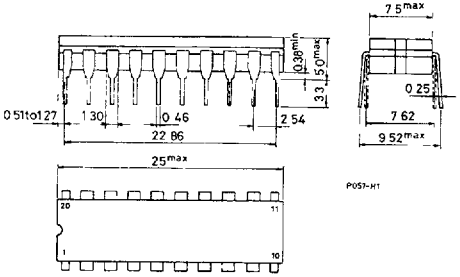
16 lead Plastic Dip (0.25)



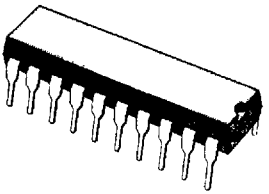


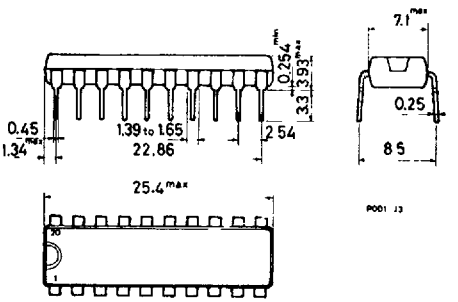
DIP-20 Ceramic



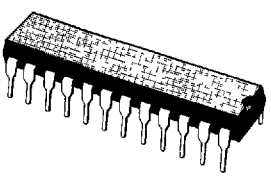


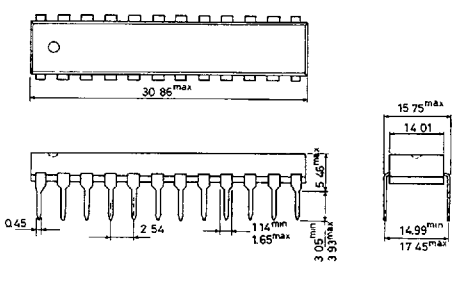
20 lead Plastic Dip (0.25)



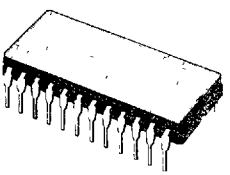


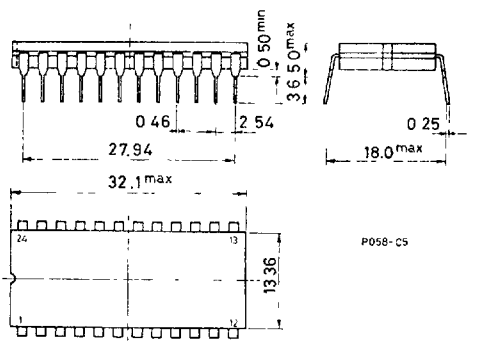
DIP-24 Plastic



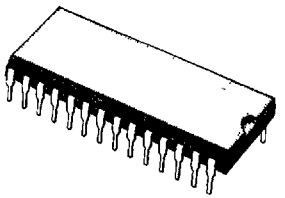


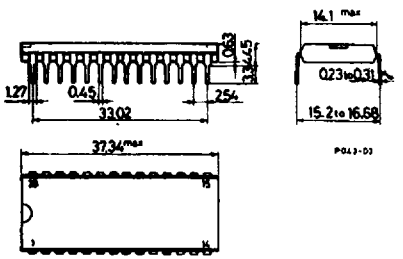
DIP-24 Ceramic (0.25)



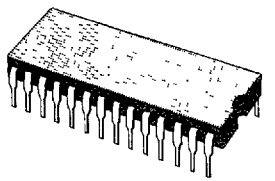


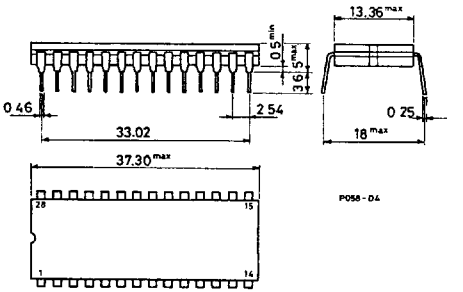
28 lead Plastic Dip



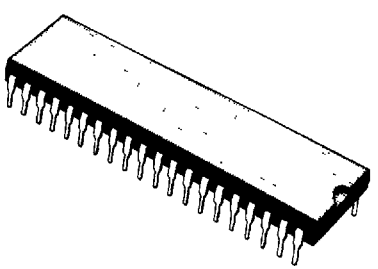


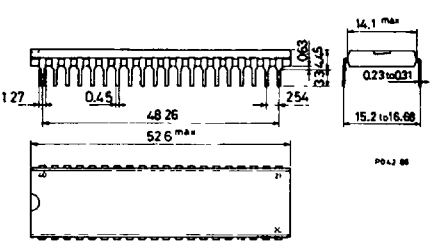
DIP-28 Ceramic (0.25)



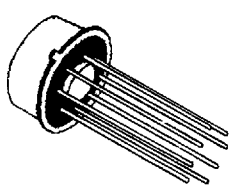


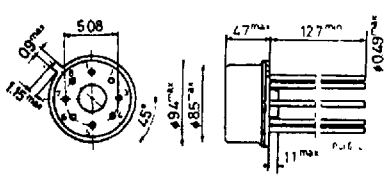
40 lead Plastic Dip





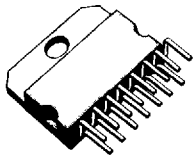
TO-99

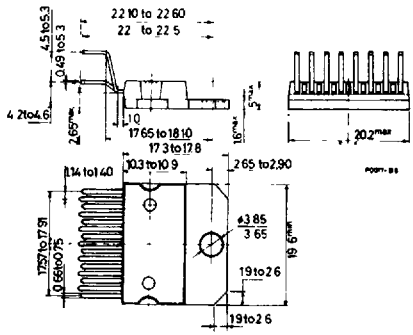




PACKAGES

MULTIWATT-15





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