F8680A PC/CHIP™

Product Overview

A true single-chip PC, the F8680A PC/CHIP™ features the SuperState® R management system, low power consumption, high performance, direct support of PCMCIA 2.0 memory and I/O cards, and flexible memory support.

Chips and Technologies, Inc. has designed the F8680A microchip to accommodate a wide variety of low power, cost-sensitive DOS applications: palmtop, laptop, and desktop computers, electronic notebooks and handhelds, and embedded controller systems. Third-party designers can build complete systems around the F8680A chip by adding only memory, storage, and peripheral devices.

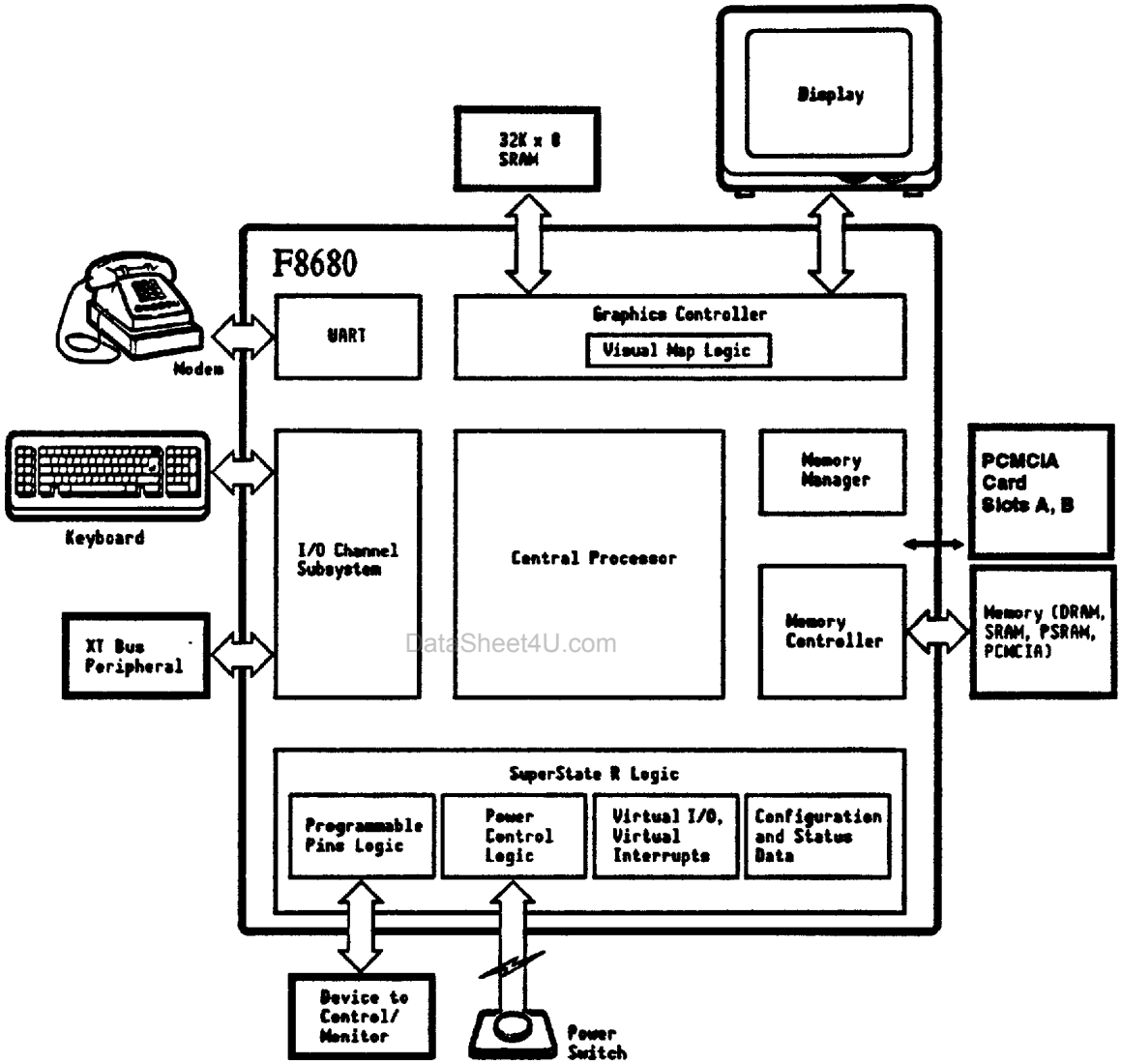
Features

The F8680A PC/CHIP has the following features:

- 3.3V/5V operation, fully static design, and intelligent sleep mode reduce power consumption approximately 60 percent and allow direct battery drive.
- PC-compatible design supports PC software and 8-bit ISA cards.
- SuperState R mode provides a separate operating environment and enables complete I/O and interrupt monitoring without BIOS modification.
- Virtual I/O™ feature allows device emulation as well as I/O monitoring and control.
- Virtual Interrupts™ feature allows interrupts to be monitored and/or redirected before any operating system, application program, or TSR sees them.
- Full PCMCIA 2.0 memory and I/O card support ensure compatibility with current and future expansions.
- 26-bit address bus enables 64MB memory map and allows direct support of PCMCIA memory card.
- Four-stage pipeline and 14MHz operation give performance comparable to a 286 or 386SX™ system.
- Flexible memory management supports PCMCIA cards and up to three banks of PSRAM, SRAM, and/or DRAM.
- Bank switching and high memory access overcome the 1MB addressing limitation of the 8086 processor, and enable PCMCIA and EMS support.
- Single CGA controller manages a CRT or LCD panel display and requires only a single 32Kx8 SRAM to minimize power consumption and board space.
- Visual Map™ gray scaling provides excellent visual contrast on any LCD panel.
- 16C450-compatible UART supports COM1 or COM2 or can be disabled.
- Over 100 configuration registers allow flexibility, control, and differentiation in system design.

A block diagram of the F8680A PC/CHIP is shown in Figure 1.

Figure 1. F8680A Block Diagram



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Introduction

The F8680A PC/CHIP microchip is designed for use in low-power and cost-sensitive DOS applications such as small entry-level computers, electronic hand-held computers, and embedded controller systems. The F8680A design integrates a high-speed 8086-compatible microprocessor with an XT subsystem, SuperState R management logic, a memory controller/manager, a PCMCIA 2.0 interface, a graphics controller, and a UART.

Pin Description

The F8680A single-chip PC is packaged in a 160-pin plastic flat pack package. Figure 2 shows the top view of the chip layout.

Figure 2. F8680A Pinout, Top View 160-Pin Plastic Flat Pack

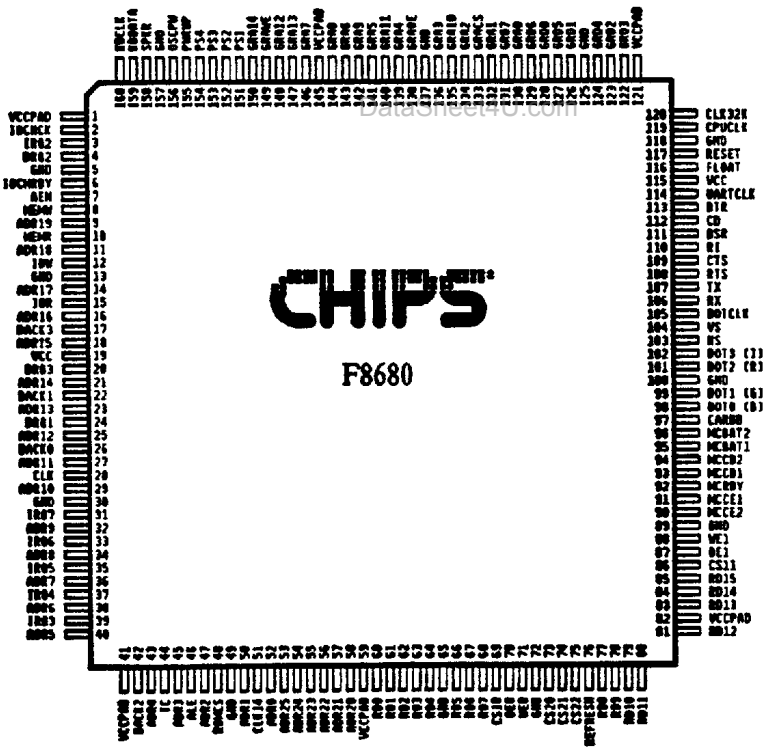


Fig. 2-2. F8680 Pinout (Filename: pin.pcx)

Table 1 lists the chip signal assignment by pin number. Those pins whose functions are programmable through the configuration registers have the additional signal possibilities listed for "1 PCMCIA" and "2 PCMCIA" card configurations. Power-up default is always "No PCMCIA".

Table 1. F8680A Pin Allocation

Pin No.	Signal No PCMCIA	Type	Description	Signal 1 PCMCIA	Signal 2 PCMCIA
1	VCCPAD	I	Power	—	—
2	IOCHCK*	I	I/O Channel Check	IOCS16*	IOCS16*
3	IRQ2	I	Interrupt Request	IOIS16*(A)	MCRDY(B)
4	DRQ2	I	DMA Request	—	—
5	GND	I	Ground	—	—
6	IOCHRDY	I	I/O Channel Ready	WAIT*	WAIT*
7	AEN	O	Address Enable	AEN & REG*	AEN & REG*
8	MEMW*	O	Memory Write	—	—
9	ADR19	O	Address Bus	—	—
10	MEMR*	O	Memory Read	—	—
11	ADR18	O	Address Bus	—	—
12	IOW*	O	I/O Write	—	—
13	GND	I	Ground	—	—
14	ADR17	O	Address Bus	—	—
15	IOR*	O	I/O Read	—	—
16	ADR16	O	Address Bus	—	—
17	DACK3*	O	DMA Acknowledge	—	RESET(B)
18	ADR15	O	Address Bus	—	—
19	VCC	I	Core Power	—	—
20	DRQ3	I	DMA Request	WAIT*(A)	MCBAT2(B)
21	ADR14	O	Address Bus	—	—
22	DACK1*	O	DMA Acknowledge	—	ENA*(B)
23	ADR13	O	Address Bus	—	—
24	DRQ1	I	DMA Request	—	MCBAT1(B)
25	ADR12	O	Address Bus	—	—
26	DACK0*	O	DMA Acknowledge	ENA*(A)	ENA*(A)
27	ADR11	O	Address Bus	—	—
28	CLK	O	XT bus clock	—	—
29	ADR10	O	Address Bus	—	—
30	GND	I	Ground	—	—
31	IRQ7	I	Interrupt Request	—	—
32	ADR9	O	Address Bus	—	—
33	IRQ6	I	Interrupt Request	—	—
34	ADR8	O	Address Bus	—	—
35	IRQ5	I	Interrupt Request	—	—
36	ADR7	O	Address Bus	—	—
37	IRQ4	I	Interrupt Request	—	—
38	ADR6	O	Address Bus	—	—
39	IRQ3	I	Interrupt Request	—	—
40	ADR5	O	Address Bus	—	—

Pin No.	Signal No PCMCIA	Type	Description	Signal 1 PCMCIA	Signal 2 PCMCIA
41	VCCPAD	I	Power	—	—
42	DACK2*	O	DMA Acknowledge	—	—
43	ADR4	O	Address Bus	—	—
44	TC	O	Terminal Count	—	—
45	ADR3	O	Address Bus	—	—
46	ALE	O	Address Latch Enable	—	—
47	ADR2	O	Address Bus	—	—
48	ROMCS*	O	ROM Chip Select	—	—
49	GND	I	Ground	—	—
50	ADR1	O	Address Bus	—	—
51	CLK14	I	14MHz timer channels clock	—	—
52	ADR0	O	Address Bus	—	—
53	ADR25	O	Address Bus	—	—
54	ADR24	O	Address Bus	—	—
55	ADR23	O	Address Bus	—	—
56	ADR22	O	Address Bus	—	—
57	ADR21	O	Address Bus	—	—
58	ADR20	O	Address Bus	—	—
59	VCCPAD	I	Power	—	—
60	RD0	I/O	Data Bus	—	—
61	RD1	I/O	Data Bus	—	—
62	RD2	I/O	Data Bus	—	—
63	RD3	I/O	Data Bus	—	—
64	RD4	I/O	Data Bus	—	—
65	GND	I	Ground	—	—
66	RD5	I/O	Data Bus	—	—
67	RD6	I/O	Data Bus	—	—
68	RD7	I/O	Data Bus	—	—
69	CS10*	O	High byte/low byte select	—	—
70	OE0*	O	Output Enable	—	—
71	WE0*	O	Write Enable	—	—
72	GND	I	Ground	—	—
73	CS20*	O	Bank select	—	—
74	CS21*	O	Bank select	—	—
75	CS22*	O	Bank select	—	—
76	REFRESH*	O	Refresh	—	—
77	RD8	I/O	Data Bus	—	—
78	RD9	I/O	Data Bus	—	—
79	RD10	I/O	Data Bus	—	—
80	RD11	I/O	Data Bus	—	—
81	RD12	I/O	Data Bus	—	—
82	VCCPAD	I	Power	—	—
83	RD13	I/O	Data Bus	—	—
84	RD14	I/O	Data Bus	—	—
85	RD15	I/O	Data Bus	—	—
86	CS11*	O	High byte/low byte select	—	—
87	OE1*	O	Output Enable	—	—
88	WE1*	O	Write Enable	WE1* & MDIR	WE1* & MDIR
89	GND	I	Ground	—	—
90	MCCE2*	O	Mem. Card Chip Slct. High	MCCE2*(A)	MCCE2*(A/B)

Pin No.	Signal No PCMCIA	Type	Description	Signal 1 PCMCIA	Signal 2 PCMCIA
91	MCCE1*	O	Mem. Card Chip Slct. Low	MCCE1*(A)	MCCE1*(A/B)
92	MCRDY	I	Memory Card Ready	MCRDY(A)	MCRDY(A)
93	MCCD1*	I	Memory Card Detect	MCCD1*(A)	MCCD1*(A)
94	MCCD2*	I	Memory Card Detect	MCCD2*(A)	MCCD2*(A)
95	MCBAT1	I	Memory Card Battery	MCBAT1(A)	MCBAT1(A)
96	MCBAT2	I	Memory Card Battery	MCBAT2(A)	MCBAT2(A)
97	CARDB	O	Card B pin	RESET(A)	RESET(A)
98	DOT0/B	O	Display data output	—	—
99	DOT1/G	O	Display data output	—	—
100	GND	I	Ground	—	—
101	DOT2/R	O	Display data output	—	—
102	DOT3/I	O	Display data output	—	—
103	HS/LP	O	Hor. Sync/Latch Pulse	—	—
104	VS/FLM	O	Ver. Sync/First Line Marker	—	—
105	DOTCLOCK	O	Dot Clock	—	—
106	Rx	I	Receive Data	—	—
107	Tx	O	Transmit Data	—	—
108	RTS*	O	Ready To Send	—	—
109	CTS*	I	Clear To Send	—	—
110	RI*	I	Ring Indicator	—	—
111	DSR*	I	Data Set Ready	—	—
112	CD*	I	Carrier Detect	—	—
113	DTR*	O	Data Terminal Ready	—	—
114	UARTCLK	I	UART clock	—	—
115	VCC	I	Core Power	—	—
116	FLOAT	I	Float all pins	—	—
117	RESET	I	Chip Reset	—	—
118	GND	I	Ground	—	—
119	CPUCLK	I	Processor clock	—	—
120	CLK32K	I	32kHz SuperState R clock	—	—
121	VCCPAD	I	Power	—	—
122	GRD3	O	Graphics Data	—	—
123	GRD2	O	Graphics Data	—	—
124	GRD4	O	Graphics Data	—	—
125	GND	I	Ground	—	—
126	GRD1	O	Graphics Data	—	—
127	GRD5	O	Graphics Data	—	—
128	GRD0	O	Graphics Data	—	—
129	GRD6	O	Graphics Data	—	—
130	GRA0	O	Graphics Address	—	—
131	GRD7	O	Graphics Data	—	—
132	GRA1	O	Graphics Address	—	—
133	GRACS*	O	Graphics Chip Select	—	—
134	GRA2	O	Graphics Address	—	—
135	GRA10	O	Graphics Address	—	—
136	GRA3	O	Graphics Address	—	—
137	GND	I	Ground	—	—
138	GRAOE*	O	Graphics Output Enable	—	—
139	GRA4	O	Graphics Address	—	—
140	GRA11	O	Graphics Address	—	—

Pin No.	Signal No PCMCIA	Type	Description	Signal 1 PCMCIA	Signal 2 PCMCIA
141	GRA5	O	Graphics Address	—	—
142	GRA9	O	Graphics Address	—	—
143	GRA6	O	Graphics Address	—	—
144	GRA8	O	Graphics Address	—	—
145	VCCPAD	I	Power	—	—
146	GRA7	O	Graphics Address	—	—
147	GRA13	O	Graphics Address	—	—
148	GRA12	O	Graphics Address	—	—
149	GRAWE*	O	Graphics Write Enable	—	—
150	GRA14	O	Graphics Address	—	—
151	PS1	I/O	Programmable Pin	—	Alt. RESET(B)
152	PS2	I/O	Programmable Pin	—	—
153	PS3	I/O	Programmable Pin	—	—
154	PS4	I/O	Programmable Pin	—	—
155	PWRUP	I	Power Up	—	—
156	OSCPW	O	Power to Oscillator	—	—
157	GND	I	Ground	—	—
158	SPKR	O	Speaker data	—	—
159	KBDATA*	I/O	Keyboard Data	—	MCCD1*(B)
160	KBCLK*	I/O	Keyboard Clock	—	MCCD2*(B)

Signal Description

The signal groups of the F8680A single-chip PC are summarized in Table 2, along with the state of each signal during suspend mode. In certain cases this state is selectable if programmed where indicated in the CREG/bit column. A signal description follows the table. The term 'inactive' as used here indicates that a signal is driven to the logic level opposite of its active state.

Table 2. Signal Names

Function	Symbol	Type	Description	State During Suspend Mode	CREG /bit	Notes
Address and Data	ADR25:0	O	Address Bus	Low or tri-state	1E/3	
	RD15:0	I/O	Data Bus	Low		
XT Bus Control	AEN	O	Address Enable	Inactive or tri-state	1E/0	
	ALE	O	Address Latch Enable	Inactive or tri-state	1E/0	
	DRQ1-3	I	DMA Request	Input (use 10k pullup)		
	DACK0-3*	O	DMA Acknowledge	Tri-state (use 10k pulldn)		
	IOCHCK*	I	I/O Channel Check	Input		
	IOCHRDY	I	I/O Channel Ready	Input		
	IOR*	O	I/O Read	Inactive or tri-state	1E/0	1
	IOW*	O	I/O Write	Inactive or tri-state	1E/0	1
	IRQ2-7	I	Interrupt Request	Input (use 10k pullup)		
	MEMR*	O	Memory Read	Inactive or tri-state	1E/0	1
	MEMW*	O	Memory Write	Inactive or tri-state	1E/0	1
	TC	O	Terminal Count	Inactive or tri-state	04/0	1
Clocks	CLK	O	XT bus clock	Inactive or tri-state	04/0	
	CLK14	I	Timer channels clock	Input (drive low)		
	CLK32K	I	SuperState R time-of-day clock	Input (always active)		
	CPUCLK	I	Processor clock	Input (drive low)		
	UARTCLK	I	UART clock	Input (drive low)		
Memory Interface	CS10-11*	O	High byte/low byte select	Inactive or tri-state	1E/3	2
	CS20-22*	O	Bank select	Inactive or tri-state	1E/3	2
	OE0-1*	O	Output Enable	Inactive or tri-state	1E/3	2
	WE0-1*	O	Write Enable	Inactive or tri-state	1E/3	2
	ROMCS*	O	ROM Chip Select	Tri-state		
Graphics Controller	DOT3:0	O	Display data output	Low or tri-state	0E/0	3
	DOTCLOCK	O	Dot Clock	Stopped or tri-state	0E/0	3,4
	GRA14:0	O	Graphics Address	Low or tri-state	0E/0	3
	GRACS*	O	Graphics Chip Select	Inactive or tri-state	0E/0	3
	GRAOE*	O	Graphics Output Enable	Inactive or tri-state	0E/0	3
	GRAWE*	O	Graphics Write Enable	Inactive or tri-state	0E/0	3
	GRD7:0	O	Graphics Data	Low or tri-state	0E/0	3
	HS/LP	O	Hor. Sync/Latch Pulse	Stopped or tri-state	0E/0	3,5
	VS/FLM	O	Ver. Sync/First Line Marker	Stopped or tri-state	0E/0	3,5
Keyboard Interface	KBCLK*	I/O	Keyboard Clock	Input		
	KBDATA*	I/O	Keyboard Data	Input		

Table 2. Signal Names (continued)

Function	Symbol	Type	Description	State During Suspend Mode	CREG /bit	Notes
PCMCIA 1.0 Memory Card Interface	MCBAT1-2	I	Memory Card Battery	Input		
	MCCD1-2*	I	Memory Card Detect	Input		
	MCCE2*	O	Memory Card Chip Select High	Inactive or tri-state	1E/1,2	1
	MCCE1*	O	Memory Card Chip Select Low	Inactive or tri-state	1E/1,2	1
	MCRDY	I	Memory Card Ready	Input		
	REFRESH*	O	Card Refresh	Inactive or tri-state	1E/3	2
PCMCIA 2.0 Card Interface	ENA*(A/B))	O	Card Buffer Enables	Inactive or tri-state	1E/7:6	7
	IOIS16*	I	I/O Is 16-bit	Input		
	MCBAT1-2(A/B)	I	Memory Card Battery	Input		
	MCCD1-2*(A/B)	I	Memory Card Detect	Input		
	MCCE1-2*	O	Memory Card Chip Selects	Low, high, or tri-state	1E/1,2	8
	MCRDY (A/B)	I	Memory Card Ready	Input		
	MDIR	O	Card Buffer Direction	Driven low	1E/7	9
	REFRESH*	O	Card Refresh	Driven low	1E/7	9
	REG*	O	Attribute Space Selection	Driven low	1E/7	9
	RESET(A)	O	Memory Card A Reset	Should be tri-stated	90/6	
	RESET(B)	O	Memory Card B Reset	Should be tri-stated	40/5:4	
	WAIT*(A)	I	Wait (cycle extender)	Input		
Programmable Pins	CARDB	O	Card B pin	Stays as last set		6
	PS1-4	I/O	Programmable Pins	Stays as last set		6
Power Control	OSCPW	O	Power to Oscillator	Low		
	PWRUP	I	Power Up	Input		
UART	CD*	I	Carrier Detect	Input		
	CTS*	I	Clear To Send	Input		
	DSR*	I	Data Set Ready	Input		
	DTR*	O	Data Terminal Ready	Active or tri-state	0F/0	1,4
	RI*	I	Ring Indicator	Input		
	RTS*	O	Ready To Send	Active or tri-state	0F/0	1,4
	Rx	I	Receive Data	Input		
	Tx	O	Transmit Data	Active or tri-state	0F/0	1,4
Miscellaneous	SPKR	O	Speaker data	Tri-state		
	RESET	I	Chip Reset	Input		
	FLOAT*	I	Float all pins	Input		
	VCC	-	Power to core of chip	–		
	VCCPAD	-	Power to pad ring of chip	–		
	GND	-	Ground	–		

1 Should be left in inactive state; set as tri-state only if connected to powered-down device
2 Tri-state only if memory is powered off during suspend mode
3 Should always be tri-state during suspend
4 State depends on programming of signal polarity
5 If stopped, state depends on phase in which clock was stopped
6 Do not tri-state during suspend mode without external pull-up or pull-down resistors
7 Bits 7:6=11, ENA* tri-stated during suspend mode; bits 7:6=10, ENA* always driven; bits 7:6=0x, ENA* always tri-stated.
8 The polarity of the MCCE1-2 lines is programmable through CREG 13h bits MCE1-2P.
9 CREG 1E bit 7=1: these lines are driven low; otherwise: MDIR and REFRESH* are controlled by CREG 1E bit 3, REG* by CREG 04 bit 0 and CREG 1E bit 0.

The following list describes all of the pin signals and is arranged in alphabetical order by signal name. An asterisk (*) indicates that the signal is active when low. The signal direction input (I), output (O), or bidirectional (I/O) is also noted.

ADR25:0	Address Bus (O) - provides system addresses for linear addressing on any byte boundary.
AEN	Address Enable (O) - indicates that the currently active memory and I/O cycles are part of a DMA cycle. It will not be driven if the XT bus is disabled (CREG 04).
ALE	Address Latch Enable (O) - indicates that a valid address is available on the system address bus. It will not be driven if the XT bus is disabled (CREG 04).
CARDB	Card B (I/O) - programmed through CREG 90h. Usually used to indicate that the current PCMCIA address refers to the second of two memory card slots.
CLK	Clock (O) - XT bus clock. It will not be driven if the XT bus is disabled (CREG 04).
CD*	Carrier Detect (I) - TTL-level input to UART.
CLK14	Clock 14 (I) - 14.31818MHz input clock used by the timer channels. Should have a 50% ±10% duty cycle.
CLK32K	Clock 32K (I) - 32767Hz input for the clock used by the internal clock logic. This clock must continue to run when the chip is in standby mode or the time of day will be lost.
CPUCLK	CPU Clock (I) - processor clock input that also sets memory timings.
CS10-11*	RAM Chip Select (O) - CS10* selects the low byte and CS11* selects the high byte. Also function as CAS* for DRAM accesses.
CS20-22*	RAM Bank Select (O) - CS20* selects bank 0, CS21* selects bank 1, and CS22* selects bank 2. The active low sense can be changed to active high through CREG 0D.
CTS*	Clear To Send (I) - TTL-level input to UART.
DACK0-3*	DMA Acknowledge (O) - response to corresponding DRQ1-3 signal (DACK0* indicates that refresh is active). These will not be driven if the XT bus is disabled (CREG 04).
DOT3:0	Display Data (O) - used as output to both CRTs and LCD panels.
DOTCLOCK	Dot Clock (O) - output to LCD panels.

DRQ1-3	DMA Request (I) - receive DMA requests from external peripherals. Ignored if the XT bus is disabled (CREG 04).
DSR*	Data Set Ready (I) - TTL-level input to UART.
DTR*	Data Terminal Ready (O) - TTL-level output from UART.
ENA*(A)	Card A Buffer Enable (O) - enables the signal buffers to PCMCIA card A for the duration of the PCMCIA memory or I/O cycle. The ENA*(A) signal is available only when programmed to replace the DACK0* signal through CREG 40h bit ENA/A.
ENA*(B)	Card B Buffer Enable (O) - enables the signal buffers to PCMCIA card B for the duration of the PCMCIA memory or I/O cycle. The ENA*(B) signal is available only when programmed to replace the DACK1* signal through CREG 41h bit ENA/B.
FLOAT*	Float Outputs (I) - commands chip to tri-state all its outputs for testing purposes.
GND	Ground for the chip.
GRA14:0	Graphics Address (O) - address bus to graphics SRAM.
GRACS*	Graphics Chip Select (O) - chip select to graphics SRAM.
GRAOE*	Graphics Output Enable (O) - output enable to graphics SRAM.
GRAWE*	Graphics Write Enable (O) - write enable to graphics SRAM.
GRD7:0	Graphics Data (O) - data bus to graphics SRAM.
HS/LP	Horizontal Sync / Latch Pulse (O) - horizontal synchronization signal to CRT when in CRT mode, latch pulse signal when in LCD mode.
IOCHCK*	I/O Channel Check (I) - input from XT bus that can trigger an NMI. Ignored if the XT bus is disabled (CREG 04).
IOCHRDY	I/O Channel Ready (I) - pulled inactive (low) by slow devices on the XT bus to lengthen a memory or I/O cycle.
IOIS16*	I/O Is 16-bit (I) - input from PCMCIA I/O interface indicating that the currently addressed I/O port is 16-bits wide. The IOIS16* signal input is available only when programmed to replace IOCHCK* for a two-card system, or IRQ2 for a one-card system, through CREG 40h bits MRDB1:0, or CREG 41h bit IO16. The IOIS16* signals from each card must be ORed together along with any IOCS16* signal from the XT bus and presented to a single input on the F8680A chip.

IOR*	I/O Read (O) - indicates that the current cycle is an I/O read cycle. It will not be driven if the XT bus is disabled (CREG 04). This signal also provides the PCMCIA IORD* command.
IOW*	I/O Write (O) - indicates that the current cycle is an I/O write cycle. It will not be driven if the XT bus is disabled (CREG 04). This signal also provides the PCMCIA IOWR* command.
IREQ*	Interrupt Request from PCMCIA I/O Card (I) - receives interrupt requests from the PCMCIA I/O card interface. The IREQ* signal name does not appear in the F8680A pin list; the F8680A signal name MCRDY must be assumed to refer to IREQ* instead of RDY/BSY* whenever the I/O interface is selected.
IRQ2-7	Interrupt Request (I) - receive interrupt requests from external peripherals. Ignored if the XT bus is disabled (CREG 04).
KBCLK*	Keyboard Clock (I/O) - receives clock pulses from the keyboard when the keyboard sends data. It can be pulled low (Control Port B) to inhibit keyboard transmission.
KBDATA*	Keyboard Data (I/O) - receives serial data from the keyboard.
MCBAT1-2 (A/B)	Memory Card Battery (I) - indicate the status of the battery on PCMCIA memory cards (PCMCIA name BVD1-2), act as status change (STSCHG*) and speaker input (SPKR*) signals on PCMCIA I/O cards. Can be read at SDATA 0A. MCBAT1-2(B) are available only when programmed to replace DRQ1 and DRQ3, respectively, through CREG 40h bits BDB1:0.
MCCD1-2* (A/B)	Memory Card Detect (I) - both pulled low by the PCMCIA memory card to indicate that the card is properly inserted. PCMCIA name is CD1-2. MCCD1-2*(B) are available only when programmed to replace the KBDATA* and KBCLK* signals, respectively, through CREG 41h bit CDB. Alternatively, CD1-2 from card A can be ANDed and input on the MCCD1*(A) input to the chip, and CD1-2 from card B on the MCCD2*(A) input, if the keyboard signal inputs are needed.
MCCE1*	Memory Card Select Low (O) - enables the low (even) bytes for I/O on the data bus. PCMCIA name is CE1. If two cards are used, MCCE1* must be gated only to the card being accessed through the ENA*(A/B) signals.
MCCE2*	Memory Card Select High (O) - enables the high (odd) bytes for I/O on the data bus. PCMCIA name is CE2. If two cards are used, MCCE2* must be gated only to the card being accessed through the ENA*(A/B) signals.

MCRDY (A/B)	Memory Card Ready (I) - indicates whether the memory card circuits are busy. PCMCIA name is RDY/BSY*. MCRDY(B) is available only if programmed to replace IRQ2 through CREG 40h bits MRDB1:0.
MDIR	Memory Card Buffers Direction (O) - controls the direction of the transceivers used to buffer the PCMCIA card to the system data bus. MDIR is generated on the WE1* line only during PCMCIA cycles; no programming is needed to enable this signal.
MEMR*	Memory Read (O) - indicates that the current XT bus cycle is a memory read. It will not be driven if the XT bus is disabled (CREG 04).
MEMW*	Memory Write (O) - indicates that the current XT bus cycle is a memory write. It will not be driven if the XT bus is disabled (CREG 04).
OE0-1*	Output Enables (O) - indicate to the low (OE0*) and high (OE1*) bytes of the currently selected RAM bank whether they should enable data from memory onto the RD bus.
PS1-4	Programmable Pins (I/O) - can be used for a wide variety of functions according to their programming through CREGs 80-8F.
OSCPW	Power Oscillator (O) - provides sequenced power to the CPU oscillators.
PWRUP	Power Up (I) - indicates that the power control state machine should power-up/power-down the system according to the programming in CREG 1C.
RD15:0	Data (I/O) - connected to system memory. RD7:0 also serve as the XT data bus.
RESET	Reset (I) - system reset input, synchronized with CPUCLK inside the chip. It must remain high for at least three CLK32K clock cycles.
REFRESH*	Refresh (O) - indicates when pseudo-SRAM should perform a refresh operation. Also provides the RFSH* signal to PCMCIA cards that require it.
REG*	Register/Memory Access (O) - indicates whether a PCMCIA card access should be decoded as a common memory space cycle or an attribute register space cycle. REG* is generated on the AEN line only during PCMCIA cycles; no programming is needed to enable this signal.

RESET(A) RESET(B)	Card Reset (O) - signals with software-selectable low, high, or tri-state output for the PCMCIA card reset function. RESET(A) replaces the CARDB line and comes up tri-stated at system reset. RESET(B) is available only if programmed to replace the DACK3* signal though CREG 40h bits DK3/1:0, and comes up high at system reset. Therefore, system designs in which card B is powered at system reset must use a PS pin for the RESET(B) function: the PS pins all come up tri-stated at system reset.
RI*	Ring Indicator (I) - TTL-level input to UART.
ROMCS*	ROM Chip Select (O) - activates the ROM for accesses to the BIOS (when not shadowed in RAM). It will not be driven if the XT bus is disabled (CREG 04).
RTS*	Ready To Send (O) - TTL-level output from the UART.
Rx	Receive Data (I) - TTL-level serial data input to the UART.
SPKR	Speaker (O) - timer channel output to an external speaker. The drive is a 4mA CMOS driver, and external conditioning may be required to match the selected sounding device.
SPKRIN*	Speaker Input (I) - speaker data input from a PCMCIA I/O card for combination with system speaker data to be output on the SPKR line. The SPKRIN* signal name does not appear in the F8680A pin list; the signal name MCBAT2 must be assumed to refer to SPKRIN* instead of BVD2 whenever the I/O interface is selected.
STSCHG*	Status Change (I) - receives status change interrupt from the PCMCIA I/O card. The STSCHG* signal name does not appear in the F8680A pin list; the signal name MCBAT1 must be assumed to refer to STSCHG* instead of BVD1 whenever the I/O interface is selected.
TC	Terminal Count (O) - indicates that the current DMA transfer is the last byte programmed for transfer. TC is not generated when DACK0* is active. It will not be driven if the XT bus is disabled (CREG 04).
Tx	Transmit Data (O) - TTL-level serial data output from the UART.
UARTCLK	UART Clock (I) - 1.8432MHz input clock for the UART.
VCC	Power to the core of the chip. This input can supply the core processor at lower voltage (nominal 3.3V) than the remaining chip circuits to save power, if desired. Otherwise it is tied to VCCPAD.
VCCPAD	Power to all chip circuits except the core processor of the chip.

VS/FLM	Vertical Sync / First Line Marker (O) - vertical synchronization signal to CRT when in CRT mode, first line indicator signal when in LCD mode.
WAIT*	Wait (I) - delays completion of memory or I/O cycle until peripheral is ready to respond. WAIT*(A) and WAIT*(B) can always be gated in, along with any IOCHRDY signal from the XT bus, on the IOCHRDY input to the F8680A chip; no programming is necessary for this performance. However, WAIT*(A) alone can replace the DRQ3 input to the chip if programmed through CREG 40h bits BDB1:0; this scheme eliminate the external gate needed to combine the XT bus IOCHRDY signal with WAIT*(A).
WE0-1*	Write Enables (O) - indicate to the low (WE0*) and high (WE1*) bytes of the currently selected RAM bank whether they should write the data on the RD bus to memory. WE0* acts as the write enable command WE*/PGM* to the PCMCIA interface, and WE1* as the MDIR signal to PCMCIA signal buffers, during PCMCIA cycles.
WP*	Write Protect (I) - indicates that a memory card is write-protected. This signal is available only on the memory card interface; when the I/O interface is selected, the card signal becomes IOIS16*. The WP* signal name does not appear in the F8680A pin list; the signal name IOIS16* must be assumed to refer to WP* instead of IOIS16* whenever the memory interface is selected.

Chip TEST Mode

The F8680A chip enters a TEST mode whenever its FLOAT* input is driven low and its RESET input is held high. In TEST mode, all pins except for DACK3* become inputs to a single large AND gate; DACK3* becomes the output to this AND gate. Putting the chip in TEST mode is useful for checking pin continuity at the board level.

Functional Description

The principal components of the F8680A architecture include:

- Fully static CMOS microprocessor
- SuperState R logic
- XT subsystem
- Memory controller/memory manager
- Graphics controller
- UART.

Refer to the system block diagram, Figure 1, for a graphic representation and to the following paragraphs for a description of these systems.

Central Processor

The F8680A microprocessor, a Chips and Technologies, Inc. innovation, is fully compatible with the 8086 processor but executes faster. It has the instruction set of an 8086 processor but performs like an 80286. In addition the processor provides:

- Full 26-bit address bus
- 24-bit internal registers
- New SuperState R operating mode and instruction set
- Microcode link to new Virtual I/O mechanism
- Microcode link to new Virtual Interrupts mechanism
- 80186 instruction set execution capability.

SuperState R Logic

The SuperState R operating environment of the CPU is separate from the normal operating environment of DOS and the BIOS. The SuperState R logic provides the mechanism for entering SuperState R mode. The switch can occur when:

- The chip is reset (always).
- A hardware or software interrupt is set to be intercepted (Virtual Interrupts feature).
- An IN or OUT instruction has executed and a device on the I/O bus must be emulated or monitored (Virtual I/O feature).
- A specified period of time elapses.
- A DMA channel must be set up or auto-initialized.
- An external request made on one of the programmable pins must be serviced.

- The PWRUP input changes state.
- An invalid opcode is encountered (always).
- A segment register is loaded.

The SuperState R logic involves the programmable pins, power control logic, configuration space, performance control feature, Virtual I/O feature, and Virtual Interrupts feature, as described in the following paragraphs.

Configuration Space

SuperState R mode provides the means of setting system configuration parameters, using a new CPU instruction. Applications cannot modify this information with any I/O or memory instruction.

Performance Control

The *performance control* feature allows the amount of time the CPU waits between executing instructions to be set anywhere from no delay to 128 cycles. Since RAM will be inactive during this time, performance control realizes a significant reduction in power consumption while allowing the CPU to remain active.

Virtual I/O Feature

The Virtual I/O feature, which is implemented as part of the SuperState R logic, allows I/O operations to every port to be monitored, redirected, emulated, or suppressed as needed. The Virtual I/O feature can be used to emulate the operation of a device that is not actually present.

Virtual Interrupts Feature

The Virtual Interrupts feature allows the SuperState R logic to trap any system interrupt, whether caused by a hardware IRQ or by a software INT instruction. SuperState R code can examine the interrupt before any TSR programs or interrupt handlers see the interrupt. Once trapped, the SuperState R code can either substitute register values and pass the call back for normal interrupt handling or emulate the interrupt handler itself and bypass the normal mechanism.

Power Control Subsystem

The F8680A chip provides many hardware and software features that allow design of an effective yet unobtrusive power management mechanism. The most basic level of management involves only two chip modes:

- The F8680A chip is in *active mode* when it is powered and its state machines for timing are running.
- The F8680A chip is in *suspend mode* when a programmed power-down has occurred. The core logic is powered but only the 32kHz clock is running. The chip continues to keep time and maintain configuration parameters while in suspend mode.

Power must be maintained to the F8680A chip at all times. When the terms "power on," "power up," and "power down" are used in this document, they do not refer to the actual application of power to and removal of power from the F8680A chip. Rather, these terms refer to the transition between active mode and suspend mode.

Power Planes. The internal logic of the chip is supplied on two totally separate power planes.

- The core power plane (pins VCC) supplies power to the core processor logic, the 32kHz time-of-day count clock logic, and the power-up comparator logic. Core power must always be present. When the chip is in suspend mode, core power consumption is extremely low (refer the the "DC Characteristics" section of this document for the exact value).
- The pad power plane (pins VCCPAD) supplies power to the chip I/O interface. All data and command lines are powered on the pad power plane. Pad power can be removed when the chip is in suspend mode, if desired, but doing so does not save power: when the chip is in suspend mode, pad power consumption drops to zero. Pad power cannot be controlled by OSCPW because the OSCPW logic is powered by the VCCPAD plane.

The core power plane can be supplied by 3.3V instead of 5V if desired to reduce power consumption. However, the setup time for accessing system memory will increase.

A system design should leave power connected to the F8680A chip VCC pins and to the 32kHz clock generation logic at all times. This arrangement is sufficient to keep all configuration information active in the F8680A chip and maintain the time-of-day count.

The PWRUP input commands the power-up of the F8680A chip into active mode and power-down into suspend mode. Power-up or power-down can be commanded through either a pulse or a steady signal sense. Pad power (VCCPAD pins) must be supplied for PWRUP to be sensed.

Logic Level Sensing. The F8680A chip interfaces equally well to logic operating at TTL voltage levels or at CMOS voltage levels. The chip circuitry assumes a +5V system (TTL) at power-up. CREG 32h must then be written with bit VL=0 to reset the input buffer sensing to 3.3V levels (CMOS). When the system is powered up at 3.3V but before it is programmed to this level, instruction fetches from ROM will still occur reliably; only the upper limit of V_{IL} is affected. However, it is recommended that CREG 32h be reprogrammed immediately on power-up.

Note that when designing a system with CMOS logic to operate at 3.3V, any clock oscillator "cans" to be designed in must be CMOS also.

Power-On Clock Comparator. Power-up can be commanded through the clock comparator register of the F8680A chip. When in suspend mode, power will be restored when the time in the power control comparator matches the time-of-day count value. Operation will resume regardless of the PWRUP input signal level. CREGs 18h through 1B comprise the 32-bit comparator register. If the F8680A chip is already active when the time-of-day reaches the comparator value, the comparator will have no effect. Refer to the *F8680A PC/CHIP Programmer's Reference Manual* for details of this comparator.

Power Control State Machine. The power control state machine can be instructed to remove power from the oscillators through the POFF bit at CREG 1C. When POFF is set to 1, the power control state machine will begin to sequence the F8680A chip into suspend mode. Refer to the *F8680A PC/CHIP Programmer's Reference Manual* for programming details. The power control sequencing operates as follows.

- Upon receiving a power-up request (initiated by either the PWRUP input or the power control comparator), the power control state machine sets the OSCPW output active within 0.5s. It then enables the various timing state machines in the F8680A chip 0.5s after setting OSCPW active.
- Upon receiving a software-commanded power-down request (the only kind possible), the power control state machine disables the various timing state machines within 0.5s. It then sets the OSCPW output inactive 0.5s after disabling the timing state machines.

Therefore, power-up and power-down sequences always require at least 0.5s, but always less than 1.0s, to execute.

In designs where the oscillator stabilization time is of less importance than the need for a rapid resume sequence, the QR bit is provided in CREG 1C. When QR=1, the power control state machine restarts the timing state machines within 0.1ms after setting OSCPW active.

Connections to the PWRUP Input. The power-up pin PWRUP indicates when the F8680A chip should exit suspend mode and begin normal operation. Once the F8680A chip is operational, the PWRUP signal can be used to initiate a power-down into suspend mode.

Note: PWRUP by itself cannot cause a power-down; it can only *request* a power-down. Software must command a power-down. However, PWRUP can be programmed to cause a switch to SuperState R mode, which in turn can power down the F8680A chip.

Two choices are available when incorporating the power switch into a system design: a toggle switch or a momentary switch. The SuperState R configuration register at CREG 1C provides a bit to select whether a high or a low signal on PWRUP will cause a switch to SuperState R mode. The programming of this register will depend on the choice of power-up switch.

If an SPDT toggle switch is connected, the PWRUP input is pulled to logic ground to turn the system off, and is pulled up to VCC to activate the F8680A chip. Software that recognizes a low signal at PWRUP as a power-down request must be provided.

If a momentary switch is connected, it pulls PWRUP to VCC to activate the F8680A chip. A pull-down resistor allows PWRUP to go back to logic ground as soon as the momentary switch is released. Software that recognizes a high pulse at PWRUP as a power-down request must be provided.

Programmable Pins

The chip provides five pins with programmable functions. These pins can be used for such functions as programmable chip selects, clock outputs, and status monitoring inputs.

The programmable pins can be used in a variety of ways. Software control makes these pins extremely flexible and easy to incorporate in any design. The pins can operate as either inputs or outputs and can source/sink 4mA minimum (refer to the "DC Characteristics" section for specific values) when used as outputs. Table 3 lists the specific functions available through the programmable pins.

Table 3. Programmable Pin Functions

Function	Type	Available on:				
		PS1	PS2	PS3	PS4	CARDB
CLK32	O	x	x	x	x	x
CLK1/16	O	x	x	x	x	x
CLK1/32	O	x	x	x	x	x
PCS	O	x	x	x	x	
FR0	O	x	x			
512Hz	O	x				
256Hz	O		x			
16384Hz	O			x		
8192Hz	O				x	
IFACTIVE	O		x	x	x	
IFBRNCH	O		x			
CLKCANRUN	O			x		
FLAG9	O			x	x	
ACDCLK	O		x	x	x	
ICMPLT	O			x		
CLKCANRUN	O			x	x	
EXTSS	I	x	x	x	x	
DOTCLK	I				x	

where:

CLK32 32kHz Clock - PS1-PS4 and CARDB can provide a 32kHz clock pulse.

CLK1/16 1/16 32kHz Clock - PS1-PS4 and CARDB can provide a clock with a positive pulse that occurs once every sixteen 32kHz clock cycles. The programmable pin stays high only for the duration of one phase (1/2 clock period) of the 32kHz clock.

CLK1/32 1/32 32kHz Clock - PS1-PS4 and CARDB can provide a clock with a positive pulse that occurs once every thirty-two 32kHz clock cycles. The programmable pin stays high only for the duration of one phase (1/2 clock period) of the 32kHz clock.

PCS Programmable Chip Select - PS1-PS4 can decode I/O reads and/or writes at any I/O address or range of addresses.

FR0 Frame Rate 0 - PS1-PS2 can provide the vertical interval signal divided by 2.

256Hz
512Hz
8192Hz
16384Hz These frequencies can be output on PS2, PS1, PS4, and PS3 respectively.

IFACTIVE Instruction Fetch Active - PS2-PS4 can indicate whether the current memory request is for instruction data.

IFBRNCH	Instruction Fetch on Branch - PS2 can indicate whether the current memory request is for the first instruction after a program branch (jump, call, etc.)
ICMPLT	Instruction Complete - PS3 can output a pulse at the end of each instruction executed. This signal can be counted to indicate true MIPS. PS3 stays high only for the duration of one phase (1/2 clock period) of the CPU clock.
FLAG9	Flag bit 9 - PS3-PS4 can indicate whether maskable interrupts are enabled.
ACDCLK	AC Drive Clock - PS2-PS4 can output a square wave with a 50 percent duty cycle and a programmable period for use with LCD panels.
CLKCANRUN	Clock Can Run - PS4 can indicate whether the power control state machine has completed the power-up sequence and instruction execution is allowed.
EXTSS	External SuperState R Switch - PS1-PS4 can be used as inputs to trigger a switch to SuperState R mode.
DOTCLK	Dot Clock - PS4 can be used to input a non-standard dot clock frequency for the graphics controller.

Programming Simultaneous Input and Output. If a pin is programmed to input an external SuperState R switch request, it can be simultaneously used for output. For example, selecting a 256Hz output on PS2 and programming PS2 for SuperState R input at the same time would result in a periodic switch to SuperState R mode (like the timer tics provide). However, PS2 should not be driven by external circuitry in this configuration.

XT Subsystem

The F8680A chip logic supports the functions of the following components found in the standard XT subsystem:

- Interrupt controller
- Direct memory access (DMA) controller
- Timer
- Keyboard interface
- External XT bus.

For the most part, the XT subsystem is implemented in hardware.

For performance of the functions available in an XT environment, the interrupt controller is functionally equivalent to the 8259A component, and the timer to the 8254 component.

The F8680A microchip implements the functions normally associated with the 8237 DMA Controller through a combination of hardware, CPU microcode, and software.

The keyboard interface and associated circuitry is compatible with that of the XT, including read access to the XT configuration switch settings. These switch settings are programmed through a configuration register.

Table 4 shows the system I/O address space occupied by the F8680A chip.

Table 4. XT-Compatible I/O Port Assignment

Range	IOR* Cycle Internal/External	IOW* Cycle Internal/External	Usage
000-01F	Internal	Internal	DMA Controller
020-03F	Internal	Internal	Interrupt Controller
040-05F	Internal	Internal	Timer
060, 064, 068, 06C, 070, 074, 078, 07C	Internal	External	Keyboard Data Port
061, 065, 069, 06D, 071, 075, 079, 07D	Internal	Internal	Control Port B
062, 066, 06A, 06E, 072, 076, 07A, 07E	Internal	External	Status Port C
063, 067, 06B, 06F, 073, 077, 07B, 07F	External	External	Not used by the F8680A chip
080-09F	External	External	DMA Page Registers
0A0-2F7	External	External	Not used by the F8680A chip
2F8-2FF	Internal + External	Internal + External	If UART enabled and set as COM2
	External	External	If UART disabled or set as COM1
300-3CF	External	External	Not used by the F8680A chip
3D0-3DF	External	External	If on-board CGA disabled
	Internal	Internal	On-board CGA enabled
3E0-3F7	External	External	Not used by the F8680A chip
3F8-3FF	Internal + External	Internal + External	If UART enabled and set as COM1
	External	External	If UART disabled or set as COM2

UART

A Universal Asynchronous Receiver/Transmitter, compatible with the National® NS16C450 asynchronous communications element, is provided for serial communications. The device can be assigned to respond as either COM1 or COM2, or it can be disabled.

Memory Subsystem

The F8680A single-chip PC provides an extremely versatile memory management and control system, as described in the following paragraphs.

Memory Management

The memory manager maps CPU addresses to physical RAM in 32kB or 64kB segments. Once mapped, segments can be bank-switched for implementation of EMS memory and a PCMCIA memory card interface. The maximum local system memory that is directly managed is 4MB. A total of 64MB memory can be addressed through the 26-bit address bus ADR25:0.

The system memory usage is shown in Table 5.

Table 5. System Memory Usage

Memory Range	Size (kB)	Usage
0F0000-0FFFFF	64	BIOS ROM (can be shadowed)
0E0000-0EFFFF	64	Often used for PCMCIA memory card access or ROM applications
0DC000-0DFFFF	16	Often used for EMS memory page frames
0D8000-0DBFFF	16	
0D4000-0D7FFF	16	
0D0000-0D3FFF	16	
0CF000-0CFFFF	4	Often used for PCMCIA memory windows
0CE000-0CEFFF	4	(if used, 64kB segment starting at 0C0000 becomes only 48kB)
0CD000-0CDFFF	4	
0CC000-0CCFFF	4	
0C0000-0CFFFF	64	Often used for ROM applications or PCMCIA memory card access
0B8000-0BFFFF	32	CGA graphics memory
0A0000-0B7FFF	96	Often used for alternate video controller
000000-09FFFF	640	MS-DOS and applications

Memory Controller

The memory controller of the F8680A chip supports most of the commonly used memory types. The controller provides chip-select decoding for up to three banks of memory. External address decoding must be provided for any additional banks. Each bank can be any one of the following types:

- 256k x 1, 256k x 4, 512k x 8, 1M x 1, 1M x 4, and 4M x 1 DRAM
- Any type of SRAM or PSRAM (such as 32k x 8, 128k x 8, and 512k x 8)
- PCMCIA memory card
- ROM
- Memory on the XT bus.

The three types can be mixed in any way. The best choices are DRAM, SRAM/PSRAM, and PCMCIA memory, all of which provide good performance when configured for word (16-bit) access. DRAM page mode is supported with both byte and word requests. The controller provides all timing and control signals to allow direct support for up to three banks of 8-bit or 16-bit memory. Both 8-bit and 16-bit banks can be used in the same system.

Connecting the memory is generally very routine and predictable. The only decisions to make on the hardware side are the memory type and capacity. All mapping and configuration choices are made through software. The memory configuration worksheet provided in the "Memory" chapter of the *F8680A PC/CHIP Programmer's Reference Manual* simplifies the programming calculations needed for mapping memory into the system address space.

Memory Operational Theory

This section provides only a brief summary of the concepts involved in system memory mapping. For a more detailed explanation, refer to the *F8680A PC/CHIP Programmer's Reference Manual.*

The memory manager provides independent *bank switching* and *memory mapping* mechanisms to deal with the translation from logical CPU addresses to physical addresses in RAM. The bank switching mechanism takes linear CPU addresses that fall in the B0000 to FFFFF range and moves them so that the effective logical address can fall anywhere in the 64MB address space of the F8680A chip. The memory mapping mechanism takes the logical address, after any possible shifting by the bank switching mechanism, and maps it on a block-by-block basis to available space in physical RAM. Either 32kB or 64kB blocks can be selected.

Bank Switching Logic. Figure 3 illustrates the bank switching logic used in the system. The logic first decodes address bits A19:16 from the CPU. If the address is in the B0000 to FFFFF range, the decoder signals the multiplexer to use the contents of one of the nine Bank Switch Registers instead of the upper bits of the address from the CPU.

The decoder selects the Bank Switch Register whose contents will substitute the upper address bits from the CPU according to the nine subranges listed in Table 6. Address bits A15:14 may or may not be substituted by the Bank Switch Register address bits, depending on the size of the subrange decoded.

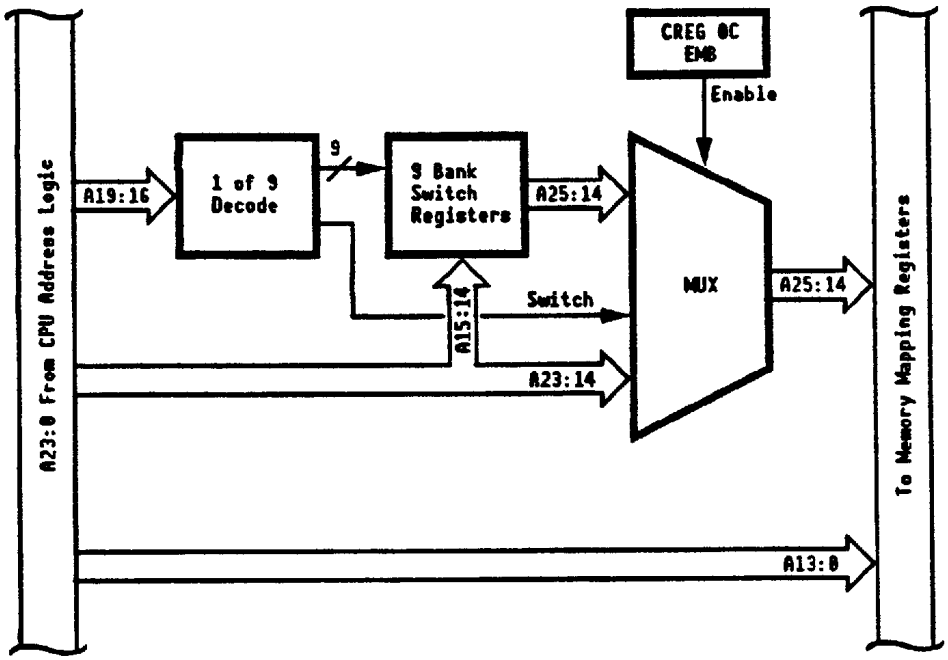
Table 6. Bank Switch Register Ranges

Bank Switch Register	Corresponding Subrange
0	B0000-B7FFF
1	B8000-BFFFF
2	C0000-CFFFF
3	D0000-D3FFF
4	D4000-D7FFF
5	D8000-DBFFF
6	DC000-DFFFF
7	E0000-EFFFF
8	F0000-FFFFF

The multiplexer passes on the substituted address bits only when enabled by the EMB bit in CREG 0C. The resulting 26-bit address A25:0 is passed on to the memory mapping logic. Note that bank switching is disabled on power-up.

Memory Window Logic. The chip also provides four Memory Window Registers that may or may not be enabled. The memory windowing logic is not shown as part of Figure 3, but it operates in a manner similar to the Bank Switch Registers. However, unlike the Bank Switch Registers, the output of the memory windowing logic does not pass to the Memory Mapping Registers. Each Memory Window Register has its own Bank Select Register to determine the cycle type to be performed for accesses in that window.

Figure 3. Bank Switching Logic



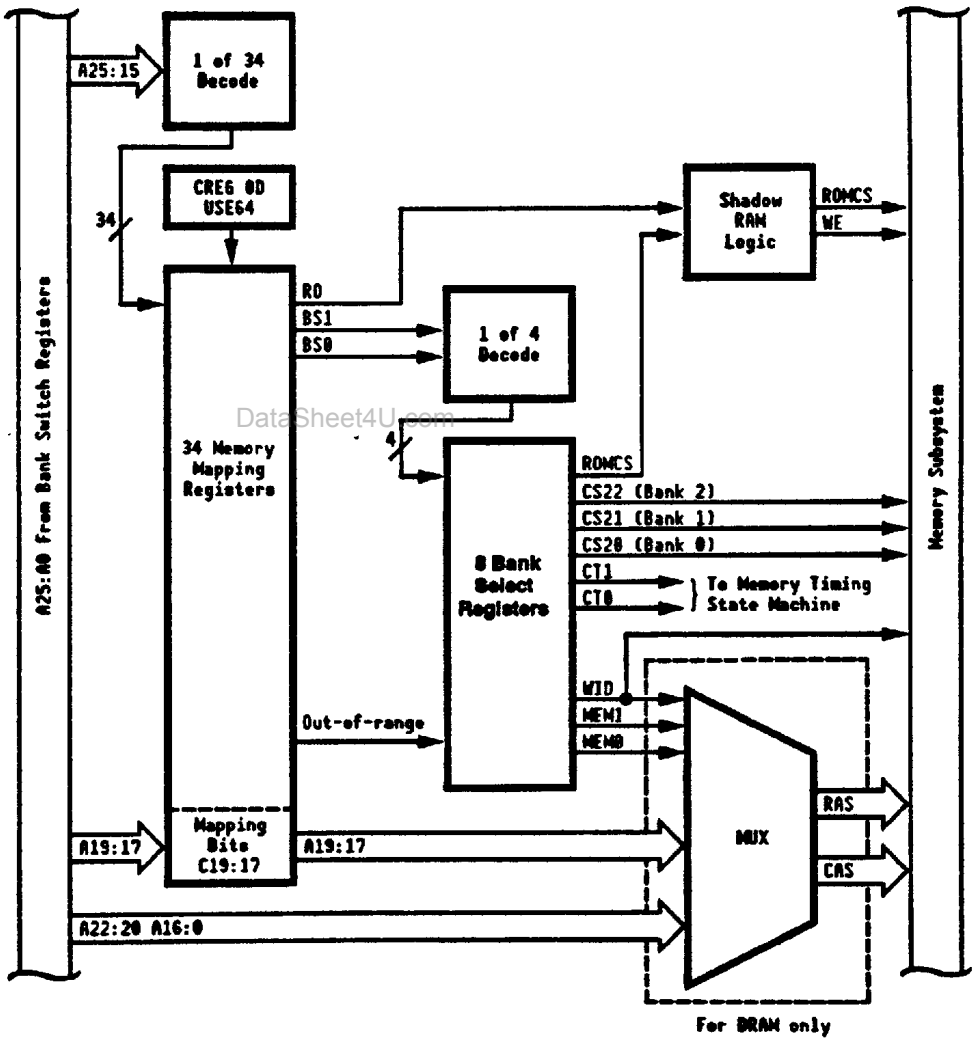
Note: A23:0 from the CPU address logic comes after Gate A20.

Memory Mapping Logic. Figure 4 illustrates the logic used to map the logical addresses from the bank switch mechanism to locations in physical RAM. The upper address bits A25:15 are decoded to select one of 34 address ranges. The USE64 bit in CREG 0D selects the decoding method. If USE64=0, each of the first thirty-two 32kB blocks of logical addresses corresponds to a separate mapping register, with the next two 512kB blocks each corresponding to a mapping register. If USE64=1, each of the first thirty-two 64kB blocks of logical addresses corresponds to a separate mapping register, with the next two 1MB blocks each corresponding to a mapping register.

Unlike the Bank Switch Registers, the Memory Mapping Registers do not contain replacements for the logical address bits from the CPU. The mapping registers simply select the physical bank of RAM to which the logical address should be directed. However, the registers do provide mapping bits. These bits serve to shift the address up or down in multiples of 128kB within the physical RAM bank, allowing "lost" RAM (such as RAM whose address would overlap the display SRAM address range) to be utilized elsewhere.

Each Memory Mapping Register selects one of four Bank Select Registers, which in turn activates the control signals for the selected bank of RAM. If the CPU generates an address outside the range of the 34 Memory Mapping Registers, the logic automatically selects one of four out-of-range Bank Select Registers reserved for this purpose. No mapping bits are provided for out-of-range accesses.

Figure 4. Memory Mapping Logic



How to Approach Memory Design

The memory controller handles three banks of RAM, providing the bank select signals CS20, CS21, and CS22 to activate banks 0, 1, and 2, respectively (see Figure 4). Additional banks can be used, but the F8680A chip provides no additional bank select signals and external decoding logic would be needed.

The memory controller is programmed through CREG locations for each bank according to the following parameters: memory cycle type (DRAM, SRAM, XT bus, or PCMCIA); bank width (one or two bytes); address multiplexing (for DRAM only); and required ROMCS line status (active/inactive) for that bank.

DRAM, SRAM, or PSRAM can be used, and all three can be mixed. Different RAM types cannot be mixed within the same bank, but different size devices of the same type can be. A PC/CHIP Application Note is available that describes an interesting application where RAMs of different sizes and widths are used to optimize performance in a certain addressing range.

Refer to the following sections for basic examples of the connections required to interface each type of memory to a bank. Then refer to the *F8680A PC/CHIP Programmer's Reference Manual* to determine the most effective way to utilize the RAM for a given hardware design.

Note: When the graphics subsystem is enabled, all accesses at segment 0B800 are considered graphics cycles and are automatically forwarded to the graphics controller.

DRAM

DRAM provides efficient, high-performance, low-cost memory space. There are drawbacks, however. For example, DRAM consumes a lot of power when compared to SRAM. Special features of the F8680A chip, such as page mode operation, slow refresh, and performance control, help to lessen the impact of this power consumption. However, a mix of DRAM, SRAM, and PCMCIA memory may yield a more efficient design.

Signals. Table 7 lists the pin assignments and signals provided for the DRAM interface. Refer to the "Signal Description" section of this manual for signal descriptions.

Table 7. Pin Assignments - DRAM Interface Signals

Address Bus		Data Bus		Control Bus	
Pin	Signal	Pin	Signal	Pin	Signal
52	ADR0	60	RD0	69	CS10*
50	ADR1	61	RD1	86	CS11*
47	ADR2	62	RD2	73	CS20*
45	ADR3	63	RD3	74	CS21*
43	ADR4	64	RD4	75	CS22*
40	ADR5	66	RD5	70	OE0*
38	ADR6	67	RD6	87	OE1*
36	ADR7	68	RD7	71	WE0*
34	ADR8	77	RD8	88	WE1*
32	ADR9	78	RD9		
29	ADR10	79	RD10		
27	ADR11	80	RD11		
		81	RD12		
		83	RD13		
		84	RD14		
		85	RD15		

Memory Address Multiplexing. The MEM bits and the WID bit of the Bank Select Registers select the type of address multiplexing that will be performed during DRAM cycles. Refer to the *F8680A PC/CHIP Programmer's Reference Manual* for Bank Select Register programming details.

Connect one-byte-wide RAM to the address bus starting with bit 0, and two-bytes-wide RAM starting with bit 1. The address bits are multiplexed according to Table 8. Address bits above bit 11 are not changed during a DRAM cycle. These bits can be decoded with external chip select decode logic if it is necessary to support more than three banks of memory and no more CS2x lines are available.

Table 8. Address Multiplexing

Period	MEM Bits	WID Bit	ADR25:0 bit											
			11	10	9	8	7	6	5	4	3	2	1	0
T1/RAS	00 256kx1	0	20	19	18	17	16	15	14	13	12	11	10	9
	01 1Mx1	0	x	19	18	17	16	15	14	13	12	11	10	19
	10 4Mx1	0	x	19	18	17	16	15	14	13	12	11	20	21
	00 256kx2	1	x	x	18	17	16	15	14	13	12	11	10	x
	01 1Mx2	1	x	19	18	17	16	15	14	13	12	11	20	x
	10 4Mx2	1	20	19	18	17	16	15	14	13	12	21	22	x
T2/CAS	—	—	11	10	9	8	7	6	5	4	3	2	1	0

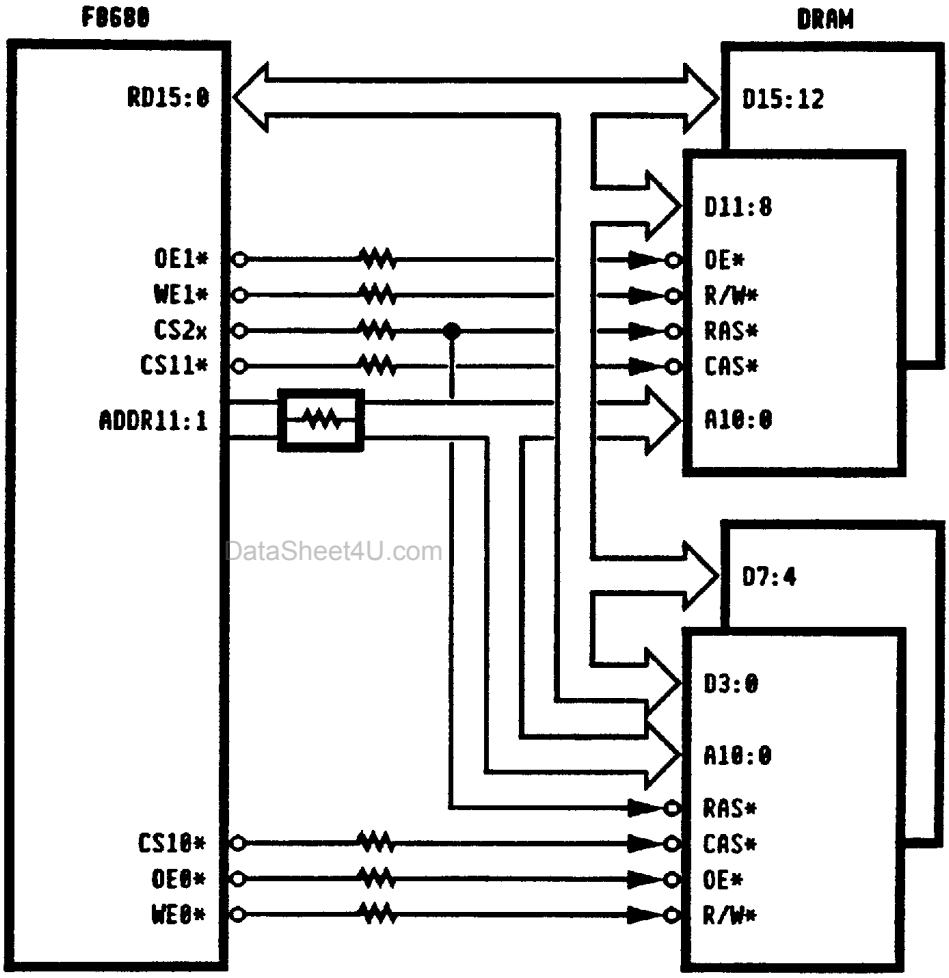
Refresh. The F8680A chip generates the periodic refresh necessary to keep DRAM contents alive. The refresh timing is set by programming timer channel 1 just as it would be for the XT. The banks to receive refresh are programmed through CREG 16h; this CREG also provides a setting for 512k x 8 DRAM refresh on the OE0-1* lines. Refer to "Refresh" in Chapter 5 of the *F8680A PC/CHIP Programmer's Reference Manual* for details on refresh.

The memory controller provides a CAS before RAS type of refresh: the controller activates the CS1x line (CAS) first, and follows this by activating the CS2x (RAS) line. This method reduces the power required to perform refresh when compared to a RAS-only refresh.

Interface to All Common Types. Figures 5 through 7 illustrate the connections necessary to interface each type of DRAM to the F8680A chip.

Figure 5 shows the connections to a bank of DRAM made up of 4-bit devices (256k x 4 or 1M x 4 DRAM).

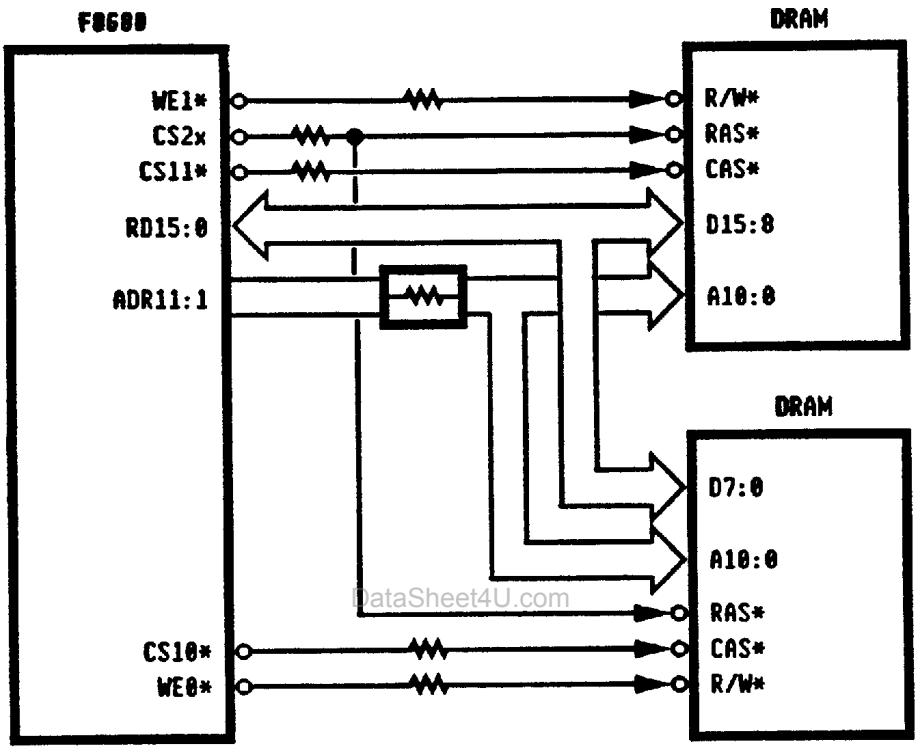
Figure 5. Interface to 4-bit DRAM



Notes:
1. Use limiting resistors in connections to DRAM; 33 ohm resistors are recommended.
2. The polarity of the CS2x lines is programmable.

Figure 6 shows the connections to a bank of DRAM made up of 8-bit devices (512k x 8 DRAM).

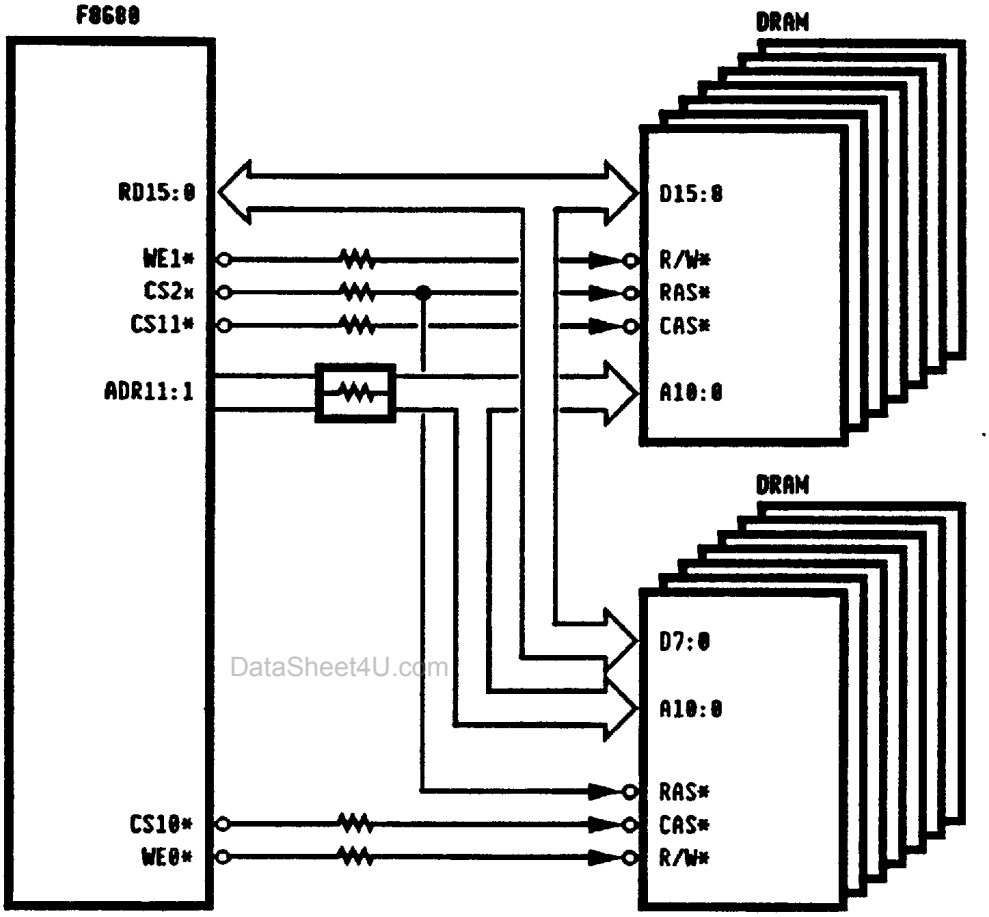
Figure 6. *Interface to 8-bit DRAM*



Notes:
1. Use limiting resistors in connections to DRAM; 33 ohm resistors are recommended.
2. The polarity of the CS2x lines is programmable.

Figure 7 shows the connections to a bank of DRAM made up of 1-bit devices (256k x 1, 1M x 1, or 4M x 1 DRAM).

Figure 7. Interface to 1-bit DRAM



Notes:
1. Use limiting resistors in connections to DRAM; 33 ohm resistors are recommended.
2. The polarity of the CS2x lines is programmable.
3. Connect one each of data bus lines RD15:0 to each 1-bit DRAM.

SRAM/PSRAM

Table 9 lists the pin assignments and signals provided for the SRAM interface. Refer to the "Signal Description" section of this manual for signal descriptions.

Table 9. Pin Assignments - SRAM Interface Signals

Address Bus		Data Bus		Control Bus	
Pin	Signal	Pin	Signal	Pin	Signal
52	ADR0	60	RD0	73	CS20*
50	ADR1	61	RD1	74	CS21*
47	ADR2	62	RD2	75	CS22*
45	ADR3	63	RD3	70	OE0*
43	ADR4	64	RD4	87	OE1*
40	ADR5	66	RD5	76	REFRESH*
38	ADR6	67	RD6	71	WE0*
36	ADR7	68	RD7	88	WE1*
34	ADR8	77	RD8		
32	ADR9	78	RD9		
29	ADR10	79	RD10		
27	ADR11	80	RD11		
25	ADR12	81	RD12		
23	ADR13	83	RD13		
21	ADR14	84	RD14		
18	ADR15	85	RD15		
16	ADR16				
14	ADR17				
11	ADR18				

Refresh for PSRAM. PSRAM provides its own internal refresh logic, allowing the PSRAM to maintain its contents when the system stops sending REFRESH* pulses. The memory controller provides a refresh signal REFRESH* that is compatible with the internal refresh logic of the PSRAM. CREG 16h bit ERPSR enables PSRAM refresh on the REFRESH* line.

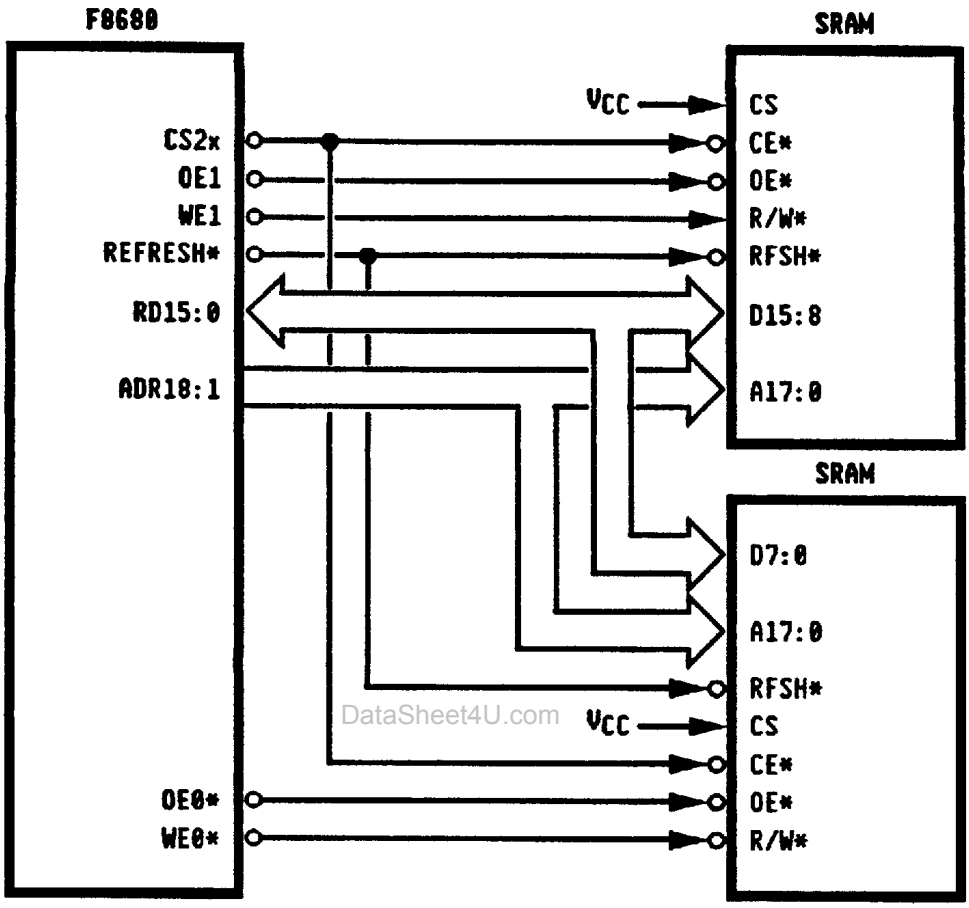
CREG 0B can select the appropriate signal pulse to initiate the internal standby refresh of the PSRAM. In this mode, just before the F8680A chip goes into suspend mode it emits a final REFRESH* pulse of minimum 8µs duration to enable the internal refresh logic of the PSRAM. The PSRAM contents cannot be accessed, but they are maintained. As soon as the F8680A chip leaves suspend mode and begins to send regular REFRESH* pulses, the PSRAM goes active and disables its internal refresh logic.

Interface to All Common Types. Figure 8 illustrates the connections necessary to interface a word-wide bank of SRAM to the F8680A chip. The interface accomodates 32k x 8, 128k x 8, and 512k x 8 devices with the same connections. Only the number of address lines connected varies, as shown in Table 10. To interface a byte-wide bank of SRAM, connect the system address lines ADR18:0 directly to the SRAM address lines A18:0.

Table 10. Address Bus Connections for Various SRAM Device Capacities

System Address	SRAM Address		
	32k x 8	128k x 8	512k x 8
ADR15:1	A14:0	A14:0	A14:0
ADR17:16	n/c	A16:15	A16:15
ADR19:18	n/c	n/c	A18:17

Figure 8. Interface to SRAM



Notes:
1. No limiting resistors are needed in connections to SRAM.
2. The polarity of the CS2x lines is programmable.

ROM

The memory controller supports ROM as a device on the XT bus. Either 8-bit or 16-bit accesses can be made to ROM according to the setting made in the Bank Select Register that points to the ROM.

BIOS ROM. The most common use of ROM is to provide the system BIOS. After reset the F8680A chip sets its ROMCS* line active and begins executing from bank 0 (BS0), which points to the XT bus by default. The BIOS ROM bank will normally be 8-bits wide. The BIOS ROM contents are usually copied from ROM to system RAM at boot time, a process known as *shadowing* ROM in RAM. Running the BIOS from RAM is much faster because ROM must be accessed with slow XT bus cycles that take at least two times as long as SRAM access.

Shadowing ROM in RAM is a decision made in software; it does not impact hardware design. However, the SuperState R code portion of the BIOS must always be RAM-resident. Refer to Chapter 5 of the *F8680A PC/CHIP Programmer's Reference Manual* for more information on shadowing the BIOS in RAM.

Applications in ROM. A system design might provide application programs in ROM. Generally these programs will be copied as needed from ROM to RAM for execution, then deleted from RAM when their execution is complete. Running applications from 8-bit ROM is not recommended, as performance is poor.

If applications are to be run from ROM, the ROM devices can be arranged as word-wide memory. If possible in the system design, the ROM should be accessed with PCMCIA cycles which execute faster than XT bus cycles yet can be adjusted to meet the timing requirements of the ROM device.

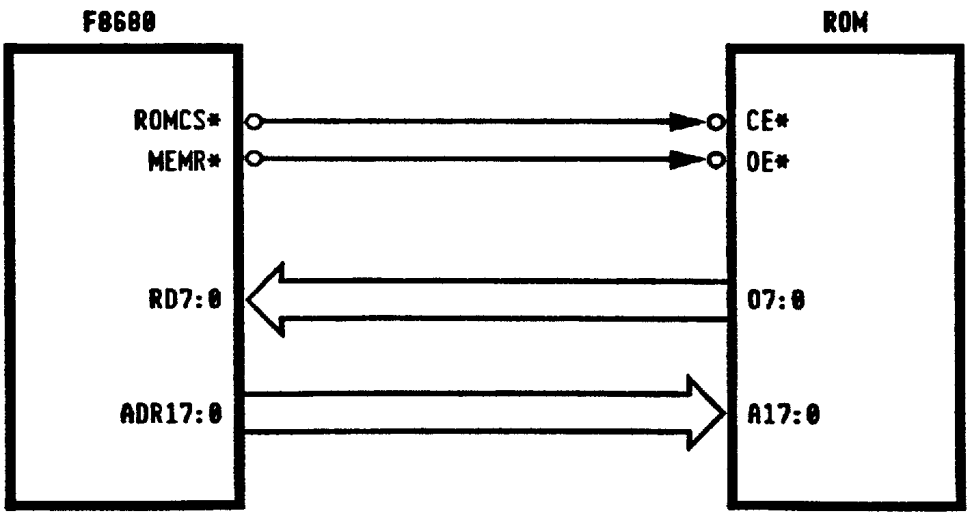
Signals. Table 11 lists the F8680A chip signals provided by the ROM/PROM interface to 8-bit devices. Refer to the "Signal Description" section of this manual for signal descriptions.

Table 11. Pin Assignments - ROM/PROM Interface Signals

Address Bus		Data Bus		Control Bus	
Pin	Signal	Pin	Signal	Pin	Signal
52	ADR0	60	RD0	48	ROMCS*
50	ADR1	61	RD1	8	MEMW*
47	ADR2	62	RD2	10	MEMR*
45	ADR3	63	RD3		
43	ADR4	64	RD4		
40	ADR5	66	RD5		
38	ADR6	67	RD6		
36	ADR7	68	RD7		
34	ADR8				
32	ADR9				
29	ADR10				
27	ADR11				
25	ADR12				
23	ADR13				
21	ADR14				
18	ADR15				
16	ADR16				
14	ADR17				
11	ADR18				
9	ADR19				

Interface to 8-bit ROM Banks. Figure 9 illustrates the connections necessary to interface a byte-wide bank of ROM.

Figure 9. Interface to 8-bit ROM



PCMCIA-Standard Interface

The PC Memory Card International Association (PCMCIA) Release 2.0 standard defines mass-storage memory cards and I/O cards in terms of their physical, electrical, and programming interfaces. All cards that adhere to these standards can use the same physical and electrical interfaces. Separate software drivers are usually required for each card type. A description of the full PCMCIA standard is provided in the *PC Card Standard* document available from PCMCIA. Refer to this document for more complete and useful information about the PCMCIA standard.

Release 2.0 defines both memory and I/O card interfaces. Memory cards include RAM cards, ROM cards, flash-type EPROM cards, and silicon disks. I/O cards include hard disk cards, modem cards, and network adapter cards. The interface signals differ between the two card types. The F8680A chip provides the M/IO bit in CREGs 42-43h to select the card interface mode for each card slot in the system; this bit determines how certain signals that are common to the two interfaces behave.

Signals. The F8680A chip provides control and status lines that conform to PCMCIA guidelines. The PCMCIA signals and the signal pins to which they are buffered on the F8680A chip are listed in Table 12. Refer to the "Signal Description" section of this manual for signal descriptions.

Table 12. PCMCIA Signal Name Equivalents

Interface	Signal Description	PCMCIA Name	Card A Name	F8680A Pin	Card B Name	F8680A Pin
Common to Memory and I/O Interfaces	Address Bus	A25:0	ADR25:0	—	ADR25:0	—
	Data Bus	D15:0	RD15:0	—	RD15:0	—
	Card Enable (even bytes)	CE1*	MCCE1*(A)	91	MCCE1*(B)	91
	Card Enable (odd bytes)	CE2*	MCCE2*(A)	90	MCCE2*(B)	90
	Attribute Memory Select	REG*	REG*(A)	7	REG*(B)	7
	Output Enable	OE*	OE0*	69	OE0*	69
	Write Enable/Program	WE*/PGM*	WE0*	70	WE0*	70
	Card Detect	CD1-2	MCCD1,2(A)	93, 94	MCCD1,2(B)	159, 160
	Card Buffer Select	—	ENA*(A)	26	ENA*(B)	22
	Buffer Direction	—	MDIR	88	MDIR	88
Memory Only Interface	Ready/Busy	RDY/BSY*	MCRDY(A)	92	MCRDY(B)	3
	Write Protect	WP	IOIS16*(A)	3 or 2	IOIS16*(B)	2
	Program Voltage	Vpp	Note 1		Note 1	
	Refresh	RFSH	REFRESH	75	REFRESH	75
	Card Detect	CD1-2	MCCD1,2(A)	93, 94	MCCD1,2(B)	159, 160
	Battery Voltage Detect	BVD1-2	MCBAT1,2(A)	95, 96	MCBAT1,2(B)	24, 20
I/O Interface	I/O Read	IORD*	IOR*	15	IOR*	15
	I/O Write	IOWR*	IOW*	12	IOW*	12
	I/O Is 16-bit	IOIS16*	IOIS16*(A)	3 or 2	IOIS16*(B)	2
	Interrupt Request	IREQ*	MCRDY(A)	92	MCRDY(B)	3
	Speaker Input	SPKRIN*	MCBAT2(A)	96	MCBAT2(B)	96
	Status Change	STSCHG*	MCBAT1(A)	95	MCBAT1(B)	95

1 Programming voltage is usually applied by activating a power control device under PS pin or configuration latch control.

Memory Card Medium Types. The PCMCIA standard provides for MaskROM, OTPROM, EPROM, EEPROM, Flash-EPROM, and SRAM as supported memory media. These are all defined in versions with 250ns, 200ns, and 150ns access times. 100ns support is also provided, but for SRAM only.

PCMCIA cards come in a variety of speeds and sizes. When running memory cards in the system, the polarity and timing of signals must be configured according to the card type in use. CREG 13h is used to make these PCMCIA control signal line settings for card slot A, and CREG 47h for card slot B.

The PCMCIA software driver must initially assume that the slowest card is being used and program the F8680A chip for the longest access time. The card attribute register space often provides information on the true access speed of the card. Only after reading this information can the access time be shortened. If two card slots are provided, the access speed of each card must be set independently.

Chip Support for PCMCIA. The F8680A chip manages a 64MB address space, of which the upper 48MB is often used for memory card access. The Bank Switch Registers and/or Memory Window Registers allow accesses in certain areas of low memory to be redirected anywhere in the 64MB address space. Low memory can also be used for memory card access. This method might be used to implement a system with no on-board RAM. In this case, the user would have to insert a PCMCIA card containing RAM before using the system. Regardless of where the PCMCIA card is accessed, the Bank Select Registers are used to choose PCMCIA cycles in that bank of memory. The Bank Select Registers also determine whether access will be 8-bit or 16-bit in all memory ranges.

Many of the F8680A chip pins can be programmed to change their function to accommodate the needs of the PCMCIA interface. When a pin is programmed for use with the PCMCIA interface, its original function is no longer available. This document presents two general schemes for implementation of the PCMCIA 2.0 interface: a one-card application and a two-card application. The following sections describe each of these schemes. The pin programming provided illustrates the most general application and the most commonly chosen configurations. However, the programming flexibility of the chip allows many variations on these schemes.

Connecting a Single Card. Figure 10 illustrates the chip pin functions that change when programmed to implement support for a single PCMCIA card slot. DREQ3, DACK0*, and IRQ2 from the XT bus cannot be used in this system because their pin functions on the F8680A chip are replaced by PCMCIA functions. To obtain this chip configuration, CREG 40h is written as 11110101b and CREG 41h is written as 00x0x000b (where the 'x' positions indicate 'set as needed'—refer to the *F8680A PC/CHIP Programmer's Reference Manual* for complete details).

Figure 10. Chip Pinout Changes for One-Card Configuration

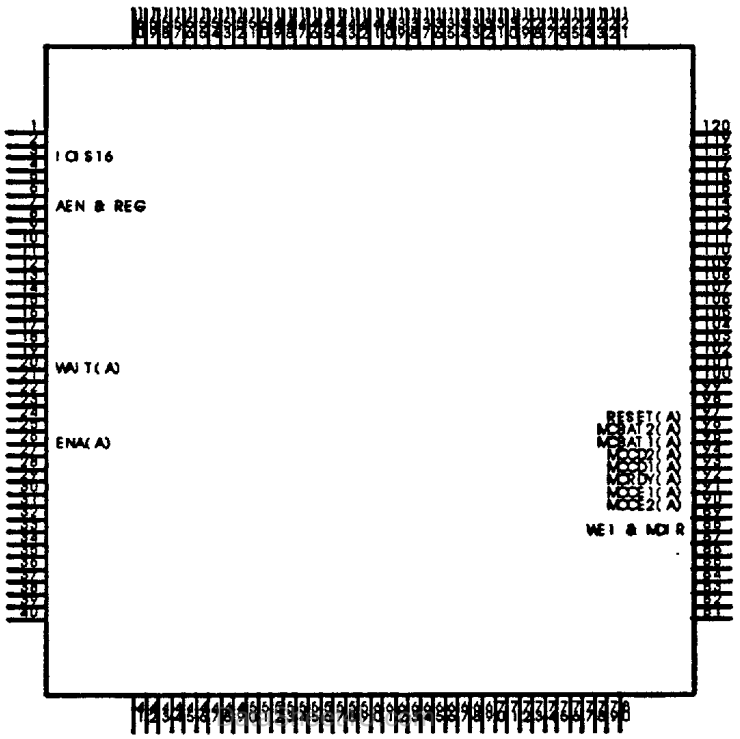
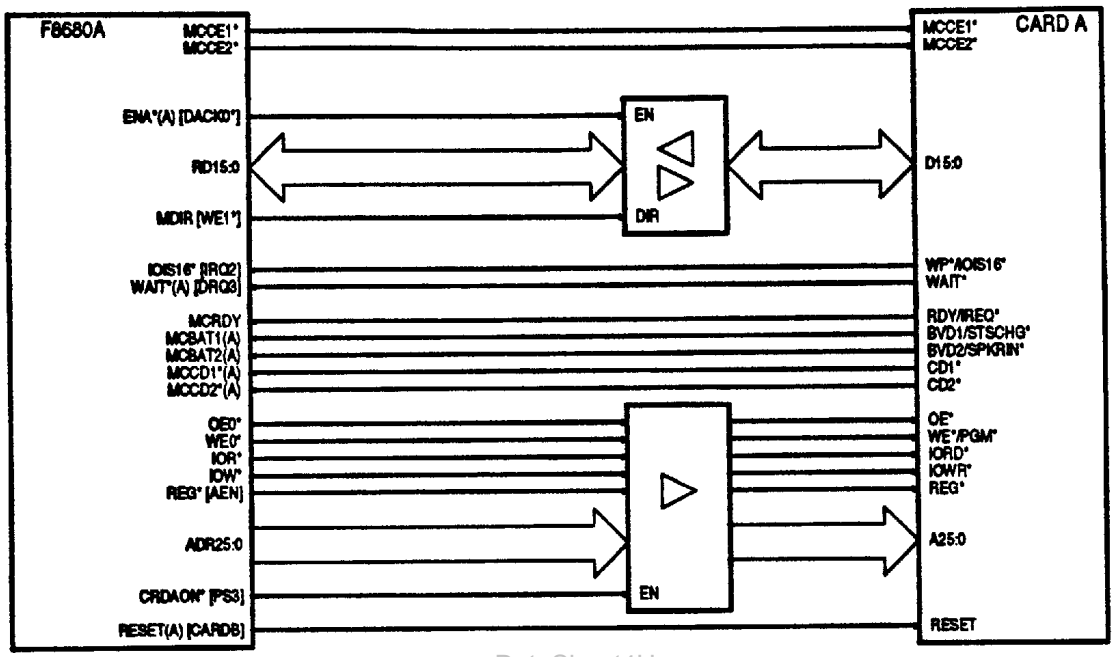


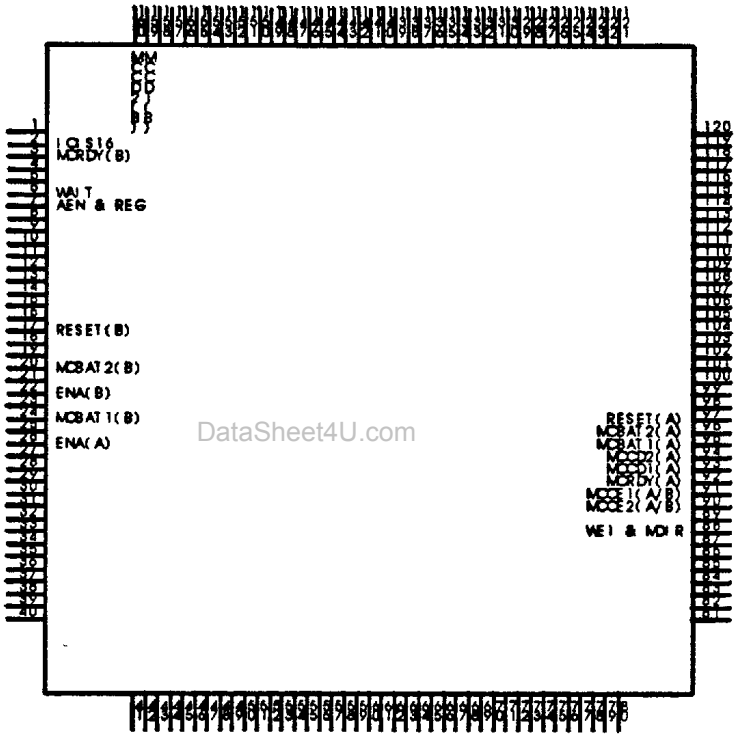
Figure 11 illustrates the circuit necessary for isolating the card slot so that it can be powered down when not in use.

Figure 11. Connections for Fully Buffered One-Slot System



Connecting Two Cards. Figure 12 illustrates the chip as programmed to implement support for two PCMCIA card slots. DREQ1, DACK1*, DREQ3, DACK3*, DACK0*, IRQ2, and IOCHCK* from the XT bus, as well as KBDATA* and KBCLK*, cannot be used in this system because their pin functions on the F8680A chip are replaced by PCMCIA functions. To obtain this chip configuration, CREG 40h is written as 11111010b and CREG 41h is written as 11x0x101b (where the 'x' positions indicate 'set as needed'—refer to the *F8680A PC/CHIP Programmer's Reference Manual* for complete details).

Figure 12. *Chip Pinout for Two-Card Configuration*



A variation on this scheme allows the KBDATA* and KBCLK* pins to be reclaimed by gating the MCCD1-2*(B) signals with the MCCD1-2*(A) signals. This adjustment is effected by writing bit 0 of CREG 41h as a '0' instead of as a '1'.

Figure 13 illustrates the circuit necessary for isolating each card slot individually so that they can be powered down when not in use. Buffers are tri-state when not enabled.

Figure 13. *Connections for Fully Buffered Two-Slot System*

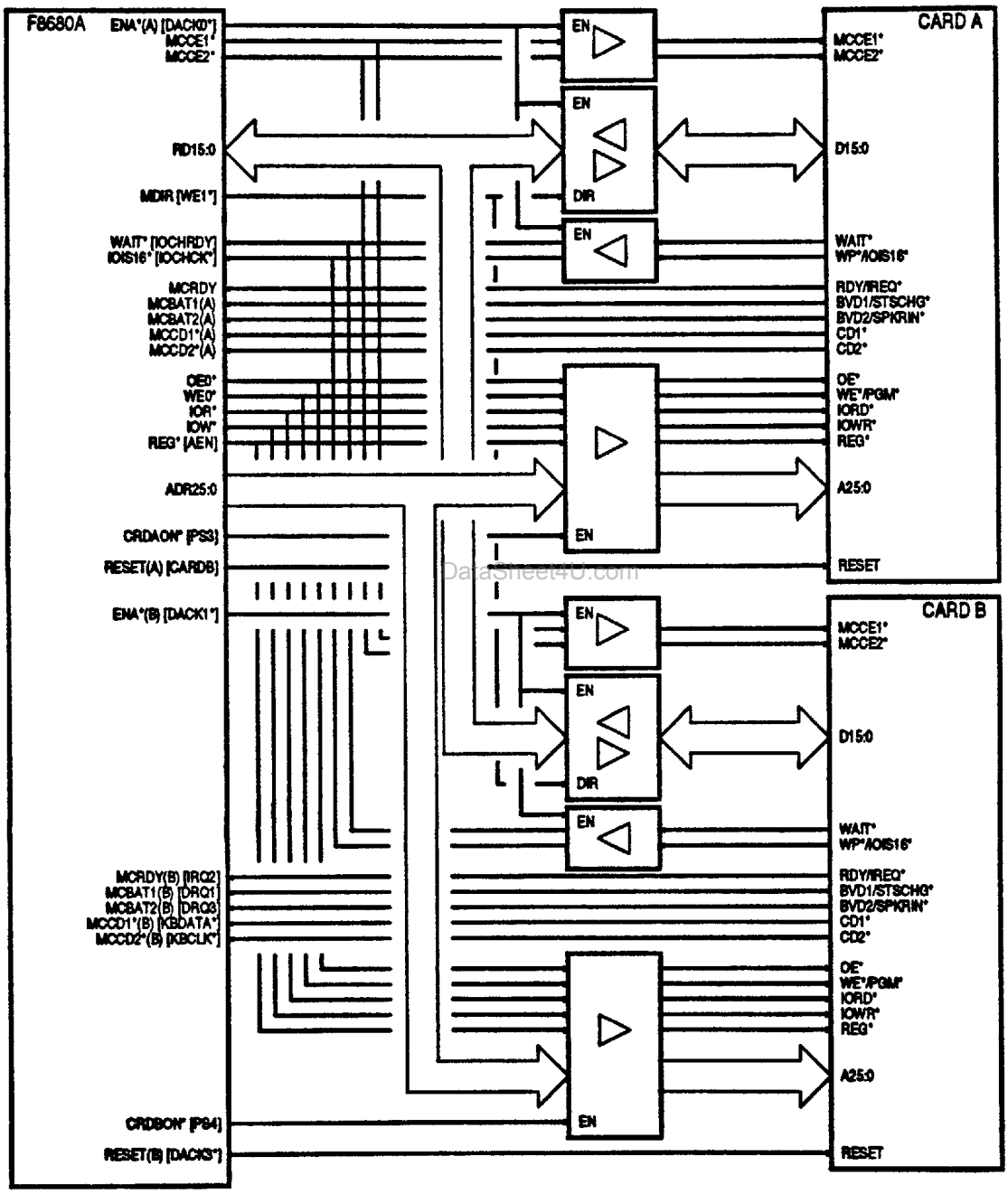
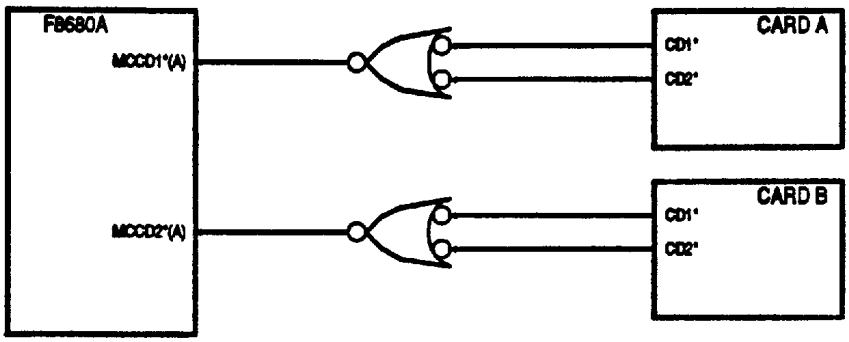


Figure 14 shows the circuitry necessary when the KBDATA* and KBCLK* lines are needed for an external keyboard. In this case, the card detect signals from each card are ORed together so that each card requires only one input to the F8680A chip.

Figure 14. Circuitry Needed for Sharing the MCCD1-2 Inputs*



CGA-Compatible Graphics Controller

The graphics controller supports both CRT and LCD panel displays with a fully CGA-compatible register set. It supports 80 x 25 and 40 x 25 text modes, as well as 640 pixel 2-color and 320 pixel 4-color graphics modes, at 200 lines of resolution. For LCD panels, the graphics controller provides a pixel panning feature to support non standard panel sizes.

When driving a CRT or a color LCD panel, the CGA-compatible graphics controller displays colors. For monochrome panels the processing of the attributes is identical, but the resulting colors are translated to gray levels. Up to 16 levels of gray can be translated.

The Visual Map feature overcomes a problem that arises when monochrome LCD panels are used with text mode applications written for a color display. Many controllers map colors to shades of gray, but colors that are close in intensity are barely distinguishable on a monochrome display. When text mode foreground and background colors are mapped to the same shade of gray, the text disappears.

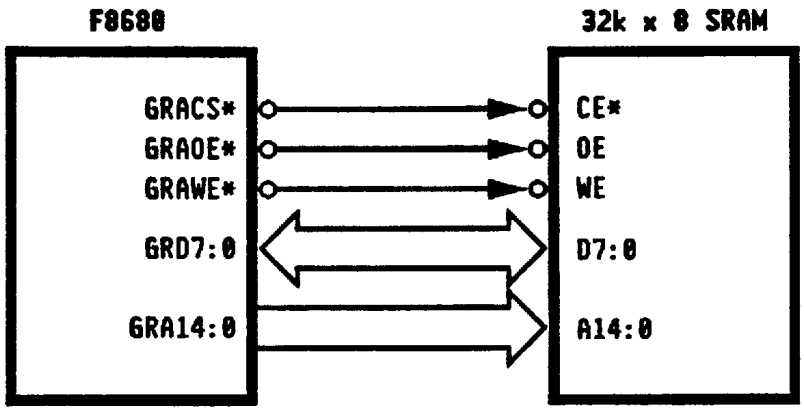
The Visual Map feature programs each possible foreground and background color combination into a table as a specific combination of shades of gray. Each combination provides contrast that is closer to that of a color display than simple mapping techniques can achieve. The Visual Map feature works with any application that displays in text mode. No application-specific tables are required.

The F8680A display controller options allows interfacing directly to an LCD panel or CRT. Alternatively, the internal display controller can be disabled and an external high-resolution display subsystem connected instead.

SRAM Interface

To use the internal display controller, a 32k x 8 SRAM rated for 120ns or better access time is required. The connection is straightforward and is illustrated in Figure 15.

Figure 15. Connection of Display SRAM

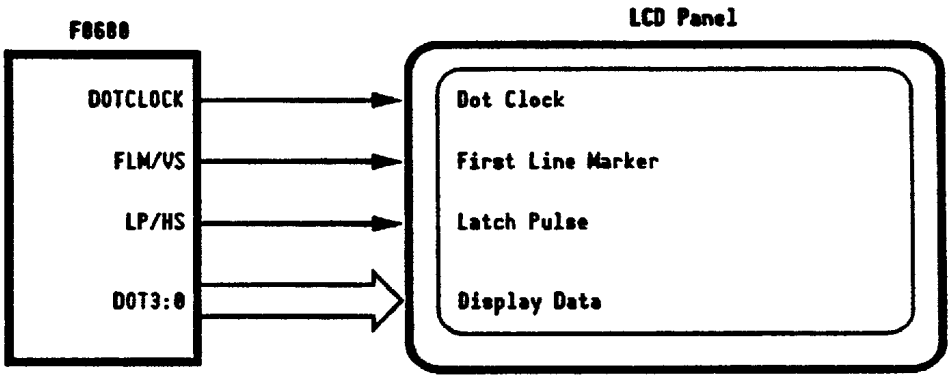


where:	GRA14:0	Graphics Address (O) - address bus to graphics SRAM.
	GRACS*	Graphics Chip Select (O) - chip select to graphics SRAM.
	GRAOE*	Graphics Output Enable (O) - output enable to graphics SRAM.
	GRAWE*	Graphics Write Enable (O) - write enable to graphics SRAM.
	GRD7:0	Graphics Data (O) - data bus to graphics SRAM.

LCD Panel Interface

The display controller circuit of the F8680A chip provides the signals shown in Figure 16 for connection to a 640 pixel x 200 line LCD panel. These signals operate as indicated only when the F8680A chip is programmed for LCD mode (through CREG 11h).

Figure 16. Display Controller Signals to the LCD Panel



where:

DOT3:0	Display Data (O) - pixel output to LCD panels.
DOTCLOCK	Dot Clock (O) - output to LCD panels.
HS (LP)	Horizontal Sync / Latch Pulse (O) - latch pulse signal when in LCD mode.
VS (FLM)	Vertical Sync / First Line Marker (O) - first line indicator signal when in LCD mode.

For panels that require special consideration, the F8680A programmable pins provide two display-related functions: alternative dot clock input and AC drive clock output.

Alternative Dot Clock Input on PS4. An LCD panel that requires a non-standard dot clock rate can be used by providing the appropriate clock input to pin PS4. Note that there is a relationship between the dot clock supplied and the speed of the display SRAM selected: the SRAM access time must be less than twice the period of the dot clock provided, or

$$T_{acc} < (2 \times T_{per}) - \text{margin}$$

For the standard 14.31818MHz input, T_{per} is 70ns; with a recommended margin of 20ns, T_{acc} becomes 120ns. If a 20MHz dot clock were chosen, using the same safety margin as above would require 80ns or better SRAM.

The alternative dot clock function is available only on PS4, and is enabled through code similar to the following:

```
LFEAT 8Ch,0              ; disable PS3 for output through CREG 88
LFEAT 11,11001000b       ; enable dot clock as PS4, set LCD mode in CREG 11
```

Note that the byte written to CREG 11h must be adjusted according to the other features that are also set through that CREG.

ACDCLK Output Option on PS2. LCD panels use an AC drive clock ("M" clock) signal to control the bias polarity of cells in the panel such that none of the pixel cells is subjected to a non-zero average DC bias. Such a bias would cause vertical lines to appear on the display, and could possibly damage the panel. While many LCD panels provide their own on-board circuitry for generating the panel AC drive clock signal, panels without this circuitry can be accommodated through pin PS2.

The AC drive clock function ACDCLK is available only on PS2 and is programmed through CREG 84h and CRT Controller register index 05 (only when in LCD mode). Code similar to the following can be used to set up ACDCLK operation:

```
LFEAT 11h,10001000b      ; set LCD mode in CREG 11
LFEAT 84h,01011110b      ; enable ACDCLK output on PS2 through CREG 84

MOV DX,03D4h             ; write CRT controller index
MOV AL,05                ; index 05 counts LPs per ACDCLK
OUT AL,DX

MOV DX,03D5h             ; write CRT controller data
MOV AL,value             ; how many LPs per ACDCLK?
OUT AL,DX
```

The *value* written depends on the frequency desired at PS2 for use as ACDCLK. The *value* indicates the number of latch pulses (LP) to count before toggling PS2, and should be an odd value because the panel uses an even number of lines. An appropriate *value* can be determined by experimentation for the specific panel in use. The AC drive clock signal produced will always have a 50 percent duty cycle.

As an alternative to using the ACDCLK function, a 256Hz frequency output can be programmed on PS2 and externally latched with the Latch Pulse signal HS(LP) to provide an alternating drive clock signal.

Register Programming. Setting up LCD panel operation requires that CREG 0E and CREG 11h be programmed. CREG 0E handles the hardware configuration as follows:

- EDC, DCPH, and DCP enable the dot clock signal out of the F8680A chip on the DOTCLOCK pin, and select signal phase and polarity.
- CP selects the signal polarity of the DOT3:0 pixel lines (to determine whether a positive or a negative image is displayed).
- CHS and CVS select the signal polarity of Latch Pulse signal LP (pin HS/LP) and First Line Marker signal FLM (pin VS/FLM).
- EGOUT enables all display controller output pins, or forces them to ground.
- GENB enables the graphics subsystem, or disables it so that an external display controller can respond instead.

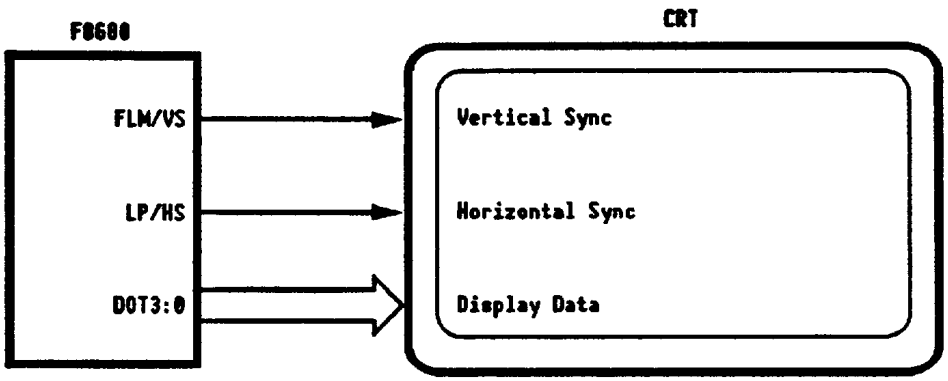
CREG 11h handles system software operational details, so they need not be considered in the hardware design. However, note that CREG 11h holds the DCSEL bit that chooses the source of the dot clock, either the internally generated clock or the optional external dot clock input on PS3. CREG 11h also holds the LCD bit, which must be set before LCD panel operation is possible.

The remaining registers, the CRT Controller registers, are all CGA-compatible in their operation.

CRT Interface

The display controller defaults to operation in CRT mode. Figure 17 shows the signals available for driving a CRT.

Figure 17. Display Controller Signals to the CRT



where:

DOT3(I) DOT2(R) DOT1(G) DOT0(B)	Display Data (O) - used as output to CRTs.
HS	Horizontal Sync (O) - horizontal synchronization signal to CRT when programmed for CRT mode.
VS	Vertical Sync (O) - vertical synchronization signal to CRT when programmed for CRT mode.

DC Electrical Characteristics

The F8680A microchip operates in the range of 3.3V -10% to 5V +10%. Table 13 shows voltage levels and ambient temperature for both 3.3V and 5V operation.

Table 13. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage			
	5V	4.5	5.5	V
	3.3V	3.0	3.6	V
T_A	Ambient Temperature	0	70	°C
T_A	Ambient Temperature Industrial	-40	85	oc

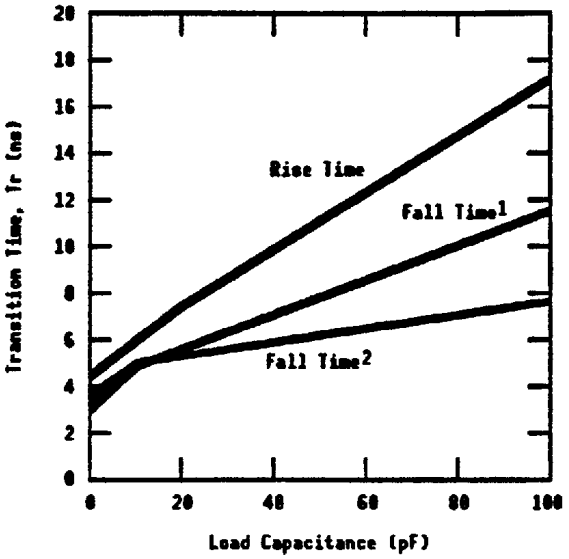
Table 14 shows input, output, and I/O capacitance values for 5V operation.

Table 14. Capacitance

Symbol	Parameter	Max.	Unit	Note
C_{in}	Input Capacitance	8	pF	Vcc = 5V
C_{out}	Output Capacitance	8	pF	Vcc = 5V
$C_{I/O}$	I/O Capacitance	8	pF	Vcc = 5V
T_r	Output Transition Time			See Figures 18,19

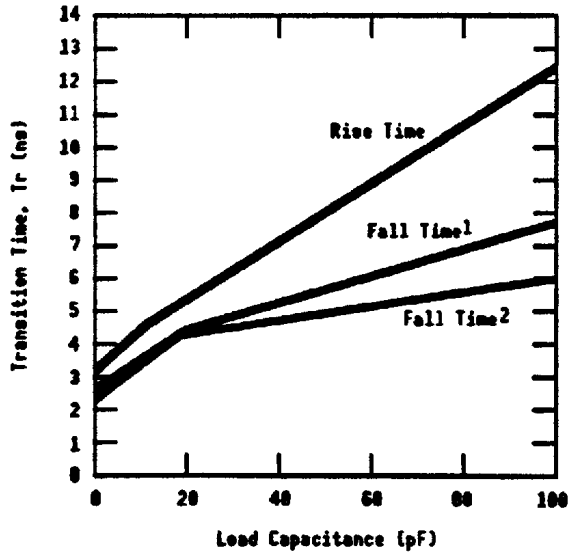
Figures 18 and 19 show the typical and minimum transition times vs load capacitance with Vcc=5.5V.

Figure 18. Typical Output Transition Time vs Load Capacitance



Notes:
1. All Except RD7:0
2. RD7:0

Figure 19. Minimum Output Transition Time vs Load Capacitance



Notes:
1. All Except RD7:0
2. RD7:0

Tables 15 and 16 and Figures 20 through 23 summarize the DC characteristics for both 5V and 3V operation.

Table 15. DC Characteristics at 5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{il}	Input Low Voltage	-0.3	--	1.0	V	
V_{ih}	Input High Voltage	Vcc-1.0	--	Vcc+0.3	V	
V_{ol}	Output Low Voltage	--	--	0.4	V	All outputs except RD7:0, Iol=8mA
V_{ol}	Output Low Voltage	--	--	0.4	V	RD7:0 outputs only, Iol=16mA
V_{oh}	Output High Voltage	2.4	--	--	V	I_{oh}=8mA
I_{oh}	Output Source Current					See Figure 20
I_{ol}	Output Sink Current					See Figure 21
I_{il}	Input Leakage Current	--	--	±10	µA	V_{in}=Vcc to 0V
I_{oz}	Output Leakage Current	--	--	±10	µA	V_{out}=Vcc to 0V
I_{cca}	Vcc Supply Current	--	40	--	mA	@8MHz
I_{ccsb}	Standby Pwr. Supply Current	--	50	--	µA	32kHz clock only
I_{ccdc}	Quiescent Current	--	10	--	µA	No clocks running

Figure 20. Output Source Current vs Output Voltage (@Vcc=4.5V)

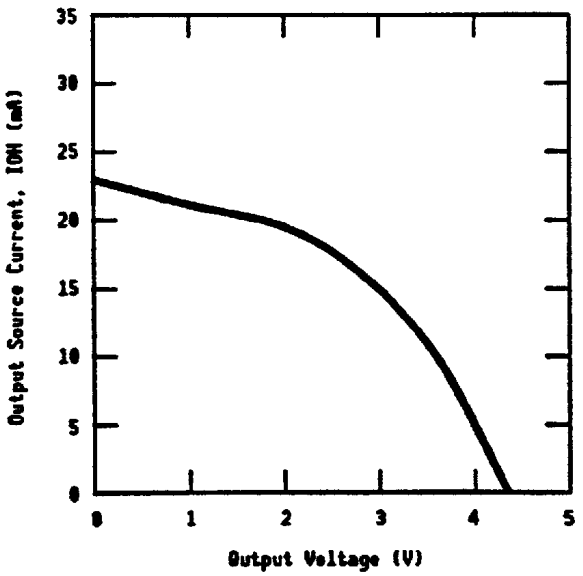


Figure 21. Output Sink Current vs Output Voltage (@Vcc=4.5V)

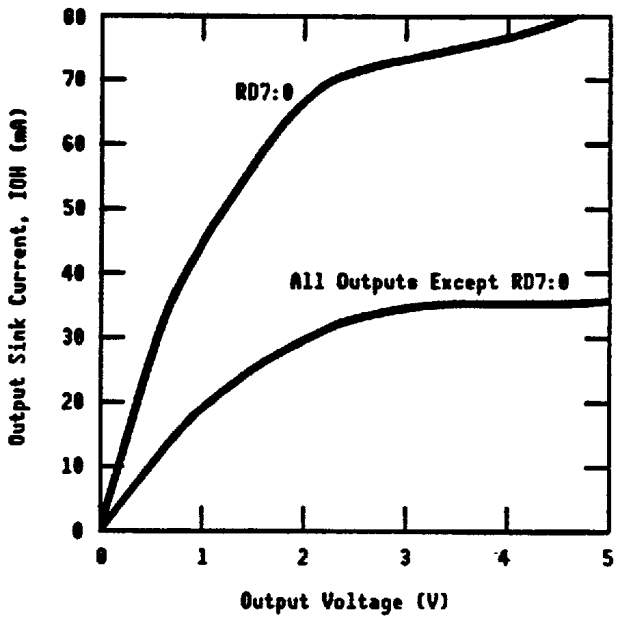


Table 16. DC Characteristics at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{il}	Input Low Voltage	--		0.5	V	
V_{ih}	Input High Voltage	Vcc-0.5		--	V	
V_{ol}	Output Low Voltage	--		0.4	V	All outputs except RD7:0, Iol=4mA
V_{ol}	Output Low Voltage	--		0.4	V	RD7:0 outputs only, Iol=8mA
V_{oh}	Output High Voltage	2.4		--	V	I_{oh}=4mA
I_{oh}	Output Source Current					See Figure 22
I_{ol}	Output Sink Current					See Figure 23
I_{il}	Input Leakage Current	--		±10	µA	V_{in}=Vcc to 0V
I_{oz}	Output Leakage Current	--		±10	µA	V_{out}=Vcc to 0V
I_{ccac}	Vcc Supply Current	--	20	--	mA	@8MHz
I_{ccsb}	Standby Pwr. Supply Current	--	30	--	µA	32kHz clock only
I_{ccdc}	Quiescent Current	--	10	--	µA	No clocks running

Figure 22. Output Source Current vs Output Voltage (@Vcc=3V)

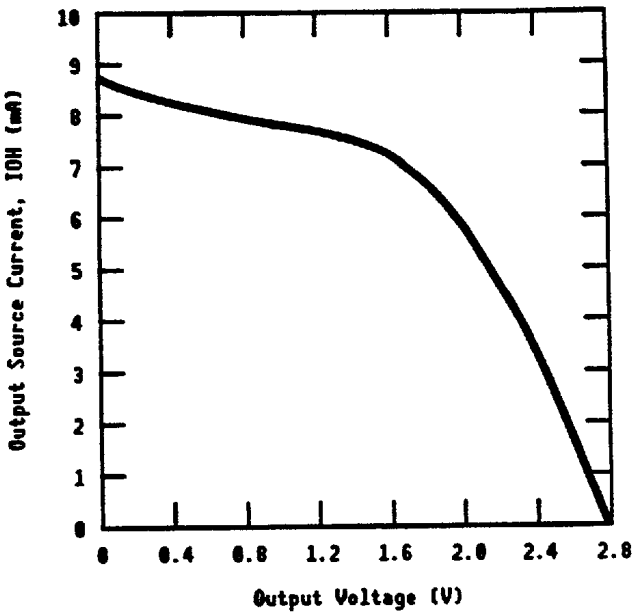
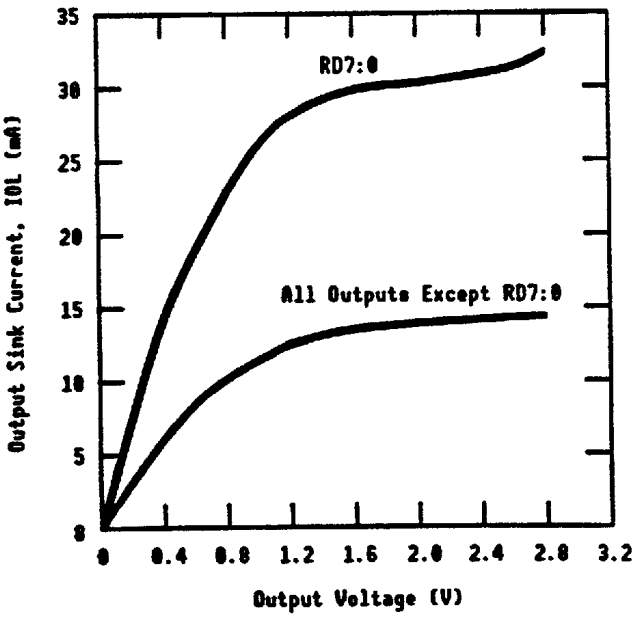


Figure 23. Output Sink Current vs Output Voltage (@Vcc=3V)



AC Specifications

The AC specifications for the F8680A consist of 12 parameters defining input setup time, input hold time, and output valid delay time. All system timings are a function of these parameters and the input frequency being used to clock the CPU.

The 12 timing parameters are defined in reference to an internal signal known as LatchCLK. The LatchCLK signal is brought out of the chip through the CLK pin (pin 28) when the XT bus is programmed for a bus clock speed of one clock cycle per state (CREG 01 bits 1:0=11).

The functional timing diagrams can be used to determine on which LatchCLK edge the various signals are generated or sampled. This information, along with the input setup time, input hold time, and output delay time data, can be used to perform a systems-level worst-case timing analysis.

Tables 17 through 32 and Figures 24 through 52 summarize the AC characteristics of the F8680A microchip. All timings are in nanoseconds (ns) unless otherwise noted.

Table 17. Timing Symbols Associated with Signal Types

	Symbol	Signals
Output Signal Types	t101, t102	ADR25:0
	t103, t104	IOW*, MEMW*, CS10-11*, CS20-22*, WE0-1*, ROMCS*, GRACS*, GRAWE*, MCCE1-2*, MDIR
	t105, t106	AEN, ALE, DACK0-3*, IOR*, MEMR*, TC, OE0-1*, REFRESH*, DOT3:0, DOTCLOCK, GRA14:0, GRAOE*, GRD7:0, HS/LP, VS/FLM, KBCLK*, KBDATA*, CARDB, PS1-4, OSCPW, DTR*, RTS*, Tx, SPKR
	t107, t108	RD15:0
Input Signal Types	t109, t110	DRQ1-3, IOCHCK*, IOCHRDY, IRQ2-7, KBCLK*, KBDATA*, MCBAT1-2, MCCD1-2*, MCRDY, PS1-4, PWRUP, CD*, CTS*, DSR*, RI*, Rx, RESET, FLOAT*
	t111, t112	RD15:0

Table 18. Timing Parameters, Commercial (TA = 0 to +70 °C)

Symbol	Parameter	3V/8Mhz		5V/8MHz		5V/14MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	Note
t101	Output address valid delay from LatchCLK		15	—	12	—	12	
t102	Output address valid hold delay from LatchCLK		18	—	18	—	18	
t103	Controls active from LatchCLK	-15	+12	-10	+12	-10	+12	1
t103a	CS2x* active from LatchCLK	0	22	0	18	0	18	2
t104	Controls inactive from LatchCLK	-8	+12	-3	+8	-3	+8	
t105	Output valid delay from LatchCLK	-6	+18	0	12	0	10	3
t105a	OE0#, OE1# active from LatchCLK	-3	+20	6	22	6	22	
t106	Output valid hold delay from LatchCLK	-10	+15	-6	15	-6	+15	
t107	Write data valid delay from LatchCLK	—	42	—	36	—	36	
t107a	Tracking spec, t107 - t103	—	50	—	28	—	28	
t108	Write data valid hold delay from LatchCLK	-8	15	0	12	0	12	4
t109	Input valid setup to LatchCLK	65	—	36	—	34	—	
t110	Input valid hold from LatchCLK	-6	—	0	—	0	—	
t111	Read data valid setup to LatchCLK	50	—	27	—	20	—	
t112	Read data valid hold from LatchCLK	-6	—	-3	—	-3	—	

Table 19. Timing Parameters, Industrial (T_A = -40 to +85 °C)

Symbol	Parameter	3V/8Mhz		5V/8MHz		5V/14MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	Note
t101	Output address valid delay from LatchCLK		15	—	12	—	12	
t102	Output address valid hold delay from LatchCLK		18	—	18	—	18	
t103	Controls active from LatchCLK	-15	+12	-10	+12	-10	+12	1
t103a	CS2x* active from LatchCLK	0	22	0	18	0	18	2
t104	Controls inactive from LatchCLK	-8	+12	-3	+8	-3	+8	
t105	Output valid delay from LatchCLK	-6	+18	0	12	0	10	3
t105a	OE0#, OE1# active from LatchCLK	-3	+22	6	22	6	22	
t106	Output valid hold delay from LatchCLK	-10	+15	-6	15	-6	+15	
t107	Write data valid delay from LatchCLK	—	44	—	36	—	36	
t107a	Tracking spec, t107 - t103	—	50	—	28	—	28	
t108	Write data valid hold delay from LatchCLK	-8	15	0	12	0	12	4
t109	Input valid setup to LatchCLK	65	—	36	—	34	—	
t110	Input valid hold from LatchCLK	-6	—	0	—	0	—	
t111	Read data valid setup to LatchCLK	50	—	27	—	20	—	
t112	Read data valid hold from LatchCLK	-6	—	-3	—	-3	—	

Note: For Tables 18 and 19 above.

1. t103 applies to IOW*, MEMW*, CS1x*, WE*. ROMCS*, GRACS*, GRAWE* MCCEx*.
2. t103a is greater than t101 under all operating conditions.
3. t105 applies to AEN, ALE, DACKx*, IOR*, MEMR*, TC, REFRESH*.
4. t108 is greater than t104 for WE* under all operating conditions.

Figure 24. Output Delay Parameters—General Case

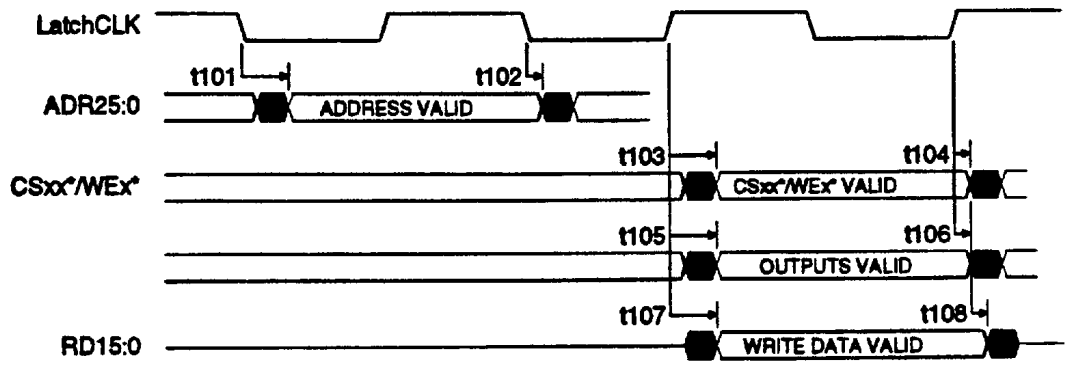


Figure 25. Input Setup and Hold Parameters—General Case

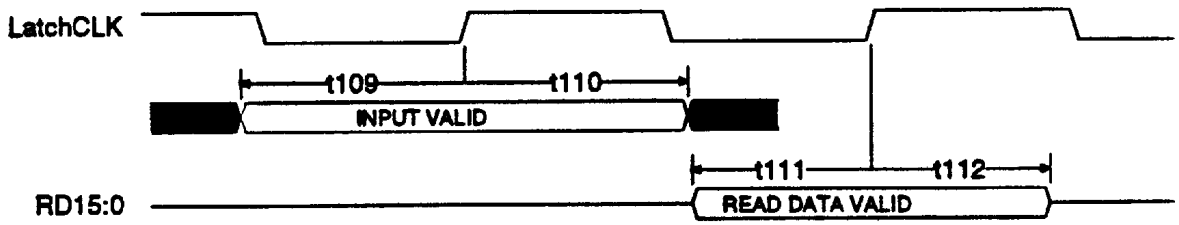


Table 20. AC Characteristics - System Clock Timings (all 50% duty cycle)

Symbol	Parameter	Min.	Max.	Figure No.	Note
t1	CPUCLK period	125	—	26	1, 8
t2	CPUCLK high time	50	75	26	2, 8
t3	CPUCLK low time	50	75	26	2, 8
t4	CPUCLK rise time	0	30	26	8
t5	CPUCLK fall time	0	30	26	
t6	CLK14 period	69	—	26	3
t7	CLK14 high time	28	49	26	4
t8	CLK14 low time	20	42	26	4
t9	CLK14 rise time	0	10	26	
t10	CLK14 fall time	0	10	26	
t11	CLK32K period	30518	—	26	5
t12	CLK32K high time	5340	21362	26	6
t13	CLK32K low time	4270	21362	26	6
t14	CLK32K rise time	0	3350	26	6
t15	CLK32K fall time	0	2500	26	6
t16	UARTCLK period	542	—	26	7
t17	UARTCLK high time	140	379	26	7
t18	UARTCLK low time	60	379	26	7
t19	UARTCLK rise time	0	80	26	7
t20	UARTCLK fall time	0	130	26	7

Note:
1. No maximum period.
2. When period is 125ns.
3. For DOS Timers compatibility, CLK14 should be 14.31818MHz.
4. When clock period is 69 ns.
5. For proper operation of time of day and sleep mode refresh, 32.768Khz is needed. Tested to 1Mhz.
6. When CLK32K is 32.768Khz.
7. UARTCLK should be 1.832 MHz for PC compatibility. Test to 5 MHz.
8. These numbers are for operation at 8 MHz, and the chip can also operate at 14.318 MHz.

Figure 26. Timing for System Clocks

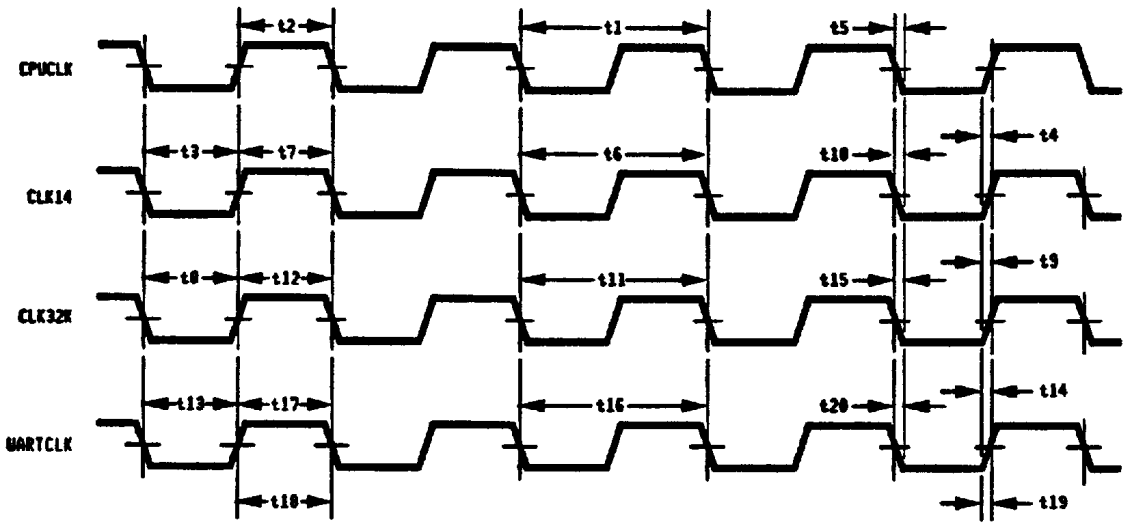


Table 21. AC Characteristics - DRAM Signal Timings

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	27, 28
t111	Read data valid setup to LatchCLK	27, 28
t112	Read data valid hold from LatchCLK	27, 28

Figure 27. Timing for Non-page-mode DRAM Cycles

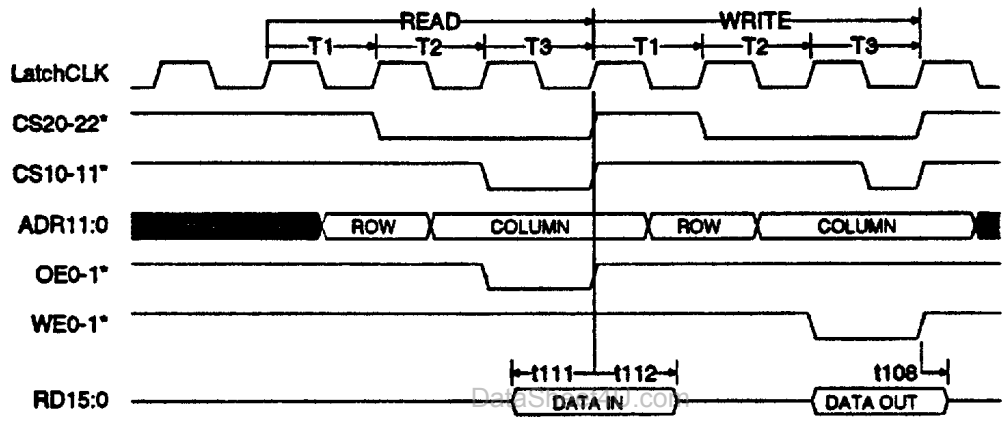


Figure 28. Timing for Page-mode DRAM Cycles

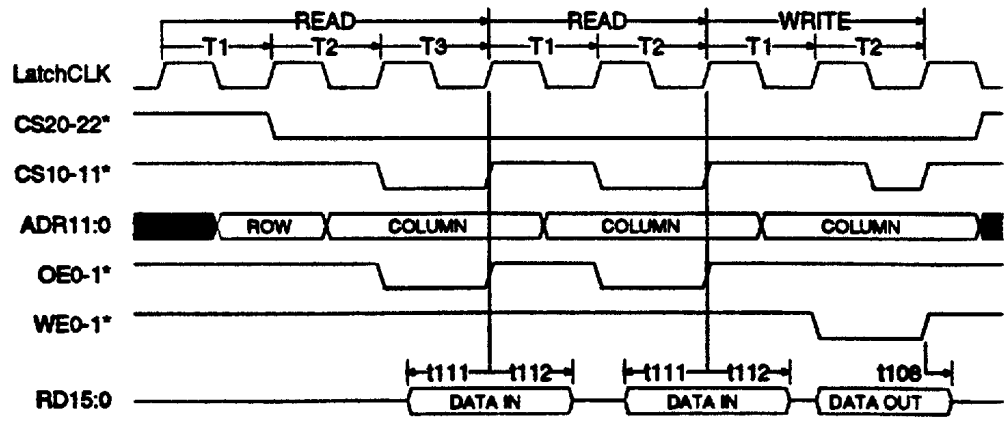
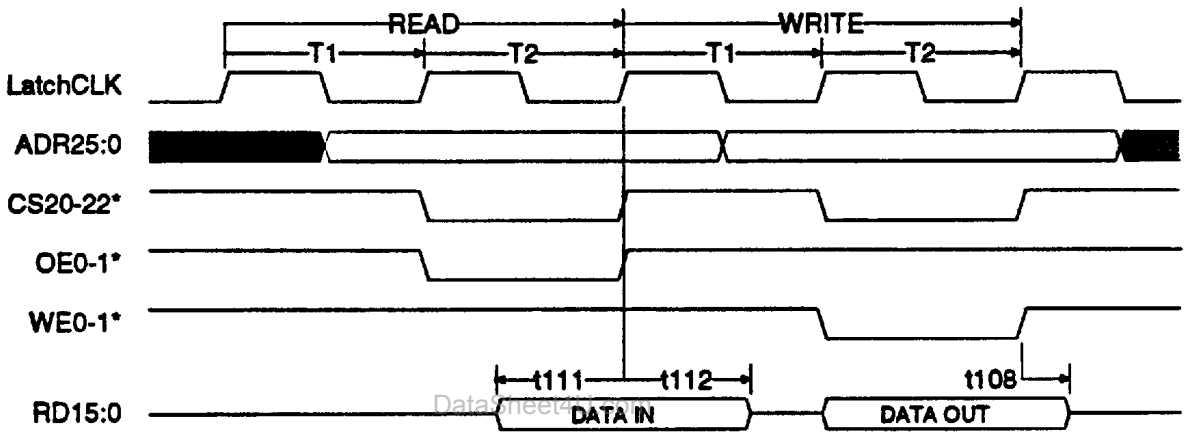


Table 22. *AC Characteristics - SRAM/PSRAM Standard Signal Timings*

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	29
t111	Read data valid setup to LatchCLK	29
t112	Read data valid hold from LatchCLK	29

Figure 29. *Timing for SRAM/PSRAM Standard Access*



Note in Figure 30 that the setup time from address to early chip select coming active is variable and can be set through CREG 36h.

Table 23. *AC Characteristics - SRAM/PSRAM Signal Timings with Early Chip Select*

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	30
t111	Read data valid setup to LatchCLK	30
t112	Read data valid hold from LatchCLK	30

Figure 30. *Timing for SRAM/PSRAM Access with Early Chip Select*

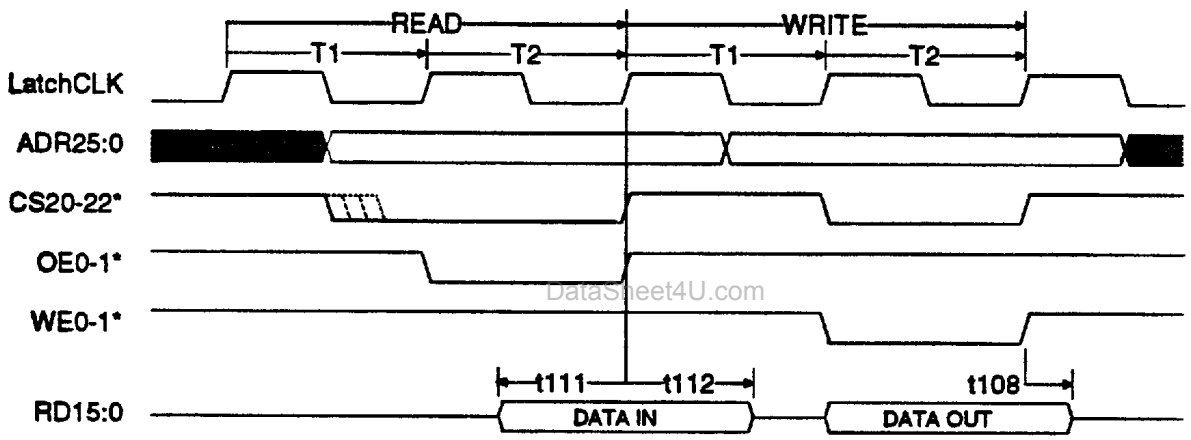


Table 24. *AC Characteristics - Suspend Refresh Signal Timings*

Symbol	Parameter	Minimum	Figure No.
t201	CAS* (CS10-11*) active from CLK32K	0	31
t202	RAS* (CS20-22*) active delay from CAS* active	15	31
t203	CAS* inactive delay from RAS* active	40	31
t204	RAS* inactive delay from CAS* inactive	120	31

Figure 31. *Timing for DRAM Suspend Mode Refresh*

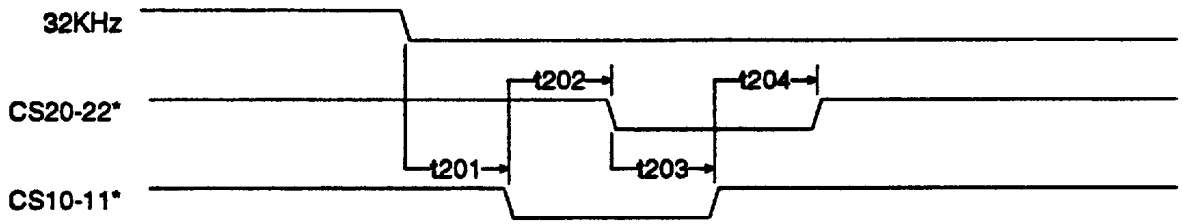


Figure 32. *Functional Timing for PSRAM Active Mode Refresh*

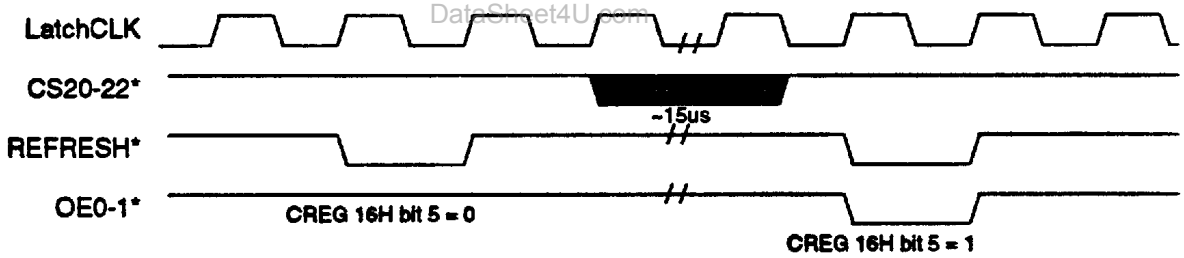


Figure 33. *Functional Timing for PSRAM Suspend Mode Refresh*

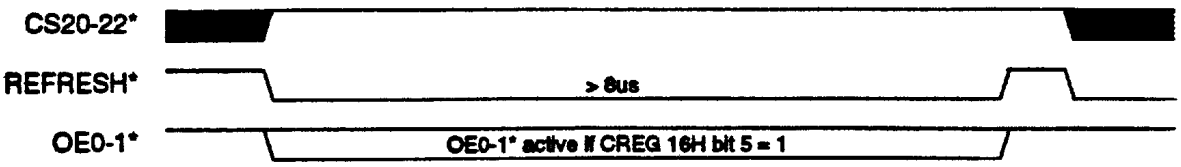
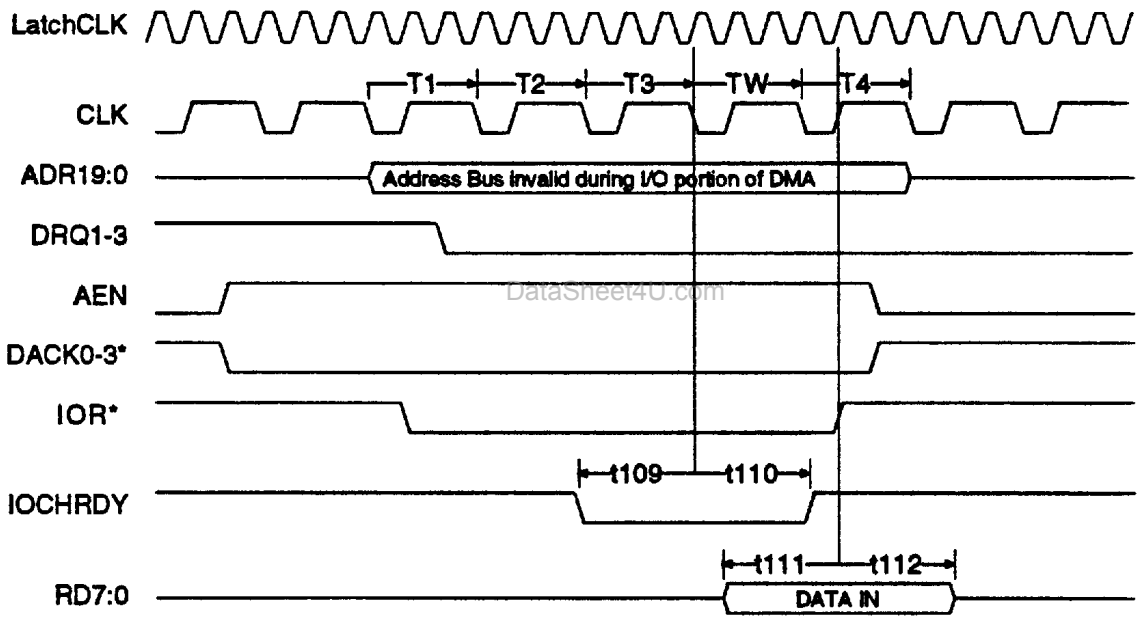


Table 25. AC Characteristics - DMA Signal Timings

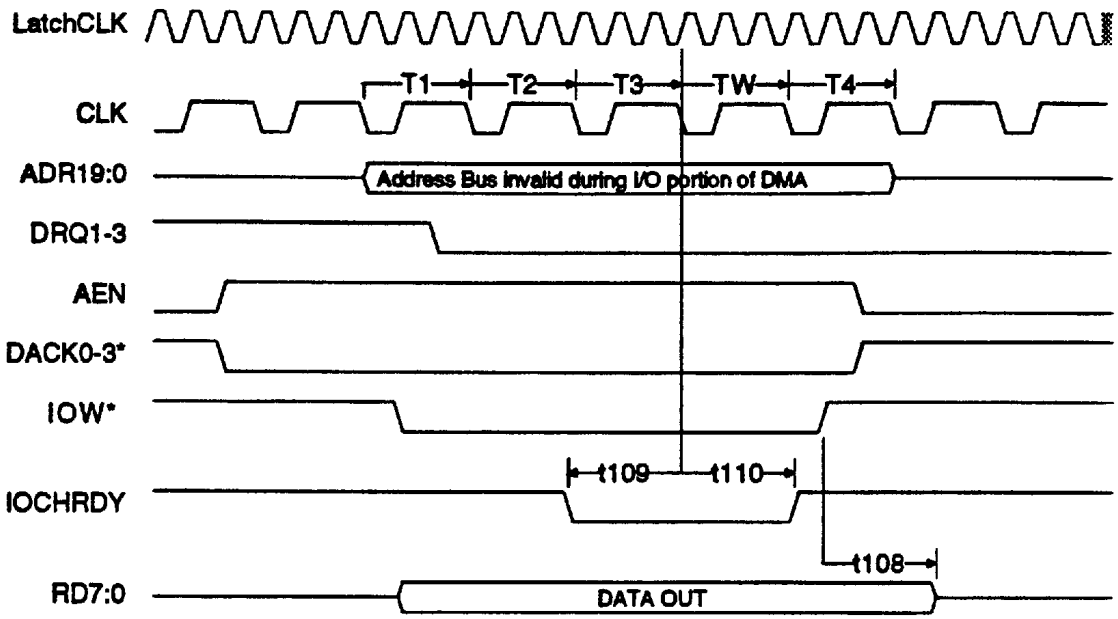
Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	35
t109	Input valid setup to LatchCLK	34, 35
t110	Input valid hold from LatchCLK	34, 35
t111	Read data valid setup to LatchCLK	34
t112	Read data valid hold from LatchCLK	34

Figure 34. Timing for I/O Read Cycles during DMA



Note: The I/O read cycle shown in Figure 34 is followed by a separate memory write cycle having the same timing as any other memory write.

Figure 35. Timing for I/O Write Cycles during DMA



Note: The I/O write cycle shown in Figure 35 is preceded by a separate memory read cycle having the same timing as any other memory read.

Table 26. AC Characteristics - XT Bus I/O Cycle Signal Timings

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	37
t109	Input valid setup to LatchCLK	36, 37
t110	Input valid hold from LatchCLK	36, 37
t111	Read data valid setup to LatchCLK	36
t112	Read data valid hold from LatchCLK	36

Figure 36. Timing for I/O Read (BUSCLK programmed to 3 cycles per state)

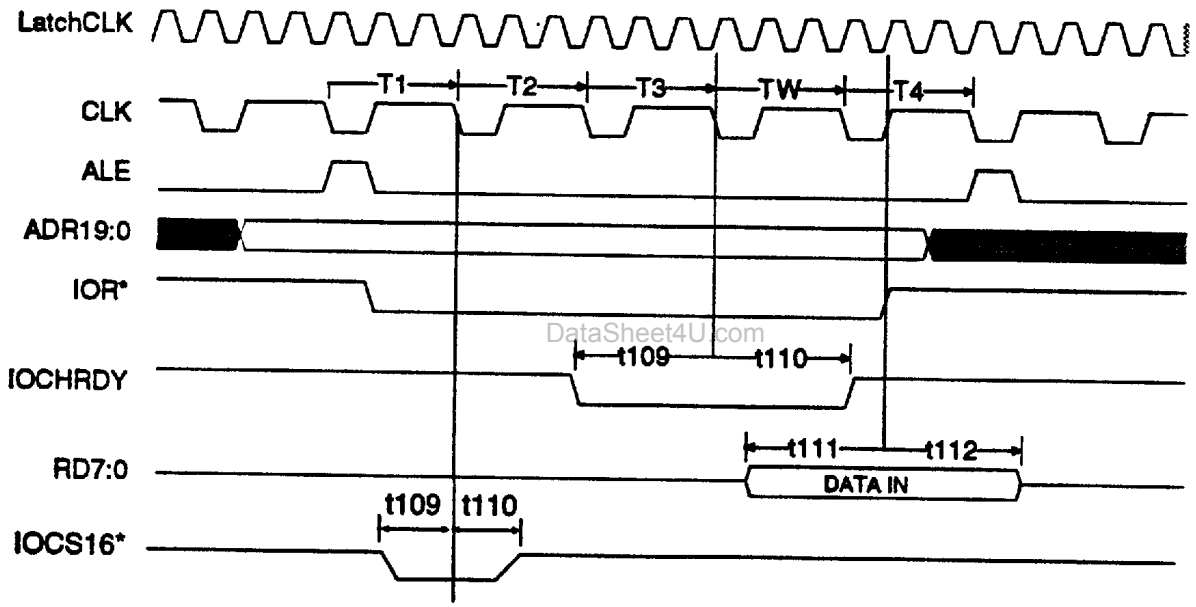


Figure 37. Timing for I/O Write (BUSCLK programmed to 3 cycles per state)

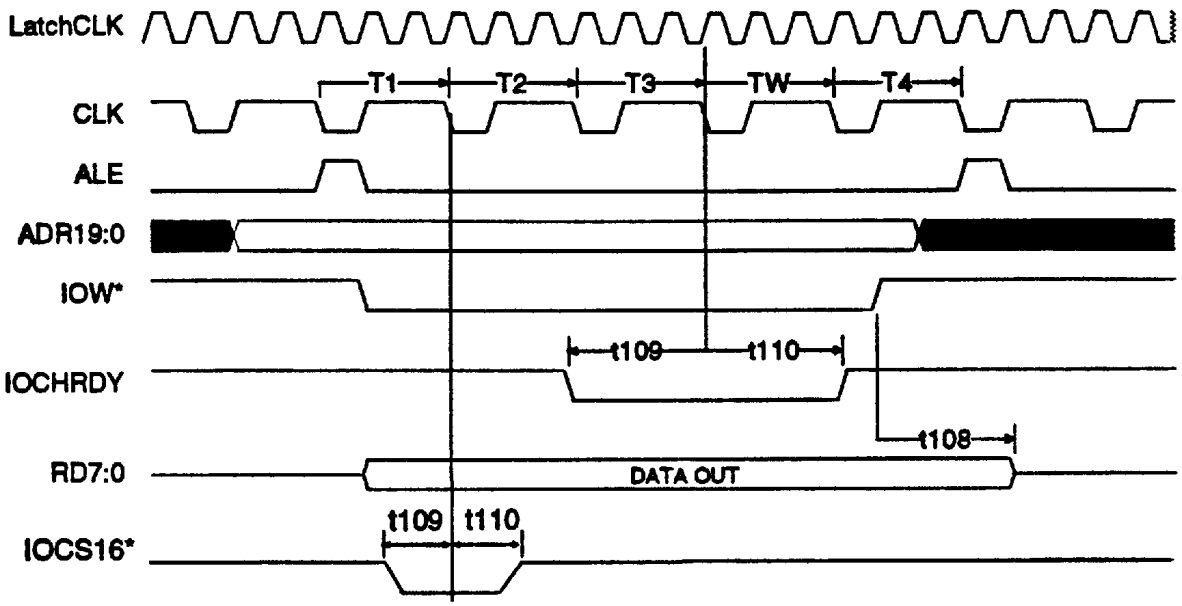


Table 27. AC Characteristics - XT Bus Memory Signal Timings

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	39
t109	Input valid setup to LatchCLK	38, 39
t110	Input valid hold from LatchCLK	38, 39
t111	Read data valid setup to LatchCLK	38
t112	Read data valid hold from LatchCLK	38

Figure 38. Timing for XT Bus Memory Read (BUSCLK programmed to 3 cycles per state)

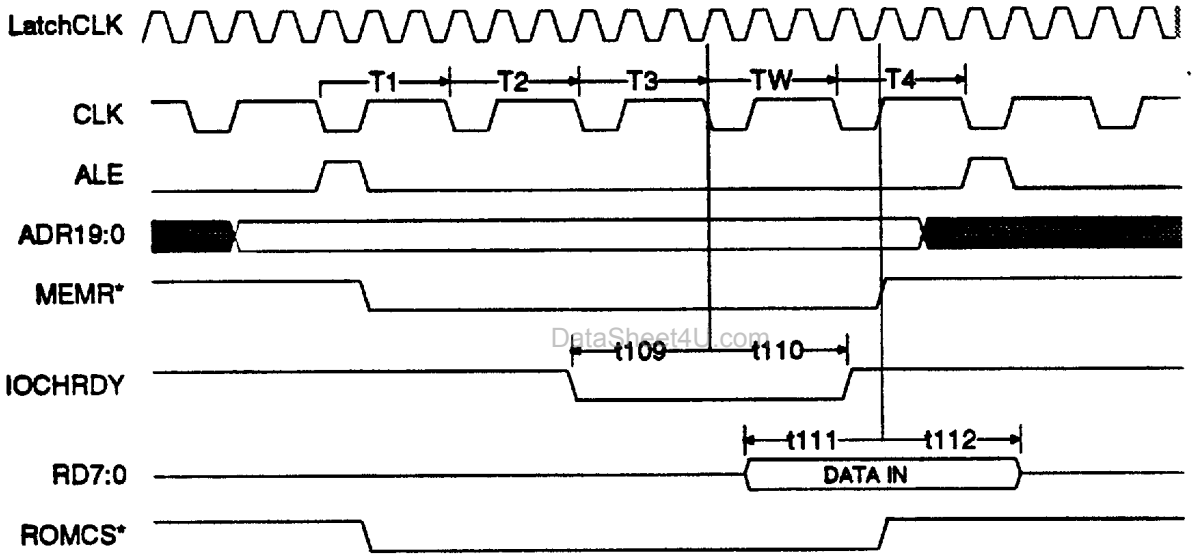


Figure 39. Timing for XT Bus Memory Write (BUSCLK programmed to 3 cycles per state)

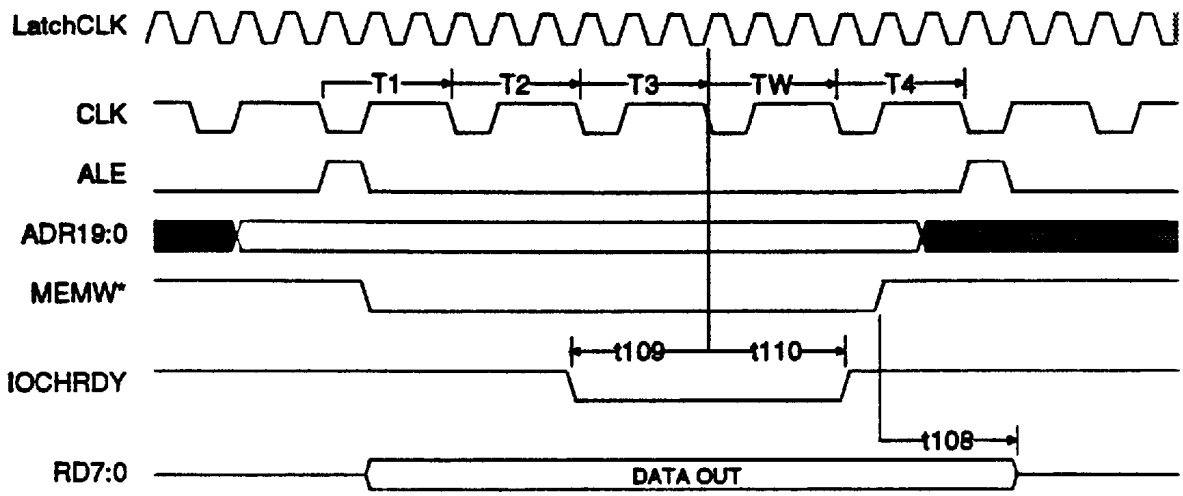


Table 28. AC Characteristics - PCMCIA Memory Interface Signal Timings

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	42, 43
t111	Read data valid setup to LatchCLK	40, 41
t112	Read data valid hold from LatchCLK	40, 41

Figure 40. Timing for PCMCIA Memory Read (1 Cycle Per State)

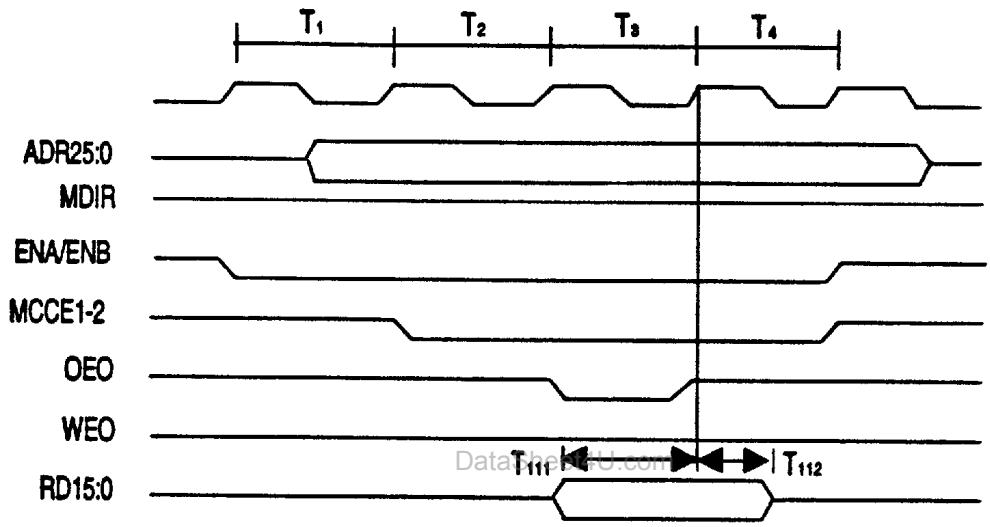


Figure 41. Timing for PCMCIA Memory Read (2 Cycles Per State)

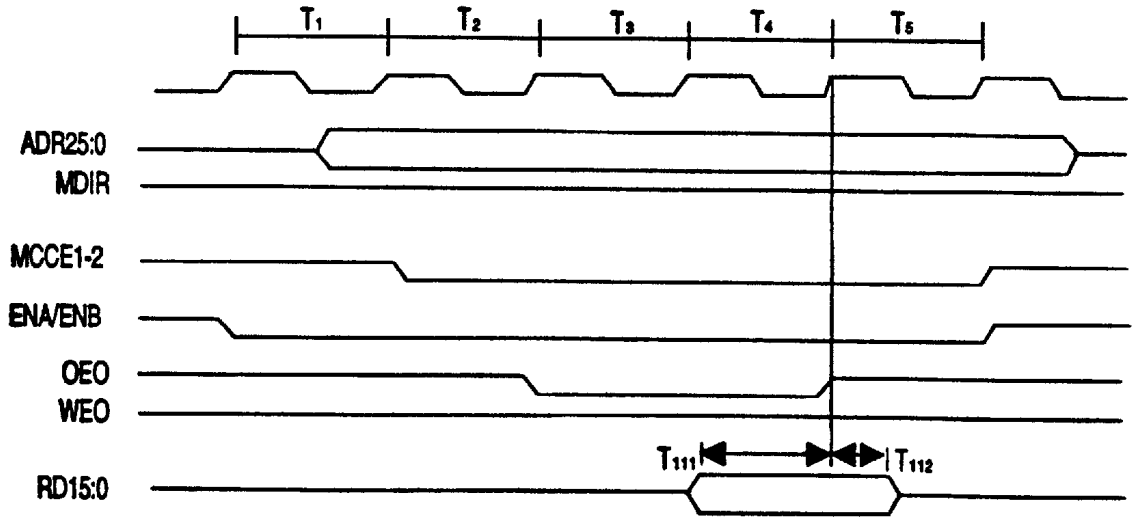


Figure 42. Timing for PCMCIA Memory Write (1 Cycle Per State)

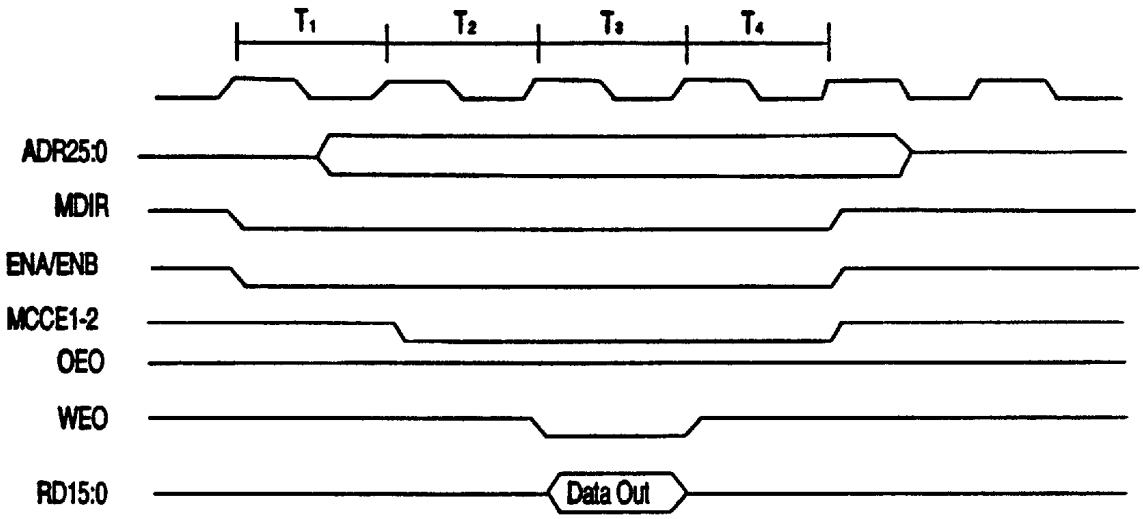


Figure 43. Timing for PCMCIA Memory Write (2 Cycles Per State)

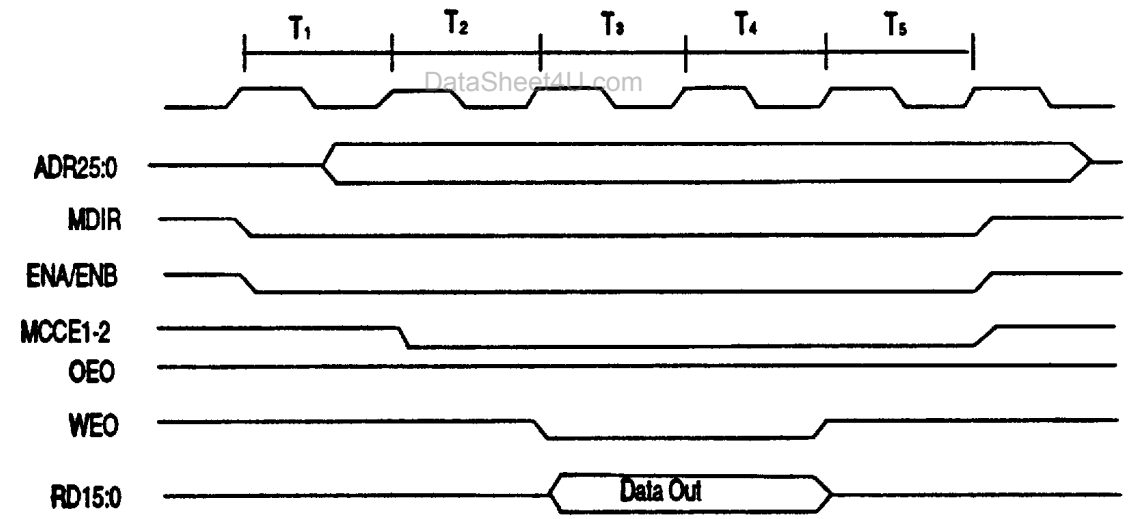
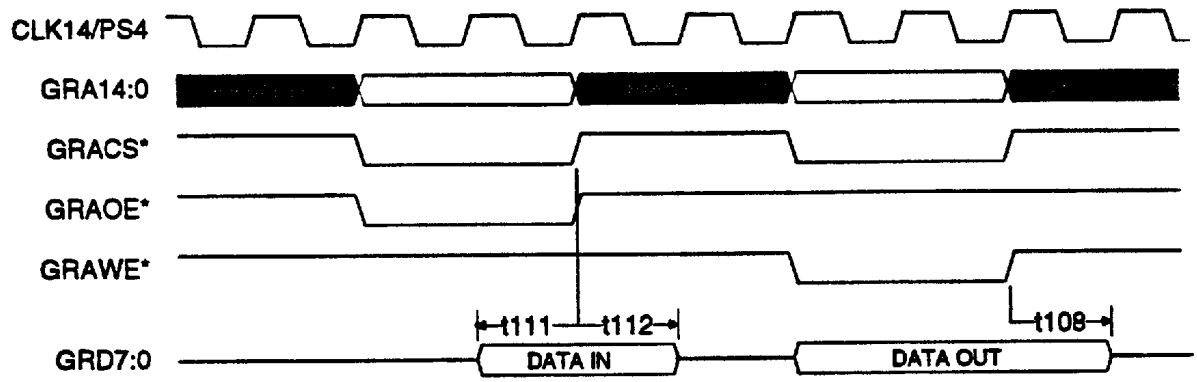


Table 29. AC Characteristics - Graphics Controller Signal Timings

Symbol	Parameter	Figure No.
t108	Write data valid hold delay from LatchCLK	44
t111	Read data valid setup to LatchCLK	44
t112	Read data valid hold from LatchCLK	44

Figure 44. Timing for Graphics SRAM



The following two figures illustrate signal synchronization characteristics for the CRT signal interface. They are functional examples only; the CRT controller registers must be set appropriately in order to achieve this operation.

Figure 45. Functional Horizontal Sync Timing for CRT

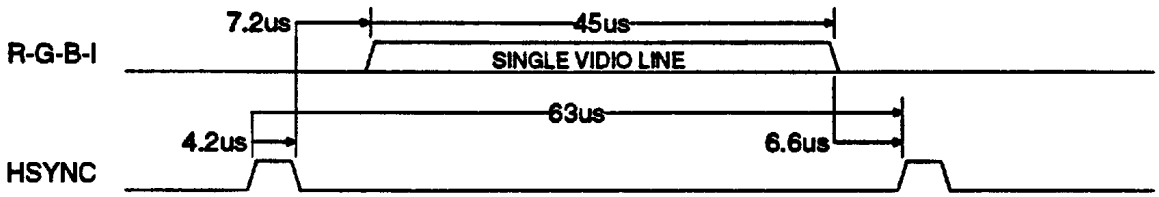


Figure 46. Functional Vertical Sync Timing for CRT

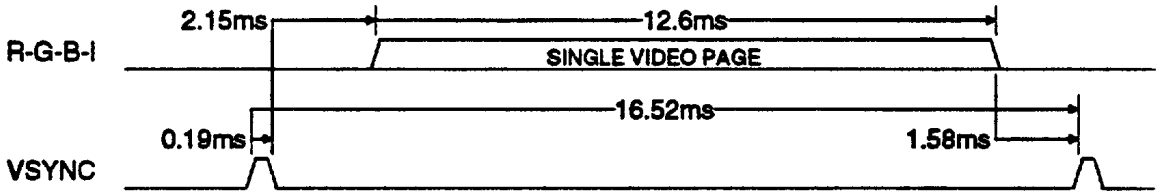


Figure 47. Functional Timing for LCD Panel Signals

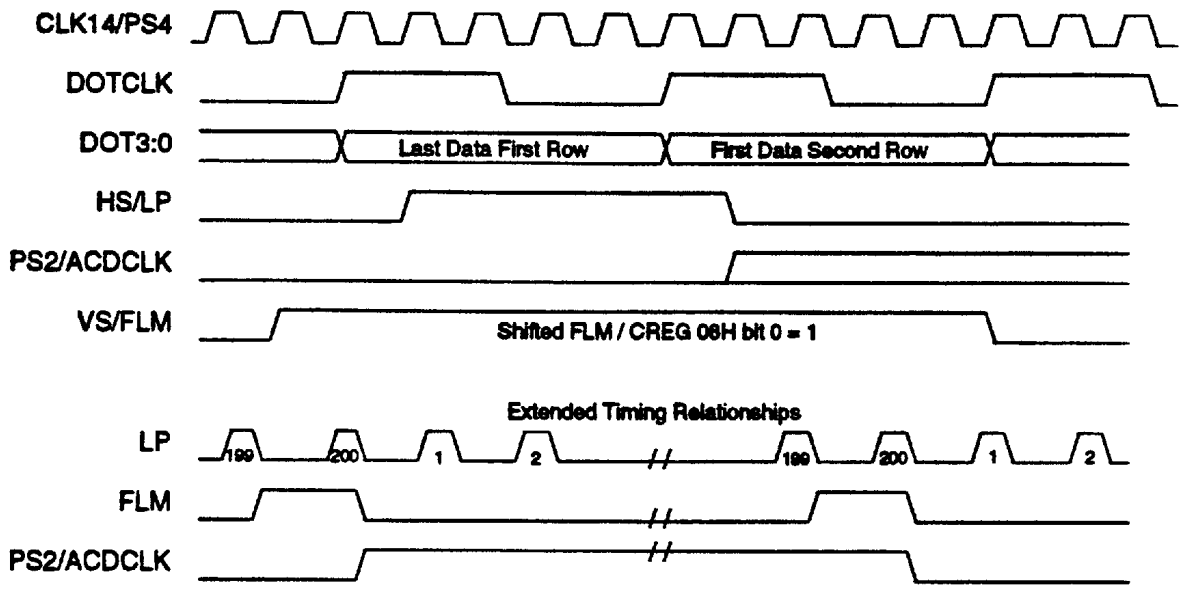
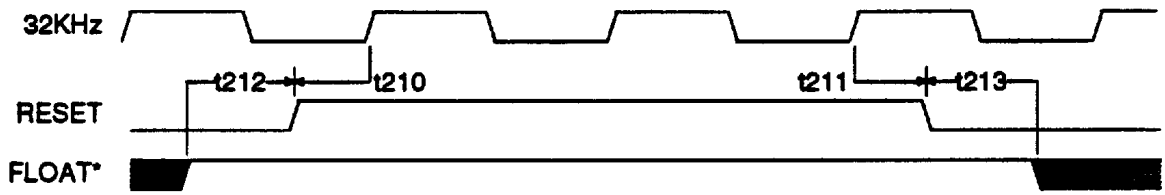


Table 30. AC Characteristics - RESET Signal Timing

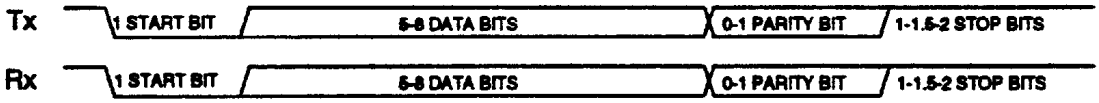
Symbol	Parameter	Minimum	Figure No.
t210	RESET active setup to CLK32K	75	48
t211	RESET active hold from CLK32K	75	48
t212	FLOAT* inactive setup to RESET active	100	48
t213	FLOAT* inactive hold from RESET inactive	100	48

Figure 48. Timing for RESET



The following figure illustrates functional UART timing relationships. The modem control signal timing is not shown, because these signal states depend on control bits in the standard UART registers and in the CREG configuration registers.

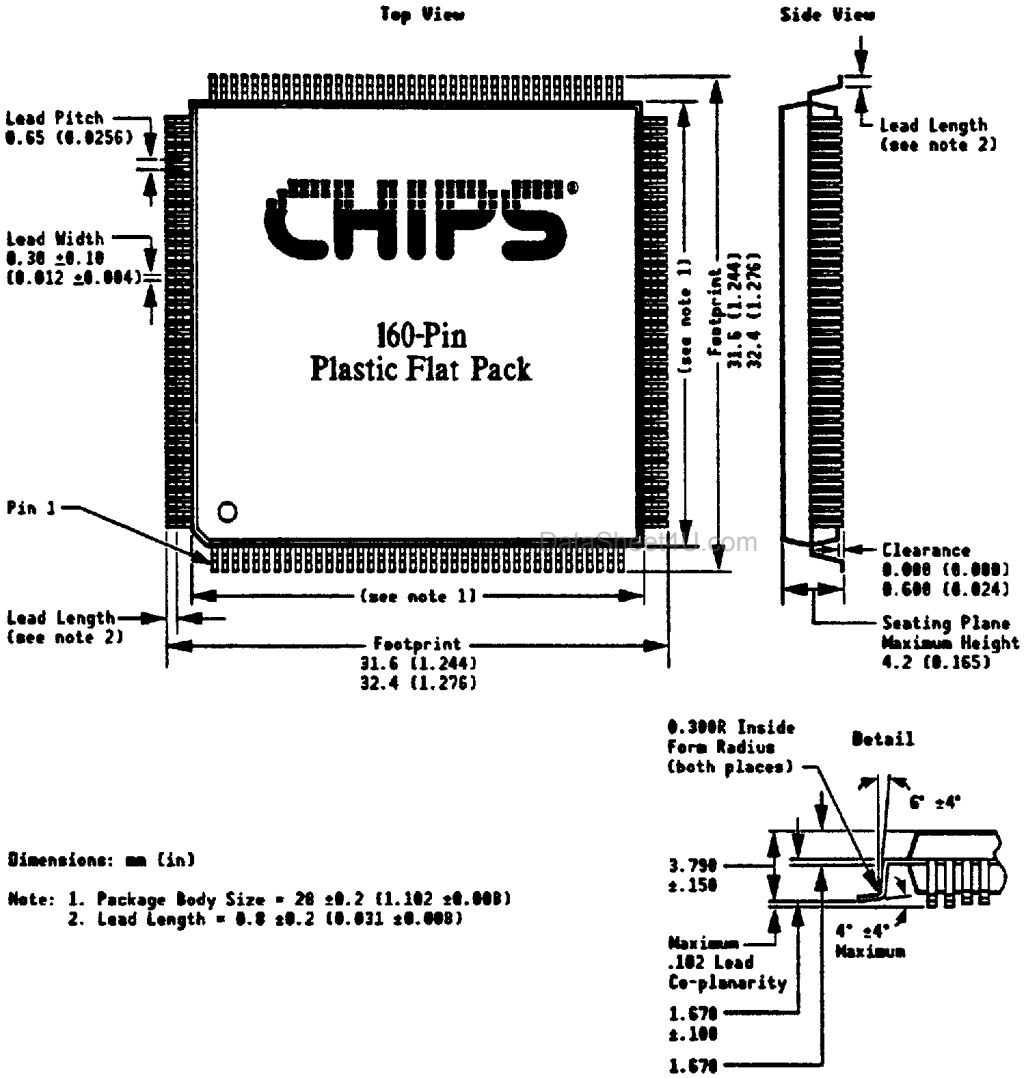
Figure 49. Timing for UART



Mechanical Specifications

The F8680A microchip is packaged in a 160-pin plastic quad flat pack. The dimensions are shown in Figure 50.

Figure 50. *160-Pin Plastic Flat Pack*



Dimensions: mm (in)

Note: 1. Package Body Size = 28 ±0.2 (1.102 ±0.008)
2. Lead Length = 0.8 ±0.2 (0.031 ±0.008)

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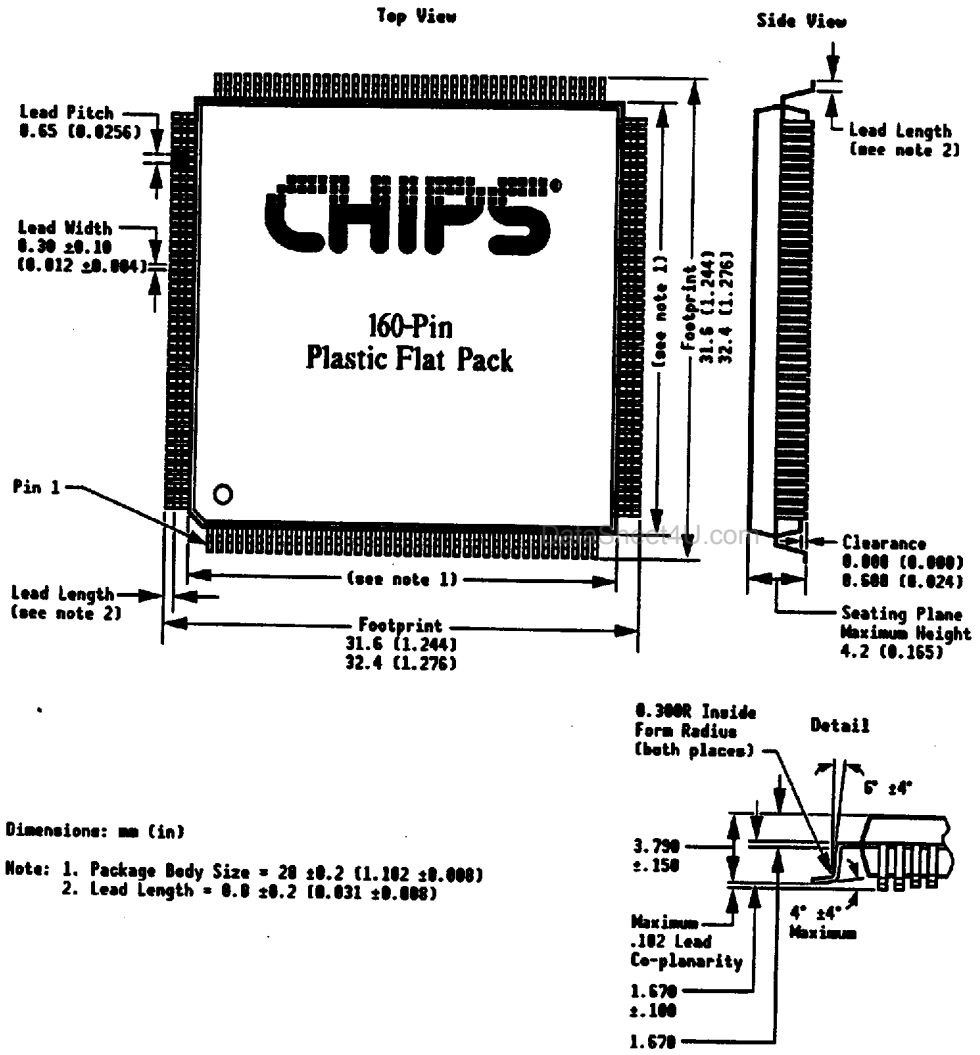
Mechanical Specifications

The F8680 microchip is packaged in a 160-pin plastic quad flat pack. The dimensions are shown in Figure 45.

Figure 45. 160-Pin Plastic Flat Pack



Dimensions: mm (in)

Note: 1. Package Body Size = 28 ±0.2 (1.102 ±0.008)
2. Lead Length = 0.8 ±0.2 (0.031 ±0.008)

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